

Reversible NanoComputing

*Jeferson Figueiredo Chaves, PhD student
Prof. Omar Paranaiba Vilela Neto, Advisor*

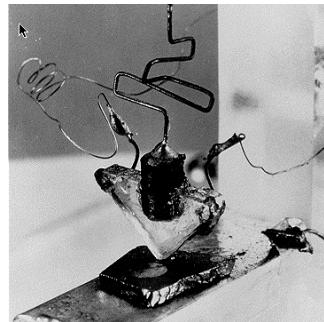
DECOM – Department of Computing, CEFET-MG, Brazil
DCC – Computer Science Department, UFMG, Brazil



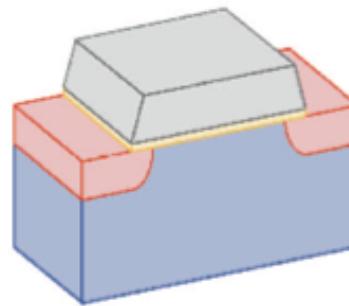
Outline

- Introduction
 - Beyond Silicon
 - QCA circuits
 - Reversible Computing
- Partially reversible pipelined QCA
- Heat dissipation bounds for nanocomputing
- Quantifying irreversible information loss in digital circuits
- Nanocomp first contributions

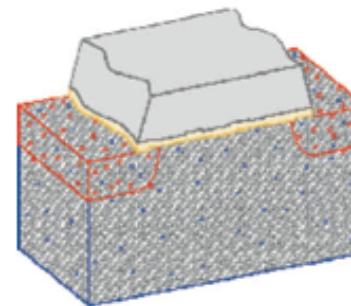
Beyond Silicon



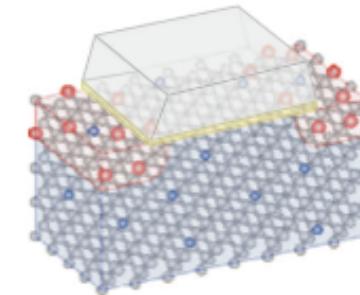
First Transistor



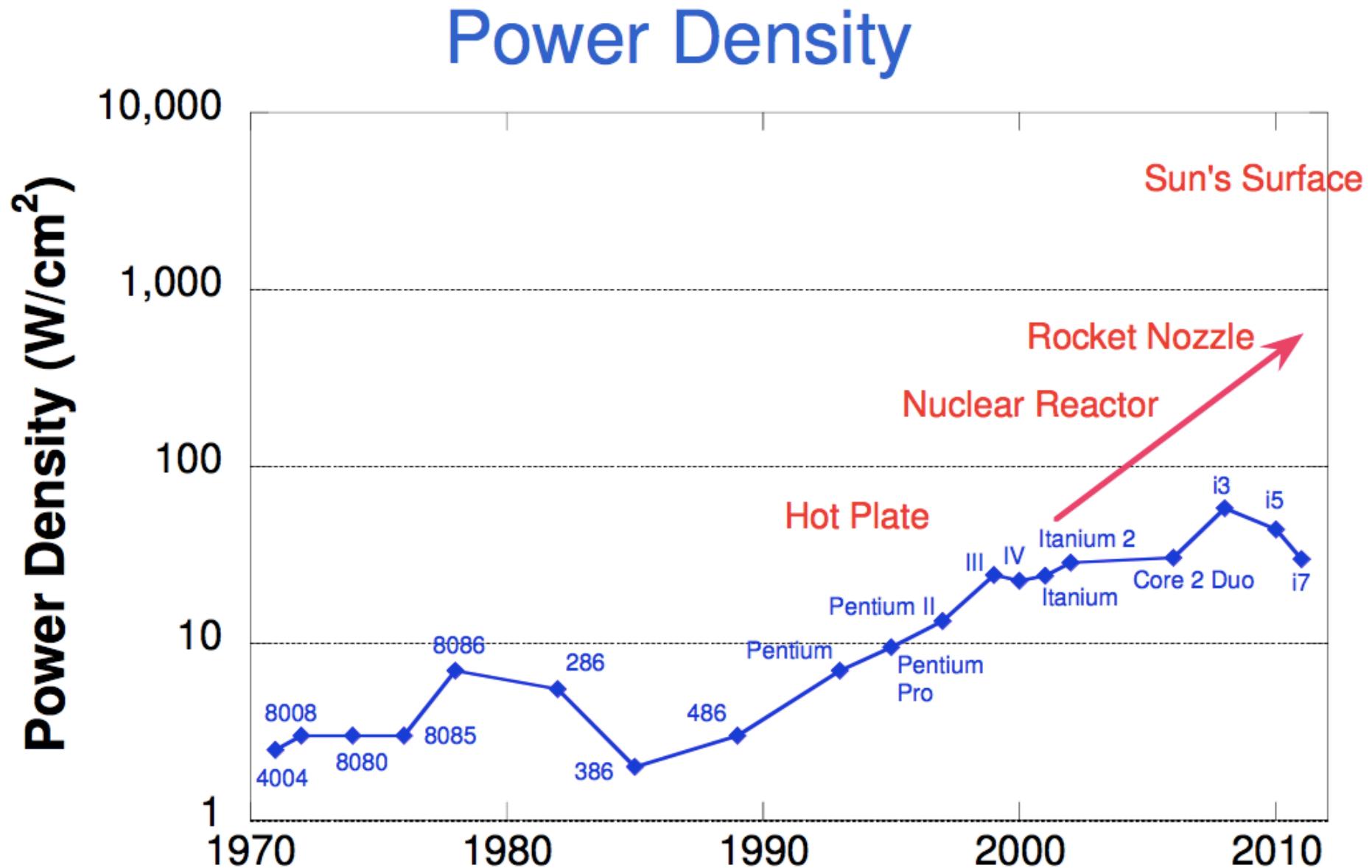
Traditional



22 nm



Sub-10 nm



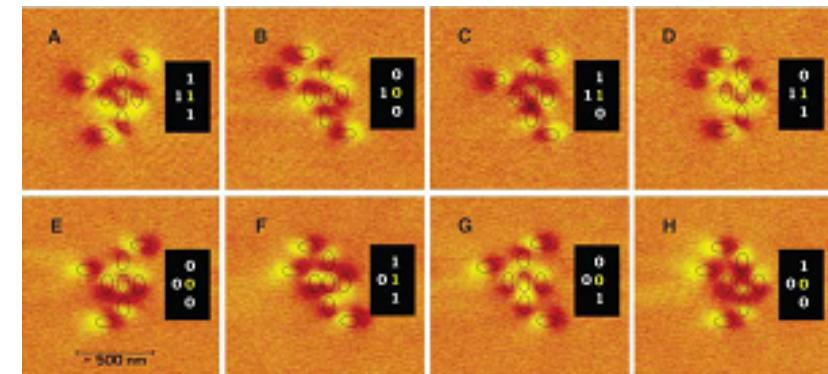
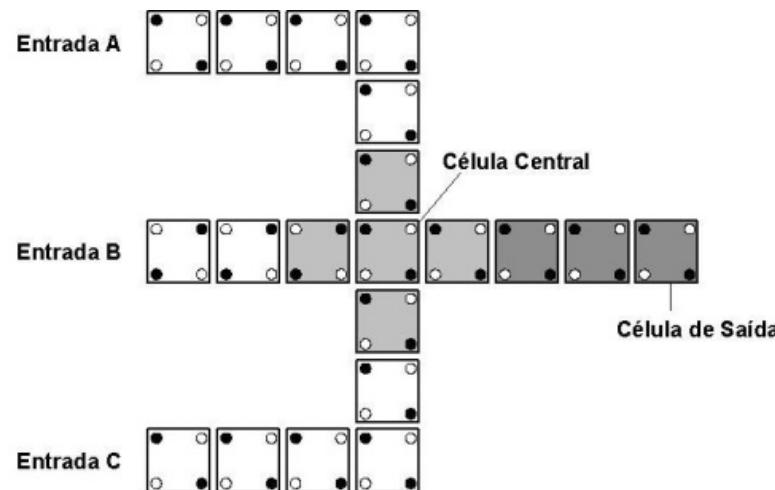
Beyond Silicon

Current technology based on Silicon is already at the nanoscale, but **it is close to the physical limit.**

What are the alternatives?

Quantum-Dot Cellular Automata - QCA

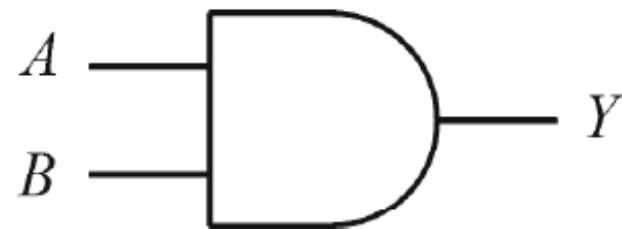
New paradigm of digital logic circuits for computing. Nanoscale; Information is transmitted without the flow of electric current (**Coulomb Interaction**); fast; low power dissipation.



Lent, Craig S., et al. "Quantum cellular automata." *Nanotechnology* 4.1 (1993): 49.

Reversible Computing

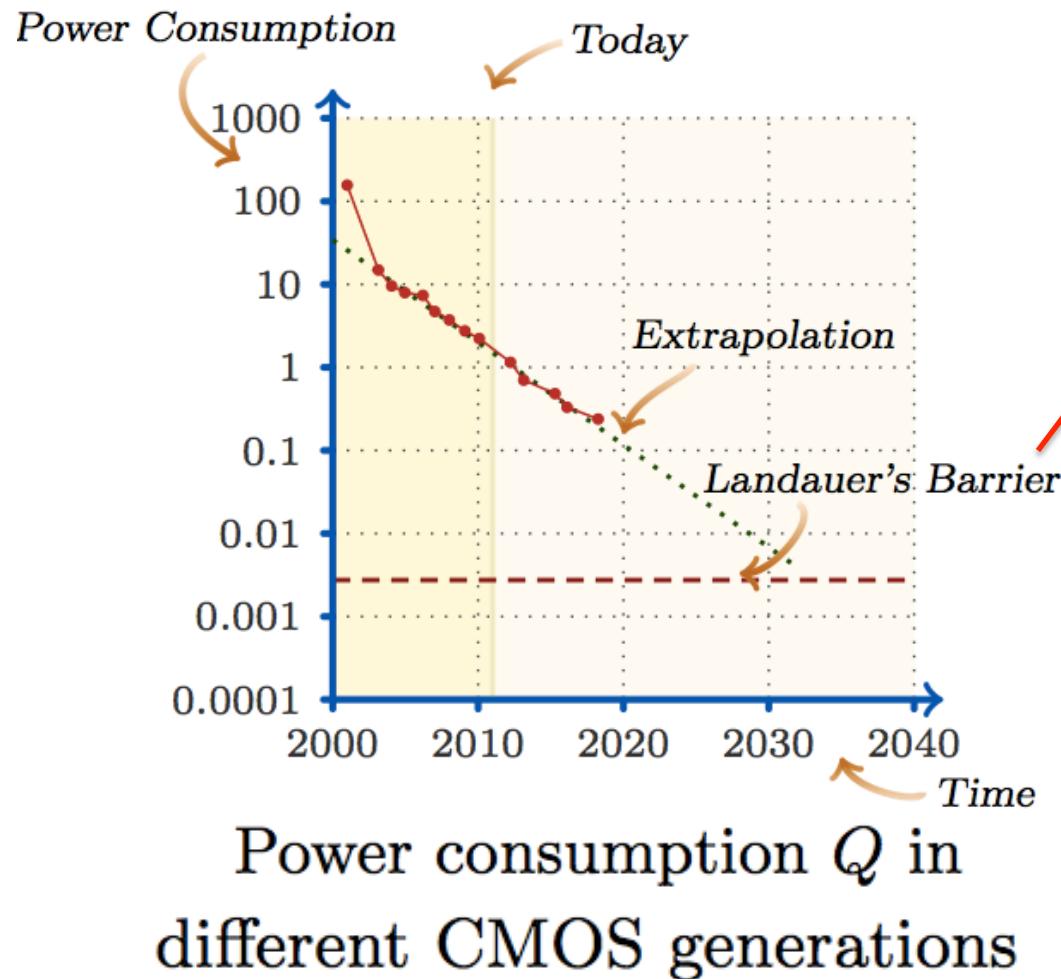
- In 1949, **John Von Neumann** estimate $k_B T \ln 2$ as the minimum dissipate energy per bit;
- In 1961, **Rolf Landauer** argued that the *erasure of information is a dissipative process*;



- The greatest portion of consumed energy by modern circuits aren't related to computation:
 - Clock;
 - Wires;
 - Repeaters;
 - Memories.

$$10^8 k_B T \ln 2$$

Reversible Computing



Bérut, Antoine, et al.
"Experimental verification of Landauer's principle linking information and thermodynamics."
Nature 483.7388 (2012): 187-189.

Drechsler, Rolf, and Robert Wille.
"Reversible circuits: Recent accomplishments and future challenges for an emerging technology." *Progress in VLSI Design and Test*. Springer Berlin Heidelberg, 2012. 383-392.

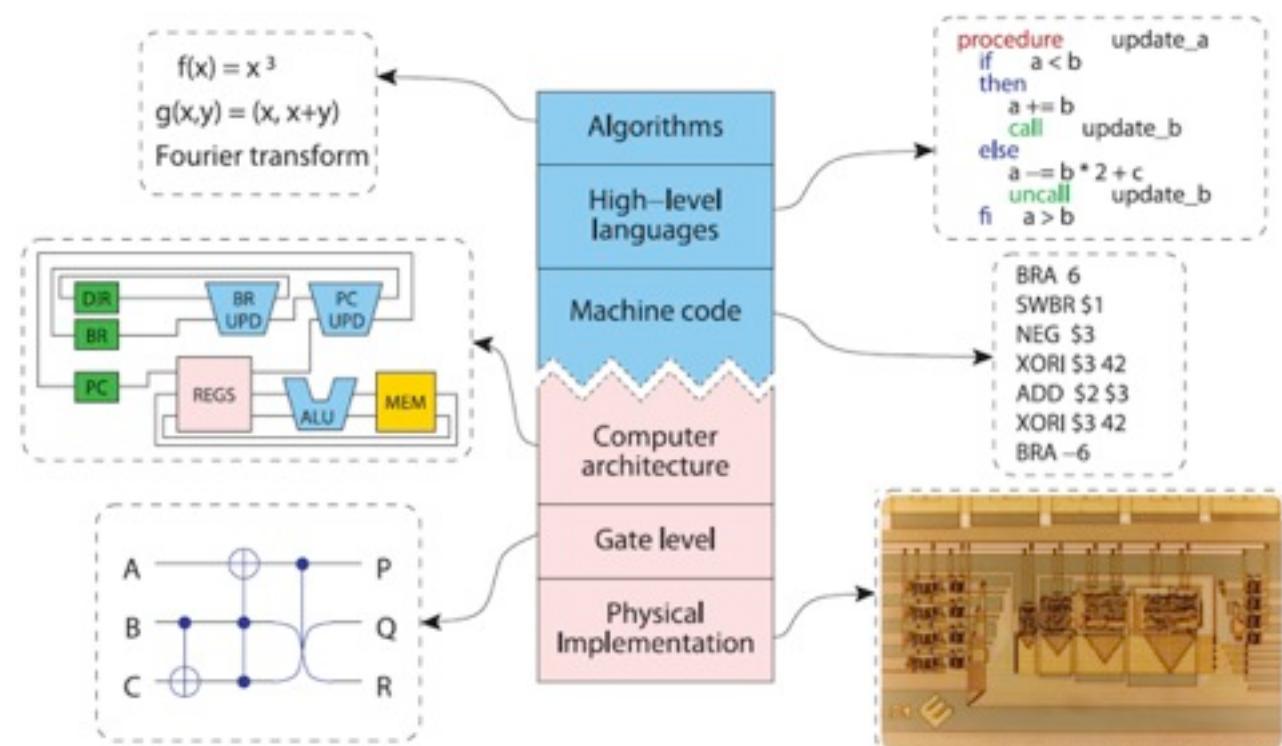
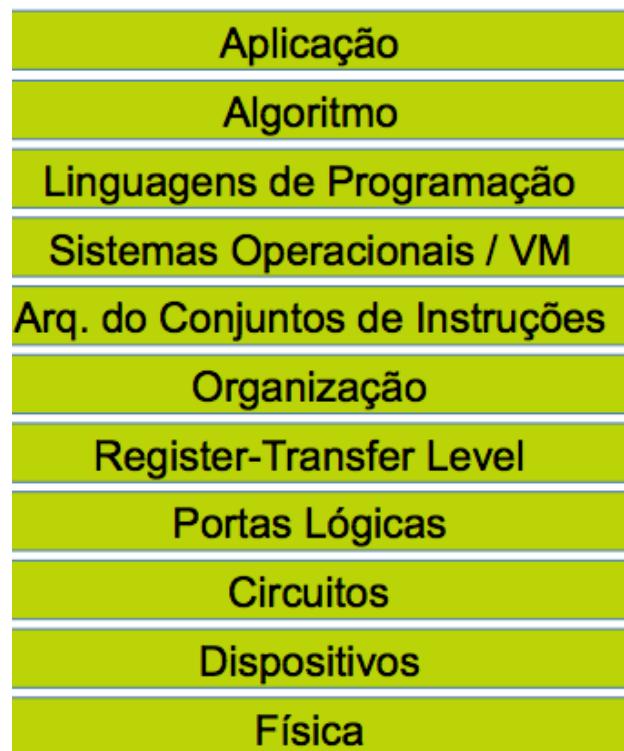
Reversible Computing

Is there a way to avoid the Landauer bound?

Reversible Computing

- One solution to avoid Landauer's limit is using trully reversible primitives for building digital systems. Toffoli and Fredkin proposed the first logically reversible gates in late 70s.
- Another possibility is design the computational machine as a Carnot heat engine.

Reversible Computing

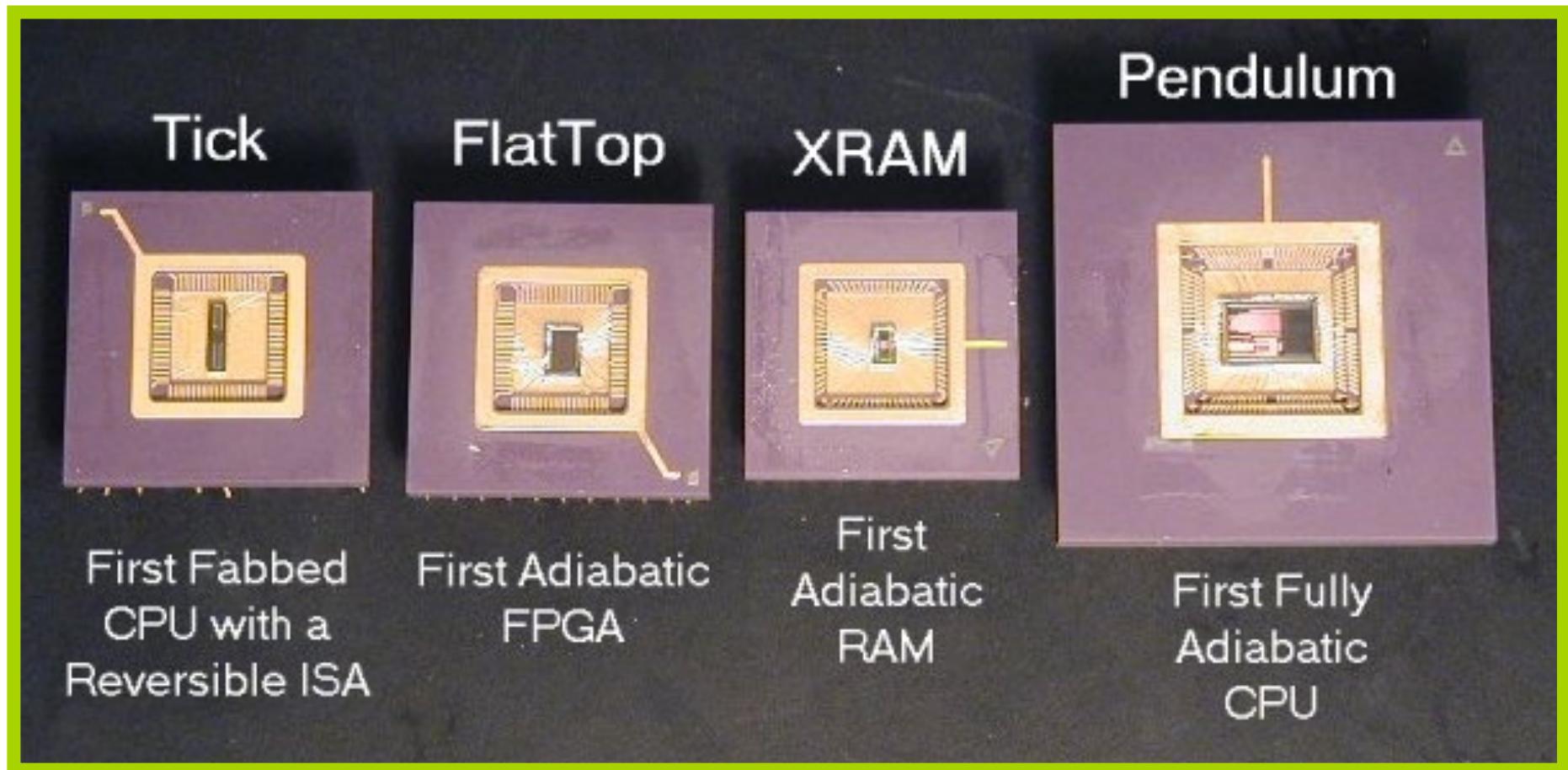


Applications

- Quantum computation
- **Future low-power computation**
- Adiabatic circuits
- Encoding and decoding devices
- Program inversion

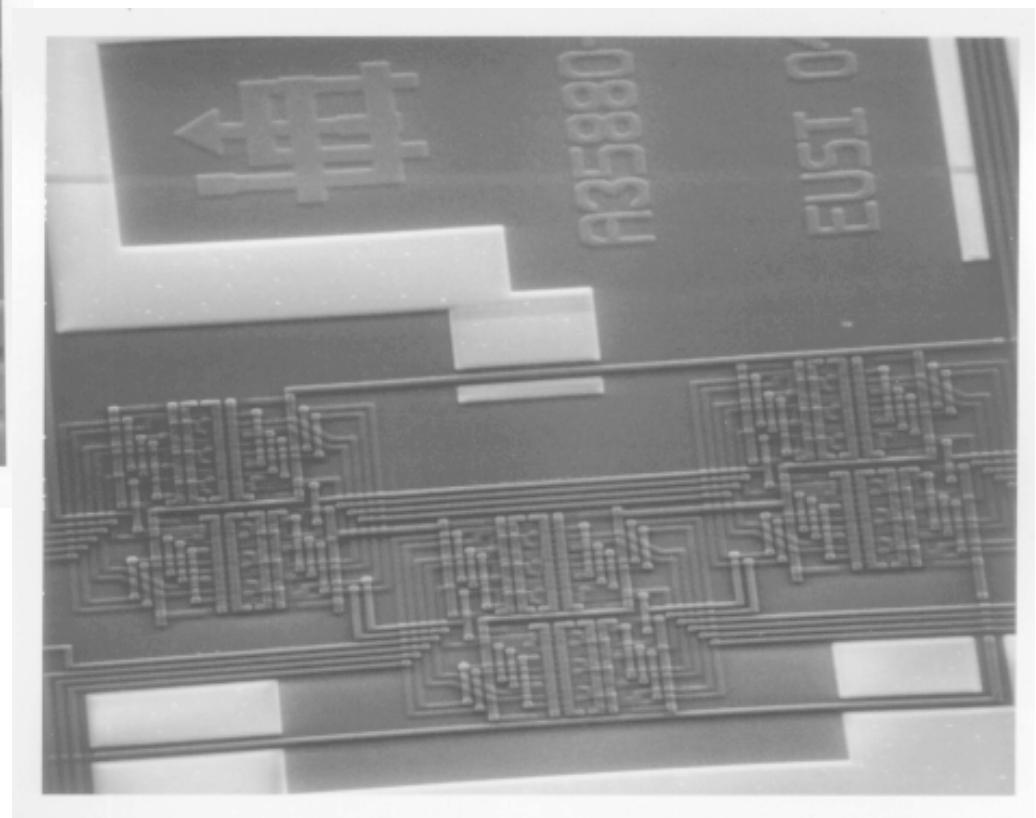
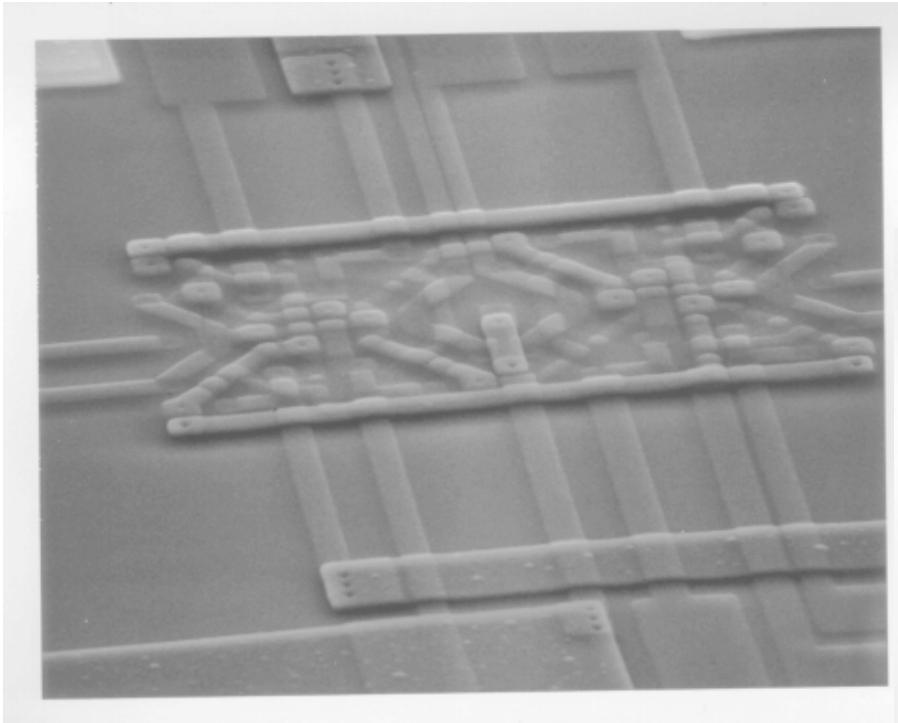
Reversible / Adiabatic Chips Designed @ MIT, 1996-1999

By the author and other then-students in the MIT Reversible Computing group,
under AI/LCS lab members Tom Knight and Norm Margolus.



Reversible / Adiabatic Chips

Designed @ U Ghent (Belgium, 2005 -)



APPLIED PHYSICS LETTERS **105**, 113109 (2014)



Enhanced architectures for room-temperature reversible logic gates in graphene

Daniela Dragoman¹ and Mircea Dragoman²

¹*Physics Faculty, University of Bucharest, P.O. Box MG-11, 077125 Bucharest, Romania*

²*National Institute for Research and Development in Microtechnology (IMT), P.O. Box 38-160, 023573 Bucharest, Romania*

(Received 16 July 2014; accepted 5 September 2014; published online 18 September 2014)

OPEN

Reversible logic gate using adiabatic superconducting devices

SUBJECT AREAS:

APPLIED PHYSICS

ELECTRICAL AND ELECTRONIC
ENGINEERING

COMPUTER SCIENCE

Received
17 June 2014Accepted
26 August 2014Published
15 September 2014

N. Takeuchi, Y. Yamanashi & N. Yoshikawa

Department of Electrical and Computer Engineering, Yokohama National University, Hodogaya, Yokohama 240-8501, Japan.

Reversible computing has been studied since Rolf Landauer advanced the argument that has come to be known as Landauer's principle. This principle states that there is no minimum energy dissipation for logic operations in reversible computing, because it is not accompanied by reductions in information entropy. However, until now, no practical reversible logic gates have been demonstrated. One of the problems is that reversible logic gates must be built by using extremely energy-efficient logic devices. Another difficulty is that reversible logic gates must be both logically and physically reversible. Here we propose the first practical reversible logic gate using adiabatic superconducting devices and experimentally demonstrate the logical and physical reversibility of the gate. Additionally, we estimate the energy dissipation of the gate, and discuss the minimum energy dissipation required for reversible logic operations. It is expected that the results of this study will enable reversible computing to move from the theoretical stage into practical usage.

LETTER

doi:10.1038/nature15263

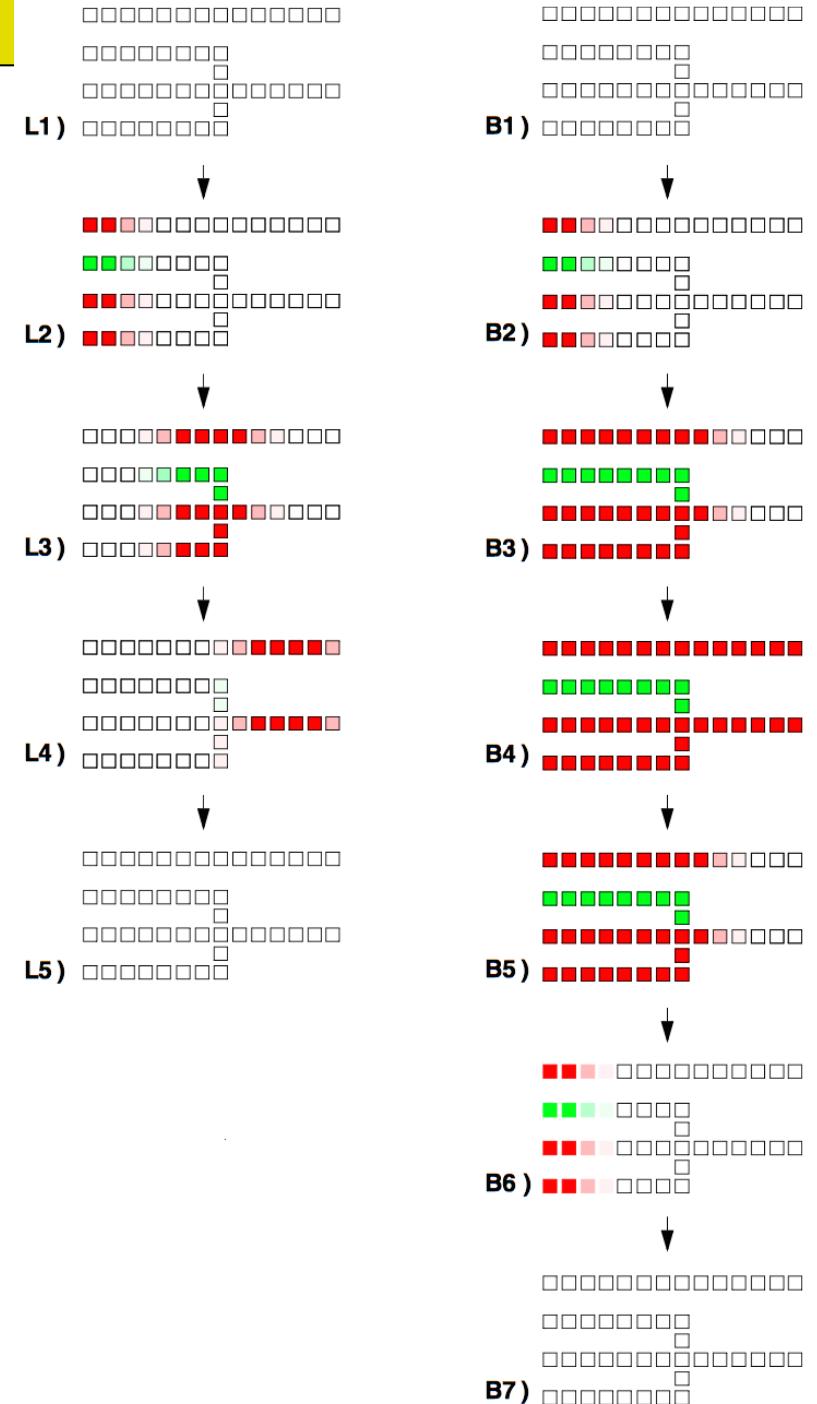
A two-qubit logic gate in silicon

M. Veldhorst¹, C. H. Yang¹, J. C. C. Hwang¹, W. Huang¹, J. P. Dehollain¹, J. T. Muhonen¹, S. Simmons¹, A. Laucht¹, F. E. Hudson¹, K. M. Itoh², A. Morello¹ & A. S. Dzurak¹

Implementing a Quantum CNOT and Quantum Memory Using a Quantum-Dot Cellular Automata Array

Seyed Arash Sheikholeslam, and Konrad Walus, *Member, IEEE*

Lent and collaborators proposed the alternative clock system called Bennett.



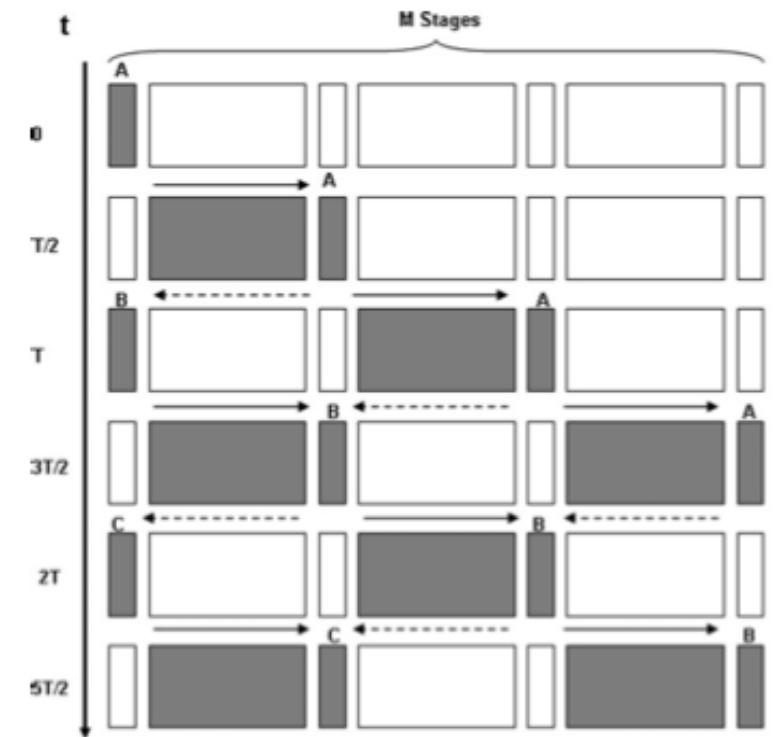
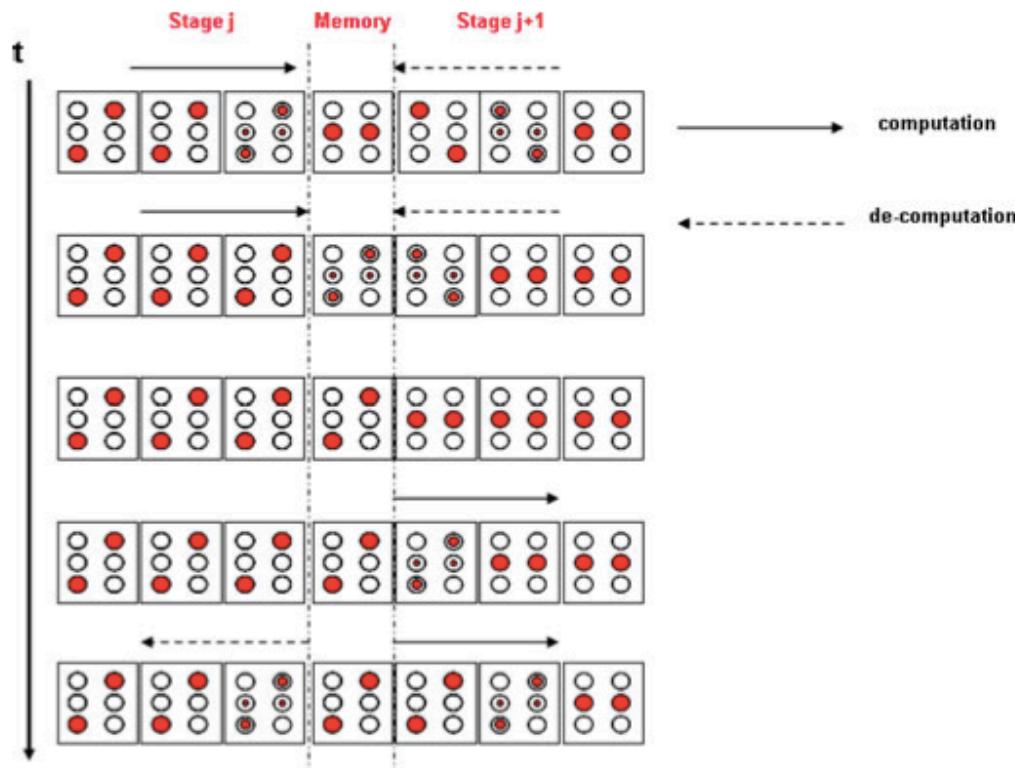
Lent, Craig S., Mo Liu, and Yuhui Lu. "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling." *Nanotechnology* 17.16 (2006): 4240.

IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 10, NO. 6, NOVEMBER 2011

Partially Reversible Pipelined QCA Circuits: Combining Low Power With High Throughput

Marco Ottavi, *Senior Member, IEEE*, Salvatore Pontarelli, Erik P. DeBenedictis, *Member, IEEE*,
Adelio Salsano, *Life Member, IEEE*, Sarah Frost-Murphy, Peter M. Kogge, *Fellow, IEEE*,
and Fabrizio Lombardi, *Fellow, IEEE*

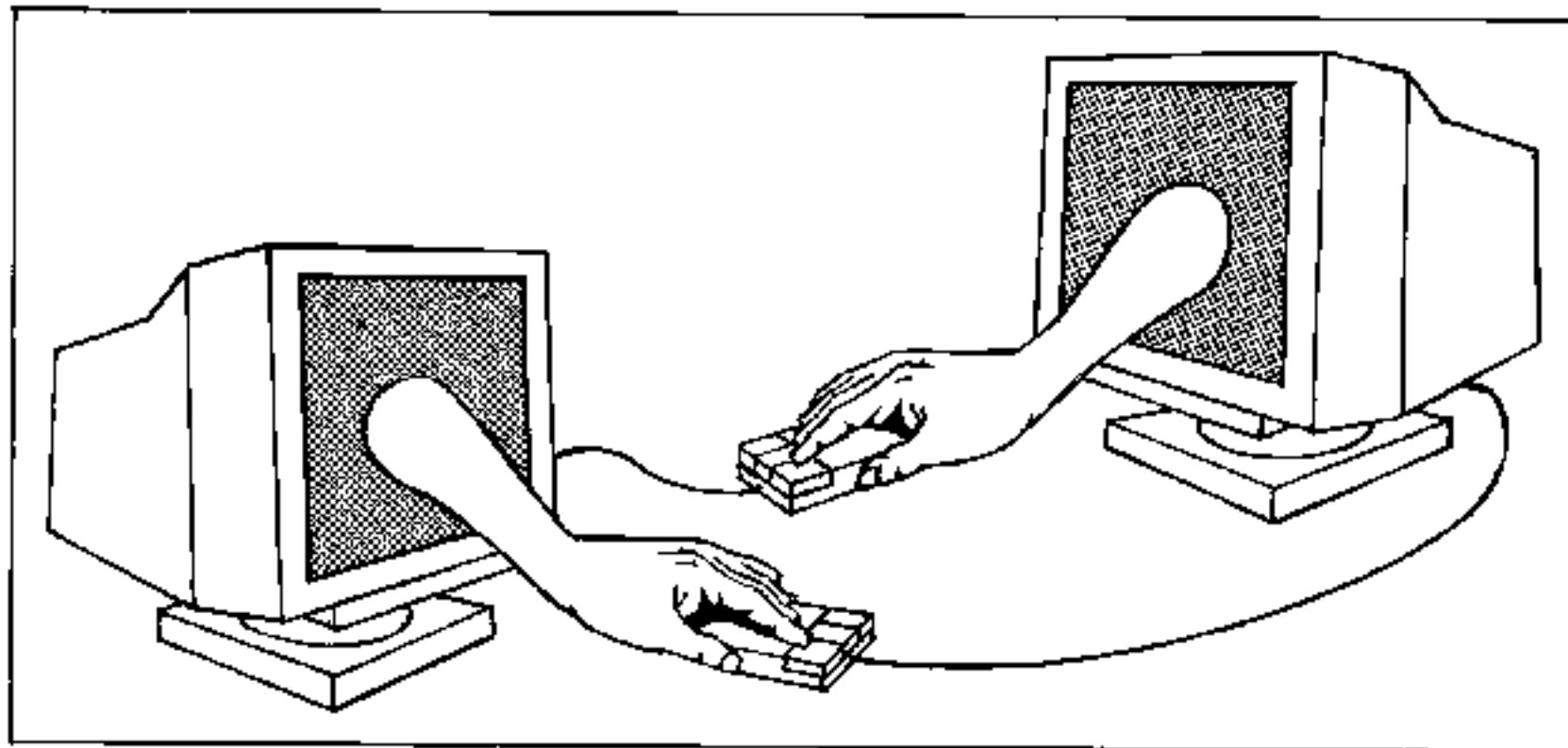
Ottavi and others proposed a partially reversible pipelined Bennett clocking strategy for controllable balancing throughput and dissipation in QCA circuits.



- **Lógica Reversível:**

- **Mapeamento um-para-um** entre entrada e saída;
 - Propriedade Bijetora;
 - Primitivas logicamente reversíveis (invertíveis);

- Computação Reversível
 - Vai e volta.



Computação Geral

- Baseada em:
 - Armazenamento;
 - Transmissão;
 - Processamento discreto de sinais.

Qualquer escolha de primitivas deve incluir blocos construtores para estas atividades computacionais.

Computação Reversível

- O Fio Unitário:

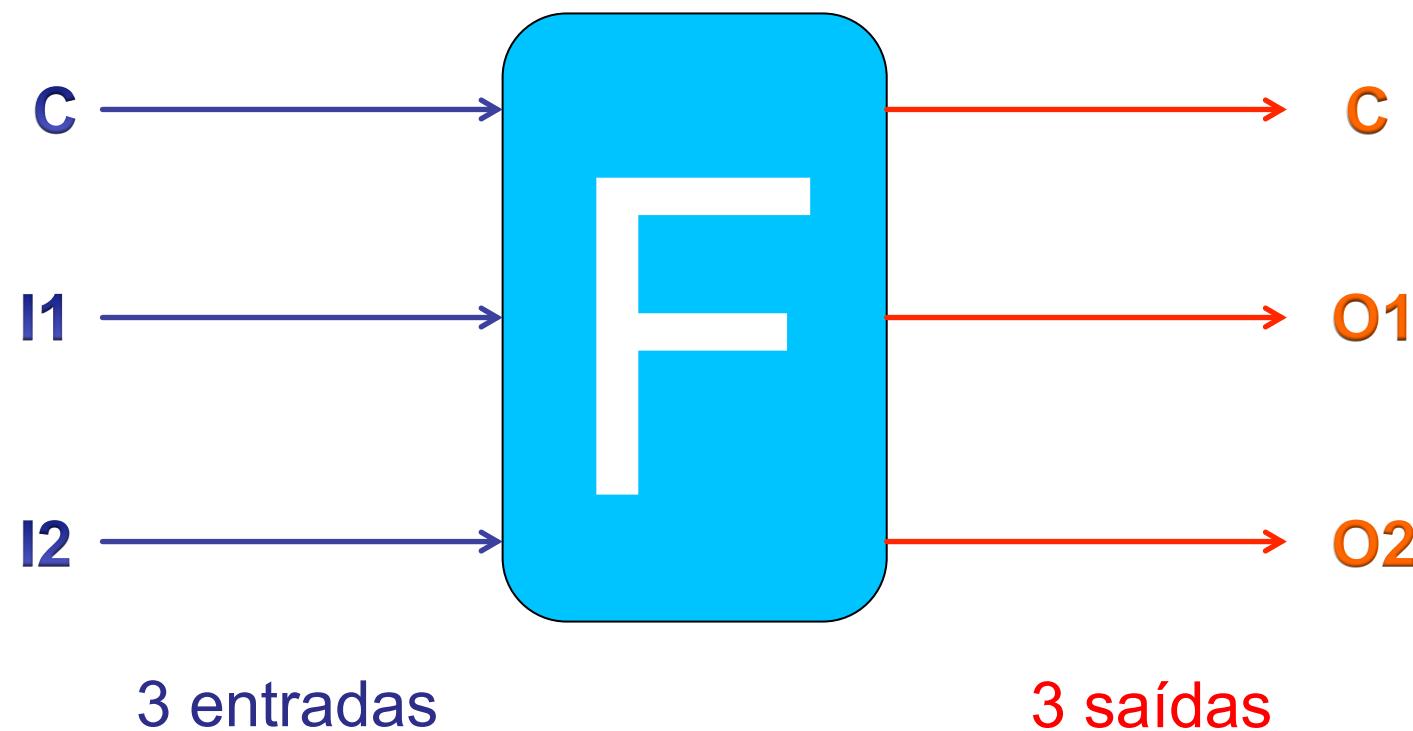
- Considere 2 Pontos (P0 e P1) no Espaço-Tempo.
 - Se P0 e P1 estão separados espacialmente, isto é uma transmissão;
 - Se P0 e P1 estão no mesmo local, isto é um armazenamento.

$$\begin{array}{ccc} x^t & \rightarrow & y^{t+1} \\ 0 & & 0 \\ 1 & & 1 \end{array}$$

$$x^t \rightarrow -y^t = x^{t-1}$$

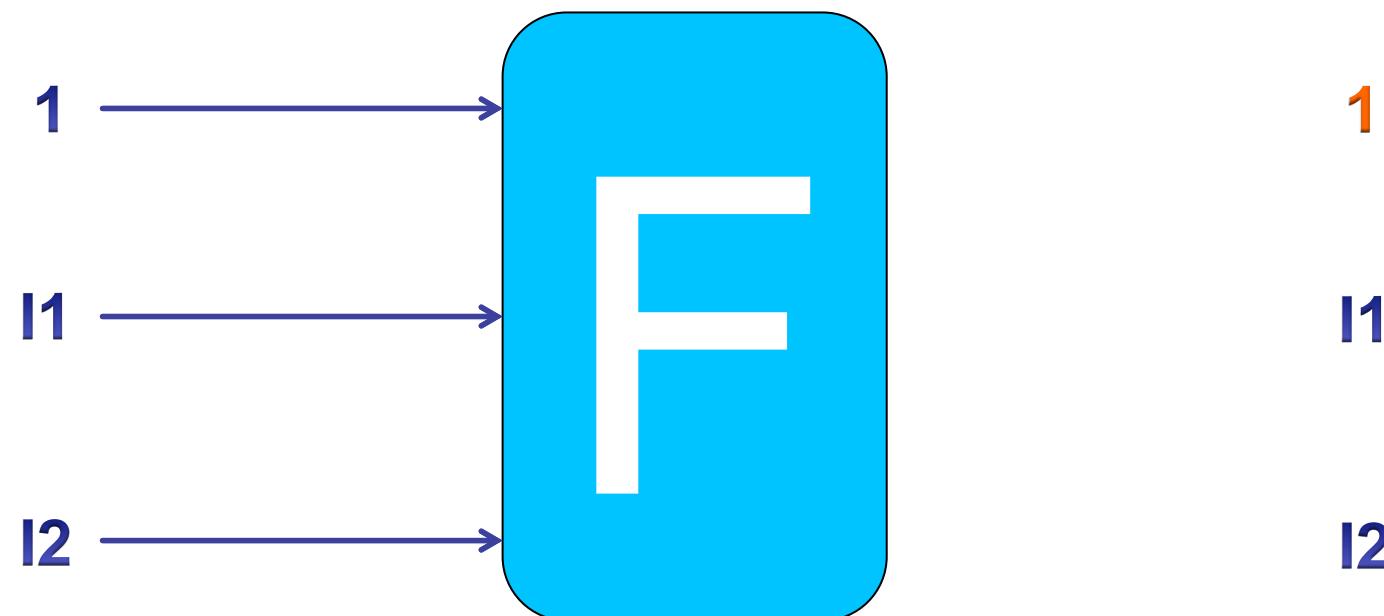
Computação Reversível

- Porta Fredkin:



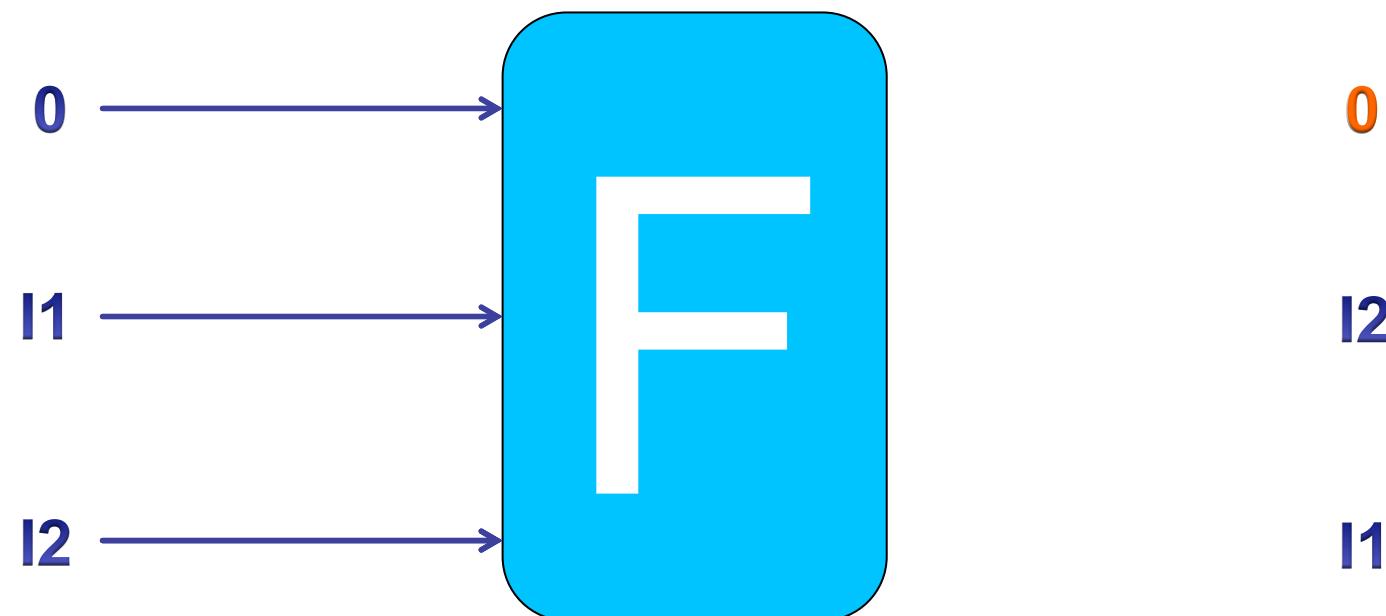
Computação Reversível

- Porta Fredkin: Funcionamento



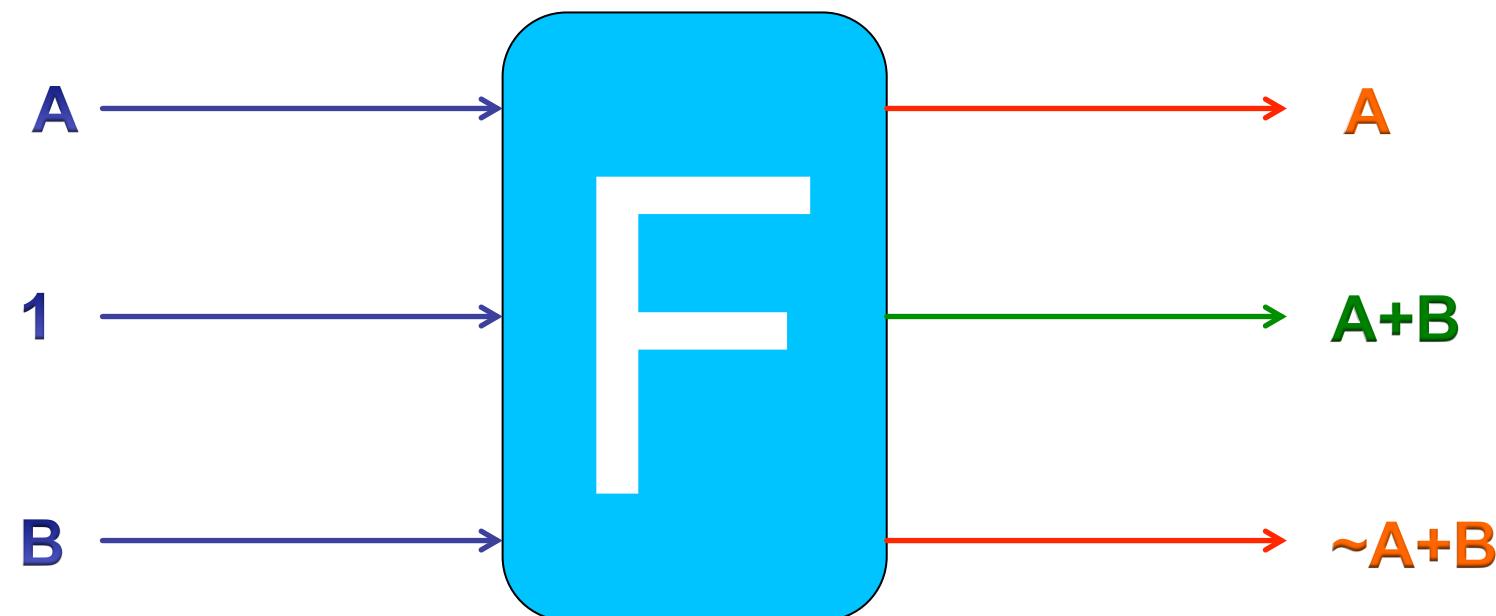
Computação Reversível

- Porta Fredkin: Funcionamento



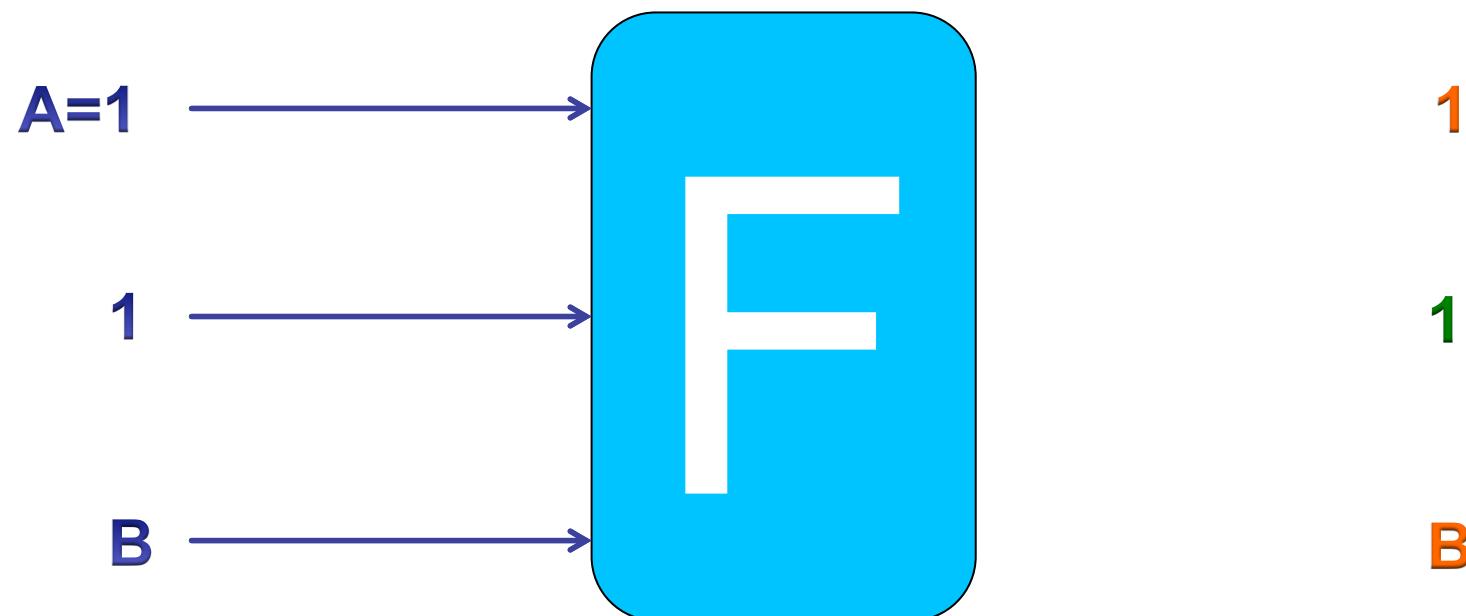
Computação Reversível

- Porta Fredkin: **UNIVERSAL**



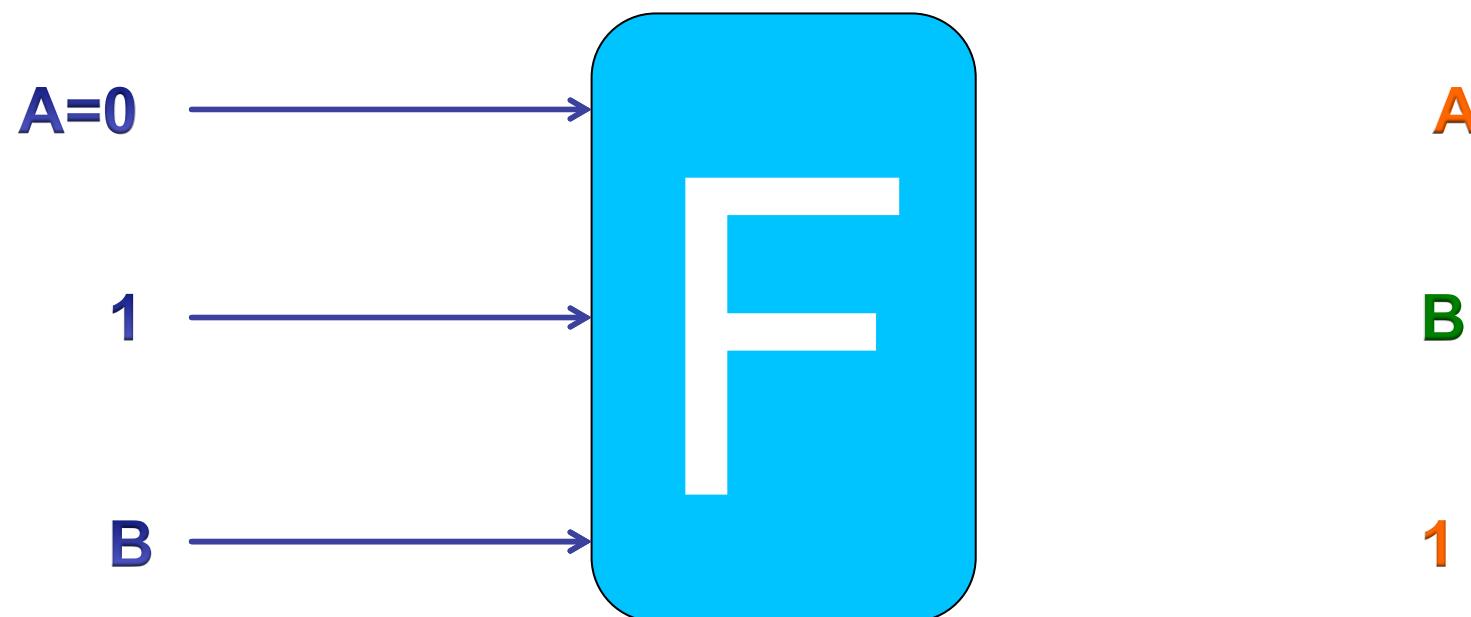
Computação Reversível

- Porta Fredkin: OR



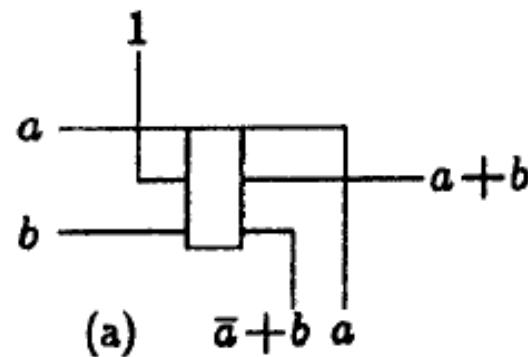
Computação Reversível

- Porta Fredkin: OR

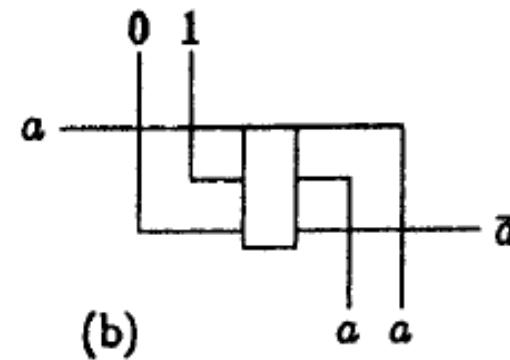


Computação Reversível

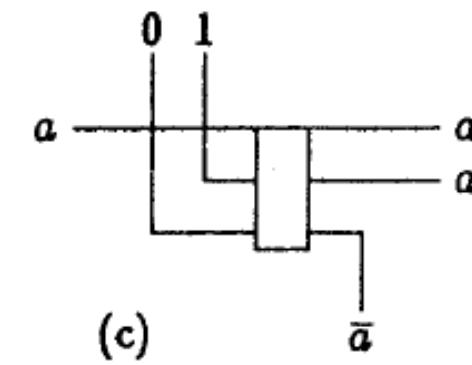
- Circuitos Lógicos Conservativos:



Porta OR



Porta NOT



Porta FAN-OUT

Computação Reversível

- Outras portas:

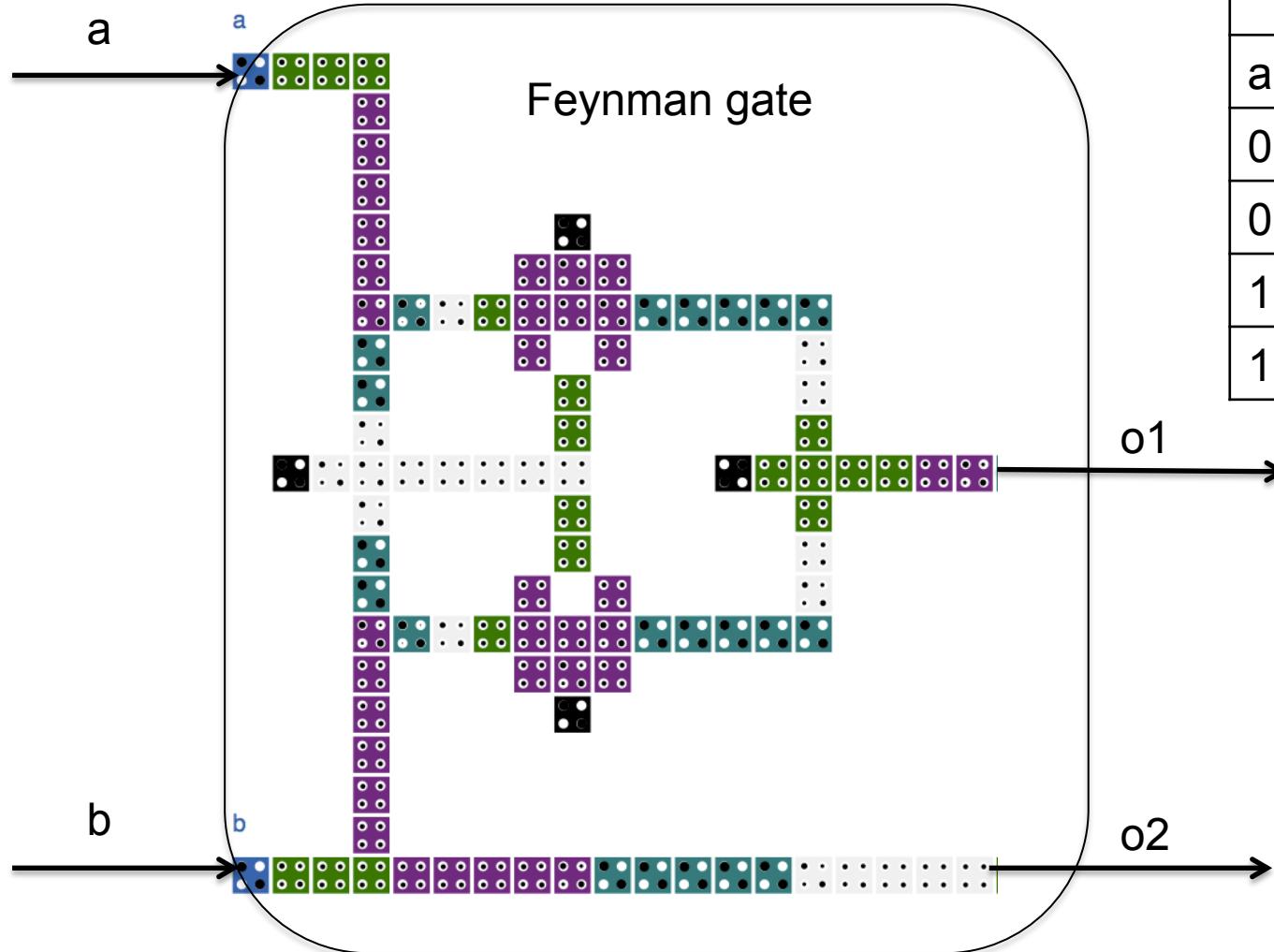
- Toffoli

- Feynman

- etc

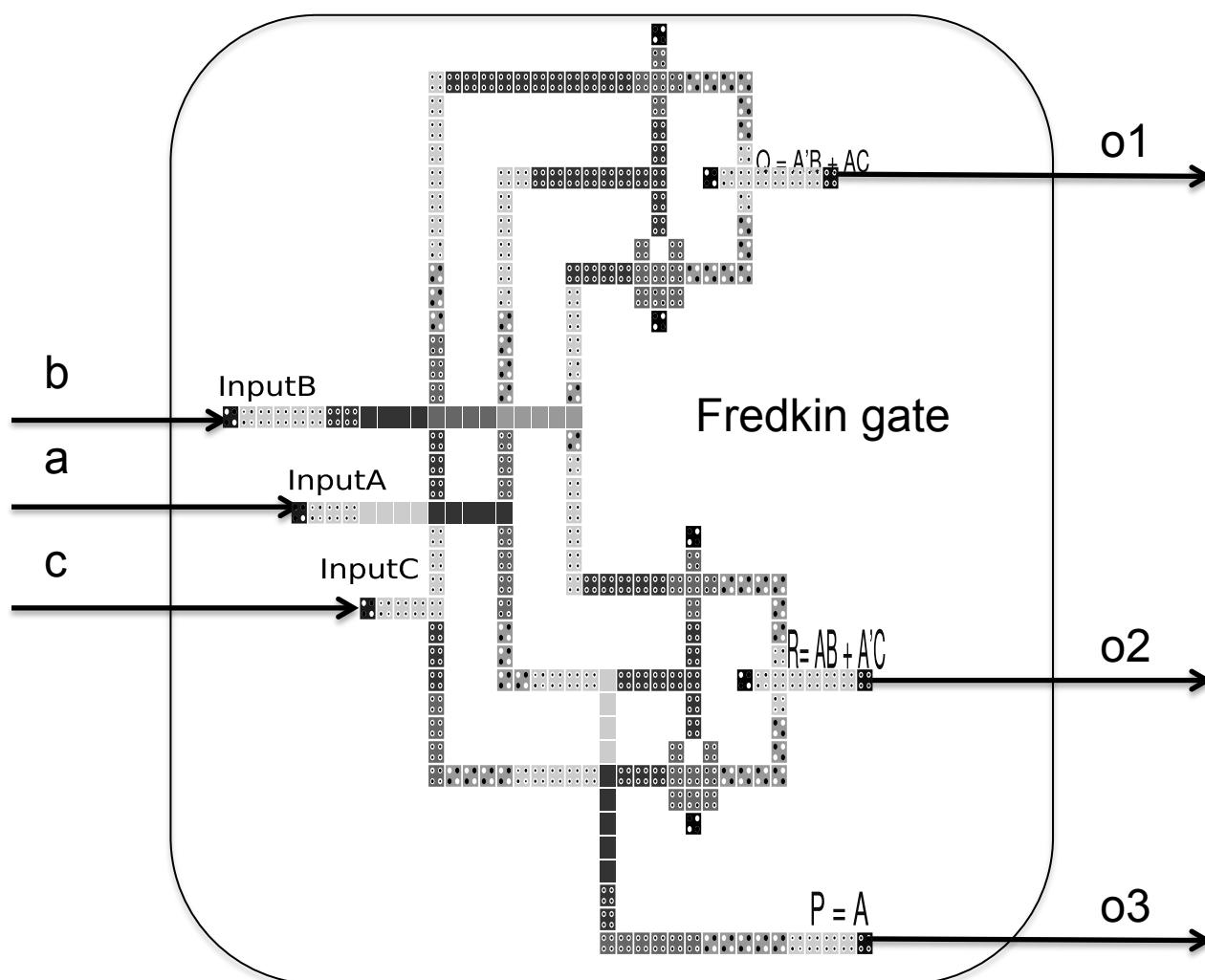
Lógica Reversível e QCA

Reversible Gates



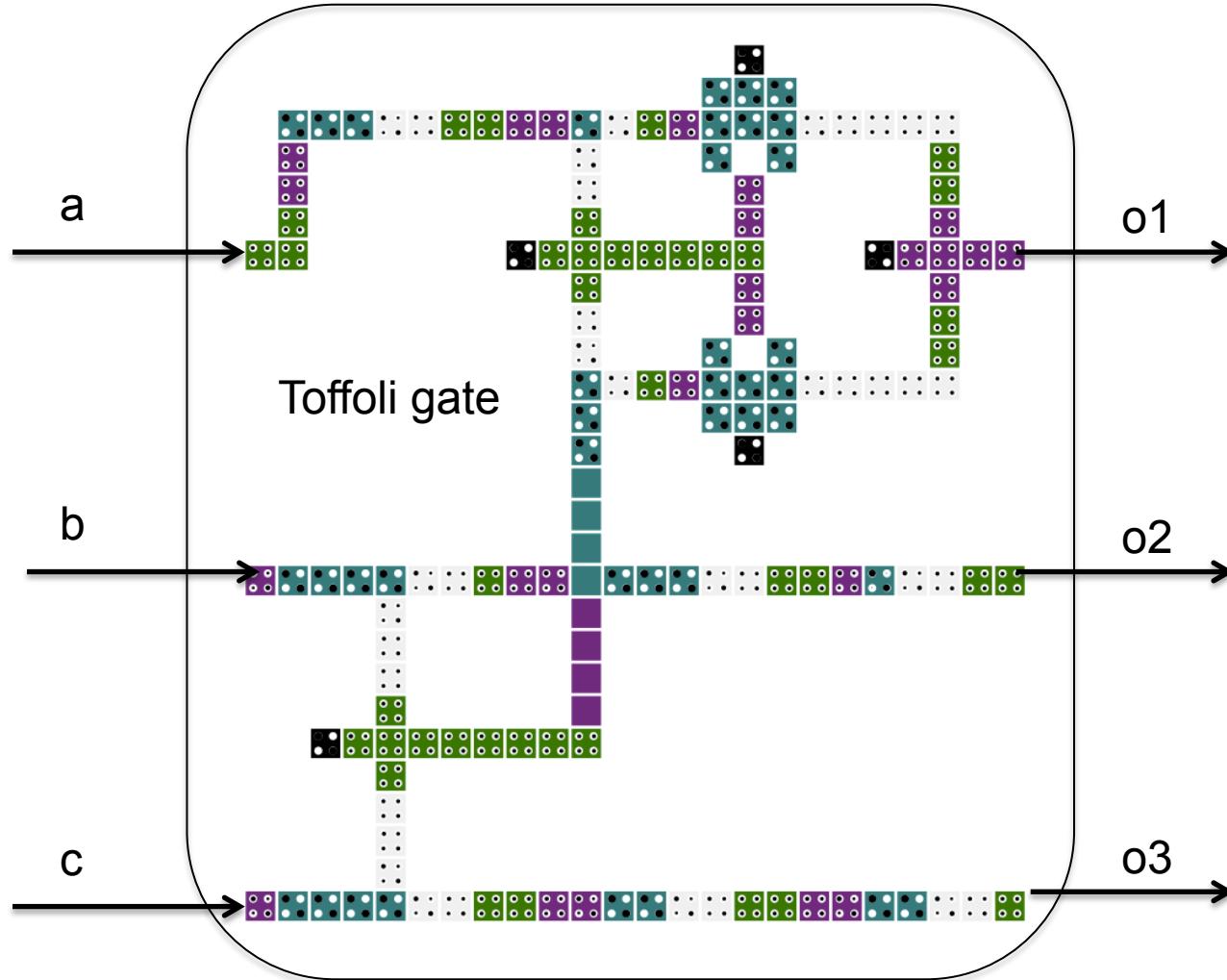
Inputs		Outputs	
a	b	$o1$	$o2$
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

Reversible Gates



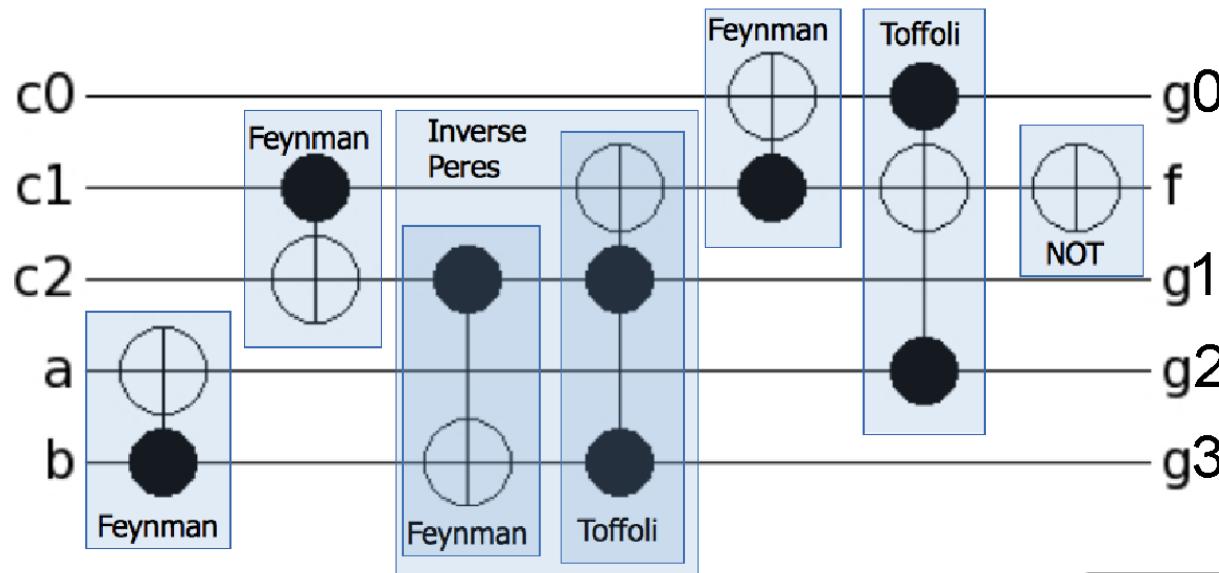
Inputs			Outputs		
a	b	c	$o1$	$o2$	$o3$
0_{10}			0_{10}		
1_{10}			2_{10}		
2_{10}			4_{10}		
3_{10}			6_{10}		
4_{10}			1_{10}		
5_{10}			5_{10}		
6_{10}			3_{10}		
7_{10}			7_{10}		

Reversible Gates



Inputs			Outputs		
<i>a</i>	<i>b</i>	<i>c</i>	<i>o</i> ₁	<i>o</i> ₂	<i>o</i> ₃
0 ₁₀			0 ₁₀		
1 ₁₀			1 ₁₀		
2 ₁₀			2 ₁₀		
3 ₁₀			7 ₁₀		
4 ₁₀			4 ₁₀		
5 ₁₀			5 ₁₀		
6 ₁₀			6 ₁₀		
7 ₁₀			3 ₁₀		

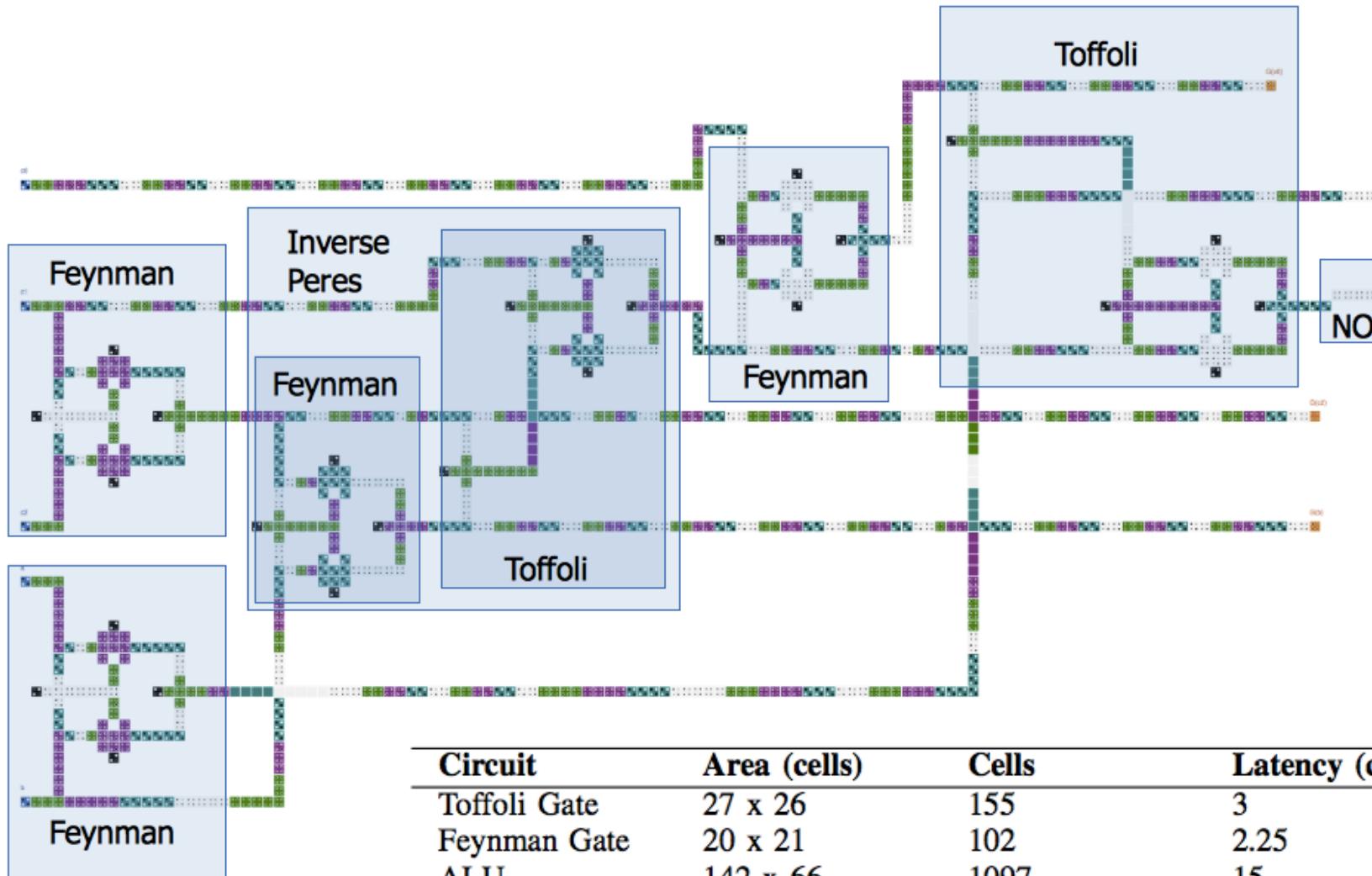
Reversible ALU



Wille, R., Große, D., Teuber, L., Dueck, G. W., & Drechsler, R. "RevLib: An online resource for reversible functions and reversible circuits." *Multiple Valued Logic, 2008. ISMVL 2008. 38th International Symposium on*. IEEE, 2008.

c0	c1	c2	Function (f)
0	0	0	constant 1
0	0	1	$a \text{ OR } b$
0	1	0	$a \text{ NAND } b$
0	1	1	$a \text{ XOR } b$
1	0	0	$a \text{ NXOR } b$
1	0	1	$a \text{ AND } b$
1	1	0	$a \text{ NOR } b$
1	1	1	constant 0

Reversible ALU

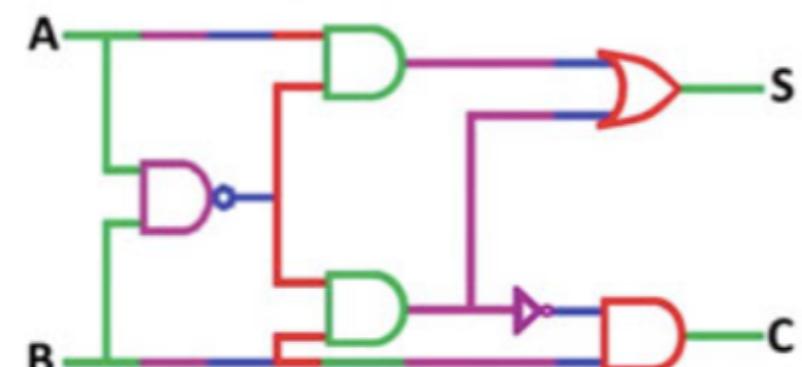
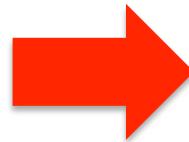
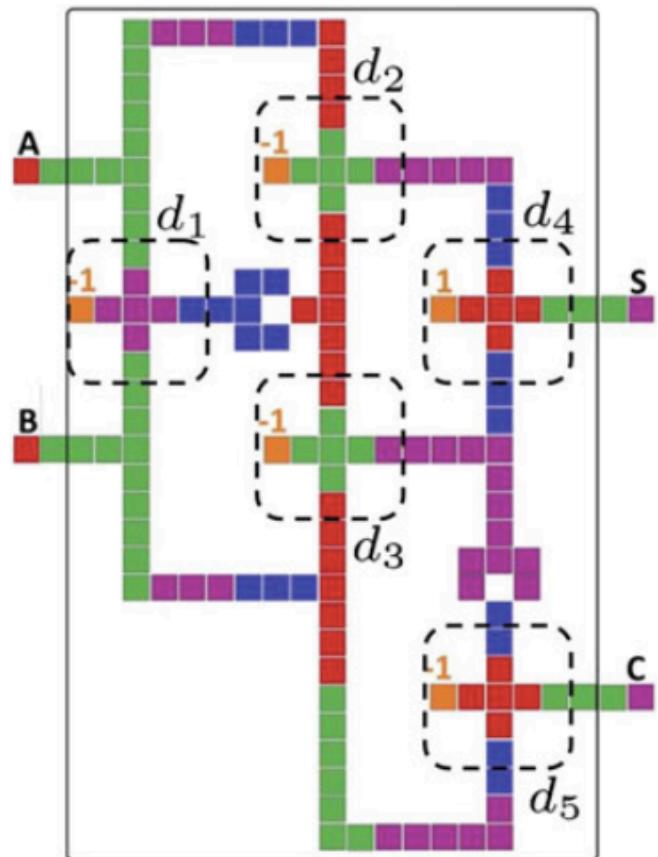


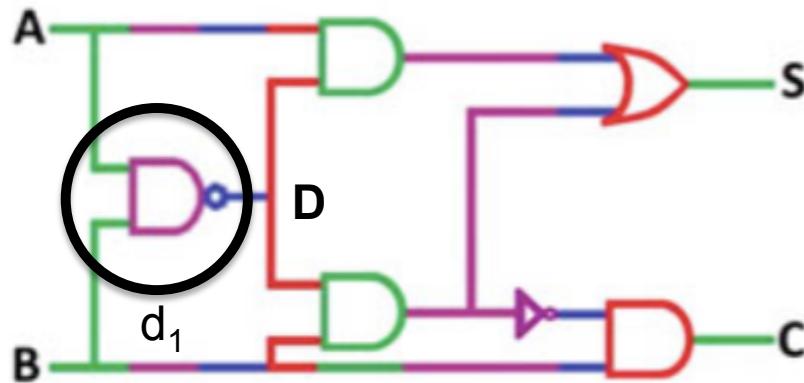
Modular Dissipation Analysis for QCA

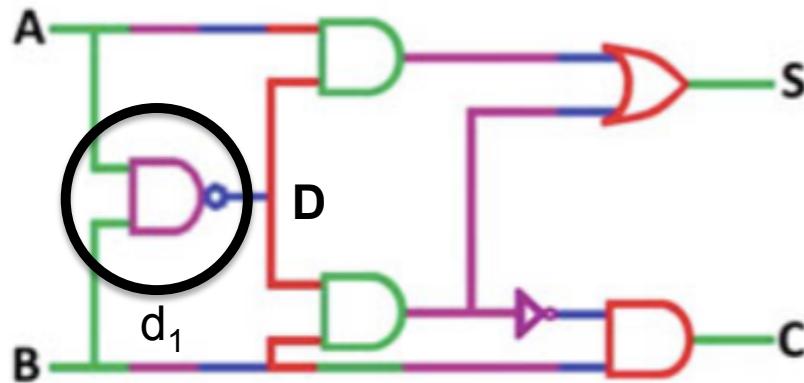
İlke Ercan and Neal G. Anderson^(✉)

Department of Electrical and Computer Engineering,
University of Massachusetts Amherst, Amherst, MA, USA
{iercan, anderson}@ecs.umass.edu

In "*Field-Coupled Nanocomputing*". Springer Berlin Heidelberg, 2014. 357-375.

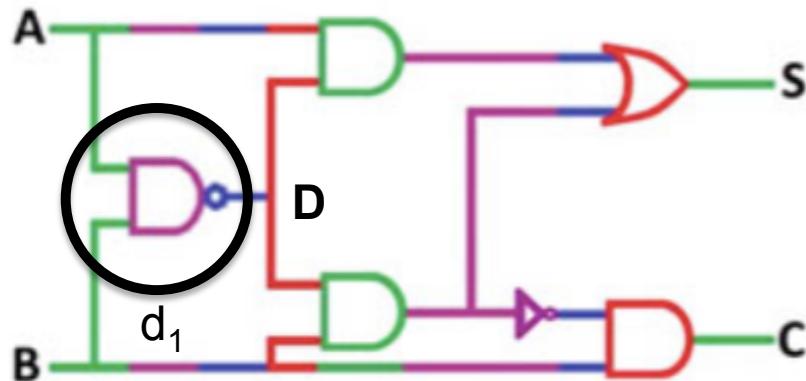




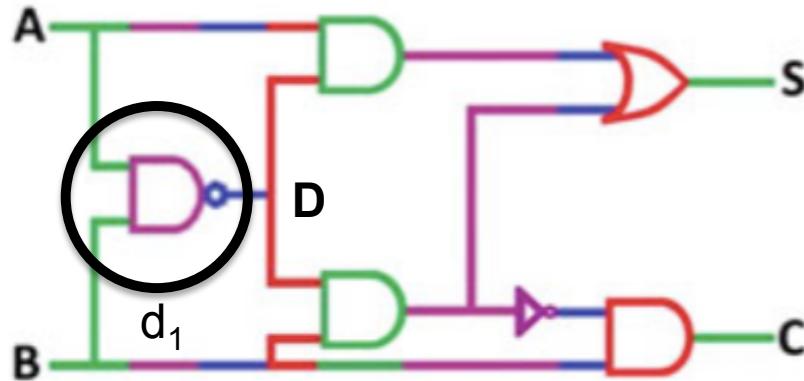


Self Information:

$$-\log_2 P(x_i)$$



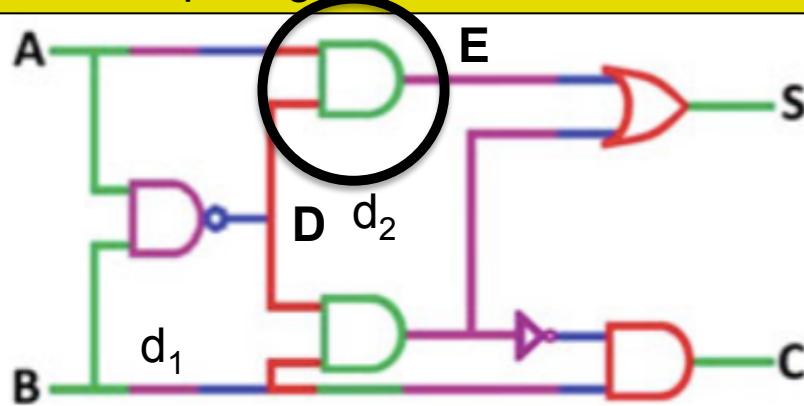
Information Entropy:
weighted arithmetic mean
using probability as a weigh

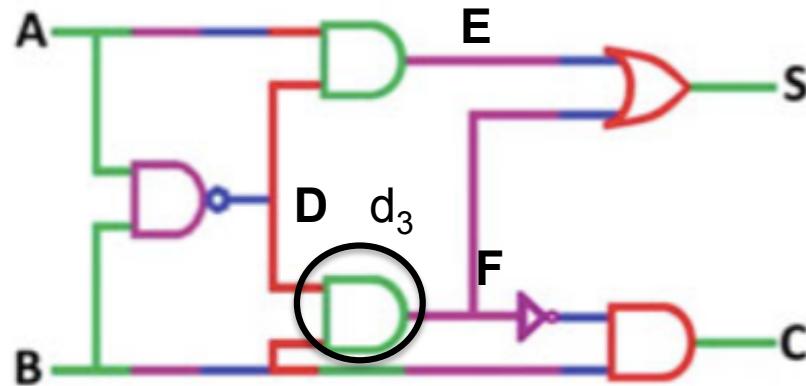


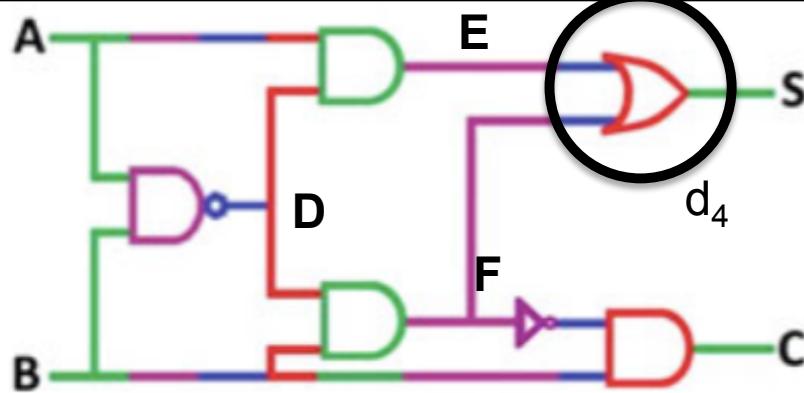
Ercan outline a general approach to determine the lower bounds on dissipative cost of computation

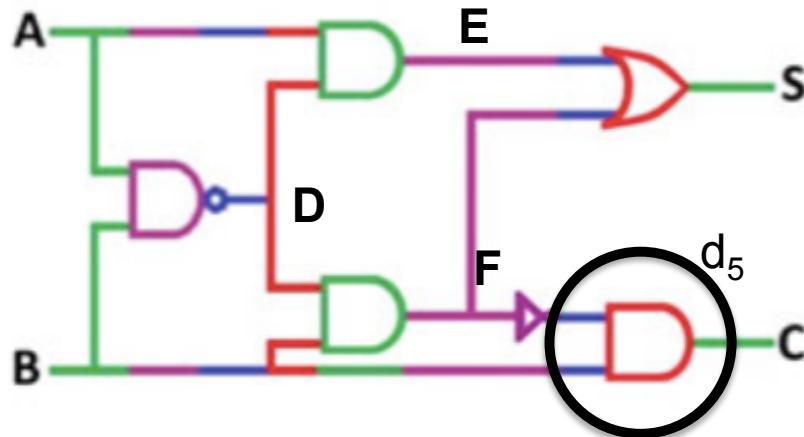
INPUT					OUTPUT				
A	B	P(x _i)	Self Information	Information Entropy	D	P(y _i)	Self Information	Information Entropy	
0	0	1/4	2	0.5	1	3/4	0.415	0.3113	
0	1	1/4	2	0.5	1				
1	0	1/4	2	0.5	1				
1	1	1/4	2	0.5	0	1/4	2	0.5	
Information Entropy H(x)				2	Information Entropy H(y)				0.8113
Entropy = H(x) - H(y) = 1.19 bits									

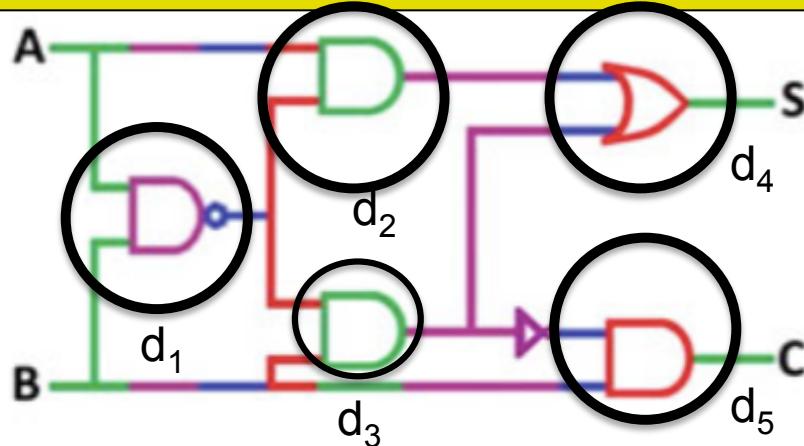
$$\Delta E = TS = 1.19k_B T \ln 2 \approx 3.3 \text{zJ at room temperature}$$











and evaluating the five required conditional entropies, we have

$$\Delta \langle E^{\mathcal{B}} \rangle_{d_1} \geq 1.1887k_B T \ln(2)$$

$$\Delta \langle E^{\mathcal{B}} \rangle_{d_2} \geq 0.6887k_B T \ln(2)$$

$$\Delta \langle E^{\mathcal{B}} \rangle_{d_3} \geq 0.6887k_B T \ln(2)$$

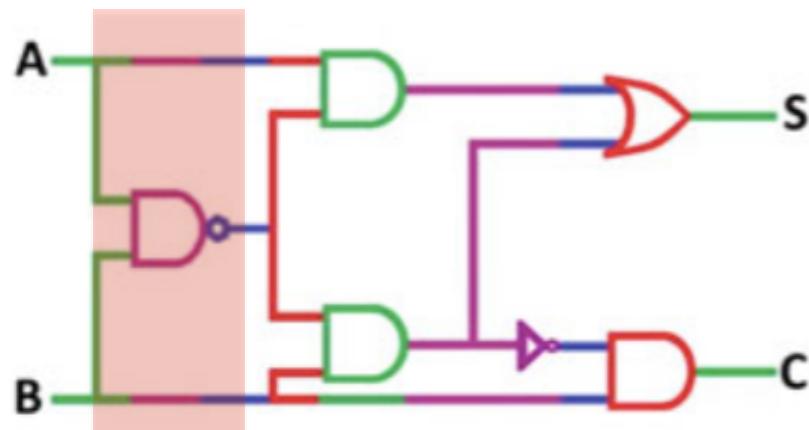
$$\Delta \langle E^{\mathcal{B}} \rangle_{d_4} \geq 0.5k_B T \ln(2)$$

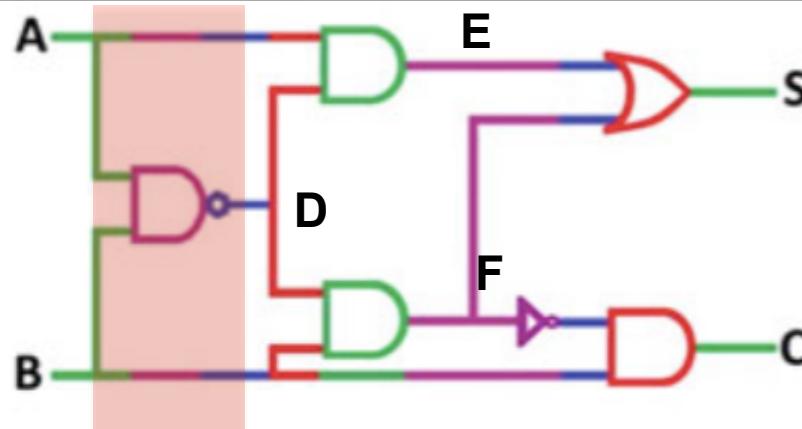
$$\Delta \langle E^{\mathcal{B}} \rangle_{d_5} \geq 0.6887k_B T \ln(2)$$

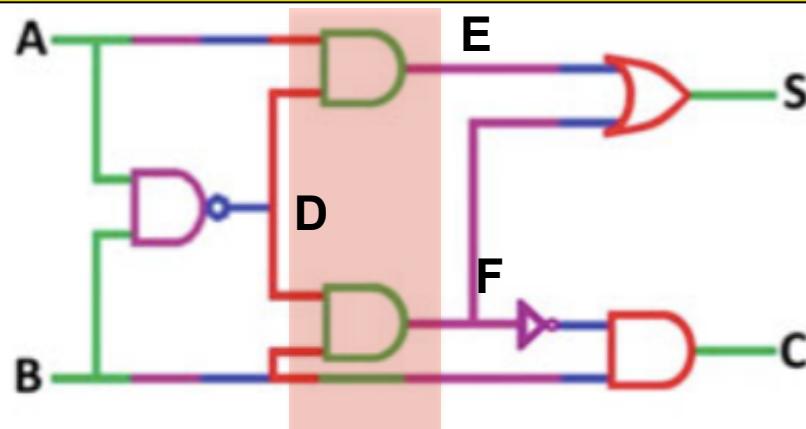
for the five dissipation zones. Summing these results, we obtain the bound

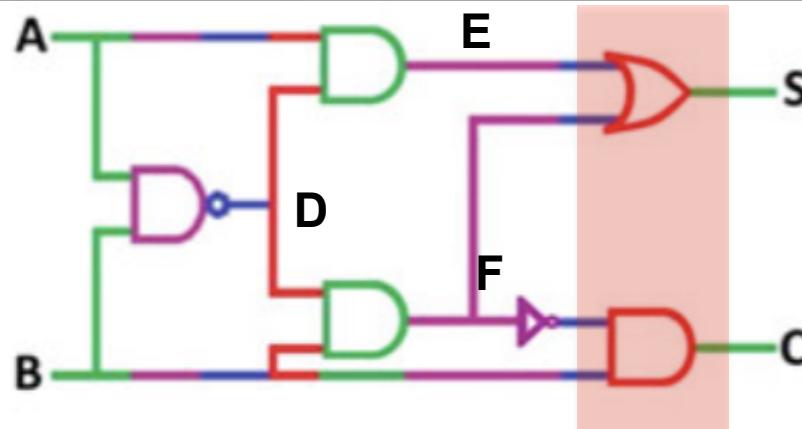
$$\Delta E_{diss} \geq (3.76)k_B T \ln(2)$$

Another possibility...





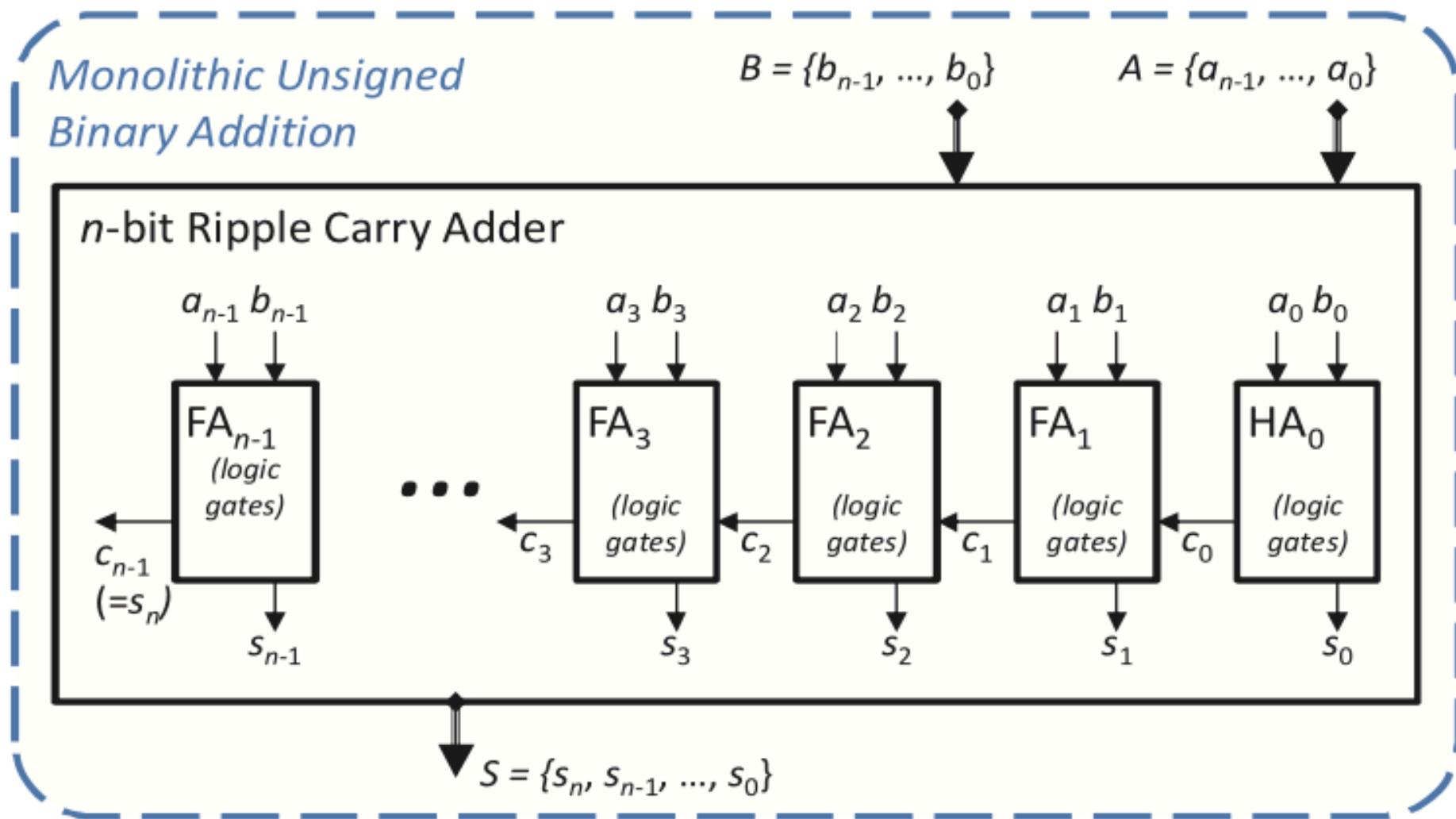


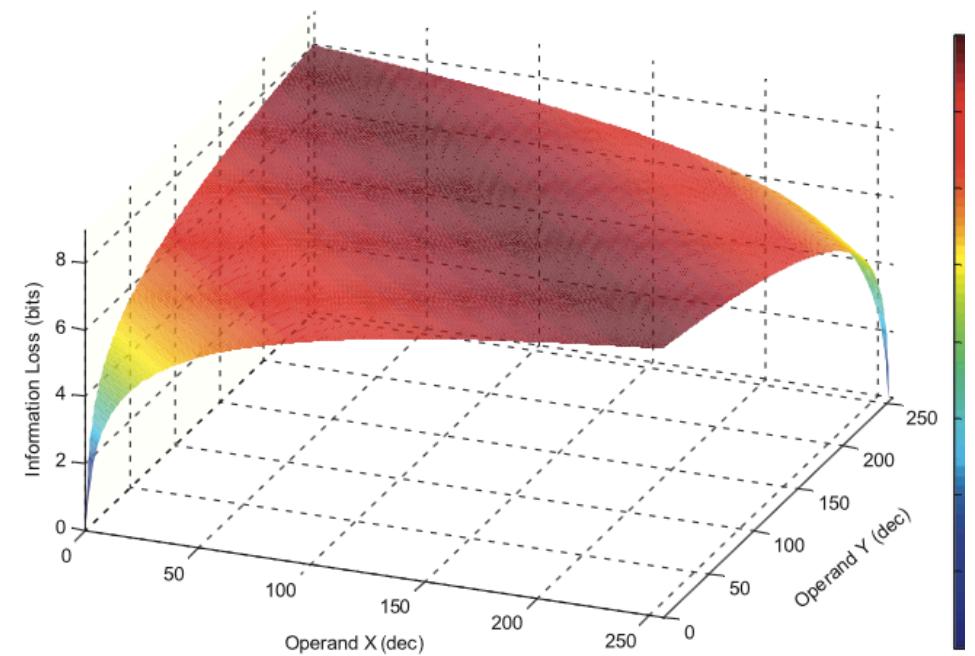
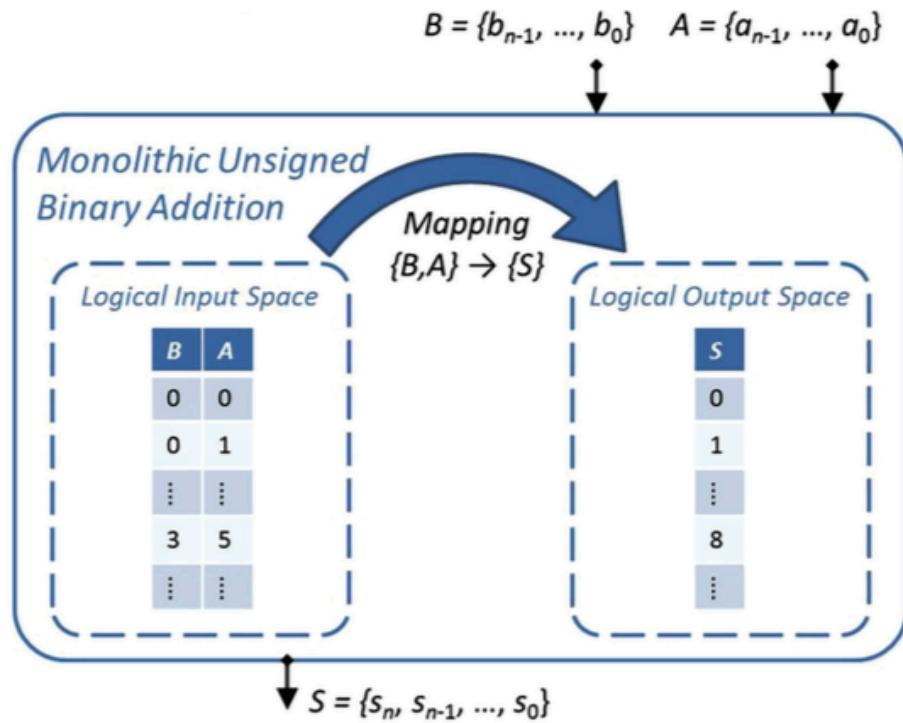


Quantifying Irreversible Information Loss in Digital Circuits

ISMO K. HÄNNINEN, CRAIG S. LENT, and GREGORY L. SNIDER,
University of Notre Dame

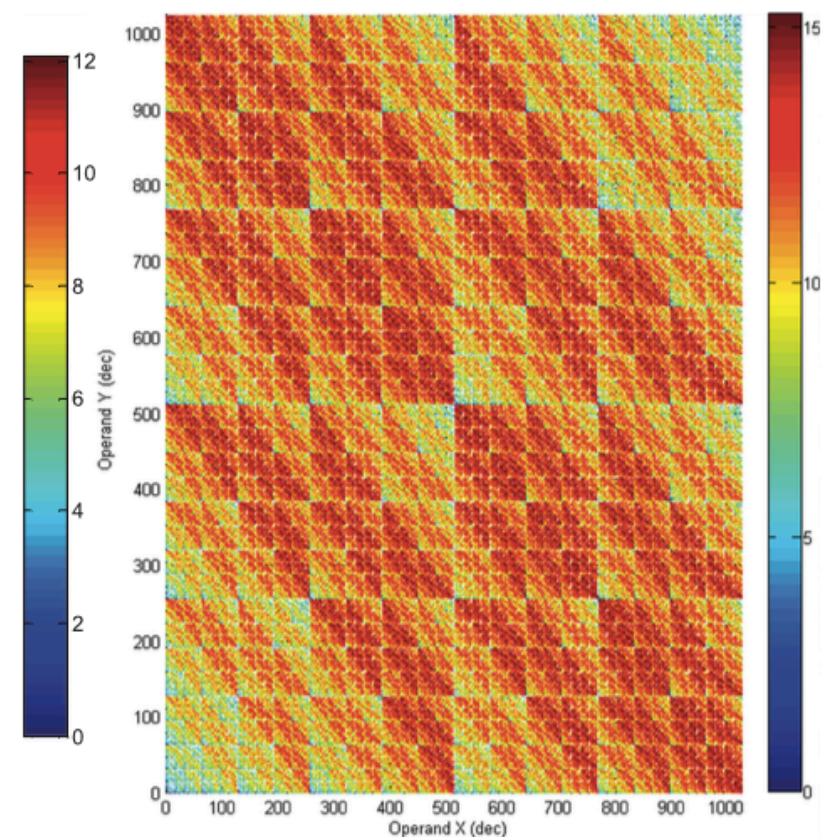
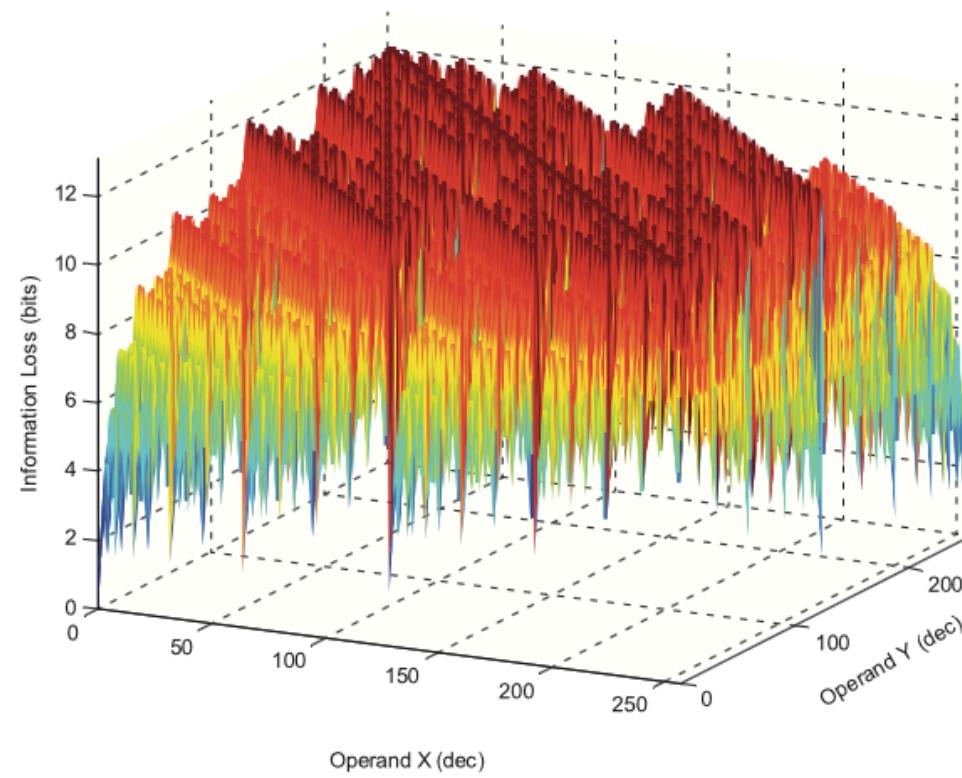
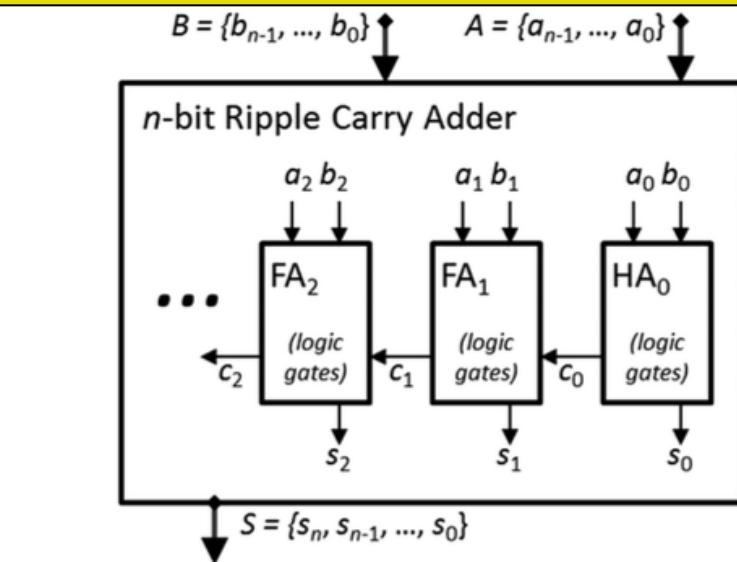
ACM Journal on Emerging Technologies in Computing Systems, Vol. 11, No. 2, Article 10, Pub. date: October 2014.





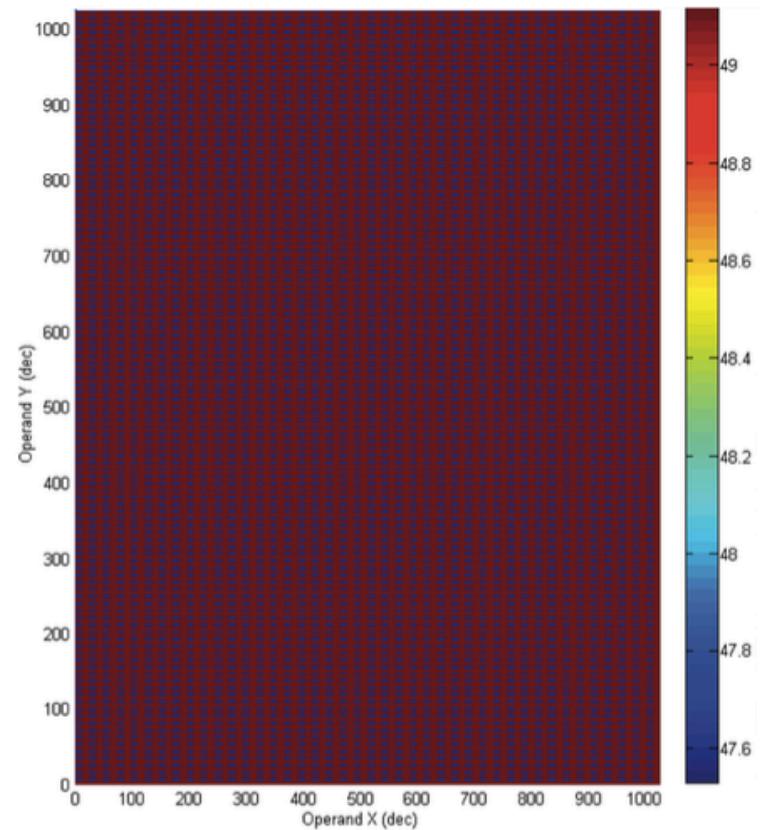
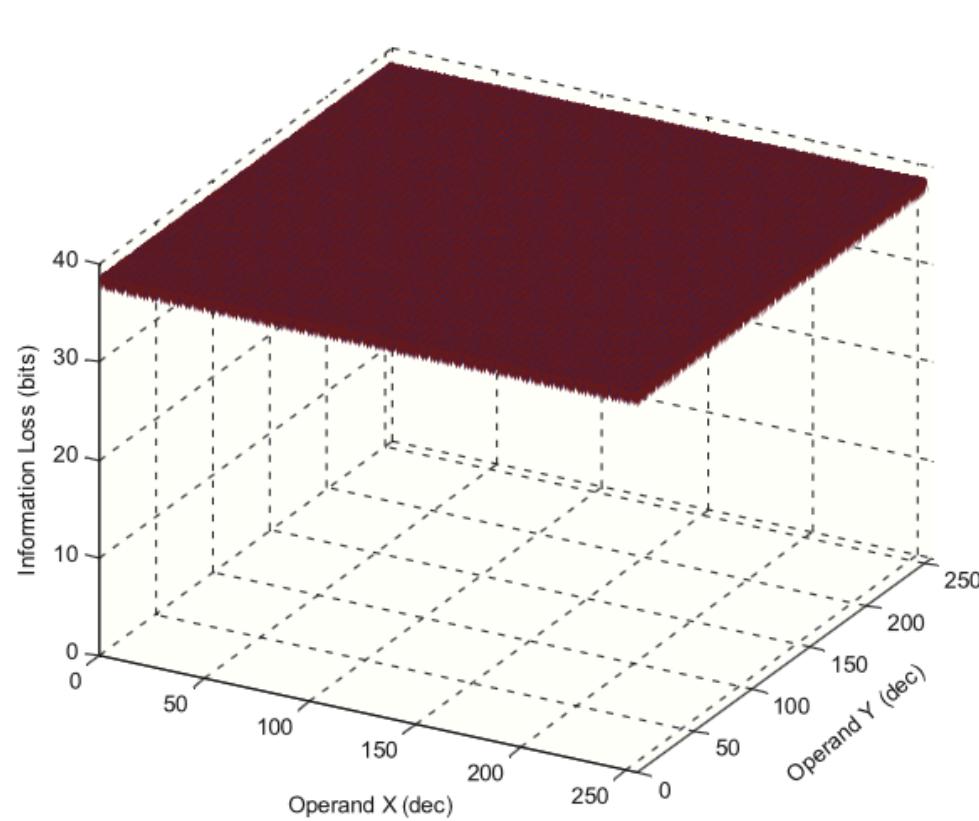
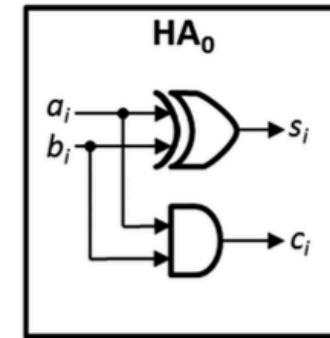
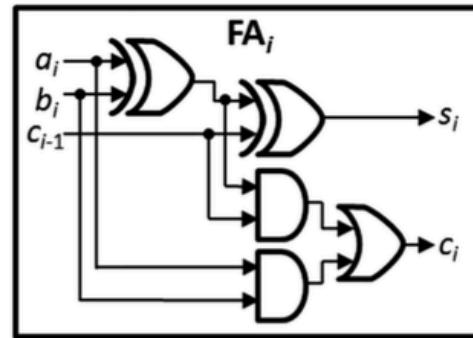
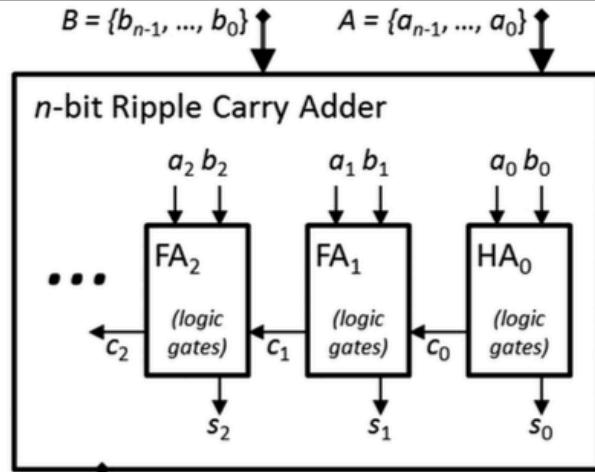
NanoComputing

Related work



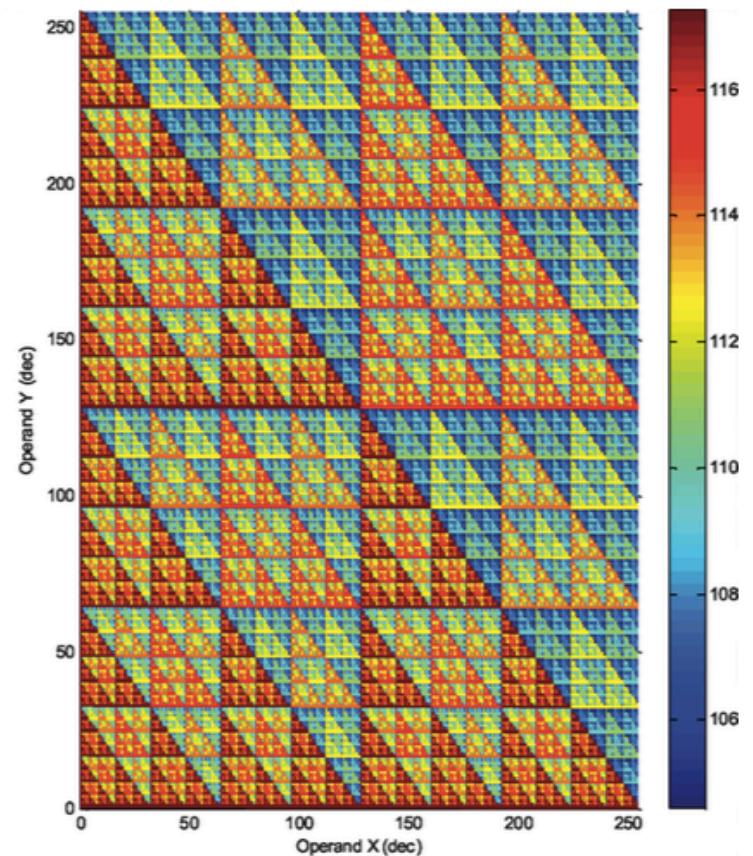
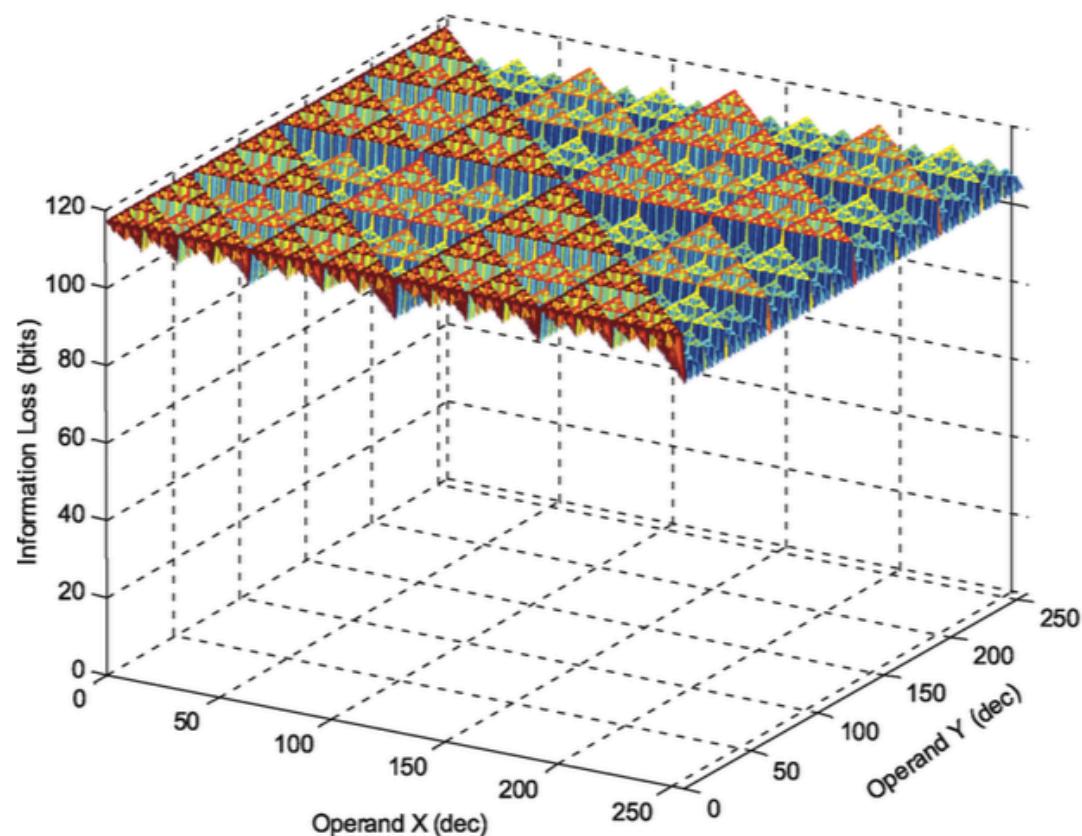
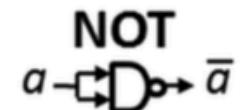
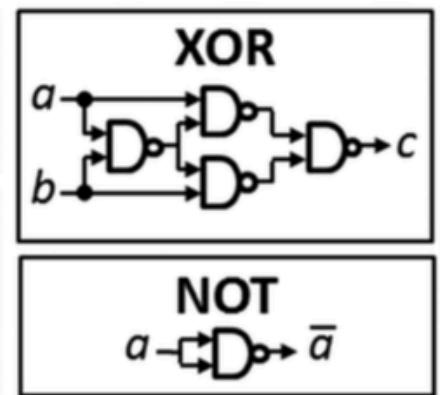
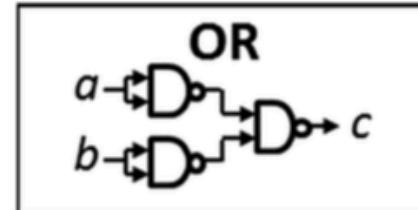
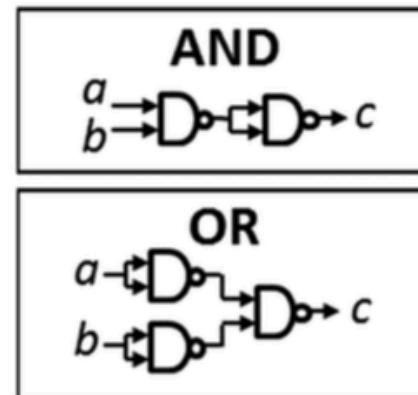
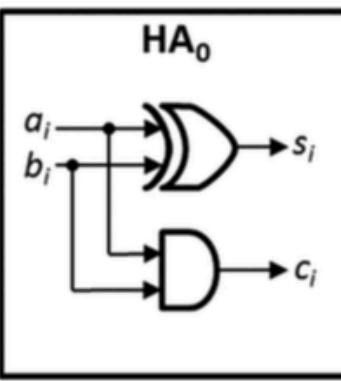
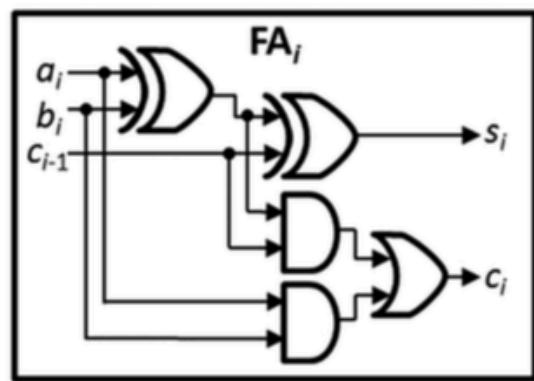
NanoComputing

Related work



NanoComputing

Related work



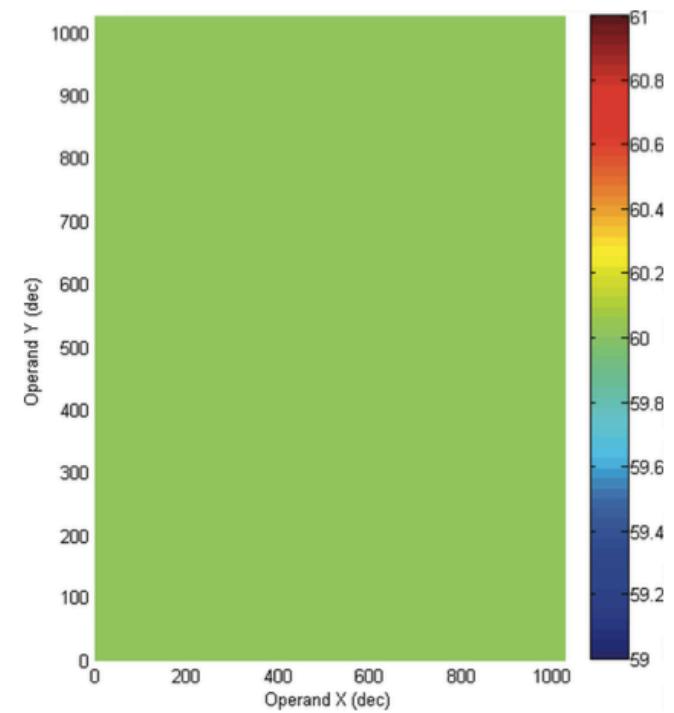
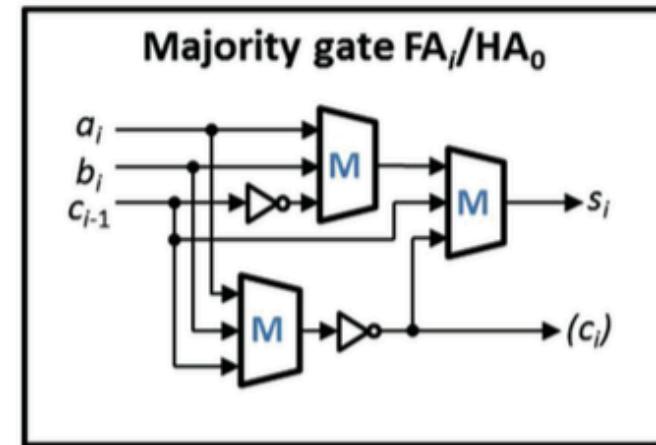
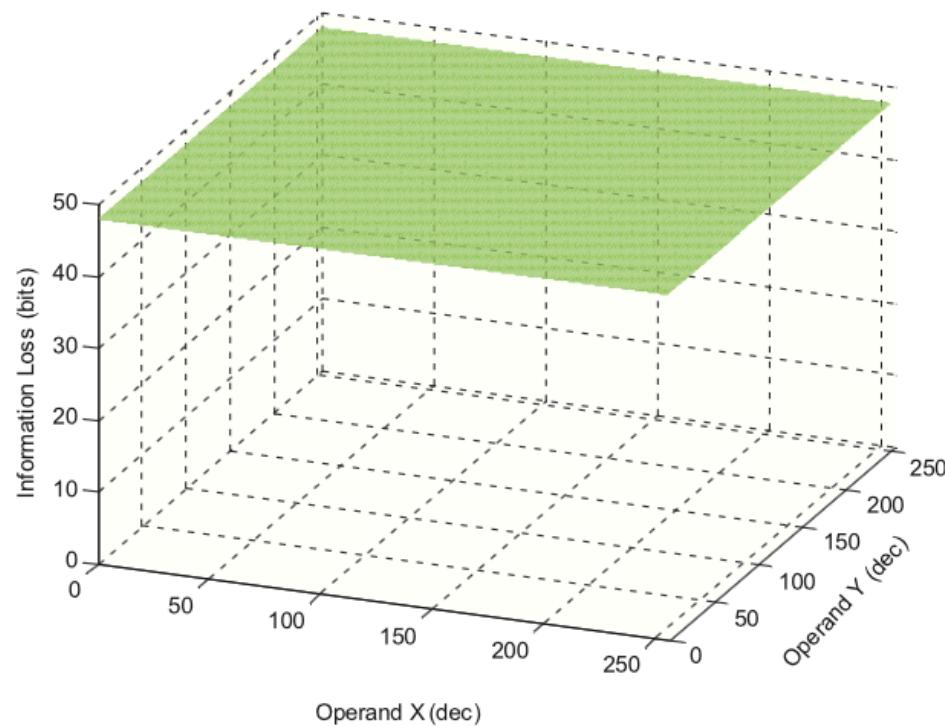
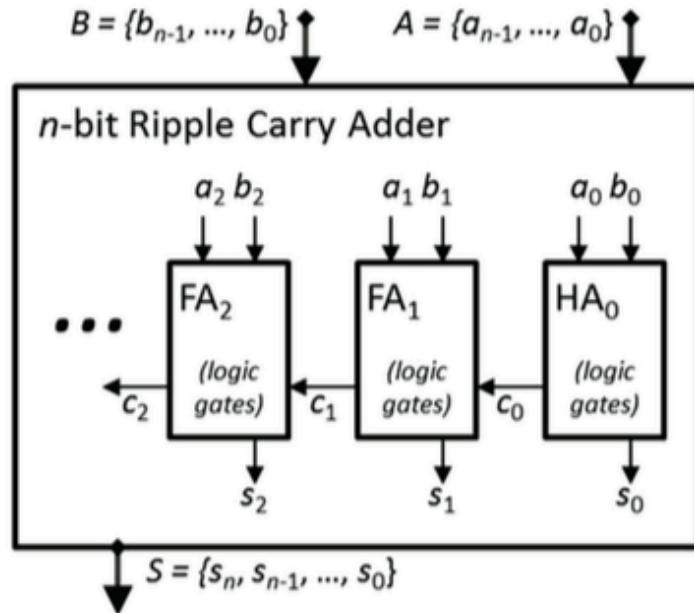


Table IX. Statistics for 8-Bit Binary Addition, assuming Uniform Input Operand Distribution

ABSTRACTION LEVEL	INFORMATION LOSS STATISTICS (bits)			
	<i>Min</i>	<i>Avg</i>	<i>Max</i>	<i>Std. dev.</i>
<i>A. Monolithic theoretical addition</i>	0	7.3	8	1.5×10^{-14}
<i>B. RCA, ideal HA/FA</i>	0	8.8	12.1	1.5
<i>C. RCA, ideal XOR, AND, OR</i>	37.2	38.4	38.8	0.4
<i>D. RCA, ideal NAND</i>	104.6	111.7	117.3	2.4
<i>E. RCA, ideal MG</i>	48	48	48	0

Contributions

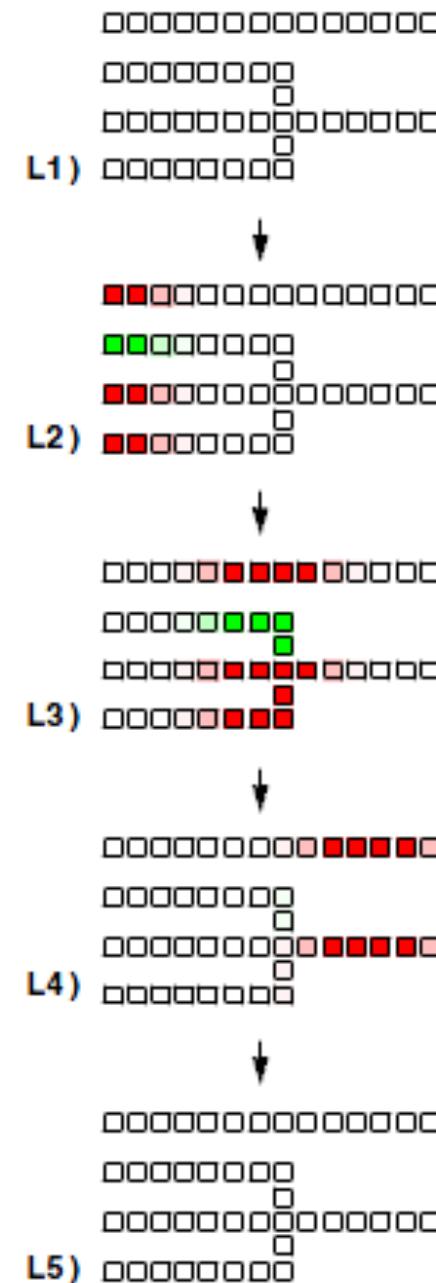
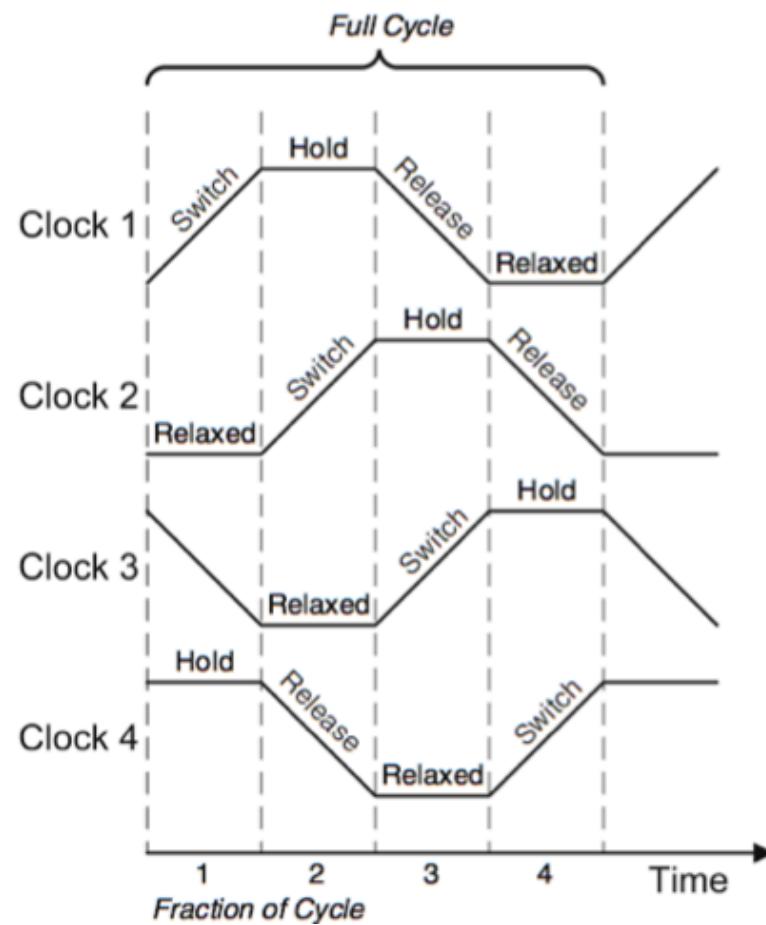
- Reversible gates
- **Bennett clocking in QCADesigner**

Reversible computing and QCAs

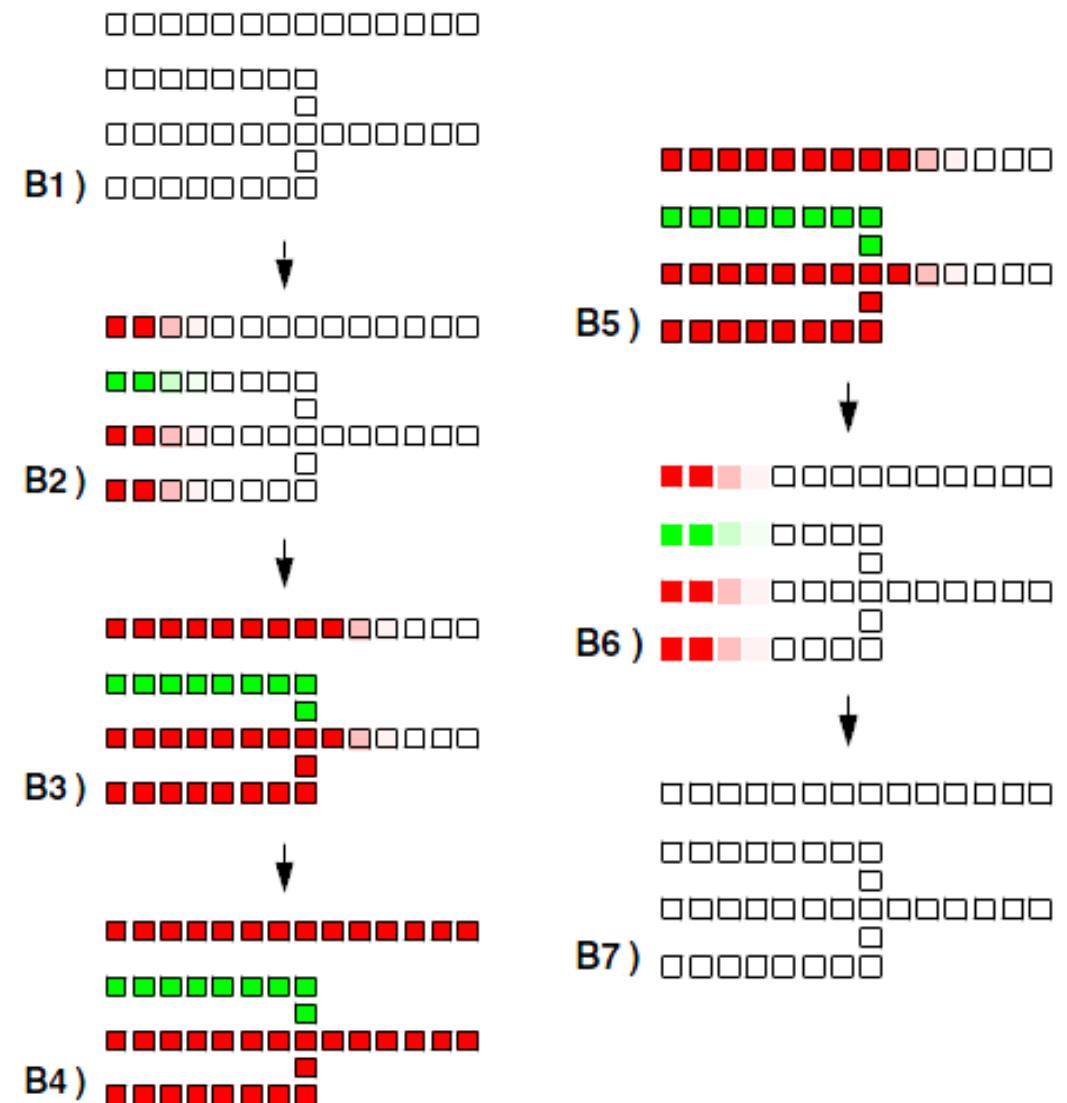
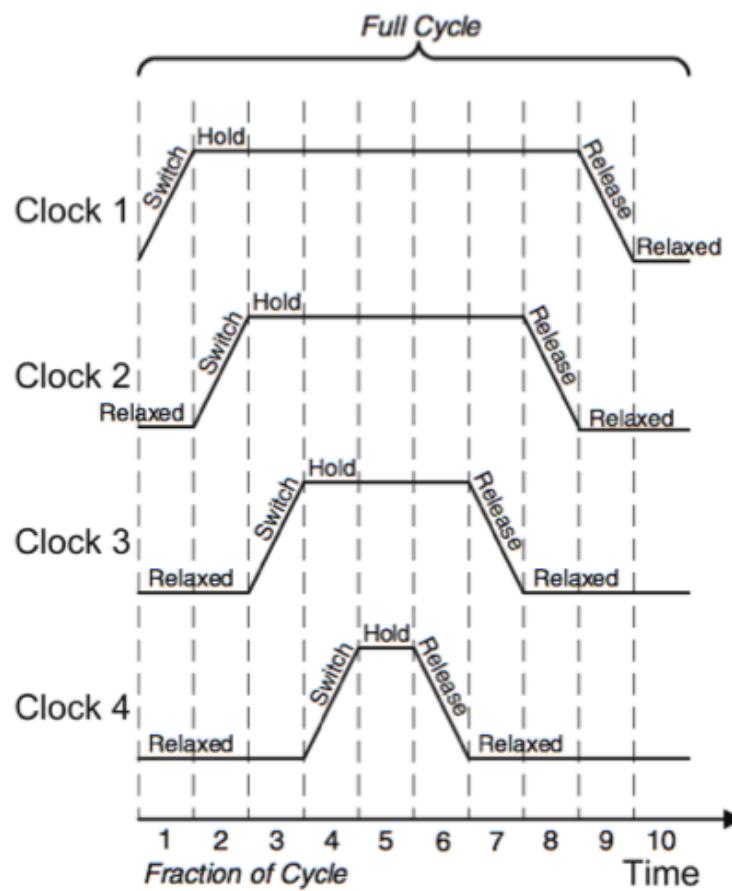
Another solution to avoid Landauer's limit is using a non-dissipative clocking system.

Lent, Craig S., Mo Liu, and Yuhui Lu. "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling." *Nanotechnology* 17.16 (2006): 4240.

Conventional clock: Landauer



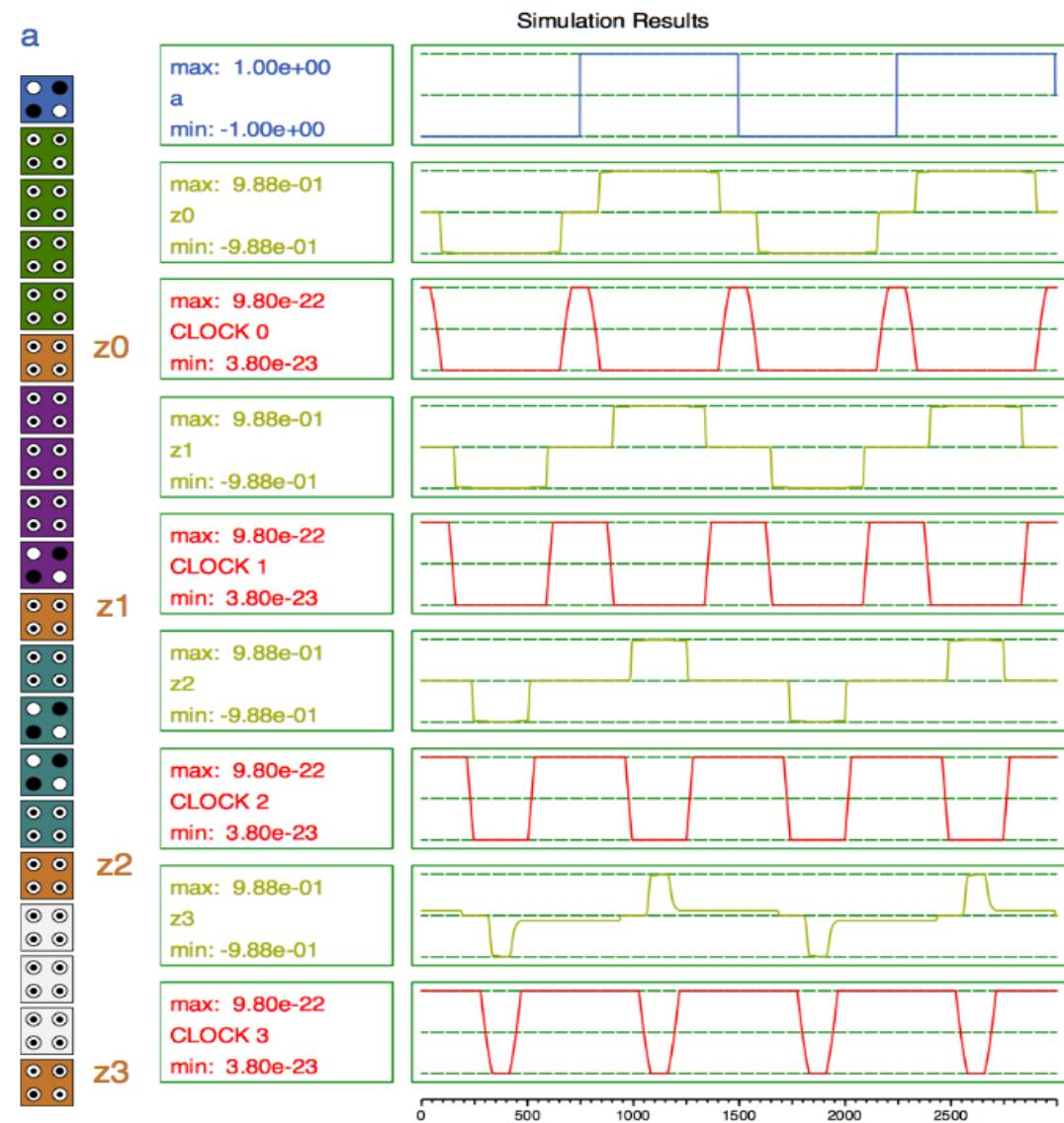
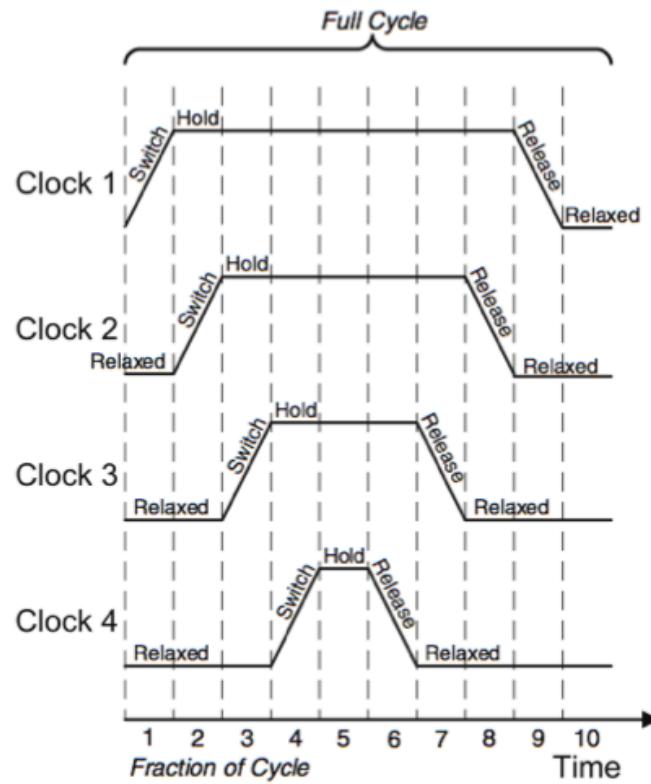
Alternative Clock: Bennett



Bennett clocking in QCADesigner

- QCADesigner is the main tool used to simulate QCA circuits.
- The latest version of the QCADesigner only performs Landauer clocked circuit simulations.
- The clock signal in the QCADesigner is calculated as a hard-saturating cosine and is tied directly to the tunneling energy.

Proof of concept for Bennett clocking scheme in QCADesigner: the transmission of data through a wire.



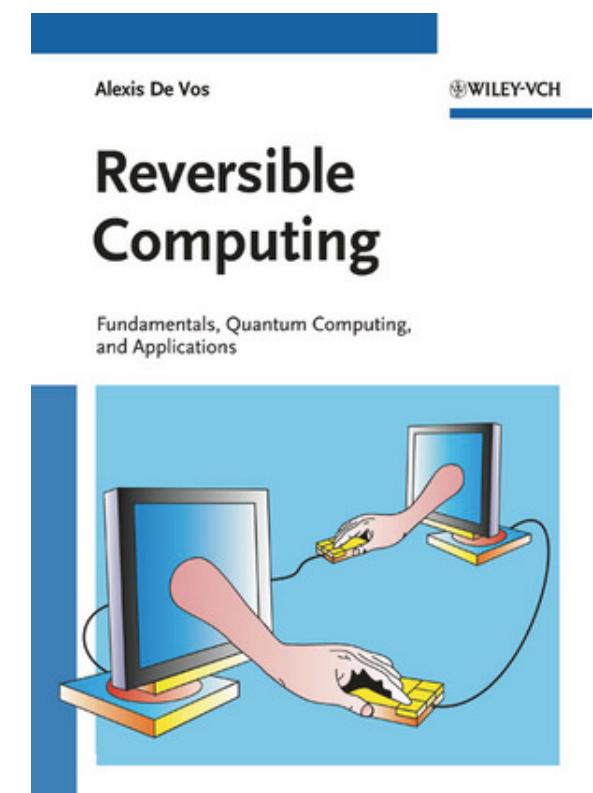
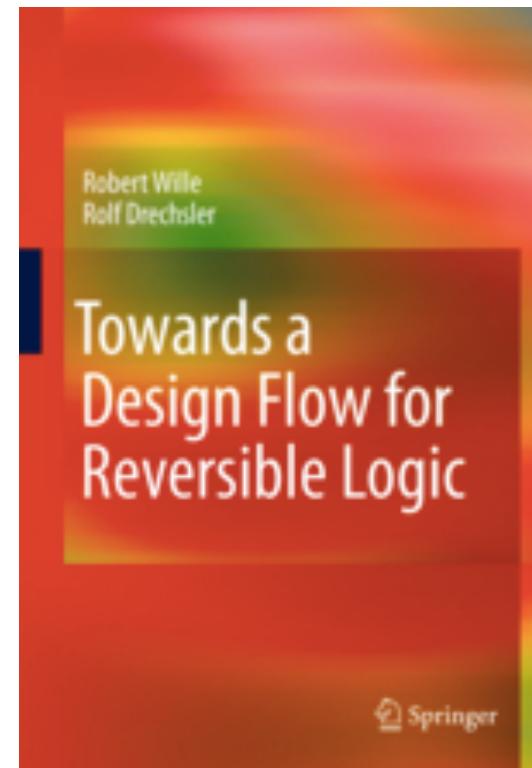
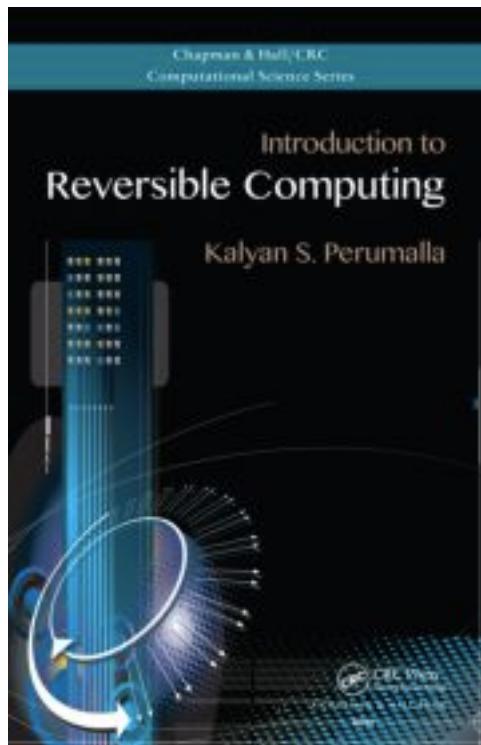
QCADesigner actually displays the tunneling probability as clock signals instead of the tunneling potential barriers!

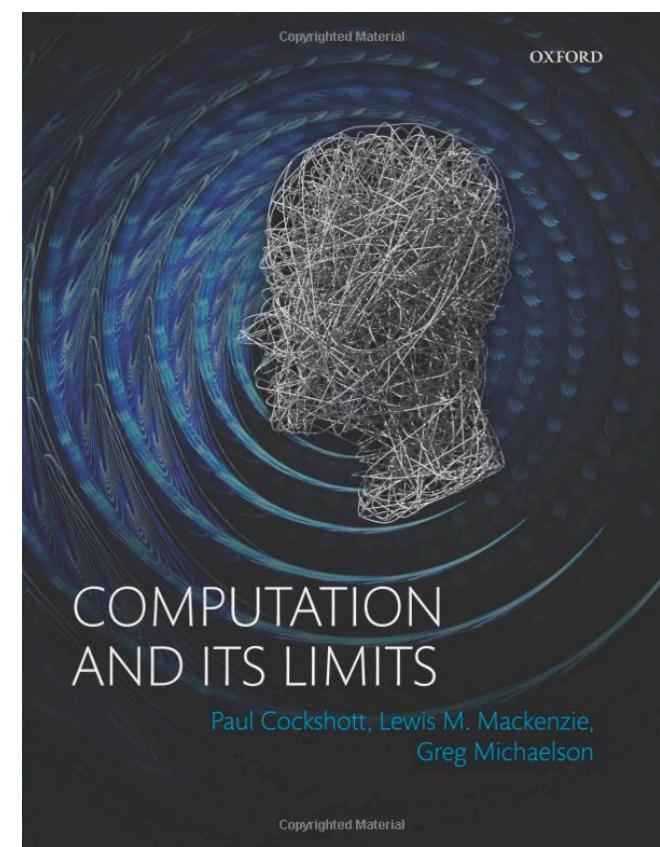
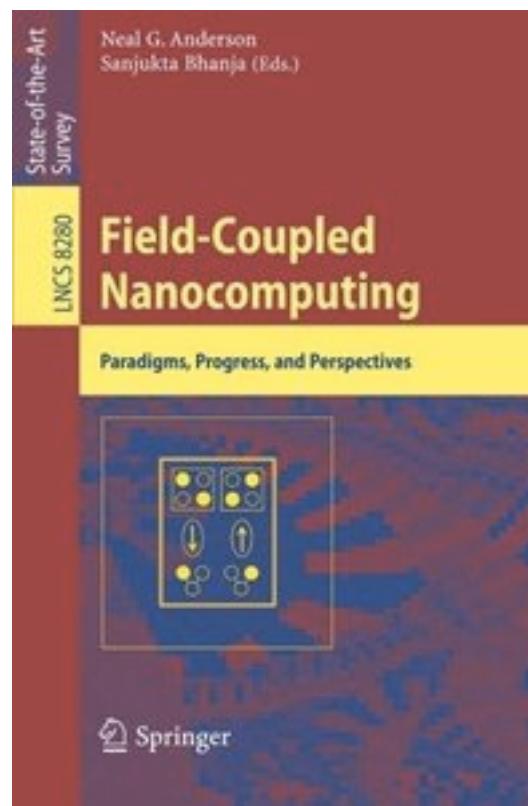
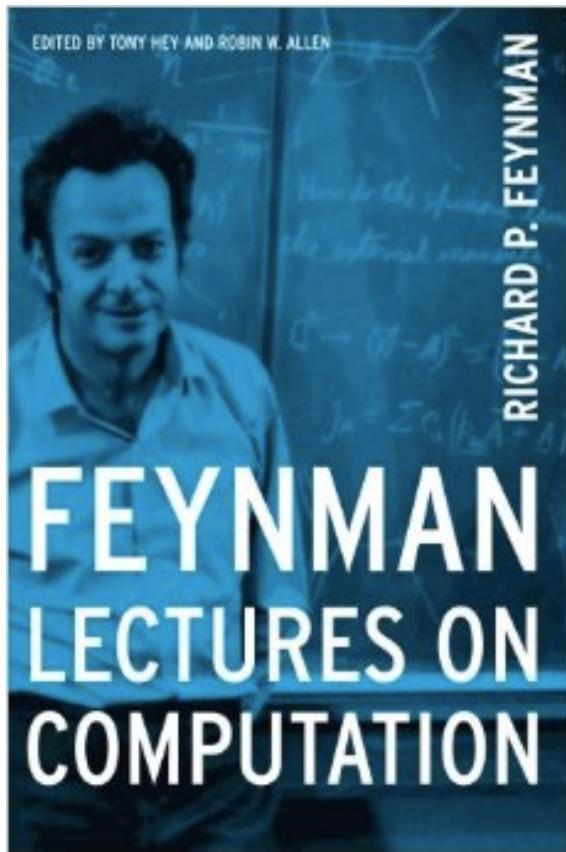
Final remarks

"Eventually all computing circuits will have to utilize energy-recovery and reuse approaches to achieve the energy efficiency required for sustaining the continuous growth of computing power in the future." Hanninen, Lent and Snider, 2014.

Reversible computing is **the most viable way** to accomplish this goal.

References





References

- CHAVES, Jeferson; et al. "Towards reversible QCA computers: reversible gates and ALU." *Proceedings of the 6th Latin American Symposium Symposium on Circuits and Systems*. IEEE, 2015.
- Landauer, Rolf. "Irreversibility and heat generation in the computing process." *IBM journal of research and development* 5.3 (1961): 183-191.
- Bennett, Charles H. "Logical reversibility of computation." *IBM journal of Research and Development* 17.6 (1973): 525-532.
- Bérut, Antoine, et al. "Experimental verification of Landauer's principle linking information and thermodynamics." *Nature* 483.7388 (2012): 187-189.
- Janez, Miha, Primoz Pecar, and Miha Mraz. "Layout design of manufacturable quantum-dot cellular automata." *Microelectronics Journal* 43.7 (2012): 501-513.

References

- SILVA, S. S.; SARDINHA, L. H. B. ; VIEIRA, L. F. M. ; VIEIRA, M. A. M.; VilelaNeto, O. P. . Nanodevices Communication with QCA. IEEE Transactions on Nanotechnology, To be published (accepted).
- SARDINHA, L. H. B. ; D. S. Silva ; VIEIRA, M. A. M. ; VIEIRA, L. F. M. ; VILELA NETO, Omar Paranaiba . TCAM/CAM-QCA: (Ternary) Content Addressable Memory using Quantum-Dot Cellular Automata. Microelectronics Journal, 2015 To be published (accepted).
- Fazzion, Elverton, et al. "A Quantum-Dot Cellular Automata Processor Design." *Proceedings of the 27th Symposium on Integrated Circuits and Systems Design*. ACM, 2014.
- Sardinha, Luiz HB, et al. "Nanorouter: A quantum-dot cellular automata design." *Selected Areas in Communications, IEEE Journal on* 31.12 (2013): 825-834.
- Panho Marciano, A. L., et al. "An efficient FPGA implementation in quantum-dot cellular automata." *Integrated Circuits and Systems Design (SBCCI), 2013 26th Symposium on*. IEEE, 2013.