**EE 316 Computer Engineering Junior Lab**

**Design Project 6**

**Spring 2017**

**Specification: Synchronous digital system using Xilinx MicroBlaze processor**

**Due Date: Thursday, April 17 - lab demo**

**Friday, May 6 - written report due.**

Please complete the Tutorial for Project 6 before you begin this project.

Design a synchronous digital system that operates at an "effective clock" of 1 Hz. The synchronous system has an output sequence of length 9 and the sequence repeats, when it is operational. The output sequence in HEX is the following:

0000, 0A0A, A0A0, FE45, ABCD, DCBA, FEED, DEAD, BEEF

The other specifications are:

* The design will be implemented on Xilinx’s NexysTM4 board using Xilinx’s Vivado and SDK tools.
* You will use Xilinx’s IP blocks that has a MicroBlaze soft-core processor to design the system, assign pins and generate the bit stream and exported to Xilinx SDK.
* You will need to add buttons to your design created in the last step of the Tutorial of Project 6.
  + The center button (BTNC) initializes the system (asynchronously) to the first number of the sequence when it is pressed and held. Once BTNC is released, the system will start counting.
  + BTNL toggles system’s direction. The system starts in the forward mode. If the key is pressed, it will change into the backward-counting mode. If it is pressed again, the direction will reverse.
  + The BTNR toggles between system-enable or disable.
* The button (not switches) inputs should use interrupts and the axi-timer should be used to provide periodic interrupts for all timing needs, e.g., refreshing seven segment displays, 1 second delays, etc.
* The output should be displayed on 4 of the on-board 7 segment displays on the right.
* (**Option: 5 points**) In this design, carry out a simulation for debugging the design. This can be a very complicated if you want to simulate all data transactions on all AXI buses. Choose one representative bus.
* (**Option: 5 points**) In this design, instantiate a debug logic Analyzer as a tool for debugging the design. Carry out a simple demo or data transaction on the bus.

Teams:

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| --- | --- | --- | --- | --- | --- | --- |
| **Team1** | **Team2** | **Team3** | **Team4** | **Team5** | **Team6** | **Writer** |
| Bruska | Griffin | Bruce | Lowit | Oliver | Marsanskis |  |
| Heck | Shippee | Craddock | Straw | Trahan | Zander |  |
| Michaels | Kuhns | Beyer | strenk | Farden | Law |  |

\_\_x\_\_ Summary

\_\_\_\_\_ Design Problem Statement

\_\_\_\_\_ Problem Decomposition

\_\_\_\_\_ Detailed Design

\_\_\_\_\_ Module Level Testing

\_\_\_\_\_ Specification Testing

\_\_\_\_\_ Alternative Designs

\_\_\_\_\_ Results and Analysis

\_\_\_\_\_ References

\_\_\_\_\_ Appendix Processor Memory Addresses

\_\_\_\_\_ Appendix Code

\_\_\_\_\_ Appendix Tickle File