**EE 316 Computer Engineering Junior Lab**

**Project 6-Tutorial**

**HelloWorld with Xilinx Microblaze**

**Spring 2017**

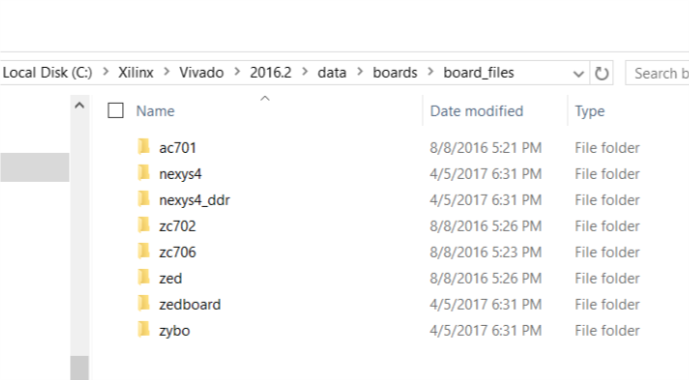
**Due Date:** Not due. Try to finish before April 13, 2017. This tutorial will be part of Project 6.

For this project, please complete the following tutorials on the **Nexys4 DDR** board.

1. Download board files for Vivado:

<https://reference.digilentinc.com/reference/software/vivado/board-files?redirect=1>

and follow the directions and add new board files as shown below.



1. <https://reference.digilentinc.com/learn/programmable-logic/tutorials/nexys-4-ddr-getting-started-with-microblaze/start>
2. Download the following tcl-file by double clicking on it. This file was generated in Vivado version **2016.1**

****

Follow the following steps.

* Open the Tcl file in Notepad++. Search for “set scripts\_vivado\_version **2016.1**” in the text. Change the text to the version number of the Vivado on your computer.
* Save the Tcl file in a folder in C drive: Say **C:\MicroBlaze**
* Open Vivado. At the bottom of Vivado, in the Tcl command window type the following.

cd C:/MicroBlaze/

pwd

dir

source design\_1\_bd.tcl

* Wait until the block diagram is ready. Note this block diagram has a few new blocks and outputs. Study the new blocks by double clicking each of the blocks one at a time.
* Now go back to step 12 first tutorial from digilentinc.com and continue from here. You may need to assign the ports and save the XDC file. Generate the bit-stream file, export to the SDK and open SDK and repeat the rest of the part 2 in this project.