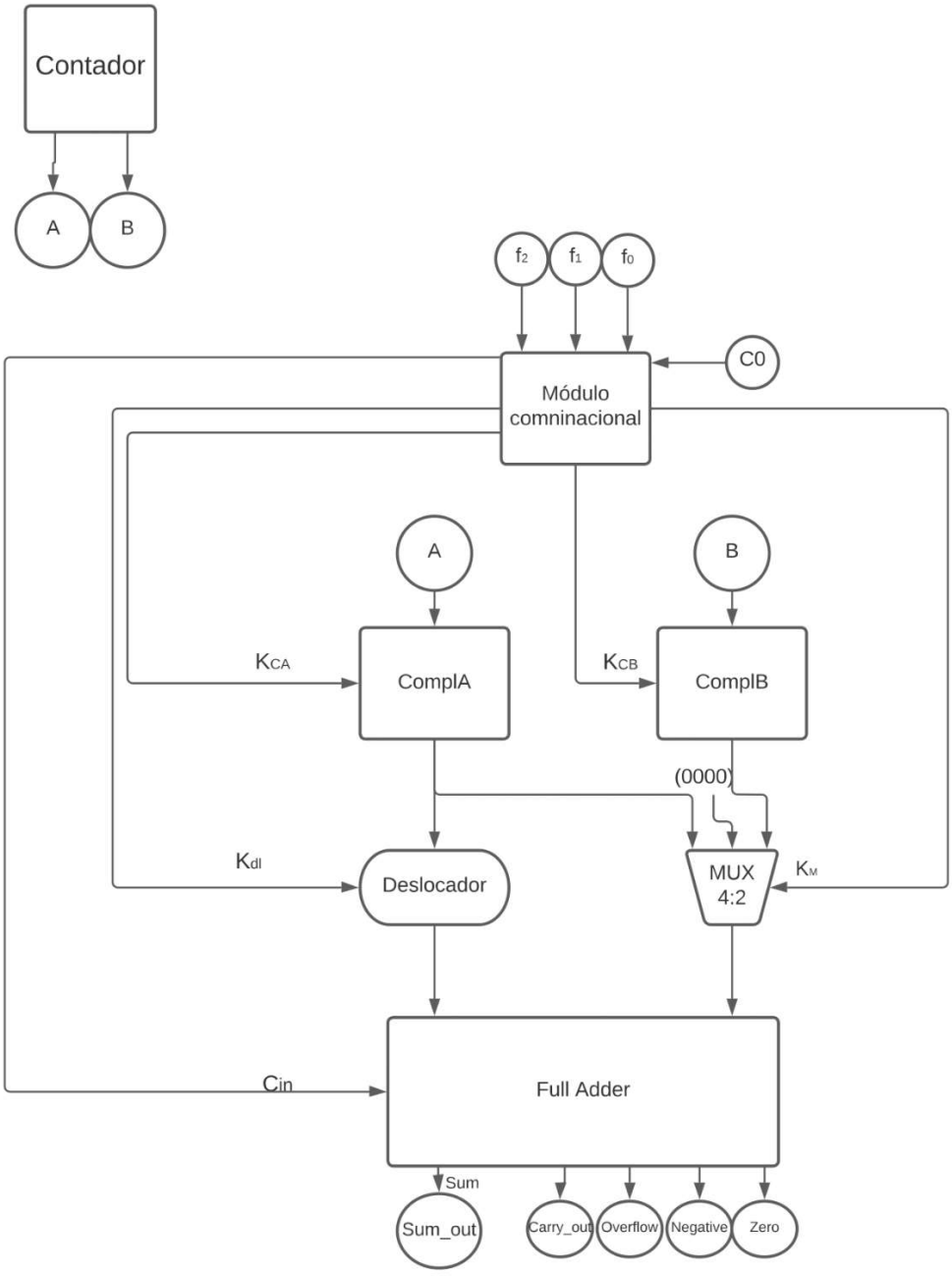
Contador
A
B
f2
f1
f0
C0
Módulo
comninacional
A
B
KCA
ComplA
KCB
ComplB
(0000)
Kdl
Deslocador
MUX
4:2
KM
Cin
Full Adder
Sum
Sum_out
Carry_out
Overflow
Negative
Zero

Módulo combinacional

Operação	Código de operação		Sinais de controle				
	$f_2f_1f_0$		K_{CA}	K_{CB}	K_m	K_{dl}	Cin
Soma	000	ADD(A,B, c_{in})	0	0	00	00	C0
Subtração	001	ADD(A, B', 1)	0	1	00	00	1
Incremento	010	ADD(A, 0, 1)	0	dc	01	00	1
T. de Sinal	011	ADD(A', 0, 1)	1	dc	01	00	1
Mult. por 2	100	ADD(A_{dlcL}, 0,0)	0	dc	01	01	0
Mult. por 3	101	ADD(A_{dlcL}, A, 0)	dc	dc	10	01	0
Desloca R	110	ADD(A_{dlcR}, 0,0)	0	dc	01	10	0
Compl. de 1	111	ADD(A', 0,0)	1	dc	01	00	0

K_{CA}	00	01	11	10
0	0	0	1	0
1	0	0	1	0

$K_{CA} = f_1f_0$

K_{CB}	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$K_{CB} = f_0$

K_{M0}	00	01	11	10
0	0	0	1	1
1	1	0	1	1

$K_{M0} = f_1 + f_2f'_0$

K_{M1}	00	01	11	10
0	0	0	0	0
1	0	1	0	0

$K_{M1} = f_2 f'_1 f_0$

K_{dI0}	00	01	11	10
0	0	0	0	0
1	1	1	0	0

$K_{dI0} = f_2 f'_1$

K_{dI1}	00	01	11	10
0	0	0	0	0
1	0	0	0	1

$K_{dI1} = f_2 f_1 f'_0$

$Cin = f_2' f_0 + f'_2 f_1 + f'_2 f'_1 f'_0 C0$

$K_{CA} = f_2' f_1 f_0$
$K_{CB} = f_0$
$K_{M0} = f_1 + f_2 f_0$
$K_{M1} = f_2 f'_1 f_0$
$K_{dI0} = f_2 f'_1$
$K_{dI1} = f_2 f_1 f'_0$
$Cin = f_2' f_0 + f'_2 f_1 + f'_2 f'_1 f'_0 C0$

Mapeamento da Placa FPGA

Entradas		
Placa FPGA	**Somador**	**ULA**
T9	C_ini	VSW(3 DOWNTO 3)
U8	f(2)	VSW(2 DOWNTO 2)
U10	f(1)	VSW(1 DOWNTO 1)
V8	f(0)	VSW(0 DOWNTO 0)
E12	-	clock_50

Saídas		
Placa FPGA	**Somador**	**ULA**
R20	S(0)	LEDG(0)
T19	S(1)	LEDG(1)
U20	S(2)	LEDG(2)
U19	S(3)	LEDG(3)
V19	zero	LEDG(4)
V20	negativo	LEDG(5)
Y22	carry_out	LEDG(6)
W21	overflow	LEDG(7)