# **Bryan Linares**

blinar55@gmail.com • (213) 275-7586 • linkedin.com/in/bryandlinares • github.com/bryanl1

#### **EDUCATION**

### California State University, Long Beach

Aug. 2022- Expected May 2024

MS, Computer Science

Long Beach, CA

- Relevant Coursework: Computer Architecture, Analysis of Algorithms, Artificial Intelligence, Computer Security
  BS, Computer Engineering, Minor Computer Science
  Jan. 2017- Dec. 2019
- Relevant Coursework: Microprocessors & Controllers, Software Engineering, Machine Learning, SoC Design
  Santa Monica College
  Feb. 2022 June 2022
- Relevant Coursework: Introduction to Cloud Computing using AWS, Ethical Hacking

#### **PROJECTS**

#### Interpreter for BASIC-like language

Programming Language Design and Extension

- Implemented and extended a BASIC clone language with more than 20 functions to implement a Calculator.
- ~700 LOC in pure Java using the Eclipse IDE with a functionality tree designed in ANTLR.

#### **Twitter Sentiment Analysis**

Cloud Based AI Computing

- Python implementation of SepCNN Twitter Sentiment analysis on over 100000 tweets on a single GPU.
- Used Google Colab on a Kaggle provided corpus of Tweets to run a Naive Bayes Sentiment Analysis.

# Senior Project: Rolling Arm

Machine Vision guided autonomous robot

- Developed C++ and OpenCV code for Realsense 3D Camera to detect for littered cans with 80% accuracy.
- Wrote Linux interface cron job code on UPBoard SBC to communicate with custom PCB and ARM controller.
- Assisted with Embedded C code for Robotic Arm's grabbing procedure controlled by an ARM Cortex 3.

# **GBRAINS: Extended MIPS Processor**

Verilog Design and Verification

- Programmed and verified Verilog with hundreds of test procedures for the MIPS32 processor.
- Designed custom machine code instructions, circuitry, and processing cores for Floating Point and parallel 64 bit Vector operations.
- Developed in Xilinx ISE and Vivado and Run on a Nexys 4 DDR aka Nexys A7 FPGA.

#### FPGA Programmed UART

Verilog FPGA Implementation of System on Chip Design

- Instantiated a custom Soft Processor based on PicoBlaze, programmed in Assembly.
- Sends and receives custom UART messages to standard terminal.

# **SKILLS**

- Programming Languages: Python, Java, C/C++, Embedded C, Verilog, Rust, Javascript
- Tools: Git, Linux, Xilinx ISE Design Suite, Vivado, Keil uVision, FPGA, ARM Microcontrollers
- Foreign Languages: Spanish (fluent)