USB Type-C™ Power Delivery using STM32xx Series MCUs and STM32xxx Series MPUs

Introduction

USB Type-C™ Power Delivery technology simplifies the consumers' daily life.

This new reversible USB Type-C™ connector makes plug insertion more user friendly. The technology offers a single platform connector carrying all the necessary data. Using the power delivery protocol, it allows negotiation of up to 100 W power delivery to supply or charge equipment connected to a USB port, the objective being fewer cables and connectors, as well as universal chargers.

The USB Type-C™ connector provides native support of up to 15 W (5 V @ 3 A), extendable to 100 W (up to 20 V @ 5 A) with the optional USB Power Delivery feature.

This application note is a guideline for using USB Type-C™ Power delivery with STM32xx Series MCUs and STM32xxx Series MPUs. It introduces some basics of the two new USB Type-C™ and USB power-delivery standards.

Table 1. Applicable products

Type	Product series
Microcontrollers with general purpose peripherals	STM32L0 Series STM32L1 Series STM32L4 Series STM32F0 Series STM32F1 Series STM32F2 Series STM32F3 Series STM32F4 Series STM32F7 Series STM32H7 Series STM32W Series
Microcontrollers with integrated UCPD IP	STM32G0 Series STM32L5 Series
Microprocessor with general purpose peripherals	STM32MP1 Series

1 General informaton

This document applies to the STM32 devices listed in Table 1. Applicable products, which are based on Arm® Cortex®-M processors.

arm

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1.1 Acronyms and abbreviations

Table 2. Definition of terms

Acronym	Definition
AMS	Atomic message sequence
APDO	Alternative power delivery object
BMC	Biphase mark coding
BSP	Board support package
CAD	Cable detection module
DFP	Downstream facing port
DPM	Device policy manager
DRP	Dual role power (ability for a product to either source or sink power)
DRS	Data role swap
GP	General purpose
GUI	Graphical user interface
HAL	Hardware abstraction layer
HW	Hardware
LL	Low layer
MSC	Message sequence chart
OVP	Over-voltage protection
PDO	Power delivery object
PE	Policy engine
PRL	Physical protocol layer
PRS	Power role swap
SNK	Power sink capability
SRC	Power source capability
UCPD	USB type C power delivery
UFP	Upstream facing port
VDM	Vendor defined messages
FWUP	Firmware update
PPS	Programmable power supply
TCPM	Type C Port Manager
TCPC	Type C Port Controller

1.2 Reference documents

STMicroelectronics ecosystem documents

- USB Type-C protection and filtering, AN4871
- STM32Cube USBPD stack user manual, UM2552
- STM32CubeMonitor for USB-C and Power Delivery, DB3747
- STM32CubeMonitor-UCPD software tool to configure and tune the STM32 for USB Type-C™ Power Delivery, UM2468
- TCPP01-M12 USB Type-C port protection for USB power delivery, Datasheet.

USB specification documents

- USB2.0 Universal Serial Bus Revision 2.0 Specification
- USB3.1 Universal Serial Bus Revision 3.2 Specification
- USB BC Battery Charging Specification Revision 1.2
- USB BB USB Device Class Definition for Billboard Devices
- Universal Serial Bus Power Delivery Specification, Revision 2.0, Version 1.3, January 12, 2017
- Universal Serial Bus Power Delivery Specification, Revision 3.0, Version 1.2, June 21 2017 (Comment: 3.2 (supercedes 3.1) is released since 2017. It is soon to be referenced in Type-C Release 1.4)
- Universal Serial Bus Type-C Cable and Connector Specification 1.3, July 14, 2017.

2 USB Type-C™ in a nutshell

The USB Implementers Forum (USB-IF) introduces two complementary specifications:

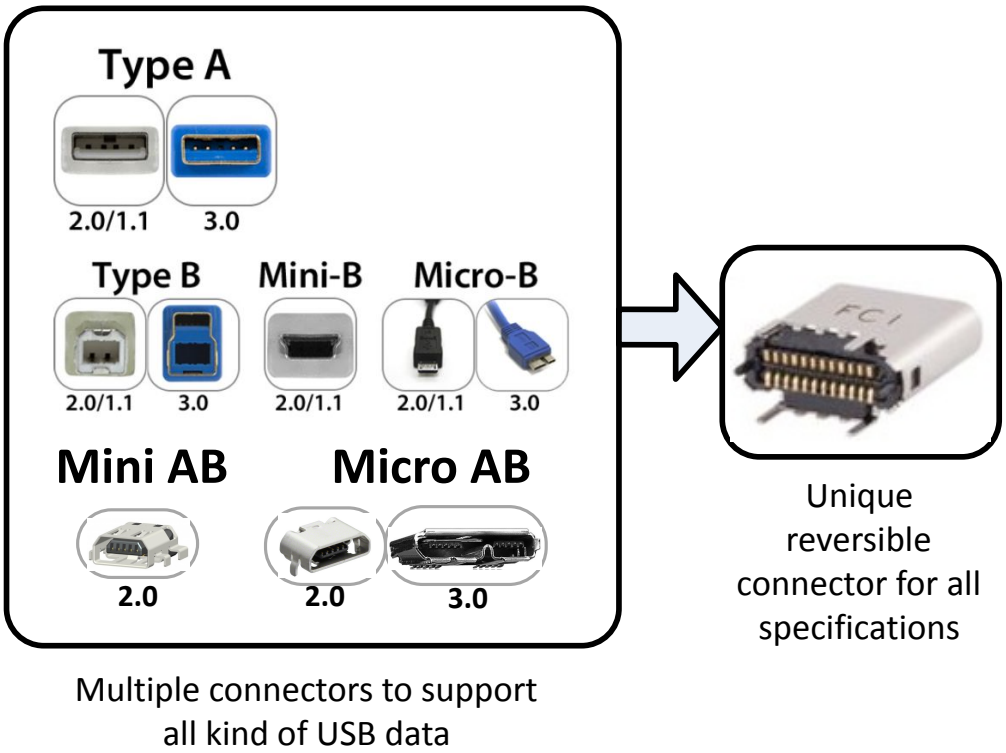
- The USB Type-C™ cable and connector specification release 1.3 details a reversible, slim connector system based on high-speed USB2.0 signals and two SuperSpeed lanes at up to 10 Gbit/s, which can also be used to support alternate modes.
- The USB Power Delivery (PD) specification revisions 2.0 and 3.0 detail how a link can be transformed from a 4.5 W power source (900 mA at 5 V on V_{BUS}), to a 100 W power or consumer source (up to 5 A at 20 V).

The new connector is designed to be non-polarized and fully reversible, no matter which way it is inserted.

This new reversible 24-pin USB Type-C™ plug is aimed to be an universal connector with all the advanced features proposed by Power Delivery:

- Negotiating power roles
- Negotiating power sourcing and consumption levels
- Performing active cable identification
- Exchanging vendor-specific sideband messaging
- Performing alternate mode negotiation, allowing third-party communication protocols to be routed onto the reconfigurable pins of the USB Type-C™ cable.

Figure 1. USB receptacle form factors



The following points should also be noted:

- USB Type-C™ cables use the same plug connector on both ends
- USB Type-C™ supports all prior protocols from USB2.0 onward, including the driver stack and power capability
- The new connector is quite small (it is 8.4 mm wide by 2.6 mm high).

As shown in Figure 1. USB receptacle form factors, the new USB Type-C™ plug allows a single connector to cover all features provided by previous plugs, which improves USB ease of use for all customers because of its flexibility in data and power roles.

A USB Type-C™ connection allows the port to be in host-mode only, device-mode only or dual role. Both data and power roles can be independently and dynamically swapped using USB Power Delivery commands.

2.1 USB Type-C™ vocabulary

The terminology commonly used for USB Type-C™ system is:

- **Downstream Facing Port (DFP)**: Associated with the flow of data in a USB connection. These are typically the ports on a host or on a hub to which devices are connected.

In its initial state, the DFP sources V_{BUS} and VCONN, and supports data.

A charge only DFP port only sources V_{BUS}

- **Upstream Facing Port (UFP)**: Associated with the flow of data in a USB connection. This is the port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, a UFP sinks V_{BUS} and supports data.
- **Dual Role Port (DRP)**: Refers to a USB port that can operate as either a source or a sink. The role of the port offers can be fixed to either source or sink, or may alternate between the two port states.

Initially, when operating as a source, the port also takes the role of DFP data provider. When operating as a sink, the port takes the role of a UFP data provider. The port role may be changed dynamically either to reverse power or data roles.

- **Source**: A port with Rp (pull-up resistor, see Figure 3. Pull up/down CC detection) on the CC pins (command control pins, see Section 4 CC pins), and providing power over V_{BUS} (5 V to 20 V and up to 5 A), most commonly a Host or Hub DFP (like legacy Type-A port)
- **Sink**: a port asserting Rd (Pull down resistor. See Figure 3. Pull up/down CC detection) on CC pins and consuming power from V_{BUS} (5 V to 20 V and up to 5 A), most commonly a device (for example a legacy Type-B port)

2.2 Minimum mandatory feature set

It is not mandatory to implement and support all of the advanced features that are defined within all Type-C and Power Delivery specifications.

The minimum features which need to be supported by the system are:

- Cable attach and detach detection
- Plug orientation/cable twist detection
- USB2.0 connection.

3 Connector pin mapping

The 24-pin USB Type-C™ connector includes:

- symmetric connections:
  - USB2.0 differential pairs (D+/D-)
  - Power pins: V_{BUS}/GND
- asymmetric connections
  - Two sets of TX/RX signal paths which support USB3.1 data speed
  - Configuration channels (CC lines) which handle discovery, configuration and management of USB Type-C™ power delivery features
  - Two side-band use signals (SBU lines) are present for analog audio modes, and can be used by alternate mode.

Figure 2. Receptacle pinout

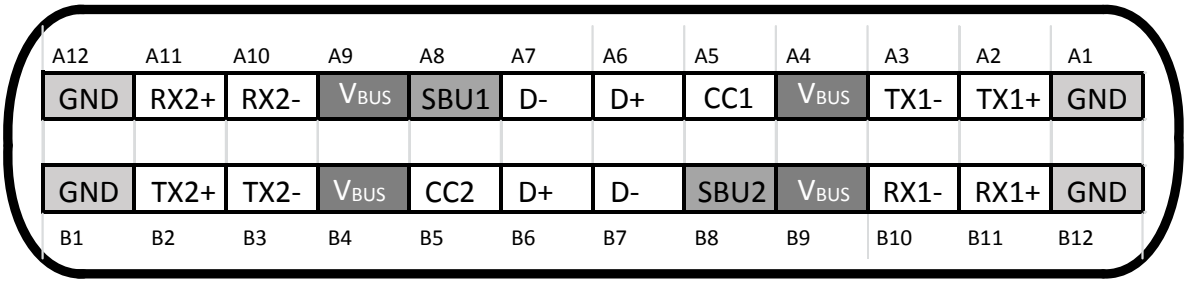


Table 3. USB Type-C receptacle pin descriptions

Pin	Name	Description	Comment
A1	GND	Ground return	can be up to 5 A split into 4 pins
A2	TX1+	USB3.0 datalines or alternate	10 Gbit TX differential pair in USB3.1
A3	TX1-		
A4	V_{BUS}	Bus power	max power is 100 W (20 V - 5 A) split into 4 pins
A5	CC1 or V_{CONN}	Configuration channel or power for active or electronically marked cable	In VCONN configuration, min power is 1 W
A6	D+	USB2.0 data lines	
A7	D-		
A8	SBU1	Side band use	Alternate mode only
A9	V_{BUS}	Bus power	max power is 100 W split into 4 pins
A10	RX2-	USB3.0 datalines or alternate	10 Gbit RX differential pair in USB3.1
A11	RX2+		
A12	GND	Ground return	can be up to 5 A split into 4 pins
B1	GND	Ground return	can be up to 5 A split into 4 pins

Pin	Name	Description	Comment
B2	TX2+	USB3.0 datalines or alternate	10 Gbit TX differential pair in USB3.1
B3	TX2-		
B4	V_{BUS}	Bus power	max power is 100 W split into 4 pins
B5	CC2 or VCONN	Configuration channel or power for active or electronically marked cable	In VCONN configuration, min power is 1 W
B6	D+	USB2.0 datalines	-
B7	D-		-
B8	SBU2	Side band use	Alternate mode only
B9	V_{BUS}	Bus power	max power is 100 W split into 4 pins
B10	RX1-	USB3.0 datalines or alternate	10 Gbit/s RX differential pair in USB3.1
B11	RX1+		
B12	GND	Ground return	Can be up to 5 A split into 4 pins

3.1 V_{BUS} power options

V_{BUS} provides a path to deliver power between a host and a device, and between a charger and a host or device. Power options available from the perspective of a device with a USB Type-C™ connector are listed below.

Table 4. Power supply options

Mode of operation	Nominal voltage	Maximum current	Note
USB2.0	5 V	500 mA	Default current based on specification
USB3.1	5 V	900 mA	
USB BC1.2	5 V	up to 1.5 A	Legacy charging
Current @1.5 A	5 V	1.5 A	Support high power devices
Current@3 A	5 V	3 A	
USB PD	Up to 20 V	up to 5 A	Directional control and power level management

Note: USB Type-C™ to Type-C cable assembly needs V_{BUS} to be protected against 20 V DC at the rated cable current (3 A or 5 A).

4 CC pins

There are two CC pins (CC1 and CC2) in the Type-C connector, but only one CC pin is present on the cable plug at each end of the cable (they are connected in common through the cable).

On both CC1 and CC2, DFP must have Rp pull up resistors, whereas UFP must have Rd pull down resistors.

Electronic cables need to provide an impedance, Ra, to ground on V_{CONN}.

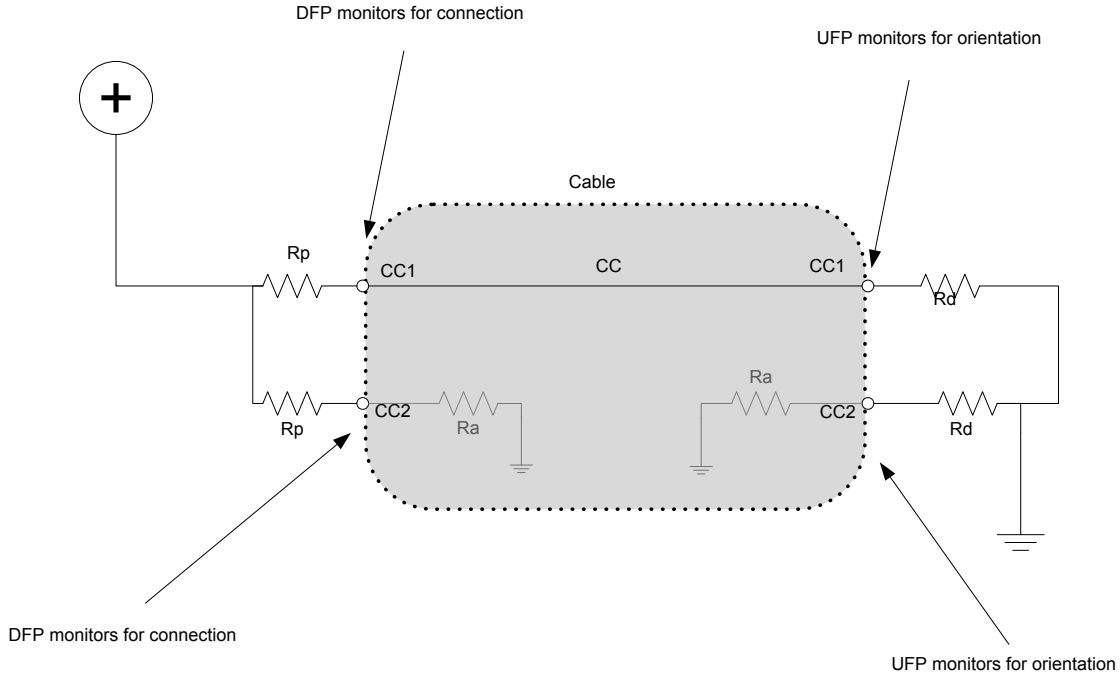
4.1 Plug orientation/cable twist detection

As USB Type-C™ can be inserted in the receptacle in either orientation, it is mandatory to first detect the orientation. The detection is done through the CC lines using the Rp/Rd resistors.

Initially a DFP presents Rp terminations on its CC pins and a UFP presents Rd terminations on its CC pins.

To detect the connection, the DFP monitors both CC pins (see figure 4-30 in USB Type-C Specification).

Figure 3. Pull up/down CC detection



4.2 Power capability detection and usage

Type-C offers increased current capabilities of 1.5 A and 3 A in addition to the default USB standard.
The current supply capability of the port to the device depends on the Rp pull up resistor value on the DFP.
5 A capability is negotiated using the USB Power Delivery protocol.
Table 5 below shows the possible values. (See table 4-15 in the USB Type-C Specification.)

Table 5. DFP CC termination (Rp) requirements

V_{BUS} power	Current Source to 1.7 V - 5.5 V	Rp pull up to 4.75 V - 5.5 V	Rp pull up to 3.3 V +/-5%
Default USB power	80 mA +/- 20%	56 kΩ +/- 20% (1)	36 kΩ +/- 20%
1.5 A @5 V	180 mA +/- 8%	22 kΩ +/- 5%	12 kΩ +/- 5%
3.0 A @5 V	330 mA +/- 8%	10 kΩ +/- 5%	4.7 kΩ +/- 5%

1. *For Rp when implemented in the USB Type-C plug on a USB Type-C to USB 3.1 Standard-A Cable Assembly, a USB Type-C to USB 2.0 Standard-A Cable Assembly, a USB Type-C to USB 2.0 Micro-B Receptacle Adapter Assembly or a USB Type-C captive cable connected to a USB host, a value of 56 kΩ ± 5% shall be used, in order to provide tolerance to IR drop on V_{BUS} and GND in the cable assembly.*

The UFP must implement Rd pull down resistors on both CC1 and CC2 to bias the detection system and to be identified as the power sink. (See also Table 4-16 in USB Type-C Specification.)

Table 6. UFP CC termination (Rd) requirements

Rd implementation	Nominal value	Can detect power capability?	max voltage on CC pin
+/- 20% voltage clamp	1.1 V	No	1.32 V
+/- 20% resistor to GND	5.1 kΩ	No	2.18 V
+/- 10% resistor to GND	5.1 kΩ	Yes	2.04 V

The UFP, in order to determine the DFP power capability, needs to monitor the CC line voltages accurately . (See also figure 4-27 in USB Type-C Specification.)

Table 7. Voltage on Sink CC pins (multiple source current advertisements)

Detection	Min voltage (V)	Max voltage (V)	Threshold (V)
vRa	-0.25	0.15	0.2
vRd-Connect	0.25	2.04	-
vRd-USB	0.25	0.61	0.66
vRd-1.5	0.70	1.16	1.23
vRd-3.0	1.31	2.04	-

5 Power profiles

The USB PD protocol enables advanced voltage and current negociation, to deliver power up to 100 W. See Figure 4. (See also Figure 10-1 in the USB Power Delivery Specification.)

Figure 4. Power profile

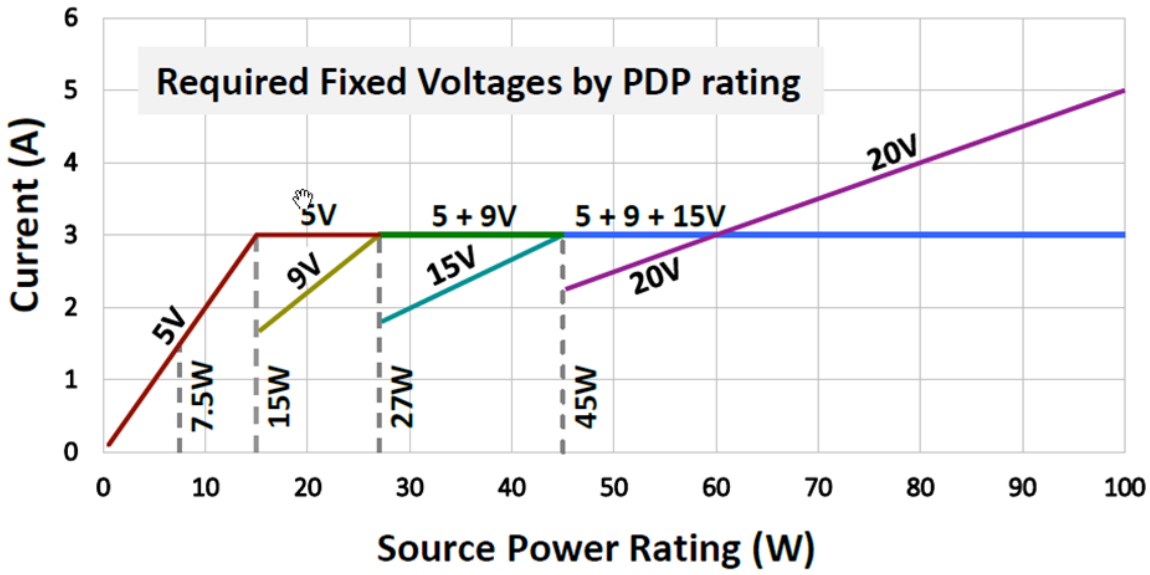


Table 8 shows the permitted voltage source and programmable power supply (PPS) selections, as a function of the cable current rating.

Table 8. Fixed and programable power supply current and cabling requirements

Power range	Fixed voltage source				Programmable power supply (PPS)			
	5 V	9 V	15 V	20 V	5 V (3 to 6 V)	9 V (3 to 6 V)	15 V (3 to 11 V)	20 V (3 to 21 V)
With 3 A cables								
0 < PDP <= 15 W	PDP / 5	-	-	-	PDP / 5	-	-	-
15 < PDP <= 27 W	3.0 A	PDP / 9	-	-	3.0 A	PDP / 9	-	-
27 < PDP <= 45 W	3.0 A	3.0 A	PDP / 15		3.0 A	3.0 A	PDP / 15	
45 < PDP <= 60 W	3.0 A	3.0 A	3.0 A	PDP / 20	3.0 A	3.0 A	3.0 A	PDP / 20
Requires 5 A cables								
60 < PDP <= 100 W	3.0 A	3.0 A	3.0 A	PDP / 20	3.0 A	3.0 A	3.0 A	PDP / 20

Further information is contained in the USB Type-C and USB PD specifications.

6 USB power delivery 2.0

In USB power delivery, pairs of directly attached ports negotiate voltage, current and/or the direction of power and data flow over the USB cable, using the CC wire as a BMC-coded communication channel.

The mechanisms used operate independently of other USB power negotiation methods.

6.1 Power delivery signaling

All communications are done through a CC line in half-duplex mode at 300 Kbit/s.

Communication uses BMC encoded 32-bit 4b/5b words over CC lines.

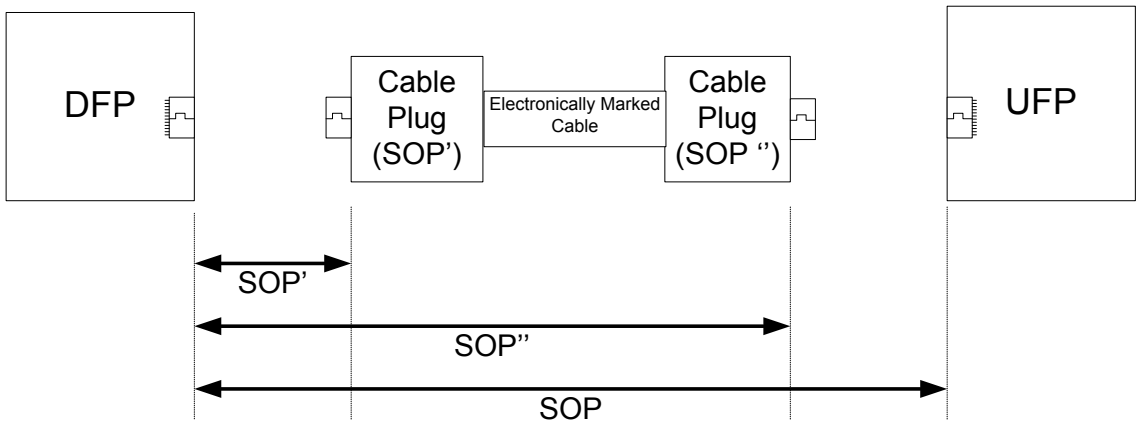
6.1.1 Packet structure

The packet format is:

- Preamble: 64-bit sequence of alternating 0s and 1s to synchronize with the transmitter.
- SOP* (start of packet) (can be SOP, SOP’ (start of packet sequence prime) or SOP” (start of packet sequence double prime) see Figure 5. SOP* signaling)
  - SOP packets are limited to PD capable DFP and UFP only
  - SOP’ packets are used for communication with a cable plug attached to the DFP
  - SOP” packets are used for communication with a cable plug attached to the UFP.

  A cable plug capable of SOP’ or SOP” communication must only detect and communicate with packets starting with SOP’ or SOP”.
- Message data including message header which identifies type of packet and amount of data
- CRC: error checking
- EOP (end of packet): unique identifier.

Figure 5. SOP* signaling



6.1.2 K-codes

K-codes are special symbols provided by the 4b5b coding. They signal hard reset and cable reset, and delineate packet boundaries.

6.2 Negotiating power

The DFP is initially considered as a bus master.

The protocol layer allows the power configuration to be dynamically modified.

The power role, data role and V_{CONN} swap are possible independently if both ports support dual power role functionality.

The default voltage on V_{BUS} is always 5 V and can be reconfigured as up to 20 V.

The default current capability is initially defined by the Rp value, and can be reconfigured as up to 5 A for an electronically marked USB PD Type-C cable.

The protocol uses start-of-packet (SOP) communications, each of which begins with an encoded symbol (K-code).

SOP communication contains a control or data message.

The control message has a 16-bit fixed size manages data flow.

The data message size varies depending on its contents. It provides information on data objects.

7 USB power delivery 3.0

From the power point of view, there are no differences between USB PD 2.0 and USB PD 3.0. All USB PD 3.0 devices are able to negotiate power contracts with USB PD 2.0 devices, and vice-versa. USB PD 3.0 adds the following key features:

- Fast role swap
- Authentication
- Firmware update
- Programmable power supply (PPS) to support sink directed charging.

The following is a summary of the major changes between the USB PD 3.0 and USB PD 2.0 specifications:

- Support for both Revision 2.0 and Revision 3.0 operation is mandated to ensure backward compatibility with existing products.
- Profiles are deprecated and replaced with PD power rules
- BFSK support deprecated including legacy cables, legacy connectors, legacy dead battery operation and related test modes
- Extended messages with a data payload of up to 260 bytes are defined
- Only the VCONN source is allowed to communicate with the cable plugs
- Source coordinated collision avoidance scheme to enable either the source or sink to initiate an atomic message sequence (AMS).
- Fast role swap defined to enable externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed.
- Additional status and discovery of:
  - Power supply extended capabilities and status
  - Battery capabilities and status
  - Manufacturer defined information.
- Changes to fields in the passive cable, active cable and AMA VDOs indicated by a change in the structured VDM version to 2.0.
- Support for USB security-related requests and responses
- Support for USB PD firmware update requests and responses.

System policy now references USBTypeCBridge 1.0.

8 Alternate modes

All the hosts and devices (except chargers) using a USB Type-C™ receptacle shall expose a USB interface.

If the host or device optionally supports alternate modes:

- The host and device shall use USB power delivery structured vendor defined messages (structured VDMs) to discover, configure and enter/exit modes to enable alternate modes.
- It is strongly encouraged that the device provide equivalent USB functionality where such exists for the best user experience.
- Where no equivalent USB functionality is implemented, the device must provide a USB interface exposing a USB billboard device class to provide information needed to identify the device. A device is not required to provide a USB interface exposing a USB billboard device class for non-user facing modes (for exmple diagnostic modes).

As alternate modes do not traverse the USB hub topology, they must only be used between a directly connected host and device.

8.1 Alternate pin re-assignments

In Figure 6, pins highlighted in yellow are the only pins that may be reconfigured in a full-feature cable

Figure 6. Pins available for reconfiguration over the Full Featured Cable

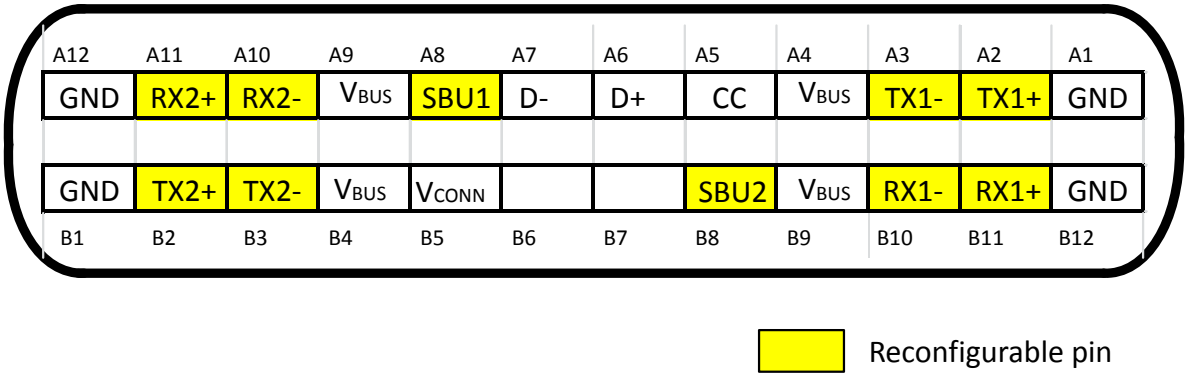
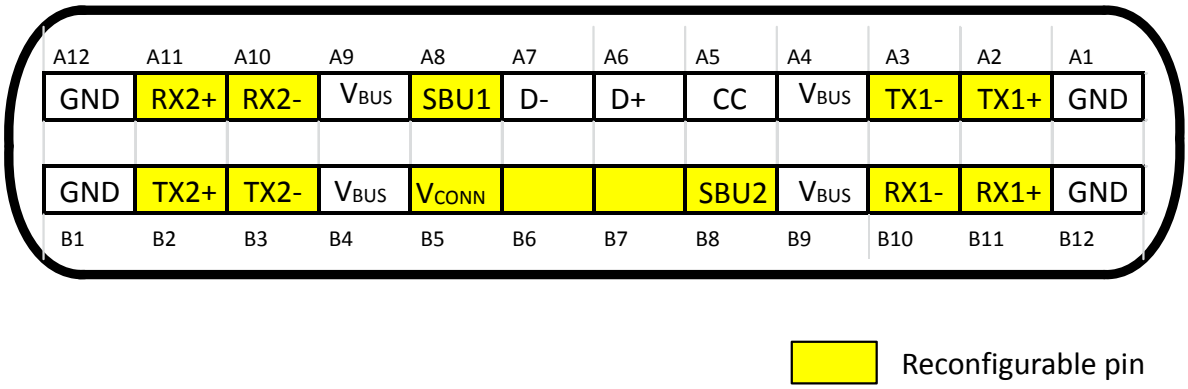


Figure 7. Pins available for reconfiguration for direct connect applications shows pins available for reconfiguration for direct connect applications. There are three more pins than in Figure 6 because this configuration is not limited by the cable wiring.

Figure 7. **Pins available for reconfiguration for direct connect applications**



8.2 Billboard

The USB Billboard Device Class definition describes the methods used to communicate the alternate modes supported by a device container to a host system.

This includes string descriptors to provide support details in a human-readable format.

For more details, refer to USB Billboard Device Class Specification, Revision 1.0, August 11, 2014, http://www.usb.org/developers/docs

9 Product offer

STM32xx Series MCUs and STM32xxx Series MPUs handle USB Type-C / USB Power Delivery interfacing by using the STM32 integrated UCPD (USB type-C Power Delivery) peripheral, or a set of general-purpose (GP) peripherals. See http://st.com/content/st_com/en/applications/connectivity/usb-type-c-and-usb-power-delivery.html

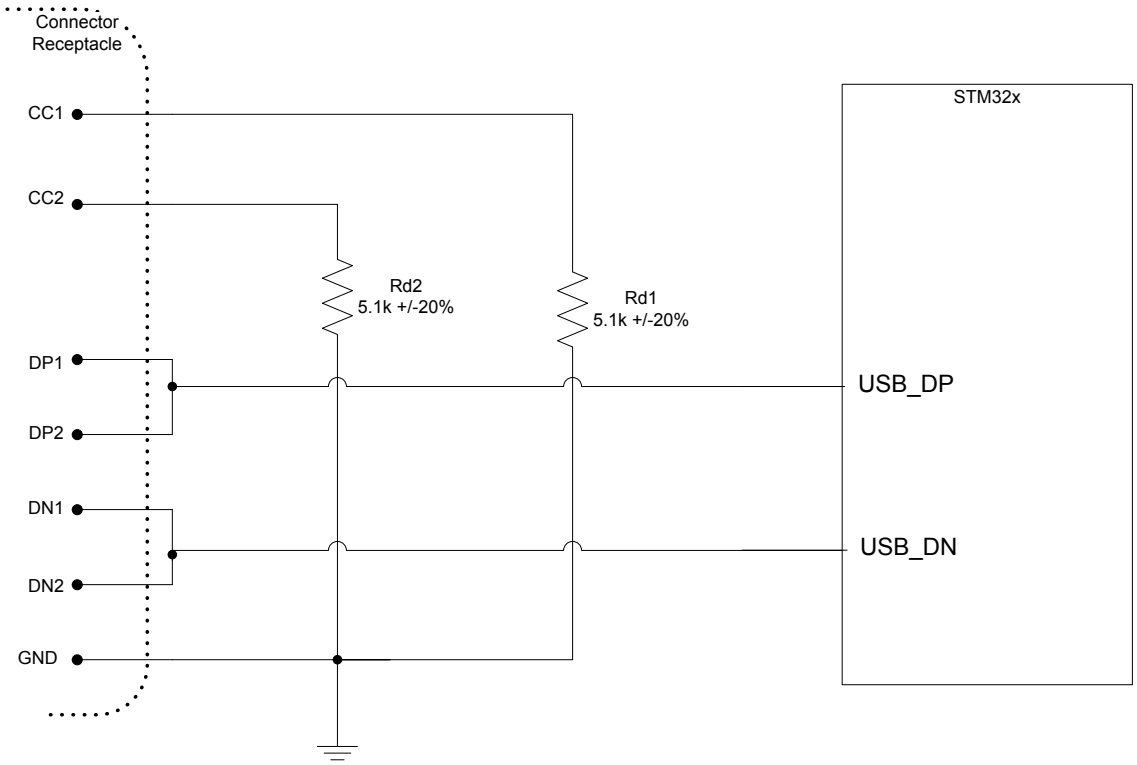
10 Using USB Type-C™ with no power delivery

10.1 STM32 USB2.0-only device conversion for USB Type-C™ platforms

A USB2.0 legacy device needs to present itself as a UFP by means of an Rd pull-down resistor between the CC line and ground. It is assumed here that the maximum legacy USB 2.0 device current is needed, and it is therefore not necessary to monitor the CC lines.

Since the plug is reversible, the two DP/DN pairs need to be connected to each other as close as possible to the receptacle, before being routed to the STM32 device.

Figure 8. Legacy device using USB Type-C™ receptacle



10.2 STM32 USB2.0 host conversion for USB Type-C™ platforms

This use case describes how to exchange a USB2.0 standard A receptacle for a USB Type-C™ receptacle.

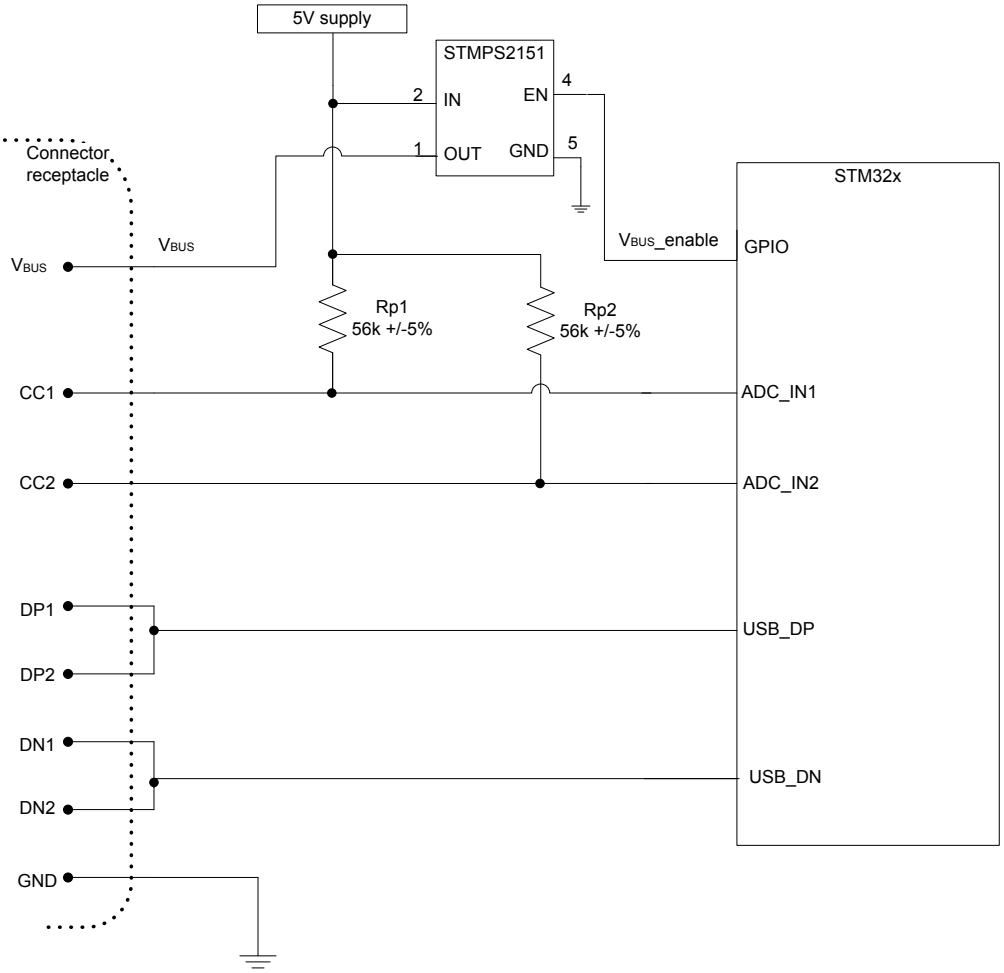
As the platform is designed for USB2.0, the maximum current capacity is 500 mA. If a higher supply current is available in the application, the Rp resistors can be adjusted to give 1.5 A or 3 A capability.

A USB2.0 legacy host needs to be configured as a DFP by means of a Rp pull up resistor between the CC line and the 5 V supply.

As the plug is reversible, the two DP/DN couples need to be connected in pairs as close as possible to the receptacle, before being routed to the STM32 device.

Monitoring CC lines through the ADC_IN inputs allow device-attachment detection and enabling of V_{BUS} on the connector.

Figure 9. **Legacy host using USB Type-C™ receptacle**



10.3 STM32 legacy USB2.0 OTG conversion for USB Type-C™ platforms

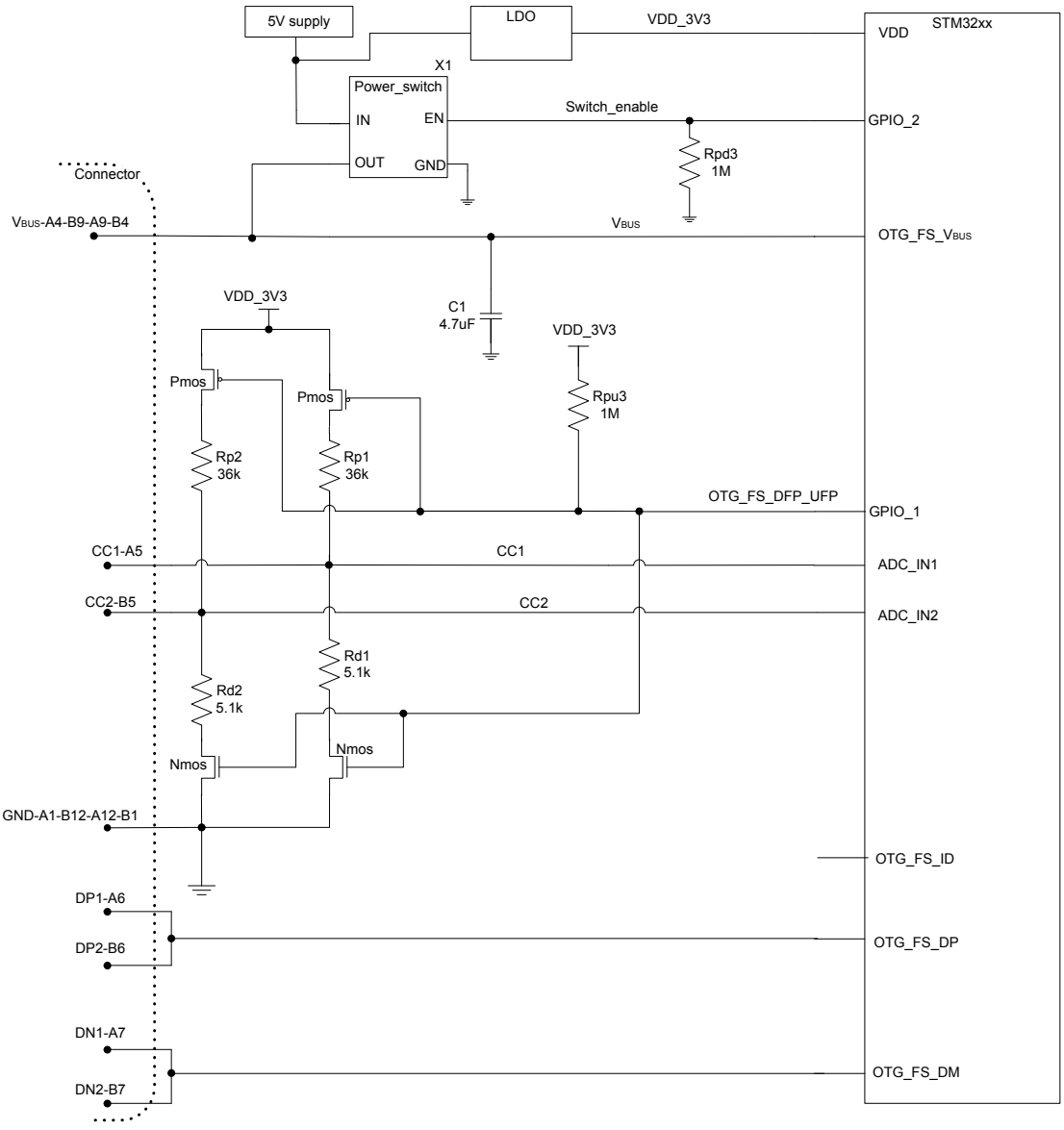
This use case explains how to exchange USB2.0 micro-AB receptacle for a USB Type-C™ receptacle.

In this use case the platform is designed for USB2.0, so the maximum current capacity is 500 mA. If a higher supply current is available in the application, the Rp resistors can be adjusted to give 1.5 A or 3 A capability.

A legacy OTG platform starts to work as host or device depending on the USB_ID pin impedance to ground provided by the cable.

USB Type-C(TM) is fully reversible, so the cable does not provide any role information. The role needs to be detected by sensing the CC lines (for example by using the ADC through its ADC_IN1 and ADC_IN2 inputs to detect the CC line level).

Figure 10. Legacy OTG using USB Type-C™ receptacle



The suggested sequence is:

1. Connect GPIO1 to OTG_FS_DFP_UFP driving a high level, and GPIO2 to Switch_enable driving a low level, to identify the platform as UFP.
2. If V_{BUS} is detected, the platform starts with the USB2.0 controller acting as a device.
3. If no V_{BUS} is detected after 200 ms minimum, OTG_FS_DFP_UFP is pulled down to be identified as a DFP through the Rp resistors, and to check whether a UFP is connected by comparing the ADC_IN1 and ADC_IN2 voltages to the expected threshold on the CC lines. Power switch X1 is kept disabled.
4. If UFP connection is detected, Switch_enable is pulled up to provide V_{BUS} on the connector, and the platform starts with the USB2.0 controller acting as host.

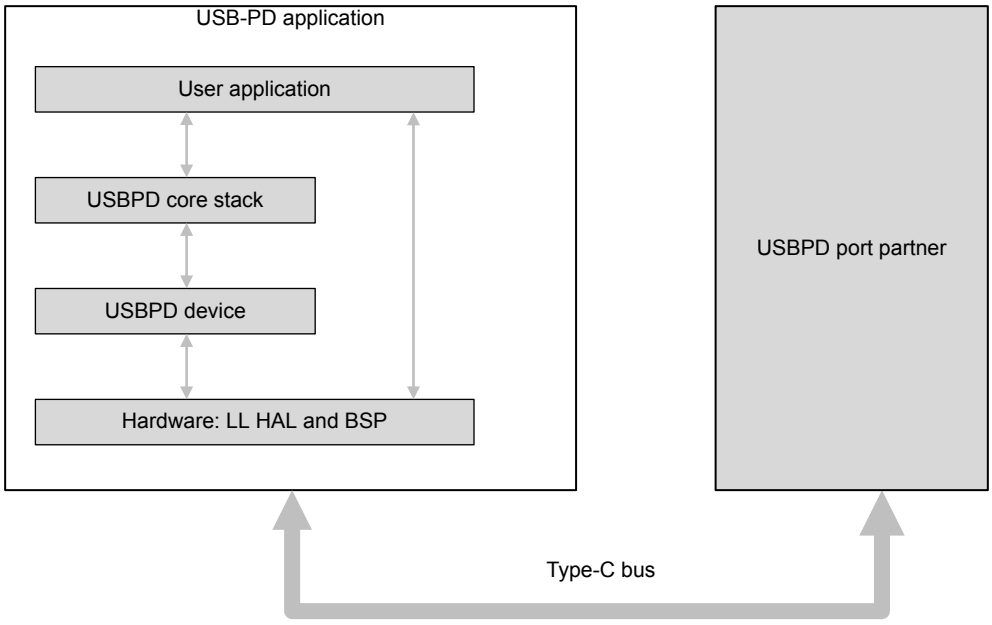
Because of the plug reversibility, the two DP/DN pairs need to be connected as pairs as close as possible to the receptacle, before routing to the STM32 device.

11 Type-C with power delivery using integrated UCPD peripherals

11.1 Software overview

STMicroelectronics delivers a proprietary USB-PD stack based on the USB.org specification. The stack architecture overview is shown below.

Figure 11. USB-PD stack architecture



Two parts are fully managed by STMicroelectronics (USBPD core stack and USBPD devices), so the user only needs to focus development effort on two other parts:

- User application part: called the 'Device Policy Manager' inside the USB organization specification. ST delivers an application template to be completed according the application need.
- Hardware part: the effort is mainly focussed on energy management, which depends on the resource materials chosen by the user to manage Type-C power aspects.

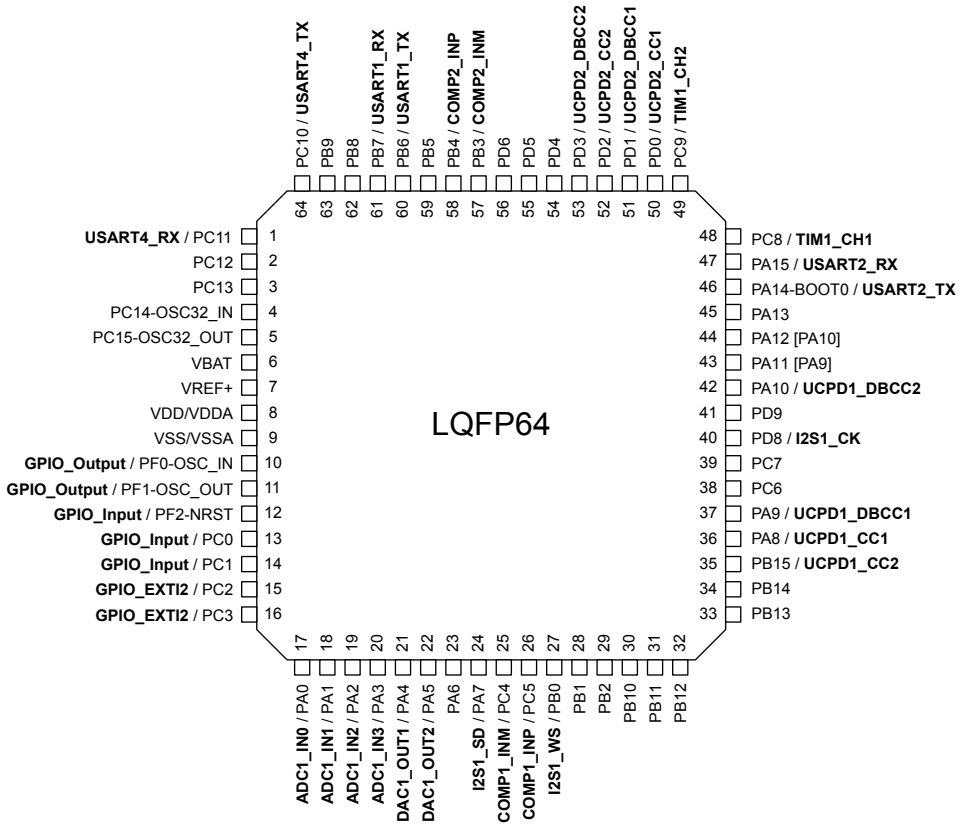
This document provides hardware implementation guidelines for the use of the STM32 resources (ADC, GPIO, and so on), but the developers' reference for power constraints is Chapter 7: 'Power Supply' of the Universal Serial Bus Power Delivery Specification.

See also UM2552 and Section 1.2 Reference documents for further information.

11.2 Hardware overview

Using the STM32 UCPD peripheral, flexible and scalable architectures can be achieved. STM32 GP peripherals such as PWM, ADC, DAC, I2C, SPI, UART, COMP, OPAMP, RNG, and RTC can be used. See the STM32CubeMx pinout tools for detailed information.

Figure 12. Device pinout example



The following sections show how to implement each power mode from the hardware point of view. All information concerning the software implementation is available in the reference specification.

11.2.1 SNK or sink modes

In SNK (Sink) modes the port (CC pins) is connected to GND through two pull-down resistors (Rd), and consumes power from V_{BUS} (5 V to 20 V and up to 5 A).

From a Sink (SNK) point of view:

- **Mandatory**:
  - Type-C port assert Rd (pull-down resistor) on CC lines
  - V_{BUS} sensing
  - Source 'detach' detection, when V_{BUS} moves outside the vSafe5V range
- **Optional**:
  - Sink power from V_{BUS}
- **Optional protection**:
  - OVP as defined by USB.org:
    - In the 'attach' state, a Sink should measure the V_{BUS} voltage level
    - An STM32 GP ADC can perform this measurement
  - Protection and EMI filtering on CC1, CC2 lines and V_{BUS} lines. See Section 14 Recommendations

The features are sumarized in Table 9:

Table 9. Sink features

Feature	STM32 peripherals involved	STM32 pin	External components or devices	Comments	Signal name
On protocol level					
Communication channels CC1 and CC2	UCPD: CC1, CC2	2	-	Mandatory. Able to handle Rd and Rp	CC1, CC2
Dead battery	UCPD: DBCC1, DBCC2	2	-	Handles Rd	DBCC1, DBCC2
V_{BUS} level, vSafe5V, measurement	ADC	1	Resistor divider bridge with or without op-amp for safety purpose	Mandatory only for OVP protection purpose	V_SENSE
On power level					
Sink power from VBUS			DCDC from V_{BUS} to 3.3 V (VDD)	Optional, LDO, DCDC, SMPS	-
Extra Power switch	GPIO	1	Power switch	Optional, MOS or power switch can be use	SNK_EN
On protection level					
CC1 and CC2			See Section 14 Recommendations	Optional	CC1 and CC2 on Type-C side
VBus			See Section 14 Recommendations	Optional	Vbus on Type-C side
On software level					
Message repetition	TIM			Used to drive timing repetition 1200 µs et 900 µs	See UM2552 for details
Message transmissions	DMA			For TX et RX transfer	See UM2552 for details

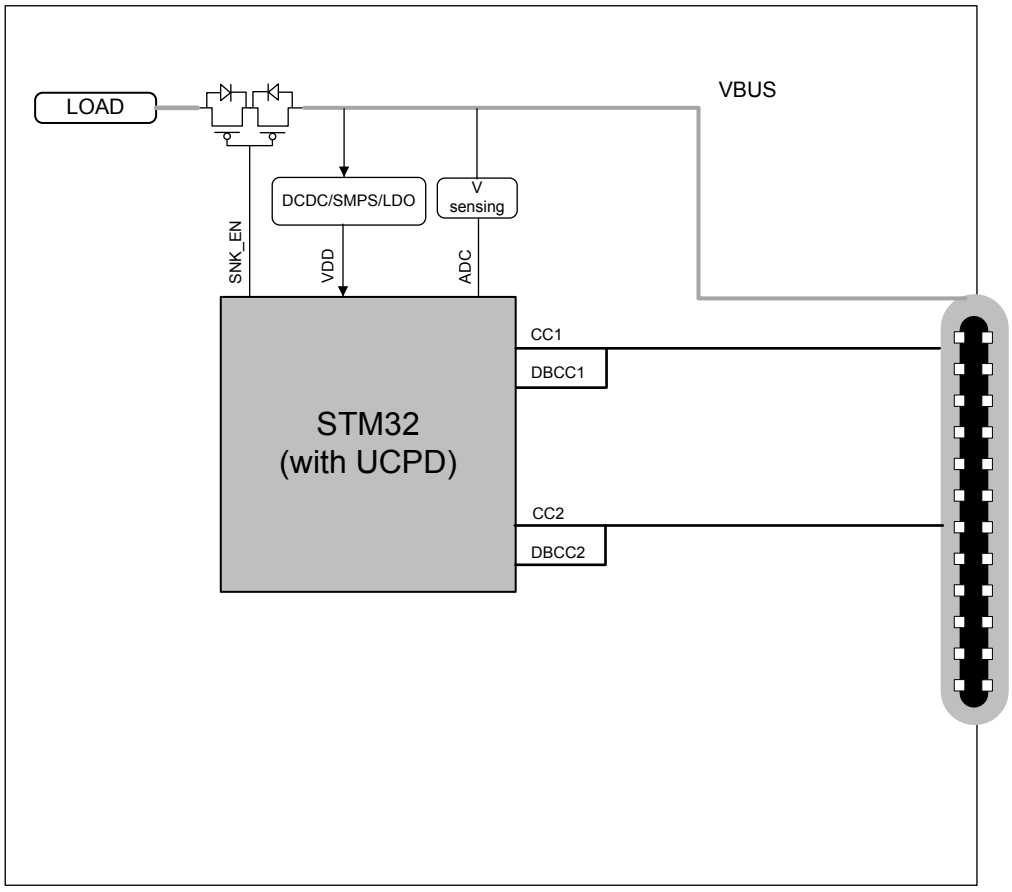
The following architecture schematics explain how to implement various Sink (SNK) modes.

11.2.1.1 *Sink V_{BUS} powered modes*

From the STM32 point of view, VDD is generated from V_{BUS}. An external LDO, DCDC or SMPS, is used, and an optional power-switch wire on V_{BUS} can power extra load. The SNK_EN GPIO pin controls this optional power-switch.

Regarding the protocol, two dedicated STM32 USBPD pins, DBCC1 and DBCC2, set Rd on the CC1 and CC2 lines. The DBCC lines must be wired to CC lines. No software action is needed, as Rd is present on the CC lines through the DBCC lines, with or without the STM32 power supply (VDD). After STM32 power-up, the USB-PD software stack switches the resistor connection from the DBCC to the CC lines.

Figure 13. SNK Vbus powered (dead battery) connections



Signal description

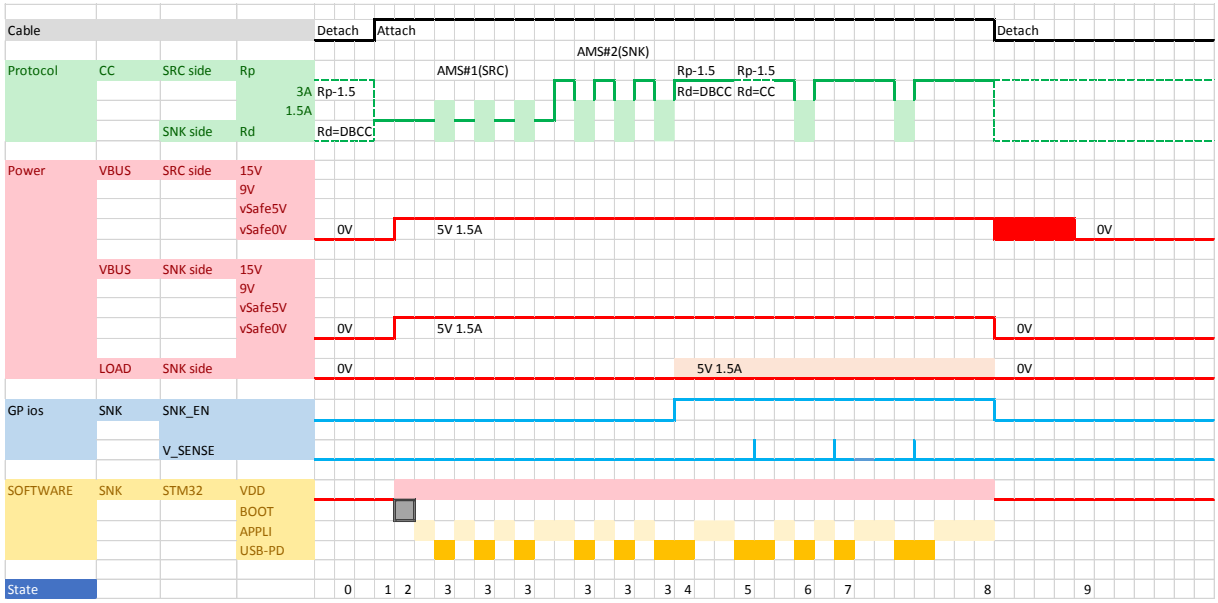
- CC1 and CC2 communication channel signals are wired to dedicated Type-C connector pins.
- The DBCC1 dead-battery signal is wired to CC1. This handles Rd when the STM32 is not powered via the CC1 line.
- The DBCC2 dead-battery signal is wired to CC2. This handles Rd when the STM32 is not powered via the CC2 line.

Optional:

- V_SENSE wired to an ADC through a resistor divider. V_{BUS} voltage measurement for OVP and safety purposes. The software stack, using the HAL_ADC driver, measures the V_{BUS} voltage level.

- SNK_EN signal GPIO connects and disconnects an optional V_{BUS} load.

Time line



The states are described below. Actions in italics are GPIO-based (ADC, IO, and so on):

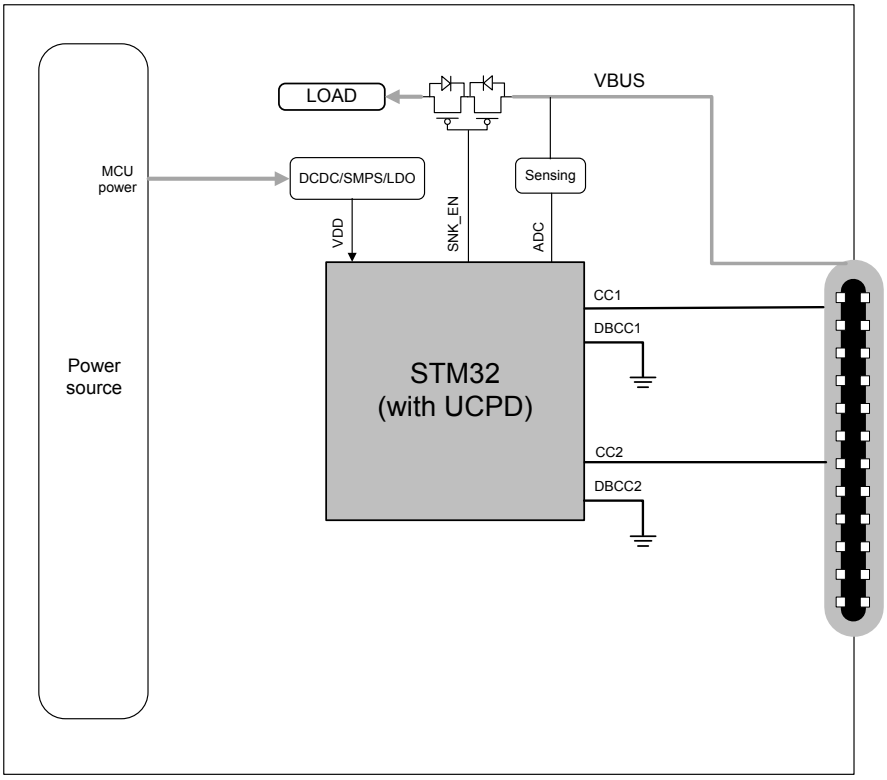
- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5A Rd = 5.1K (DBCC pin)*
- **State 1**: Connect cable. V_{BUS} is in Attach state
- **State 2**: STM32 boot, start application and initialize USB-PD software
- **State 3**: AMS between SRC and SNK
- **State 4**: *USB-PD: Enable load using SNK_EN gpio pin*
- **State 6**: *USB-PD: Use Rd from CC instead of DBCC*
- **State 7**: *USB-PD SW: OVP and safety are looking for V/I V_{BUS} senses*
- **State 8**: Disconnect cable, V_{BUS} is OFF on the Sink side
- **State 9**: Source discharges V_{BUS} to vSafe0V

11.2.1.2 *Sink using external power*

From the STM32 point of view, power comes from an external ACDC/DCDC/SMPS/LDO or battery. An optional power-switch connected to V_{BUS} can power additional load. The SNK_EN GPIO pin controls this optional power switch.

Regarding the protocol, the CC1 and CC2 lines set Rd. The DBCC1 and DBCC2 lines must be connect to GND.

Figure 14. SNK external power connections



Notes on DBCC1 and DBCC2 pins in SNK dead-battery mode

- If a UCPD peripheral is used, the DBCC1 and DBCC2 pins must be connected to the CC1 and CC2 lines. There is no way to use these pins for any alternate functions.
- The UCPDx_DBCC pins must be connected to the CC lines of USB Type-C connector
- Refer to the relevant STM32-UCPD device datasheets and reference manuals for further information (See Section 1.2 Reference documents).

Notes on DBCC1 and DBCC2 pins in SRC mode

- If a UCPD peripheral is used, the DBCC1 and DBCC2 pins must be connected to GND. There is no way to use these pins for any alternate functions.
- Refer to the relevant STM32-UCPD device datasheets and reference manuals for further information (See Section 1.2 Reference documents).
- The DBCC logic levels drive Rd on the CC line.
- In all cases:
  - DBCC = '0' (connect DBCC to GND) does not drive the CC level - mode (Rd or Rp) is not set.
  - DBCC = '1' (connect DBCC to CC) drives Rd on CC the cc line for Sink dead-battery operation
- Using extra TCPP01 protection, alternate functions can be used on the DBCC1 and DBCC2 pins.

Signal description

The CC1 and CC2 communication channel signals are wired to dedicated Type-C connector pins.

- DBCC1 signal wired to GND (as dead-battery mode is not used)
- DBCC2 signal wired to GND (as dead-battery mode is not used)

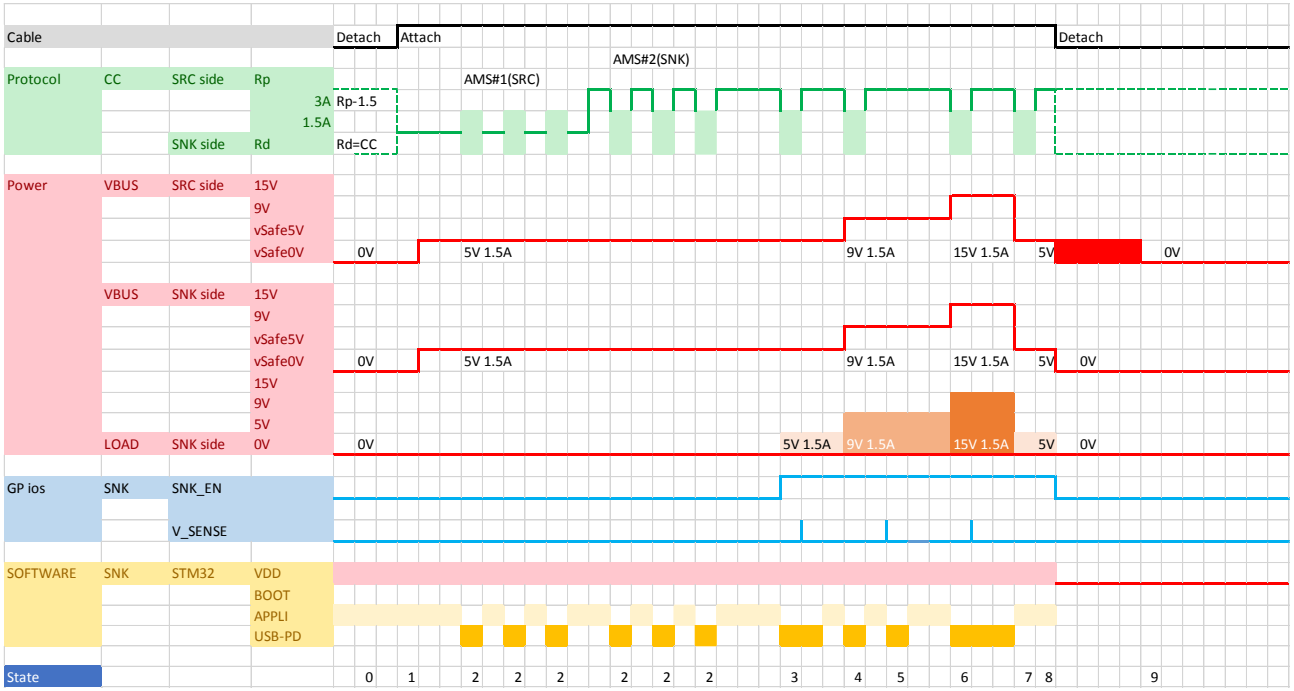
Optional:

- V_SENSE signal wired to an ADC through a resistor divider
- V_{BUS} voltage is measured for OVP and safety purposes
- The software stack, using the HAL_ADC, measures the V_{BUS} voltage level

SNK_EN signal GPIO pin connects and disconnects an optional V_{BUS} load.

Time line

Figure 15. Sink external power time line



The states are described below. Actions in italics are GPIO-based (ADC, IO, and so on)

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5 A Rd = 5.1 K (CC pin)*
- **State 1**: Connect cable. VBus is in Attach state
- **State 2**: AMS between SRC and SNK
- **State 3**: USB-PD: Enable load using SNK_EN GPIO pin
- **State 4** SNK requests 9 V
- **State 5**: *USB-PD SW: OVP and safety are looking for V/I Vbus senses*
- **State 6**: SNK requests 15 V
- **State7**: SNK requests 5 V
- **State 8**: Disconnect cable, V_{BUS} is off on Sink side
- **State 9**: Source discharge V_{BUS} to vSafe0V

11.2.2 SRC or source mode

The port asserts Rp on the CC pins and provides power over V_{BUS} (5 V to 20 V and up to 5 A).

From a Source (SRC) point of view:

- **Mandatory**:
  - Type-C port asserts Rp (pull-up resistor) on CC lines
  - Feed power to V_{BUS}
  - During detach or communication failure, the source reduces V_{BUS} to vSafe0V.
    An STM32 GP GPIO discharges V_{BUS} using an external MOS.
- **Optional**:
  - An STM32 GP ADC can do these measurements using a shunt or resistor bridge
- **Optional protection**:
  - Protection and EMI filtering on CC1, CC2 and V_{BUS} lines. See Section 14 Recommendations.

The features are summarized in Table 10.

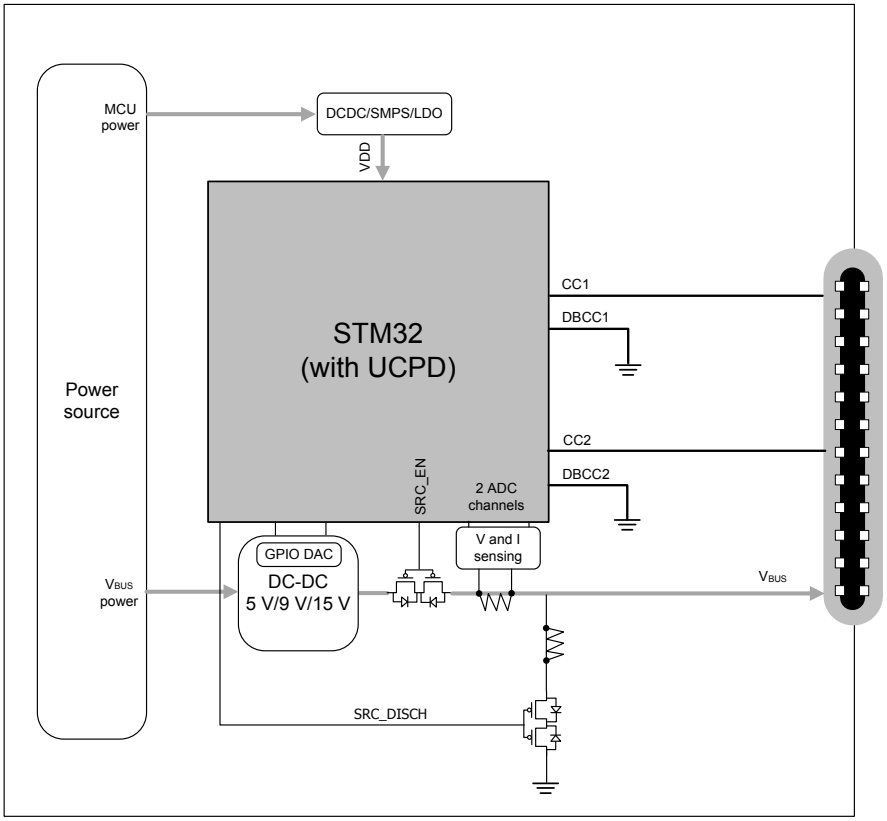
Table 10. Source features

Feature	STM32 Peripherals involved	STM32 pin	External components or devices	Comments	Signal name
On protocol level					
Communication channels CC1 and CC2	UCPD: CC1, CC2	2	-	Mandatory	CC1 CC2
Dead Battery	UCPD: DBCC1, DBCC2	2	-	Mandatory	DBCC1 DBCC1
Vbus Level, vSafe0V, measurement	ADC	1	Resistor divider bridge with or without op-amp for safety purpose	Optional	V_SENSE
On power level					
Provide power from VBUS	GPIO	1	Power switch	Mandatory, Dual-MOS can be use	SRC_EN
Discharge Vbus to vSafe0V	GPIO	1	MOS + charge Resistors	Mandatory	SRC_DISCH
ISense mesurement	ADC	1	Op-amp + shunt resistors	Optional	I_SENSE
CC1 and CC2			See Section 14 Recommendations		CC1 and CC2 on Type-C side
On protection level					
V_{BUS}			See Section 14 Recommendations		Vbus on Type-C side
On software level					
Message repetition	TIM	-	-	Used to drive timing repetition 1200 µs et 900 µs	See UM2552 for details
Message transmissions	DMA	-	-	For TX et RX transfer	See UM2552 for details

Figure 16. Source architecture explains how to handle Source (SRC) mode. From the STM32 point of view, power is provided by an external source such as an ACDC / DCDC / SMPS / LDO or battery.

Rp management is handled by the UCPD software stack. In this case, the DBCC lines must not be wired to the CC1 and CC2 lines. The DBCC1 and DBCC2 pins are wired to GND.

Figure 16. Source architecture



Signal descriptions

CC1 and CC2 communication channel signals are wired to dedicated Type-C connector pins.

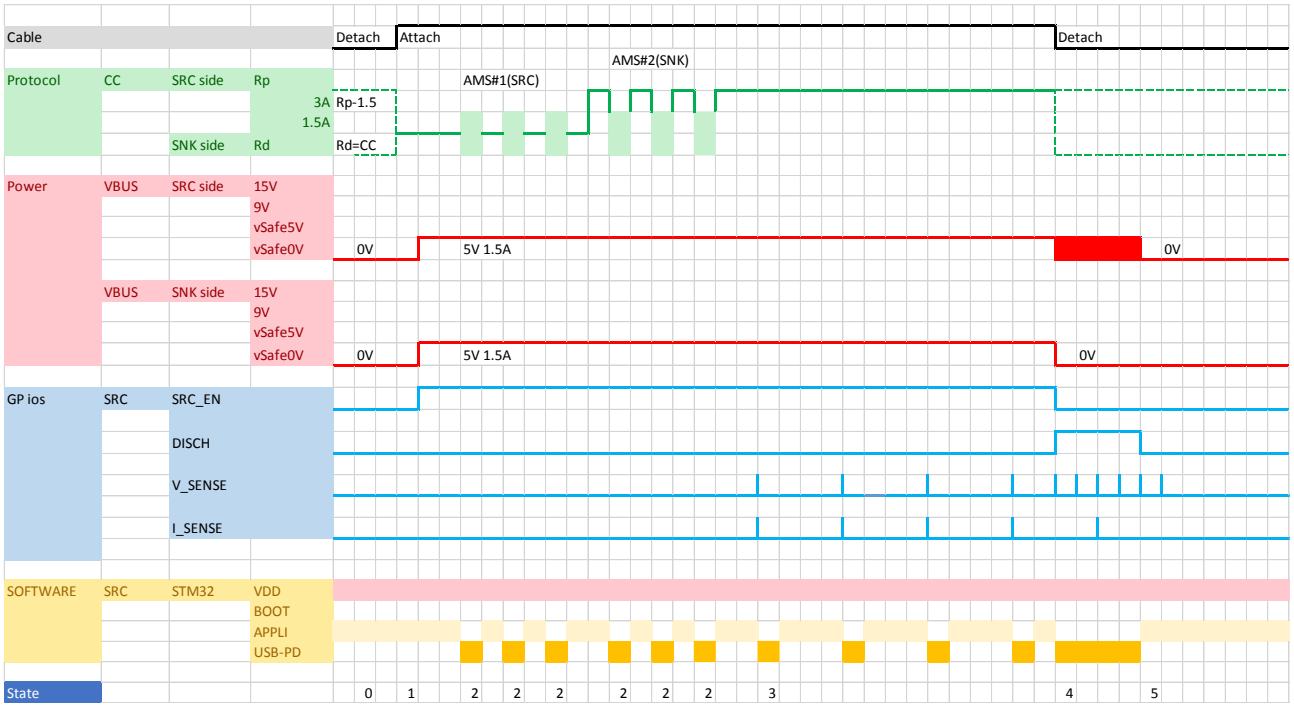
- the DBCC1 signal is wired to GND
- the DBCC2 signal is wired to GND

Optional:

- V_SENSE signal wired to an ADC through a resistor divider. V_{BUS} voltage measurement for OVP and safety purposes. Software stack, using the HAL_ADC driver to measure the V_{BUS} voltage level.

Time line

Figure 17. SRC (source) mode power timings



The states are described below. Actions in italics are GPIO-based (ADC, IO, and so on)

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5A Rd = 5.1K (CC pin)*
- **State 1**: Connect cable. V_{BUS} is on
  - Attach state
  - *USB-PD switches on V_{BUS} using the SRC_EN GPIO pin*
  - Capability exchange
- **State 2**: AMS between SRC and SNK
- **State 3**: *USB-PD SW: OVP and safety are looking for V/I V_{BUS} senses*
- **State 4**: Disconnect cable, V_{BUS} is OFF on the Sink side
  - *USB-PD initiates V_{BUS} discharge using the DISCH GPIO pin, until V_{BUS} reaches vSafe0V*
- **State 5**: Source V_{BUS} discharged to vSafe0V

11.2.4 DRP using the FRS feature

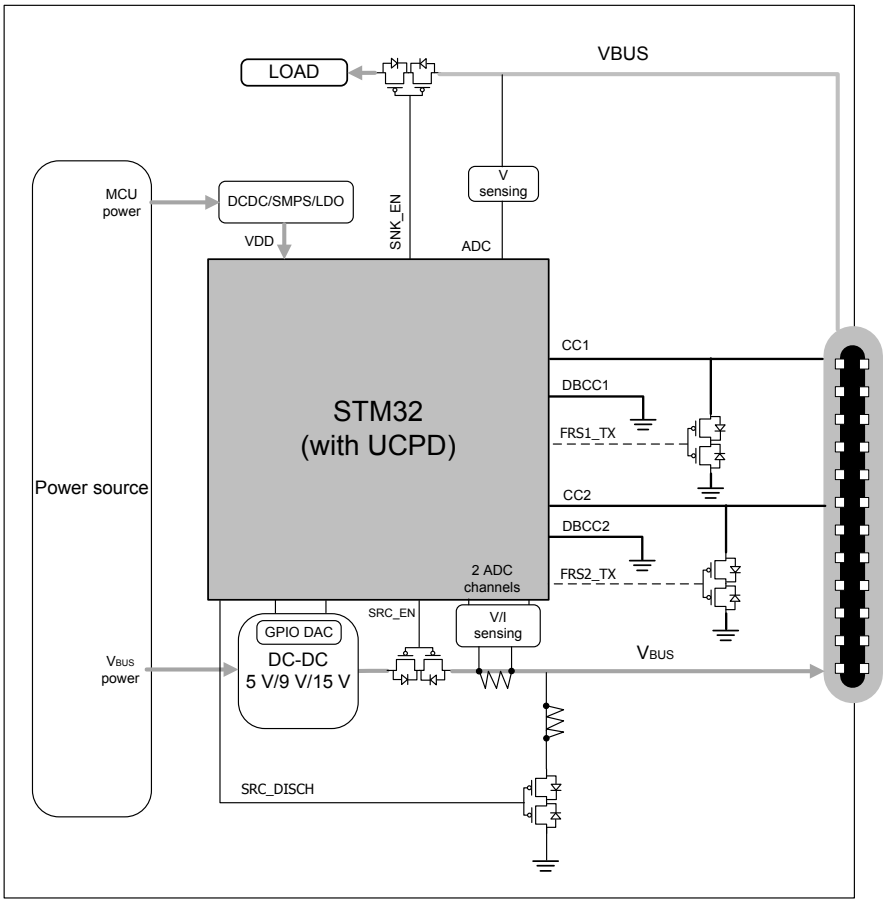
The following architecture schematics explain how to handle Dual Role Port (DRP) mode. From the STM32 point of view, power comes from an external source such as an ACDC/DCDC/SMPS/LDO, or battery.

Regarding the USB-PD protocol: the UCPD peripheral handles Rp and Rd through software.

In this case, the DRP can discuss with a SRC, a SINK or a DRP target. The power role, source or sink, can be changed on-the-fly without any cable disconnect when both devices are DRPs.

Fast Role Swap (FRS) allows any source with sudden power loss (for example mains power) to signal the condition to a sink with fast role swap capability far more rapidly than without FRS (for example FRS signaling/ detection works during messaging and regardless of collision control, thus taking no longer than 50 µs). Once the signaling is seen by the future source it prepares to detect the V_{BUS} level drop. It can take over driving V_{BUS} within the delay (150 µs) specified by the FRS procedure.

Figure 18. DRP with FRS Vbus = 5 V/9 V/15 V connections



Signal description

- The CC1 and CC2 communication channel signals are wired to dedicated Type-C connector pins.
- The DBCC1 signal is wired to GND.
- The DBCC2 signal is wired to GND.
- The SRC_EN signal GPIO pin is used to switch-on V_{BUS} using an external MOS or power switch.

- The SRC_DISCH signal GPIO pin initiates the discharge of V_{BUS} on detach. An external MOS can be used.
- The FRSTX1 and FRSTX2 fast role swap signals are wired to external MOS transistors to drive the CC lines.
- The V_SENSE signal is wired to an ADC through a resistor divider. The V_{BUS} voltage measurement for OVP and safety purpose. The software stack, using the HAL_ADC driver, measures the V_{BUS} voltage level.
- The I_SENSE signal is wired to an ADC through a resistor shunt. V_{BUS} current measurement for safety purposes. The software stack, using the HAL_ADC driver, measures the V_{BUS} current level.
- The SNK_EN signal GPIO pin is used to connect and disconnect an optional V_{BUS} load.

Time line

Figure 19. DRP with FRS mode time line example

The steps in italics are based on GPIOs (ADC, IO, and so on)

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5A Rd = 5.1K (CC pin)*

- **State 1**: Connect cable
  - *VBUS is on DRP1 set SRC_EN GPIO pin*
- **State 2**: Capabilitiy exchanges
  - DRP2 switches the on load on V_{BUS} using the SNK_EN GPIO pin
- **State 3**: *FRSTX (fast role swap) start*
- **State 4**: DRP1 move V_{BUS} to vSafe0V
- **State 5**: The DISXH GPIO pin initiates the DRP1 discharge
- **State 6**: End of V_{BUS} discharge
- **State 7**: Role swap between DRP1 and DRP2
- **State 8**: *DRP2 enables V_{BUS} using the SRC_EN GPIO pin*
- **State 9**: *DRP1 uses the SNK_EN GPIO pin on the V_{BUS} load ON*
- **State 10**: Disconnect cable
- **State 11**: End of discharge

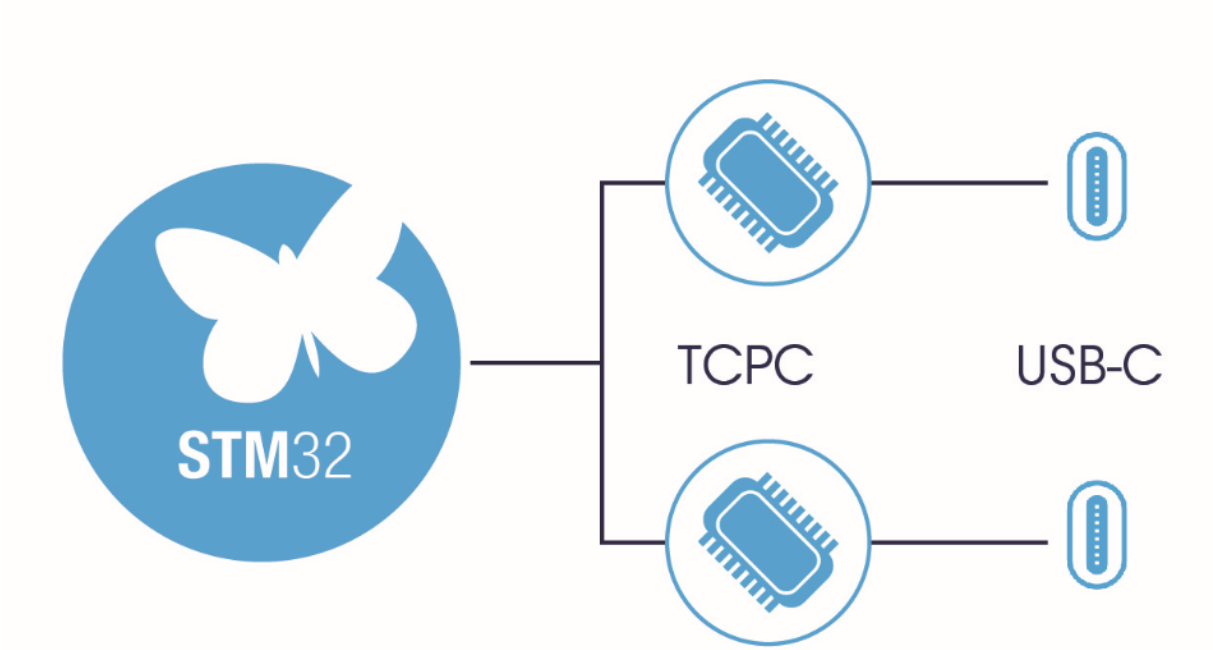
12 Type-C with power delivery using a general-purpose peripheral

12.1 Software view

The software architecture is the same as that described in Section 11.1 Software overview

12.2 Hardware view

Figure 20. Hardware view for Type-C power delivery with a general-purpose peripheral



Using a general-purpose peripheral, the TCPM/TCPC interfaces are a convenient way of handling USB power delivery. STM32xx Series MCUs and STM32xxx Series MPUs using a communication bus can handle all TCPM/TCPC companion chips.

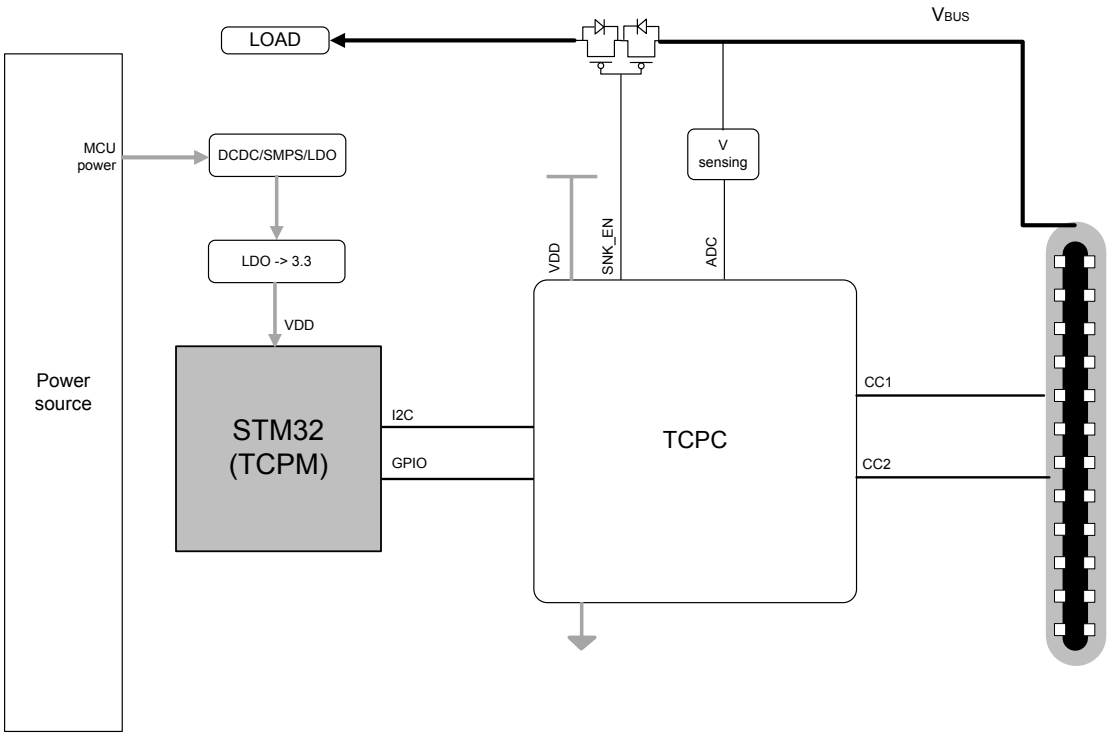
Usually the I2C, SPI or GPIOs are used to handle communication messages and exceptions.

12.3 SNK using TCPM TCPC interface

In Sink (SNK) mode, the Type-C port must assert Rd (pull-down resistor) on CC lines, and takes power from V_{BUS}. The sink detects source attachment when V_{BUS} reaches vSafe5V. Detection requires an ADC for example.

The STM32 communicates with the TCPM/TCPC interface, typically using the I2C bus. In some cases an SPI, ADC, DAC, or GPIO completes the communication between the STM32 general purpose MCU and the TCPM/TCPC external component.

Figure 21. Sink mode using TCPM TCPC interface

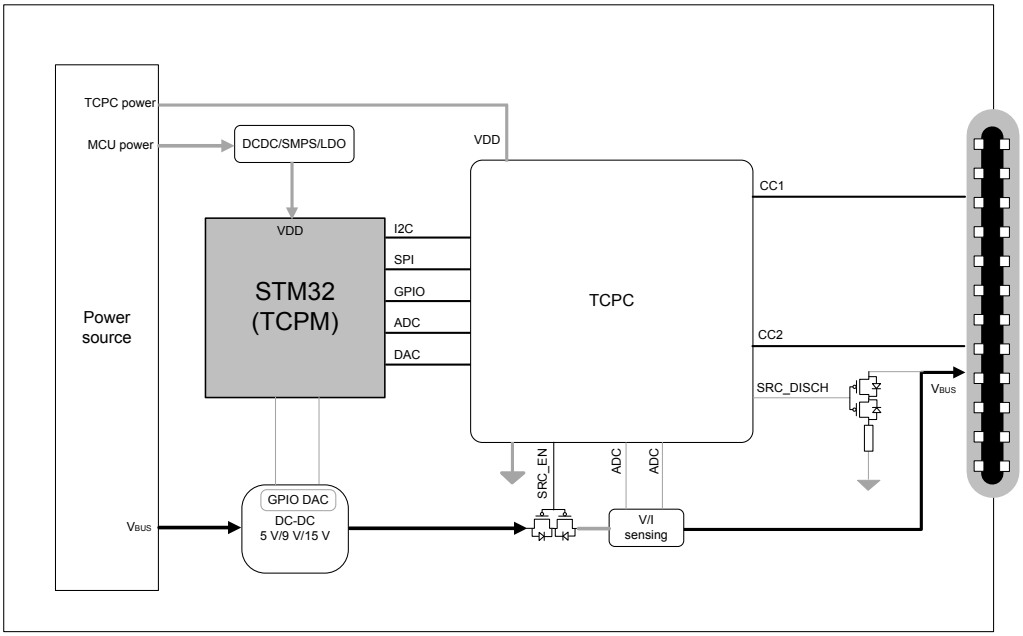


12.4 SRC using TCPM TCPC interface

In Source (SRC) mode, the Type-C port must assert Rp (pull-up resistor) on the CC lines and provide power through V_{BUS}. During detach or communications failures, the source must reduce V_{BUS} to vSafe0V. This means that a device must discharge V_{BUS}.

The STM32 (acting as TCPM) usually communicates with TCPM/TCPC interfaces using the I2C bus. In some cases an SPI, ADC, DAC, or a GPIO complete the communication between the STM32 general-purpose MCU and TCPM/TCPC external components.

Figure 22. Source mode using TCPM TCPC interface

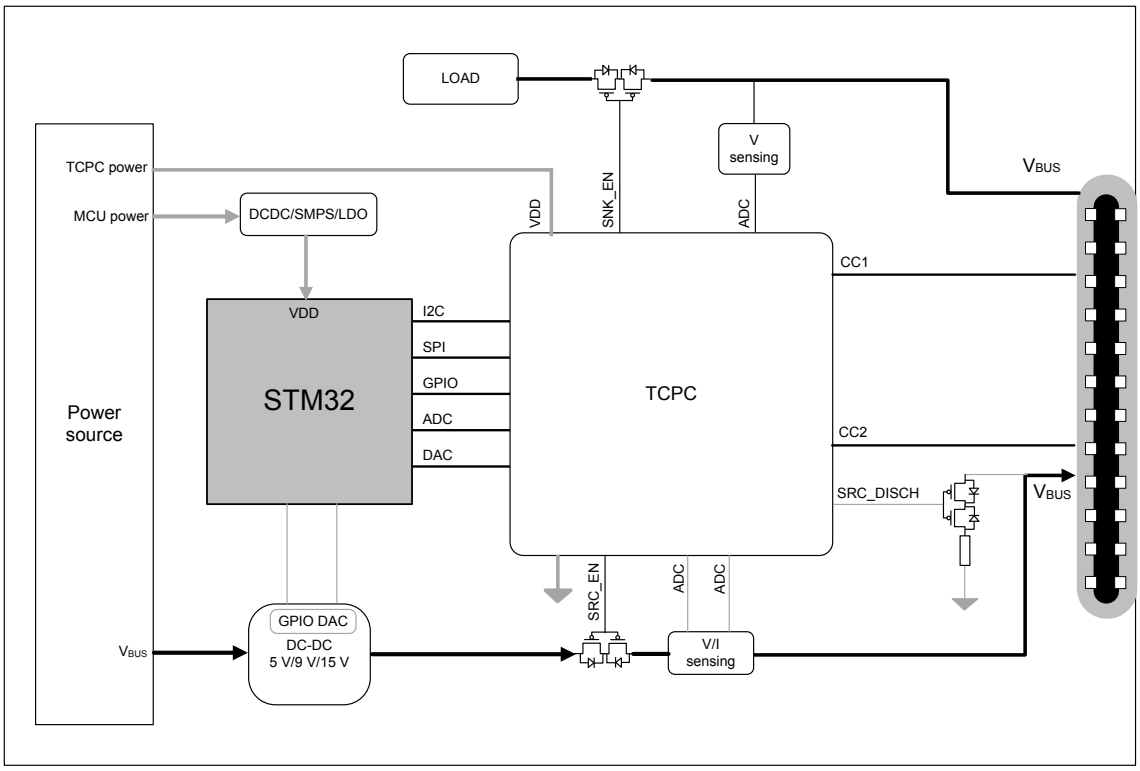


12.5 DRP using TCPM TCPC interface

A Dual Role Port (DRP) can operate as either a Source (SRC) or a Sink (SNK). The role of the port can be fixed to either source or sink, or it can alternate between the two port states. Initially when operating as a source, the port also takes role of a downstream facing port (DFP), and when operating as a sink, the port takes the role of an upstream facing port (UFP). The port role may change dynamically to reverse either power or data roles.

The STM32 usually communicates with the TCPM/TCPC interface using the I2C bus. In some cases an SPI, ADC, DAC, or GPIO completes communications between the STM32 general purpose MCU and the TCPM/TCPC external component.

Figure 23. Dual-role port mode using TCPM TCPC interface

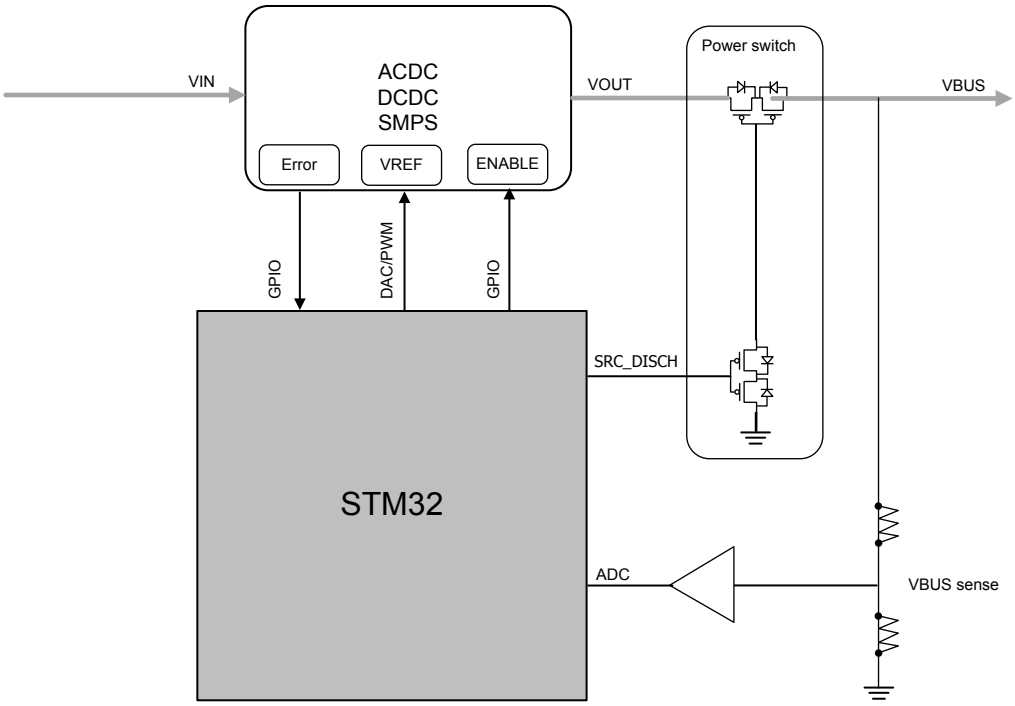


13 Dedicated architecture proposals and solutions

13.1 How to supply V_{BUS} SRC and DRP modes

SRC and DRP modes source V_{BUS} to the Type-C connector. Commonly used power stages include DC-DC, ACDC and switched-mode power supplies (SMPS), with or without a battery. A power switch, or MOS, helps to connect and disconnect V_{BUS} to the power output stage. The general-purpose STM32 ADCs, DACs, GPIOs and I2C allow flexible and scalable power-stage control. STM32 GP peripheral enable, measurement and register control is possible usng the I2C bus.

Figure 24. Vbus monitoring



Signal descriptions

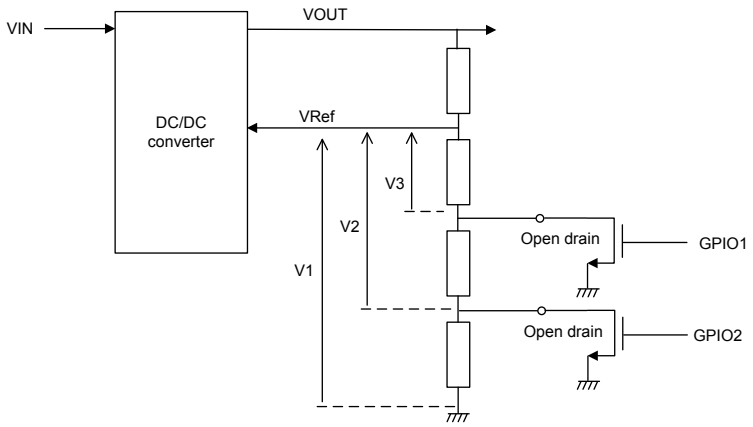
- ADC: the STM32 GP ADC measures V_{BUS} voltage level
- GPIO: the STM32 GP GPIO controls power switch or power-stage enable signals
- PWM: the STM32 GP PWM and RC provide the power-stage voltage reference
- DAC: the STM32 GP DAC provides the voltage reference to the power stage

In the G0 implementation, the DCDC is driven by a PWM generated with a timer (available in the STM32,). The aim is to determine the PWM corresponding to the requested voltage. An iteration algorithm estimates the target PWM, and a voltage measurement confirms whether the expected value is reached.

13.2 DCDC Vout management using GPIO: resistor-bridge mode

The VRef voltage level can be monitored using a few GPIOs in open-drain mode. The implementation is shown in Figure 25. Adjusting Vref using OpenDrain GPIO. According the GPIO1 and GPIO2 levels, we can change VRef, and hence the VOUT level.

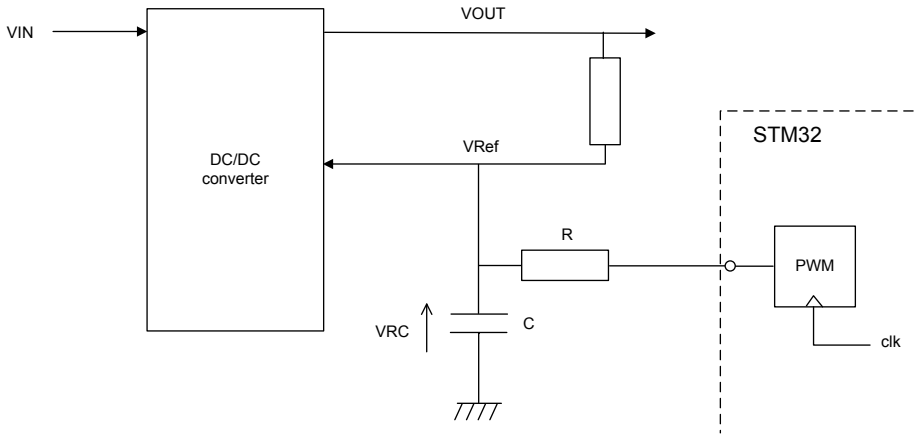
Figure 25. Adjusting Vref using OpenDrain GPIO



13.3 DCDC Vout management using GPIO: RC mode

The Vref voltage level can be monitored using one GPIO in PWM mode. The RC low-pass filter values and duty-cycle PWM ratio sets the Vref voltage level. Figure 25. Adjusting Vref using OpenDrain GPIO this implementation.

Figure 26. Adjusting Vref using PWM GPIO channel

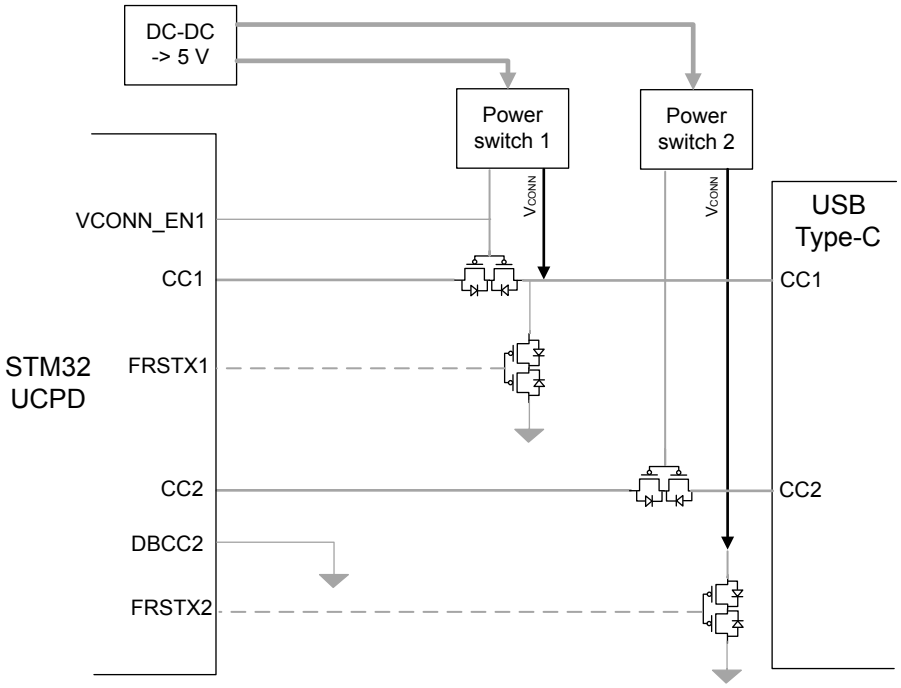


13.4 How to supply VCONN in SRC and DRP mode

A VCONN enabling function is required for Type-C SRC or DRP roles. A single VCONN voltage generator is present in the system. Two power switches apply the VCONN 5 V source to either the CC1 or CC2 pin, and two MOSFETs isolate the UCPD CC1 and CC2 lines from the VCONN 5 V source. Two FRS commutation MOSFETs discharge the CC lines when the VCONN 5 V source is switched-off.

This implies the use of at least two GPIOs to control VCOMM_EN1 and VCONN_EN2 in Figure 27.

Figure 27. VCONN monitoring



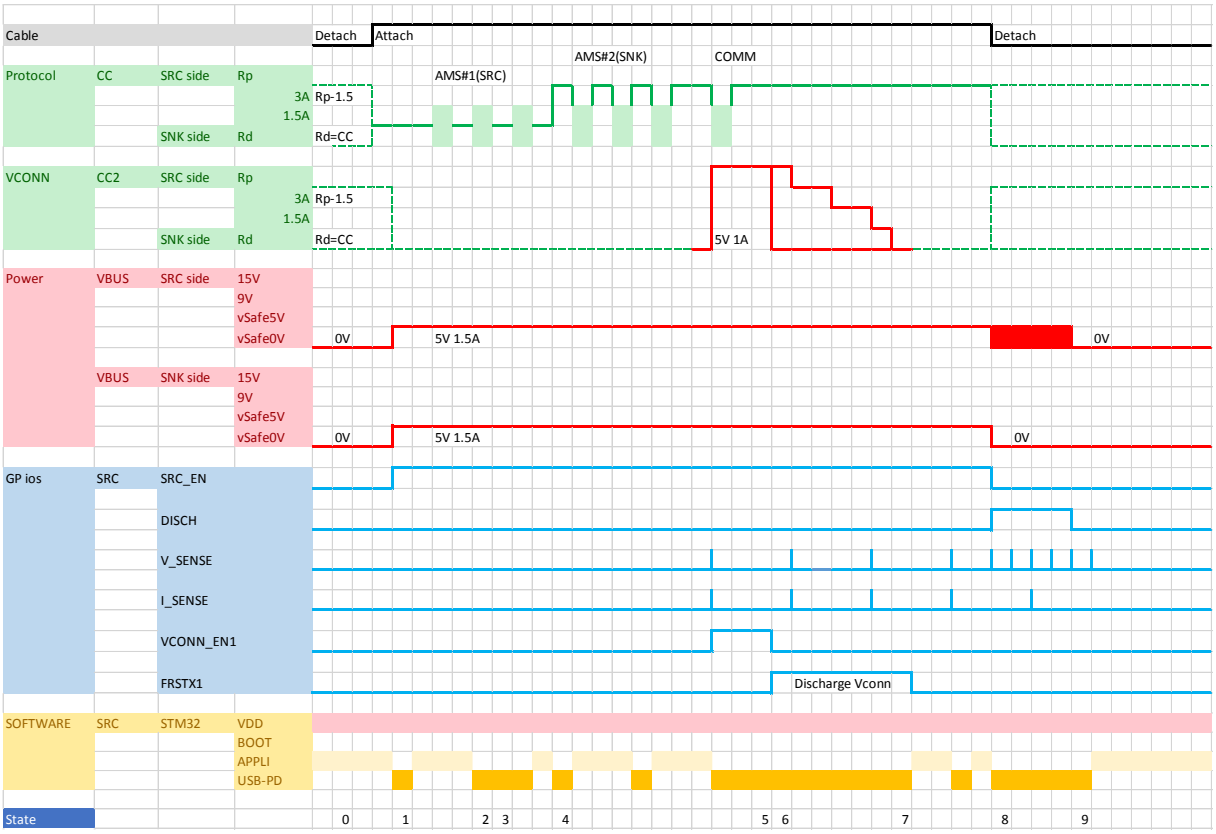
Signal description

The EN_VCONN1 and EN_VCONN2 signal GPIO pins provide control of the connection of VCONN to the Type-C CC lines and isolate the STM32 CC lines from VCONN.

For software details see Section 1.2 Reference documents, UM2552.

Time line

Figure 28. **VCONN monitoring time line example**



The sequence is as follows, where actions in itallics are based on GPIOs (ADC, IO, and so on):

- **State 0**: No connection between equipment
  - Detach state
  - *Rp = 1.5A Rd = 5.1K (CC pin)*
- **State 1**: Connect cable. V_{BUS} is turned on using the SRC_EN GPIO pin. Attach state.
  - *USB-PD switch on VBUS using SRC_EN GPIO pin*
  - capabilities excahanged
- **State 2**: Request VCONN ON
- **State 3**: Enable VCONN using VCONN_EN1/2 GPIO pins
- **State 4**: *USB-PD SW: OVP and safety are looking for V/I V_{BUS} senses*
- **State 5**: Request VCONN ON
- **State 6**: Disable VCONN using VCONN_EN GPIO pin
  - *Start to discharge CC2/VCONN using FastRoleSwap pin or FRSTX GPIO pin*
- **State 7**: Disconnect cable, V_{BUS} is OFF on the sink side
  - *USB power delivery uses the DISCH GPIO pin to initiate the V_{BUS} discharge using until V_{BUS} reaches vSafe0V*
- **State 8**: The source discharges V_{BUS} to vSafe0V

13.5 How to implement fast role swap (FRS) signalling in DRP mode

FRS signaling is only required for Type-C DRP roles. Only the powered hub sends FRS signals on power-outage detection. This is entirely optional.

TX (FRS signaling): USBPD peripheral requires hardware to drive the CC line strongly to GND

- This implies two external NMOS transistors, controlled by the STM32 USBPD peripheral
- One per CC line

RX (detection of FRS signaling): For detection of FRS signaling (RX aspect) is internal and can be enabled by software.

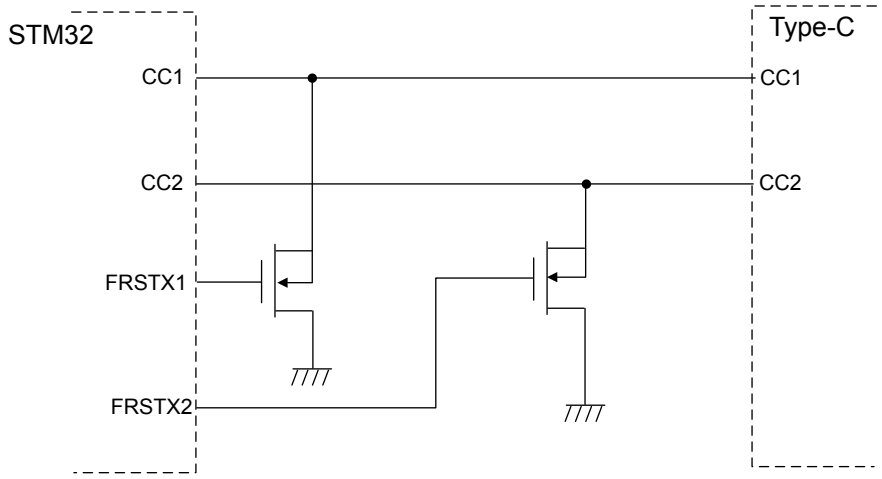
- Software uses a USBPD interruption. The FRSTx AF GPIO choice is handled by software.

The USBPD peripheral provides a control bit (FRSTX) that is available through alternate-function multiplexing. It is only written to 1 to start the 'FRS signaling' condition. The condition is auto-cleared in order to respect the required timing. See the relevant STM32xx Series MCU or STM32xxx Series MPU datasheet for further details. This behavior is introduced in Power Delivery3.0, is optional, and only applies to DRP roles. It allows a fast solution to swap power roles for a source that loses its ability to supply power.

A DRP in source (SRC) mode signals 'FRS' as an alert condition in order to swap power roles (that is, the V_{BUS} source) as quickly as possible. Typically, this is useful in the absence of a local battery.

When the VCONN feature is used, FRSTX1 and FRSTX2 discharge the CC1 and CC2 lines through MOS transistors.

Figure 29. Fast role-swap DRP mode circuit



13.6 How to monitor V_{BUS} voltage and current in SNK, SRC and DRP modes

Protection and safety

A DC-DC converter circuit, such as the L7987, is used to generate V_{BUS} and VCONN, and includes built-in OTP / OVP / OCP generation. These errors can be handled in software at the user application level for safety purposes. To do this, the DC-DC fault output signal can be routed to EXTI on the STM32 side.

PD protocol

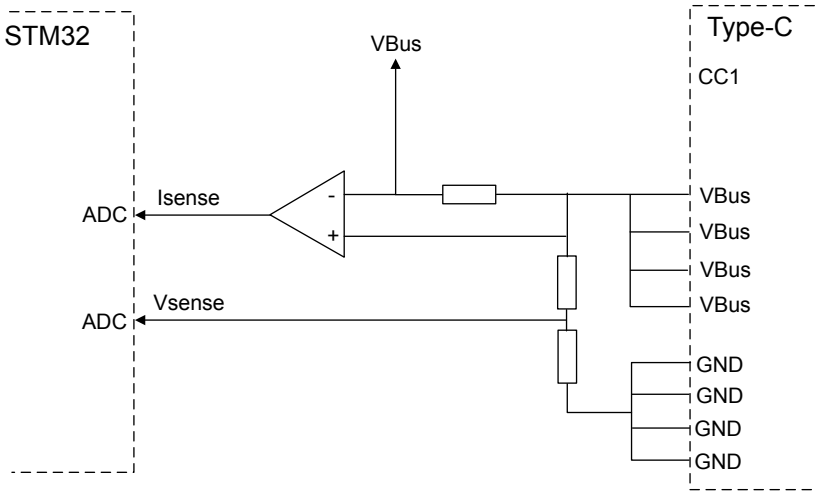
In SNK roles, we must measure the V_{BUS} level to handle REQUEST_ACCEPT / PS_RDY / DETACH protocol messages on the software side. In this case, one ADC is mandatory on the STM32 side.

In SRC roles, V_{BUS} voltage tracking should be implemented to adjust V_{BUS}, through DC-DC output, for PDO or APOD uses cases.

Method

Use a low resistance shunt to measure the V_{BUS} current. Use a basic resistor bridge to measure V_{BUS} voltage. Optionally add an OpAmp for OVP and safety purposes.

Figure 30. **V_{BUS} voltage and current monitoring circuit**



14 Recommendations

14.1 ESD/EOS protection devices for USB Type-C

Dedicated ESD and EOS protection can be used on:

- V_{BUS} power delivery signals
- D+/D-, TX/RX Super- and High-speed signals
- CC, SBU side-band usage and communication channel signals

For further information,refer to:

- AN4871 (Section 1.2 Reference documents)
- www.st.com/protection-typec for protection and filtering devices for USB Type-C

Table 11. Recommended protection devices

Power supply	3.3 V: SMLVT3V3 5 V: DSDA7P120-1U1M 9 to 12 V: ESDA15P60-1U1M
User push	ESDALC6V1-1U2 (1 line, pitch 350 µm)
Button	ESDA5V3L (2 lines)
Joystick	ESDA6V1-5SC6 (5 lines)

USB power delivery drives voltages higher than 5 V on V_{BUS}, as consequence, TVS must be selected according this voltage:

- ESDA7P120-1U1M for 5 V V_{BUS}
- ESDA13P70-1U1M for 9 V V_{BUS}
- ESDA15P60-1U1M for 12 V V_{BUS}
- ESDA17P50-1U1M for 15 V V_{BUS}
- ESDA25P35-1U1M for 20 V V_{BUS}

14.2 Capacitors on CC lines

The USB PD specification allows CC receiver (cReceiver) capacitance in the range of 200 pF to 600 pF.
For noise filtering purposes, an extra 390 pF +/- 10% capacitance must be added on each CC line.

14.3 TCPP01 Type-C port protection

Two Type-C power delivery failure modes are identified:

- V_{BUS} high voltage short circuit to the CC lines when hot a unplug is done with a poor mechanical quality connector. Over voltage protection is needed on the CC line. This use case appears only when power delivery is used.
- V_{BUS} line compromised if a defective charger is stuck at a high voltage. Overvoltage protection is needed on the V_{BUS} line. This use case can occur even when power delivery is not used.

A dedicated single chip can be used for system protection. The TCPP01-M12 is a cost effective solution to protect low-voltage MCUs or other controllers performing USB-C Power Delivery management. It is especially suited to sink or source applications. The TCPP01-M12 provides 20 V short-to-V_{BUS} over-voltage and IEC ESD protection on CC lines, as well as programmable over-voltage protection with an NMOS gate driver for the V_{BUS} line.

The TCPP01-M12 also integrates dead battery management, and can be completely turned off for battery-powered devices. A fault report is also generated.

TVS is still required on V_{BUS} (ESDA25P35-1U1M), and then only the maximum voltage is considered.

14.3.1 Sink modes

In the Sink V_{BUS} powered case, the system is only powered through the USB-C connector.

Figure 31. Sink V_{BUS} powered case

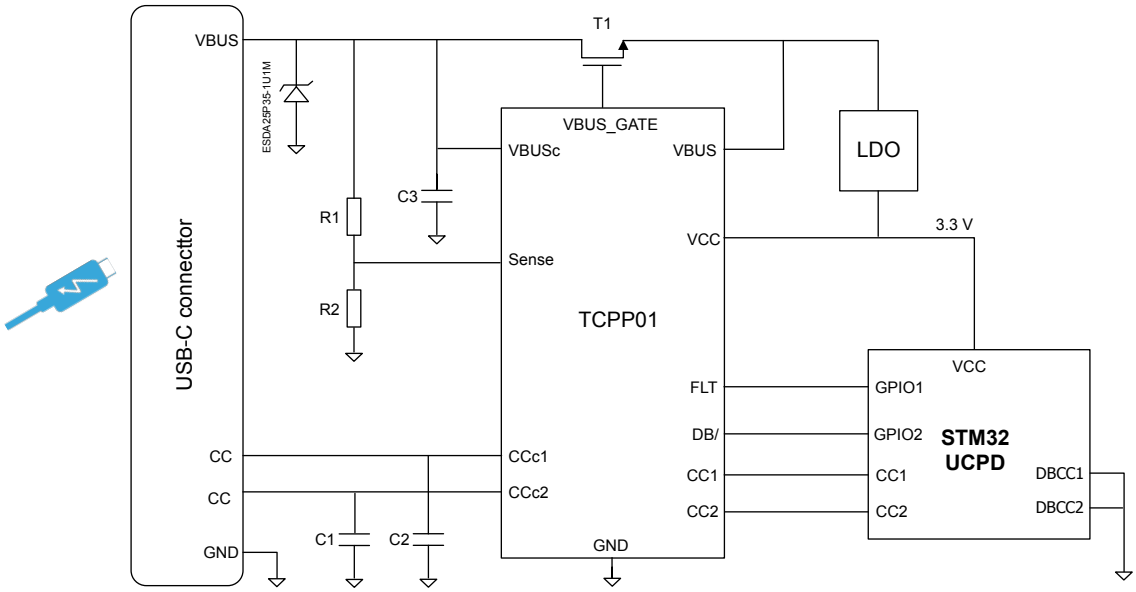
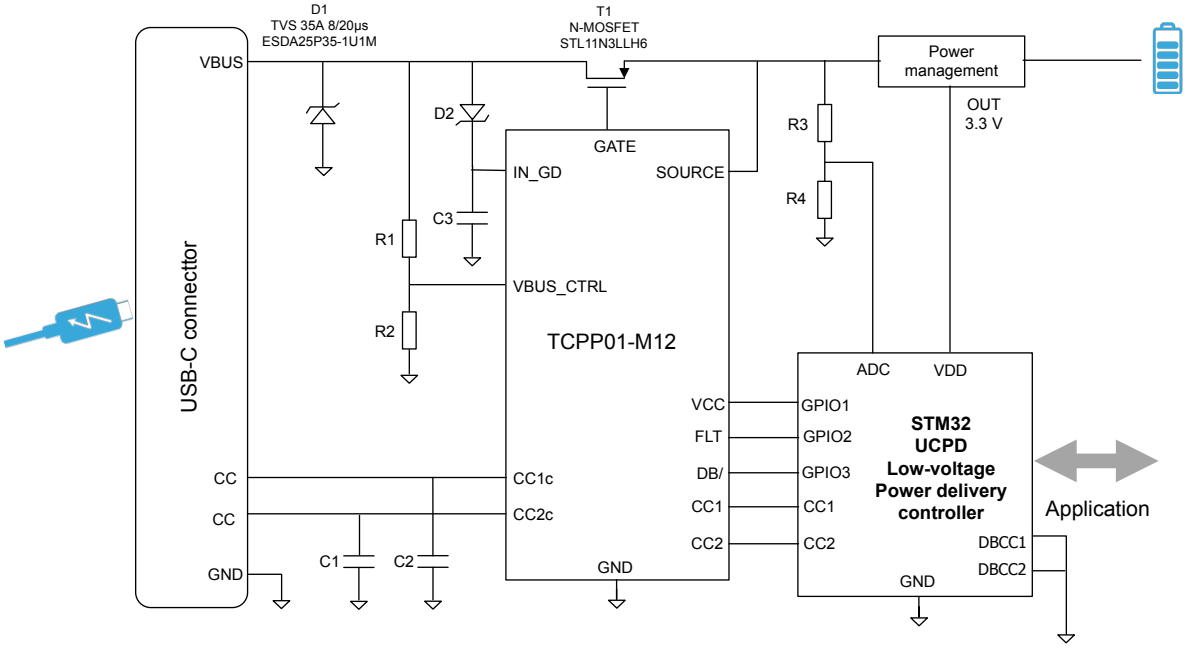
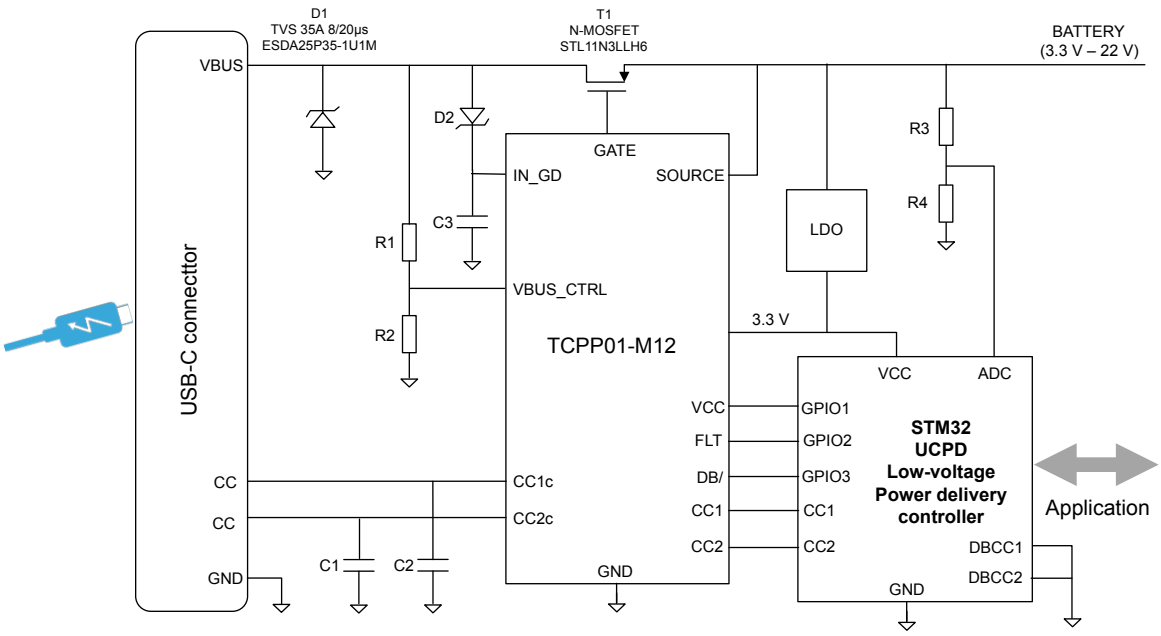


Figure 32. **Sink PD3.0 applications, with battery**



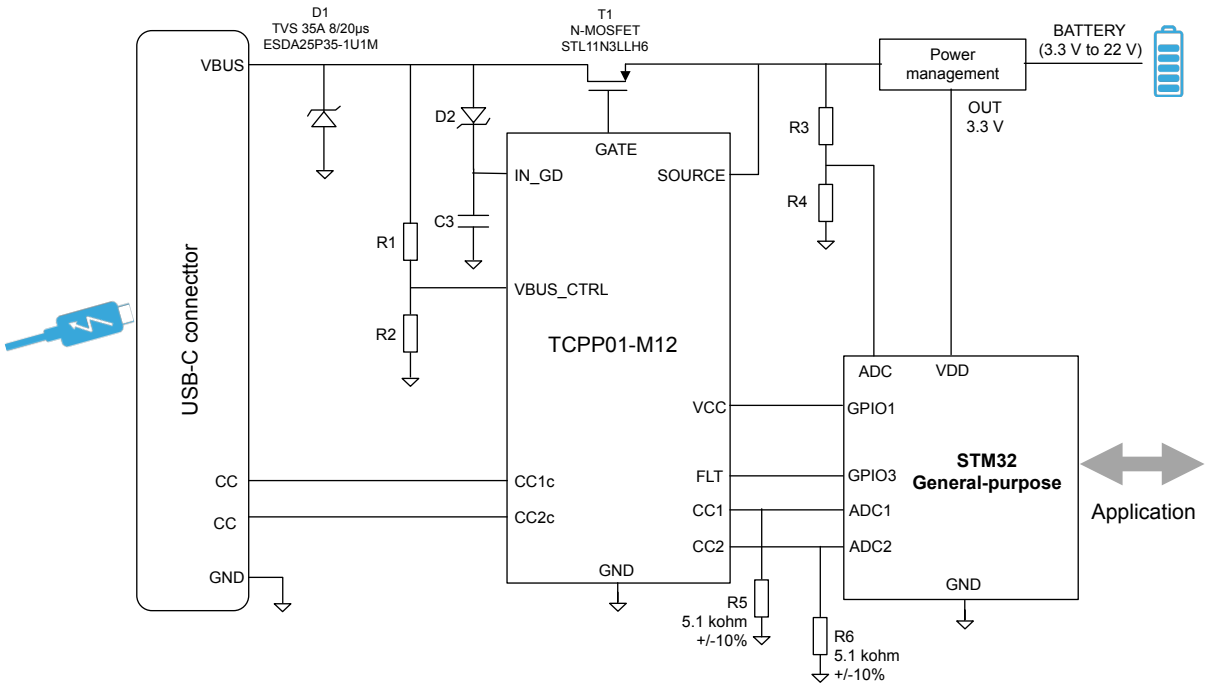
- FLT (FAULT) is an open-drain output pin.
- DB/ is a pull-down TCPP input. Connect to 3.3V if not managed by MCU software.

Figure 33. **Sink applications, without battery**



- FLT (FAULT) is an open-drain output pin.
- DB/ is a pull-down TCPP input. Connect to 3.3 V if not managed by MCU software.

Figure 34. **15 W sink applications, with battery**



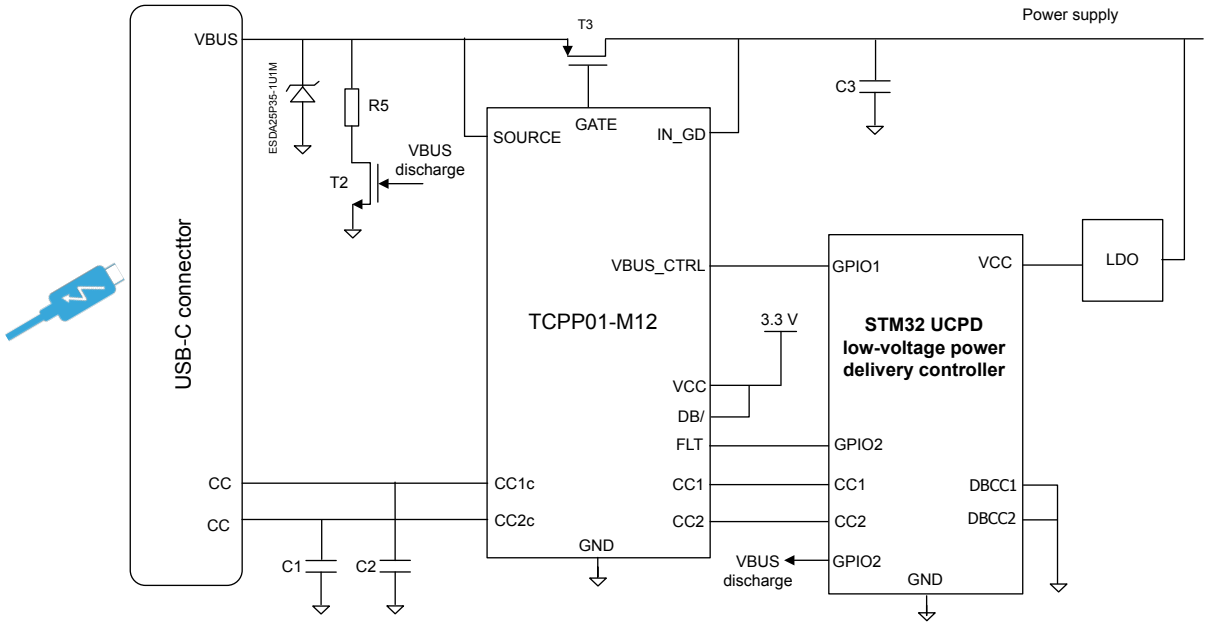
- FLT (FAULT) is an open-drain output pin. Left open if not connected
- When GPIO1 is low, TCPP01-M12 is OFF with ZERO current consumption (see note below)
- When GPIO1 is low, TCPP01-M12 is ON with ADC1 or ADC2 checking the source capability.

Note: In dead battery condition the sequence below applies:

1. TCPP01-M12 dead battery present clamp (1.1 V) on CC1 and CC2 lines)
2. The source detects the clamp presence and applies 5 V on V_{BUS}
3. N-MOSFET T1 is normally ON and power management is supplied with 5 V
4. The MCU wakes-up and applies 3.3 V on GPIO1, and wakes up the TCPP01-M12
5. The TCPP01-M12 removes its clamp on the CC lines so that ADC1 or ADC2 can sense the SOURCE pin capability with the voltage across R5 or R6.

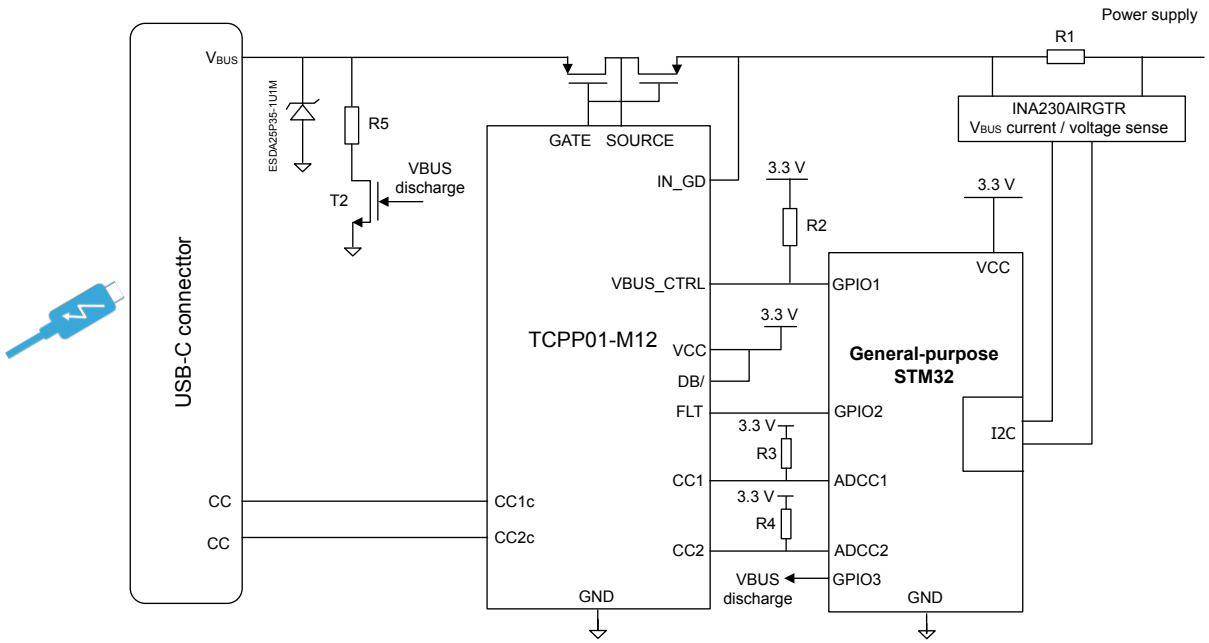
14.3.2 Source modes

Figure 35. Source application with programmable power supply (PD3.0 specification)



- FLT (FAULT) is an open-drain output pin.
- DB/ is a pull-down TCPP input. Connect to 3.3V if not managed by MCU software.

Figure 36. 15 W source applications with STM8/32 general-purpose MCU



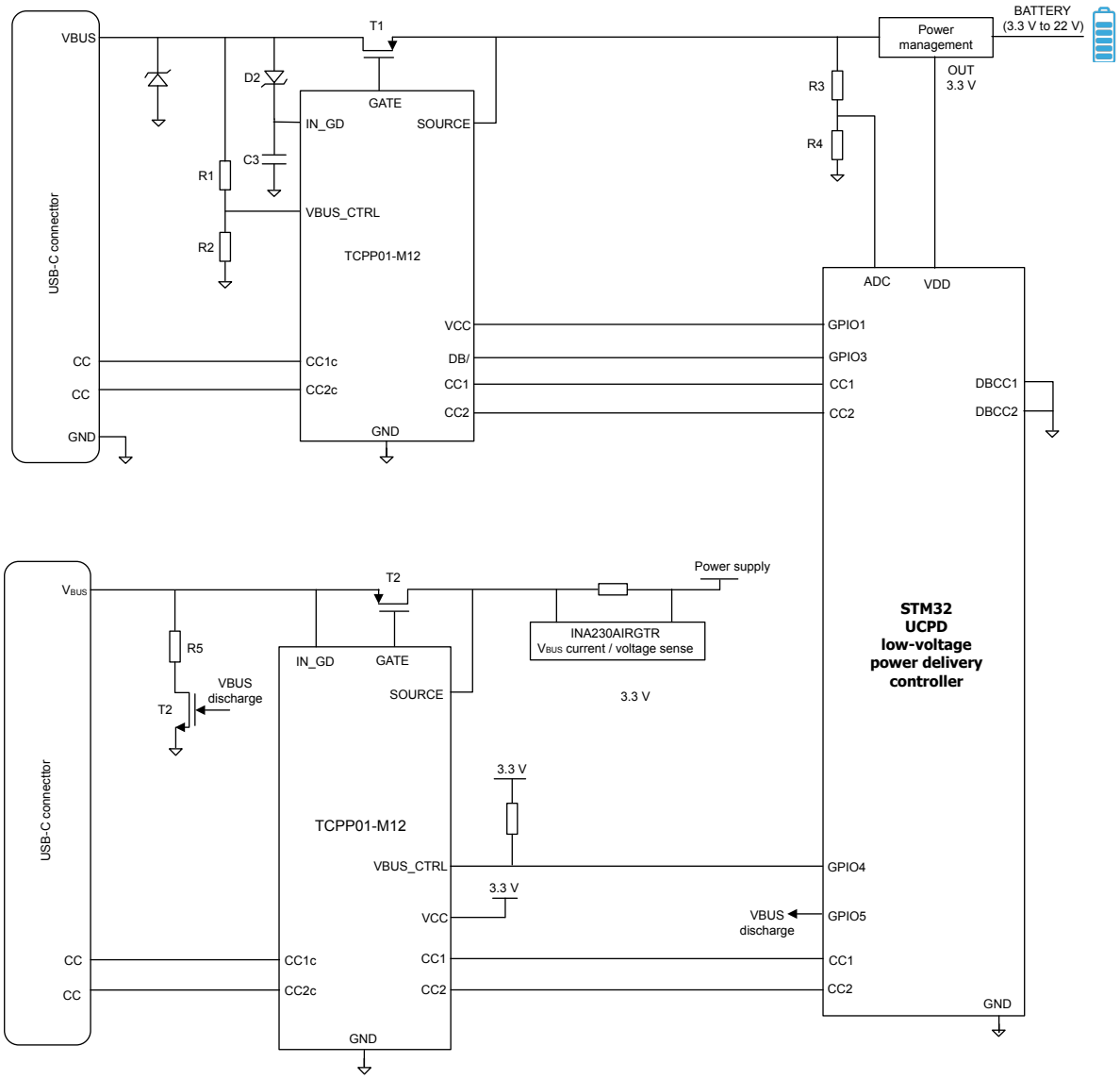
- VBUS_CTRL turns the MOSFET on when needed (the MOSFET is normally-off due to the pull-up resistor)
- Dead battery signals are not present (DB/ at 3.3 V)

Table 12. **R3 and R4 values**

Source profile	R3, R4 value
0.5 A	36 kΩ +/- 20%
1.5 A	12 kΩ +/- 5%
3.0 A	4.7 kΩ +/- 5%

14.3.3 Sink-source solutions

Figure 37. **Sink-source solution**



14.3.4 How to handle dead battery condition with the TCPP01

The DB/ or 'dead battery resistor management' pin is a pulled-down active-low TCPP01 input. The DB/ pin can be used in two ways:

• the DB/ pin is connected to VCC

or

• the DB/ pin is driven by an MCU GPIO

As long as the DB/ pin is low or high-impedance (an internal 5 kΩ pull-down sets the level to ‘0’), the dead-battery resistors are connected and CC switches are opened (OFF state).

When the DB/ pin is tied to VCC, the DB/ resistors are disconnected and CC switches are closed (ON state).

DB/ usage in SNK or Sink mode:

- After system power-up, the DB/ pin must be kept at 0. In this case Rd is enabled at TCPP01 level.
- Once Rd is enabled in the UCPD, the DB/ pin must be set to 1.

For DB/ usage in SRC or Source mode, the DB/ pin must be tied to VCC.

15 Additional information

The USB Power Delivery protocol over CC lines is defined as an extension to both USB2.0 and USB3.1, available only with a Type-C connector

Protocol purpose

The purpose of this protocol is to negotiate the use of a USB type-C cable to deliver power to USB (or other protocol) connected devices

- Maximum power is increased from 2.5/7.5 W on standard/BC environments, to up to 100 W (20 V/5 A)
- The power delivery role (Source or Sink) is dissociated from the upstream/downstream-facing port roles
  - for example, a USB device/hub can deliver power to the USB host
  - during initial connection, the UFP is the Sink and the DFP is the Source
  - Both role pairs (Source/Sink and UFP/DFP) can be swapped on the type-C connector

New Type-C cable additional pins

The new Type-C cable has two additional pins, CC1 and CC2, for configuration control.

Optionally, one of these pins can be configured as a 'VCONN' supply to power an external accessory. In this case, the signalling function of the pin is not available.

Type-C product pull-up/down resistors

A Type-C product must pull the 'CC' line up or down:

- Pull-up 'Rp' for a power source (3 values allow different current draw capabilities)
- Pull-down 'Rd' for a power sink

Note: Note: dual role (source/sink) alternates these roles to achieve connection.

System attach

Once a debounce period has elapsed, the system becomes attached:

- On CC, power delivery messaging can be used for communication over CC lines
  - power capabilities, for example beyond 5 V/3 A
  - power-role swaps
  - data-role swaps (similar to HNP in OTG)
  - VCONN swap
- On VCONN: on seeing an Ra resistor a 5 V supply must be provided

Single Type-C port pins

- Source/sink/DRP cases:
  - Two 'CC' pins (CC1/CC2) allow for unknown orientation of the cable
- Cable and accessory cases:
  - Orientation is pre-determined
  - A single CC pin is needed

Dead battery behavior

Dead battery behavior is basically a pull down/clamp when a Type-C source voltage is applied to CC. It is interpreted as a request to receive V_{BUS}. It thus facilitates the charging of equipment with a dead battery, and also powering one with no battery.

- It *must* be present in most cases
- It *must not* be present in the case of a (pure) Type-C Source, for example a wall charger.

Revision history

Table 13. **Document revision history**

Date	Version	Changes
15-Apr-2019	1	Initial release.

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