Elec 391 Academic Year: 2022-W2

Syllabus Summary

Modules

- Mini-Project
 - Individual Effort
 - Pass / Fail
- System Design
 - Collaborative Effort
 - 2 Sub-Systems / System
- System Integration
 - Team Effort
 - Individual grades adjusted by Duty Roster

Week	Class Time	Deliverable				
1	Intro					
2		Mini-Project				
3	Lectures (Mon / Wed)	Mini-Project				
4		Mini-Project				
5		Mini-Project				
6	ALL TEAMS FORMED					
Spring Break						
7	Tutorial (Monday)					
8	System Demos	Design Document				
9	Tutorial (Monday)					
10	Tutorial (Monday)					
11	Tutorial (Monday)					
12	Final Demos	Slide Deck & Duty Roster				

Grade

Deliveral	ole	Grade			
Mini-Project	(SW)	10%		Individu	al (Pacc / Fail)
Mini-Project	(HW)	10%	Individual (Pass / Fai		ai (Pass / Paii)
)		
Sub-Sys De	esign	30%*	\longrightarrow	Self	Opt-out option
Docume	nt	10%*		Partner	∫ option
Final Demo		35%*	ر Submit c	uty roster	
Slide De	ck	5%*	∫ Grade adjusted		djusted
			}		duty roster djusted

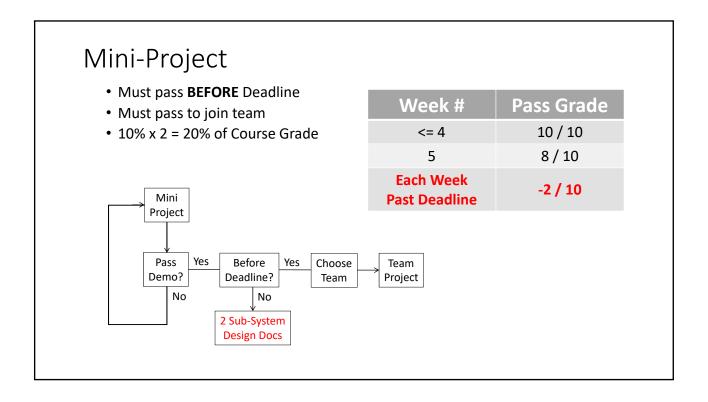
^{*}Marks awarded for **design** work only

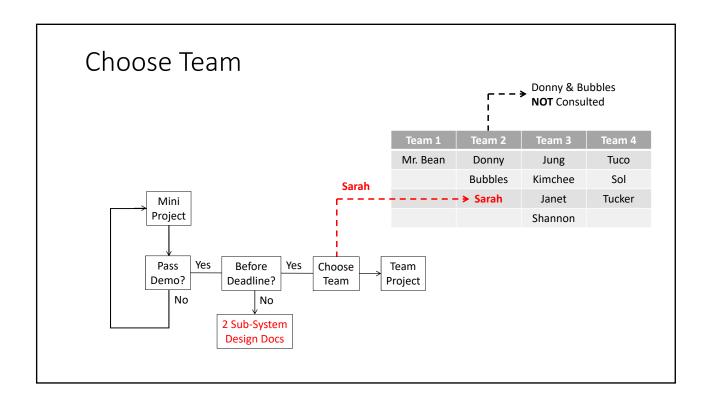
Design Document

- 50%
 - Sub-System Design Document (SSDD)
 - Clear, complete & professional
- 50%
 - 5 **Performance Related** RCGs (10% each)
 - Identify RCG
 - Work Done to Satisfy RCG
 - Measure RCG

Not acceptable:

- Cost
- Effort
- Completion Time
- Subjective Measures





Software System Group

System Identification

- Develop mechanism (SolidWorks)
- Identify mechanical parameters
- Generate linear model (Matlab)
- Generate non-linear model (Simscape)
- Compare step responses
- Add non-linearities

Optimal Control

- Develop System ID stub
- Develop decoder stub
- Identify motor parameters
- Generate linear model (Matlab)
- · Design feedback path
- Design control algorithm & ISR
- Select micro-controller
- Port to C/C++ (API)

Hardware System Group

Digital

- Develop PLD logic (WinCupl)
 - Implement on proto-board
 - · Verify Missed Pulses
 - Verify Counter Overflow
 - Verify Latch & Read Command Sequence
- Develop C logic
 - Subroutine
 - · Returns angle in deg or rad
- Develop Daughter Board (NI)

Analog

- Develop Driver CCT (NI)
 - Implement on Proto-Board
 - Verify Source Spec
 - Verify Output Current / Power
- Develop Linear Model (Matlab)
 - Loaded Step Response
- Develop Daughter Board (NI)
- Develop Mother Board (NI)
 - Verify Connectivity

System & Sub-System Design

Software System Group

- Mech Design & System ID
 - Matlab
 - SolidWorks
 - Simscape
- Controller Design
 - Matlab
 - C/C++ API

Hardware System Group

- Digital Circuit Design
 - WinCUPL
 - C/C++ API
 - NI Suite
- Analog Circuit Design
 - Matlab
 - NI Suite

System Integration

Prototype Demo

- High level RCGs
- System demo
- Extra features
- Design & integration work
- Evidence of iterations
 - · Early versions

Slide Deck

- Photo of prototype
- Supporting evidence to clarify presentation
- DO NOT repeat sub-system design documents
 - Necessary elements only

Resources

- Labs
 - Attend any section
- Maker Space
 - Consult posted schedule for open hours
 - Conduct / Cleanliness
 - Closure
 - Student Volunteer to address issue
- Safety Training
 - Register ASAP
 - Violations
 - Suspension
 - Grade Cap

Rest of term 67 (C+)

- Budget
 - \$800 UBCD
 - Per team (\$200 UBCD / student)
 - PCB
 - Elec components (DigiKey)
 - Mech components (McMaster-Carr)
 - Materials (metals & filaments)
 - \$100 CAD
 - Per student (NOT reimbursed)
 - Micro-Controller
 - · Whatever else you need

