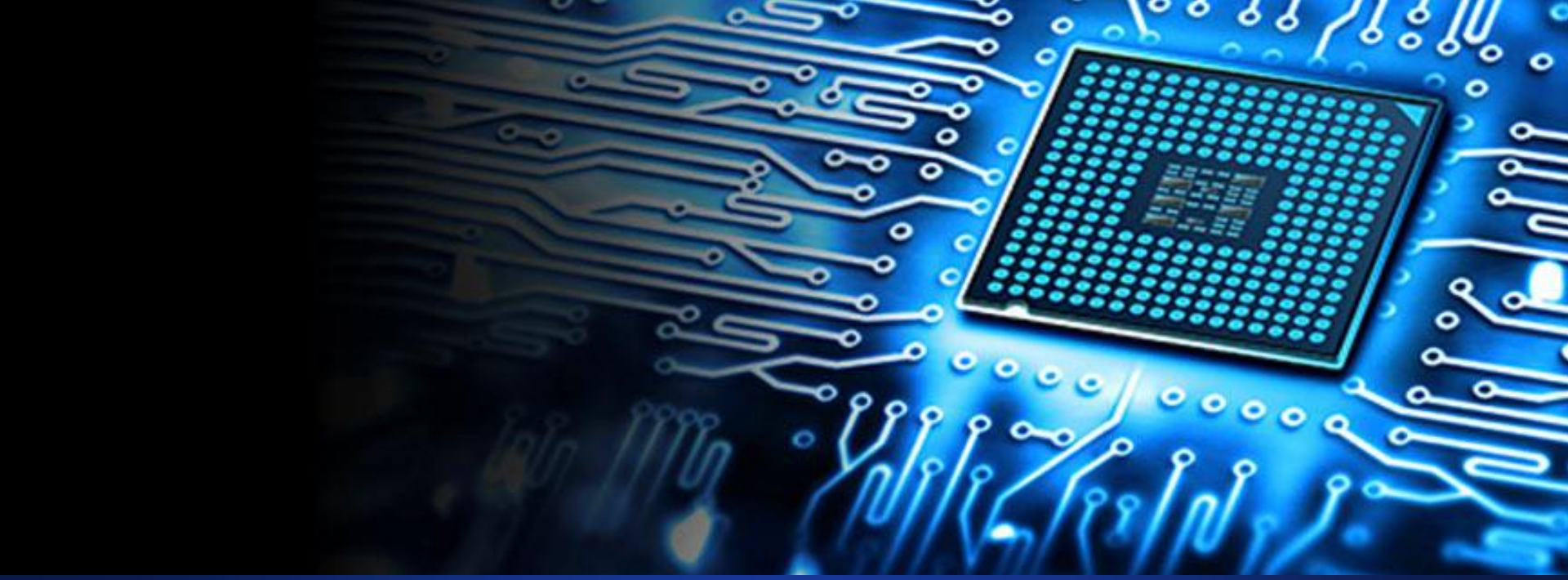
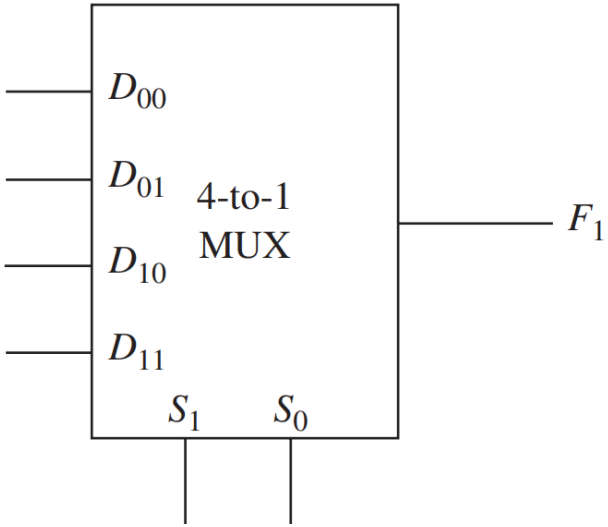


Chapter 3: Exercises

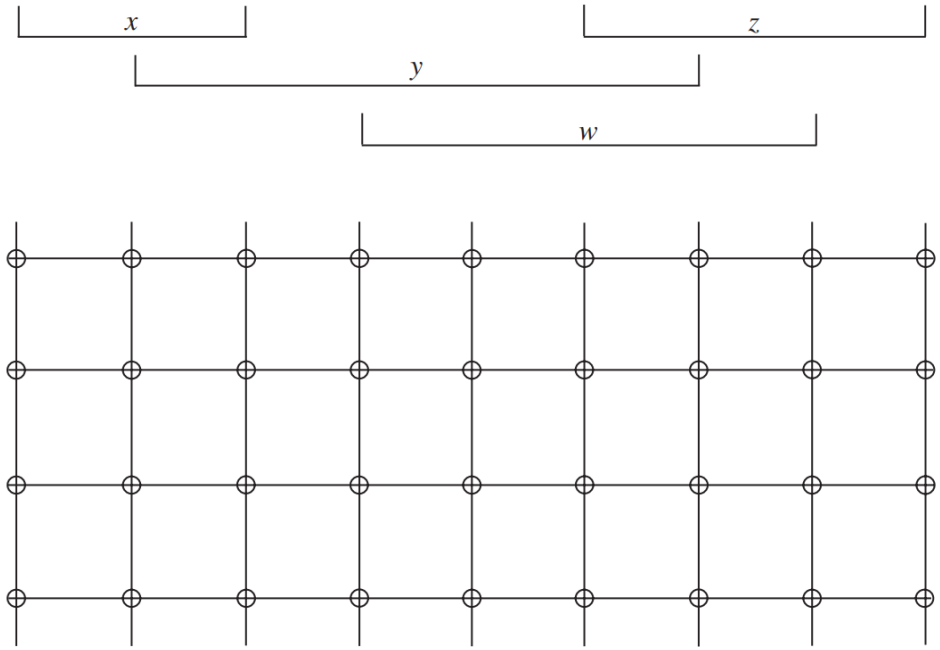
Version: 2024/01/02

1. **(a)** Implement the function $F_1 = A'BC + B'C + AB$ using an FPGA with programmable logic blocks consisting of 4-to-1 multiplexers. Assume inputs and their complements are available.

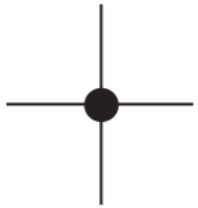


1.**(b)** Implement the function $F_1 = A'B + AB' + AC' + A'C$ using a multiplexer. What is the size of the smallest multiplexer needed, assuming inputs and their complements are available?

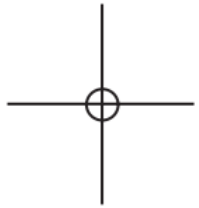
2. **(a)** Route the “w”, “x”, “y”, and “z” nets on the non-segmented tracks shown in the diagram that follows. Use the minimum number of tracks possible.



Nonsegmented tracks

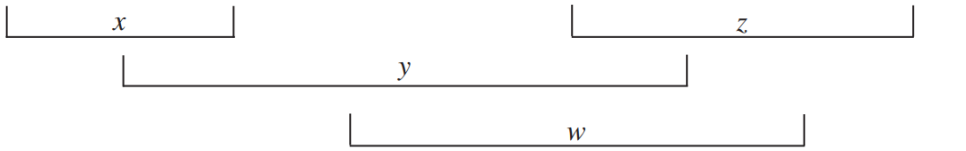


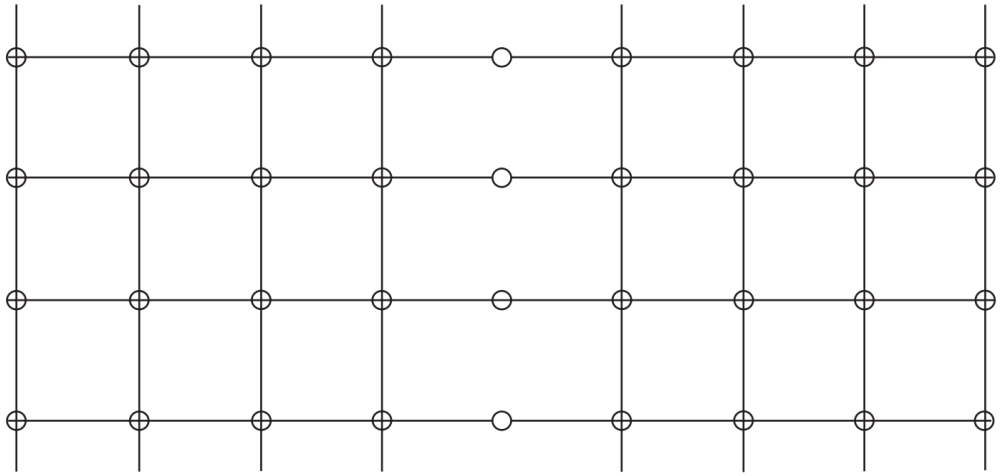
Fused switch



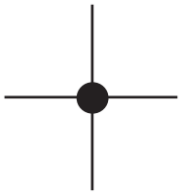
Unfused switch

2. **(b)** Route the “w”, “x”, “y”, and “z” nets on the segmented tracks shown in the diagram that follows. Use the minimum number of tracks possible.

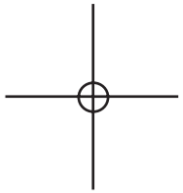




Segmented tracks



Fused switch



Unfused switch

Intersegment switch

3. Consider the following programmable I/O block.

Highlight the connections to configure this I/O block as an INPUT pin. Specify the five configuration bits.