



# Chapter 6: Exercises

Version: 2023/12/20

1. Write a VHDL function for generating an even parity bit for a 16-element `std_logic_vector`. The input is 16-element `std_logic_vector` and the output is a `std_logic` that indicates whether the parity of the input vector is even or not. Parity is even if the vector has an even number of bits that are 1s or in none of its bits are 1s.

2. Write a VHDL procedure that counts the number of ones in an input bit-vector that is  $N$  bit long ( $N \leq 31$ ). The output should be an unsigned vector that is 5 bit long.