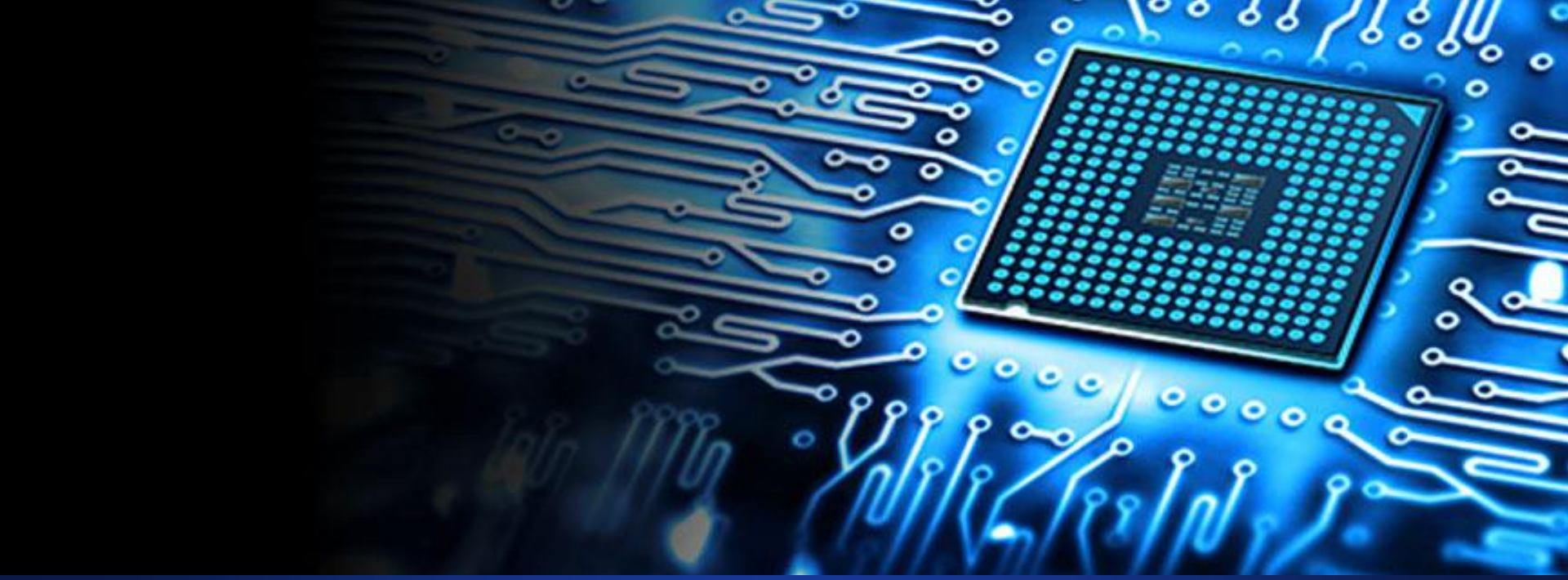

Chapter 2: Exercises

Version: 2024/01/02

1. What do the acronyms VHDL and VHSIC stand for?

2. (a) Which of the following are legal VHDL identifies? **123A, A_123, _A123, A123_, c1__c2, and, and1**

(b) Which of the following identifiers are equivalent? **aBC, ABC, Abc, abc**

3. (a) A full subtracter computes the difference of three inputs X, Y, and Bin, where Diff = X - Y - Bin. When X < (Y+Bin), the borrow output Bout is set. Fill in the truth table for the subtracter and derive the sum-of-products equations for Diff and Bout.

(b) Write VHDL code for a full subtractor using logic equations.

(c) Write VHDL code for a 4-bit subtractor using the module defined in (a) as a component.

4. In the following VHDL process A, B, C, and D are all integers that have a value of 0 at time = 10 ns. If E changes from '0' to '1' at time = 20 ns, specify the time(s) at which each signal will change and the value to which it will change. List these changes in chronological order (20, 20+Δ, 20+2Δ, etc.)

```
p1: process
        begin
                wait on E;
                A <= 1 after 5 ns;
                B <= A + 1;
                C <= B after 10 ns;
                wait for 0 ns;
                D <= B after 3 ns;
                A <= A + 5 after 10 ns;
                B <= B + 7;
end process p1;
```

5. An inhibited toggle flip-flop has input I0, T, and Reset and outputs Q and QN. Reset in active high and overrides the action of the other inputs. The flip-flop works as follows. If I0 = '1', the flip-flop changes on the rising edge of T, if I0 = '0' no state change occurs (except on reset). Assume the propagation delay from T to output is 8 ns and from reset to output is 5 ns. Write a complete VHDL description of this flip-flop.