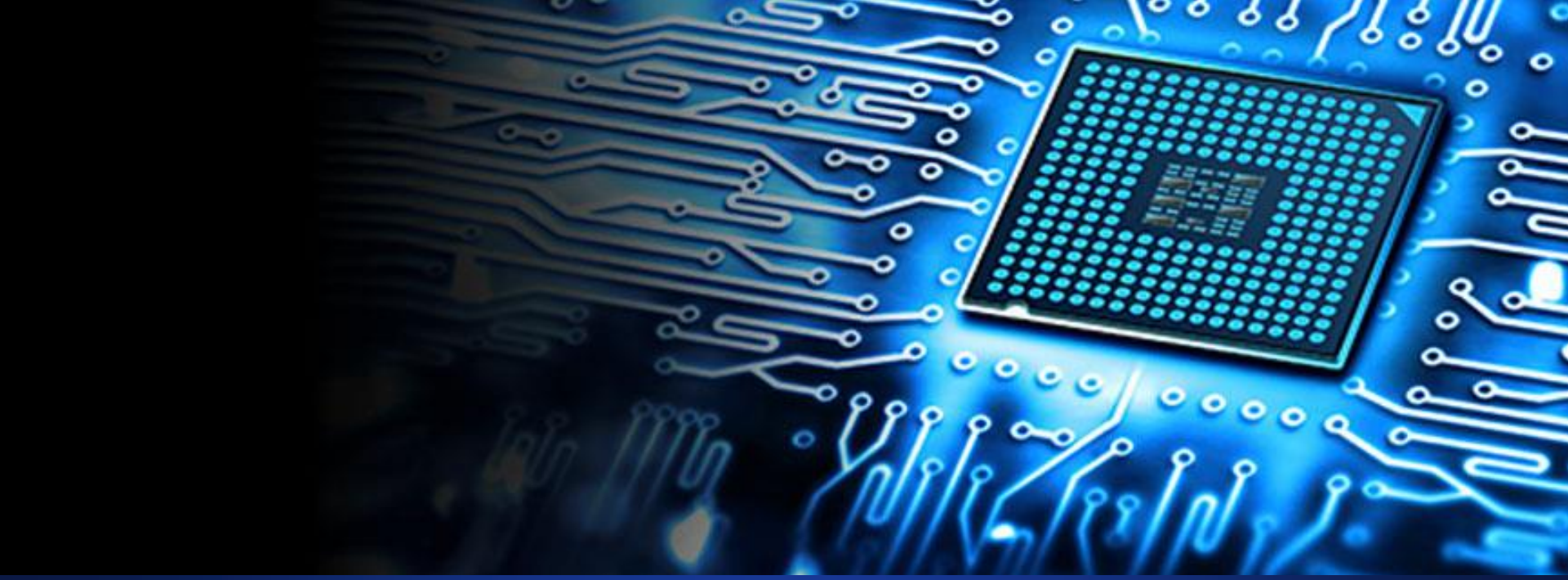
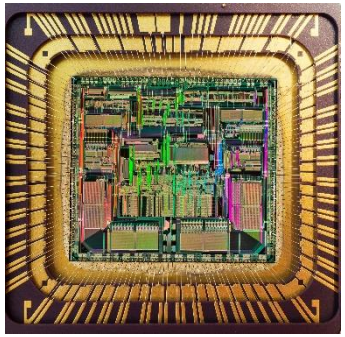


FPGA系统原理与应用

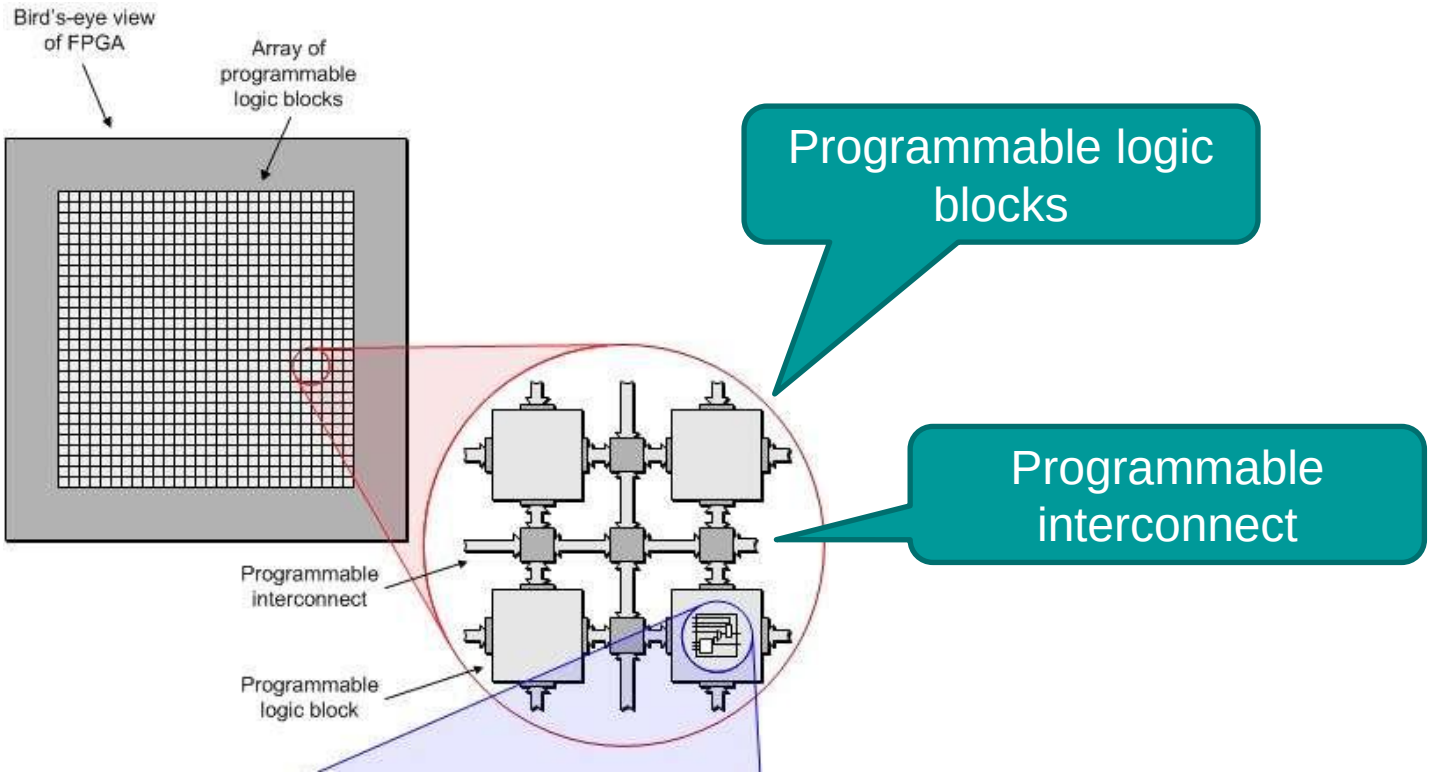
Version: 2023/11/14

Hardware of Microprocessor

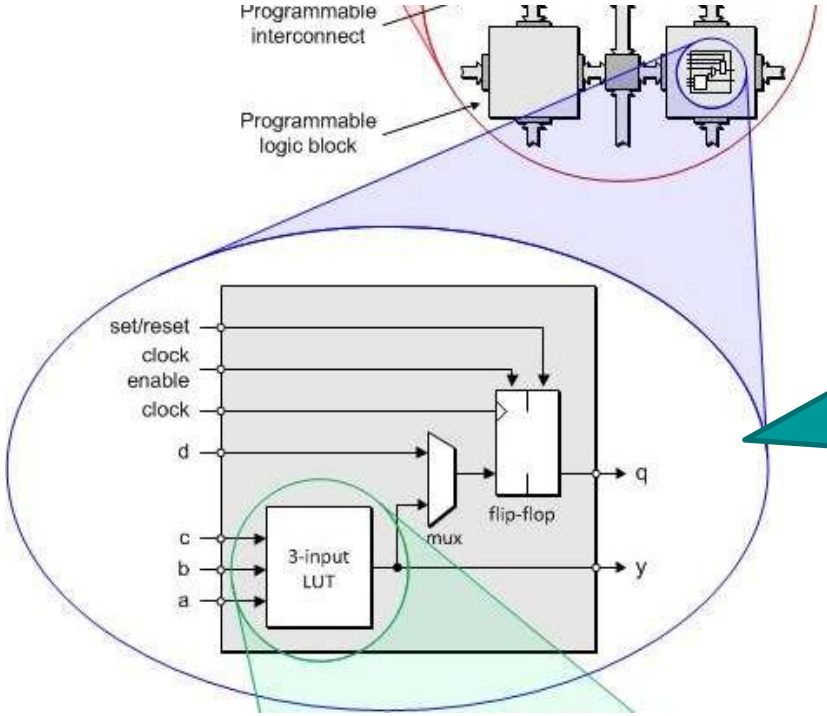


Hardware of FPGA

- FPGA = Field Programmable Gate Array
- 现场可编程门阵列



Hardware of FPGA

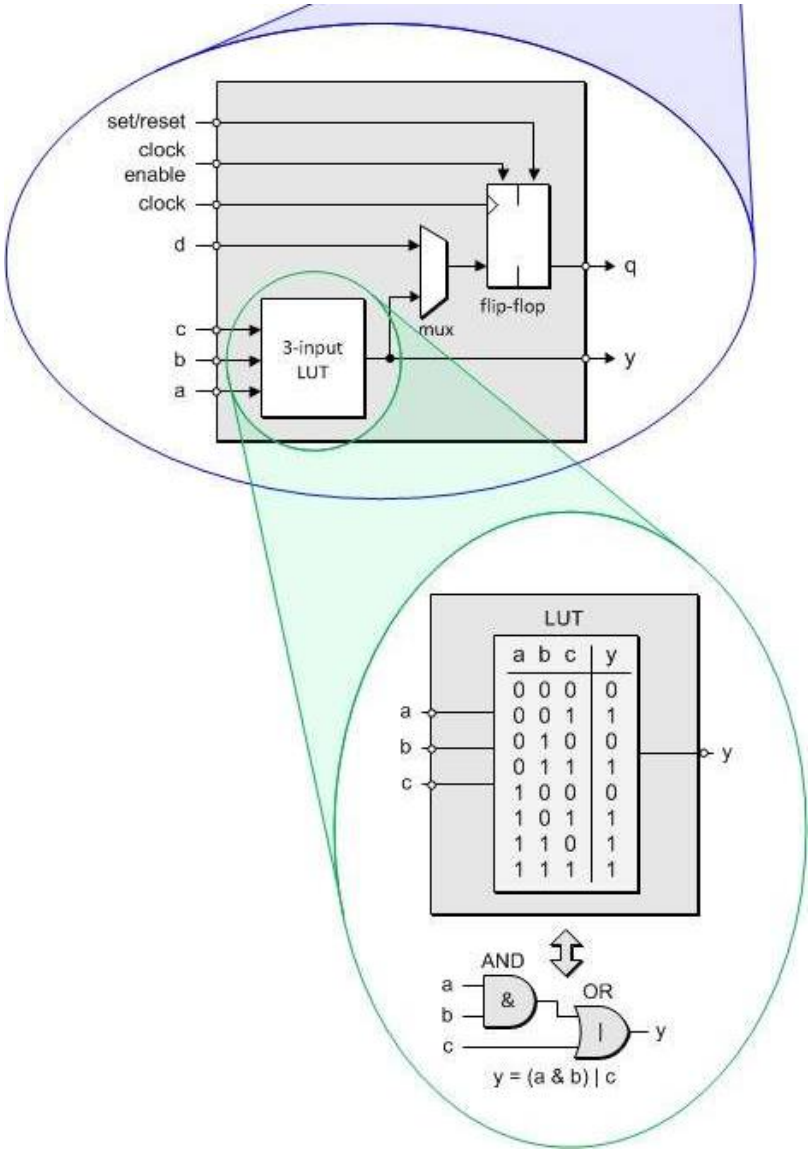


Each programmable block contains several digital functions

- 3-input lookup table (LUT)
- Multiplexer (多路选择器)
- Flip-flop (触发器)

The number and types and sizes of these functions varies from family to family

A Closer look at LUTs



Lecture instructor

- Instructor: **ZHENG Ronghao (郑荣濠)**
  - **Email: rzheng@zju.edu.cn**
  - **Include "FPGA2023" in title, e.g., "FPGA2023_关于状态机"**
  - **Office: Room 218, EE Building**
- Course materials: **course.zju.edu.cn**
  - **Slides notes**
  - **Supplemental materials**

Topics covered

- The fundamentals of logic design
- VHDL description of digital systems
- FPGA design using VHDL

Goals

- **When completing this course**
  - **Understand the basic strategies for digital systems design using VHDL**
  - **Have a firm understanding of FPGA technology and the relevant issues**

Hours allocation and teaching plan

学年: 2023-2024学期: 冬 教学部门: 教师姓名: 郑荣濠

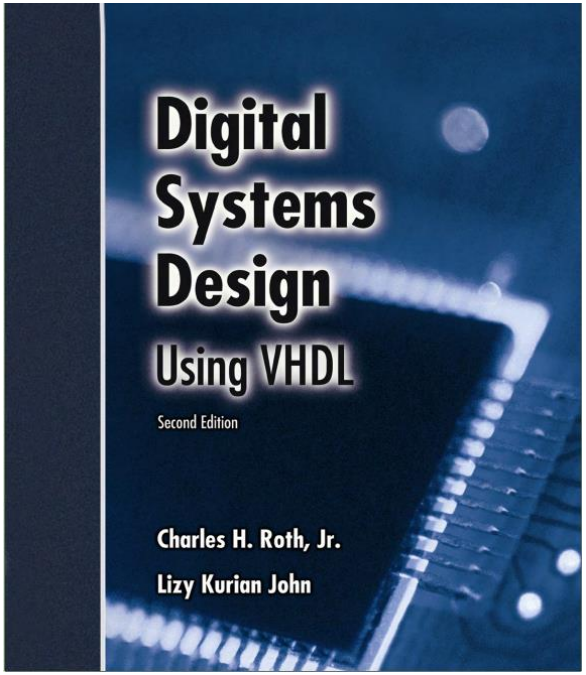
时间	星期一		星期二		星期三		星期四		星期五		
	单	双	单	双	单	双	单	双	单	双	单
早晨											
上午 第一节				08:00~08:45			FPGA系统原理与应用 冬{第1-8周|2节/周} 郑荣濠/张建良 玉泉教7-102(录播.4) [双语]				
第二节				08:50~09:35							
第三节											
第四节											
第五节											
下午 第六节			14:15~15:00								
第七节			15:05~15:50								
第八节			FPGA系统原理与应用 冬{第1-8周|2节/周} 郑荣濠/张建良 玉泉教7-102(录播.4) [双语]								
第九节							FPGA系统原理与应用 冬{第1-8周|2节/周} 郑荣濠/张建良 玉泉第2教学大楼-104 [双语]				
第10节											

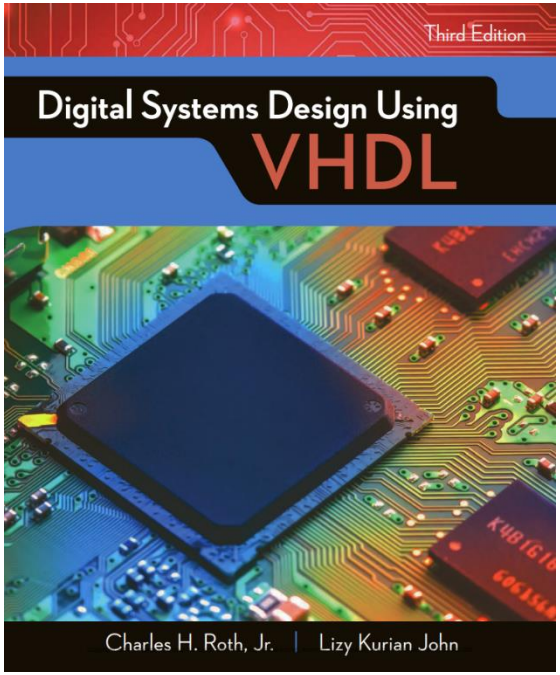
4 lecture hours + 2 lab hours per week

- **Slides presentation together with blackboard**
- **Exercises (not required to hand in)**

Textbook


国外电子与通信教材系列
英文版
GENGAGE Learning
数字系统设计与VHDL
Digital Systems Design with VHDL
[美] Charles H. Roth, Jr. Lizy Kurian John 著
梁松涛 改编

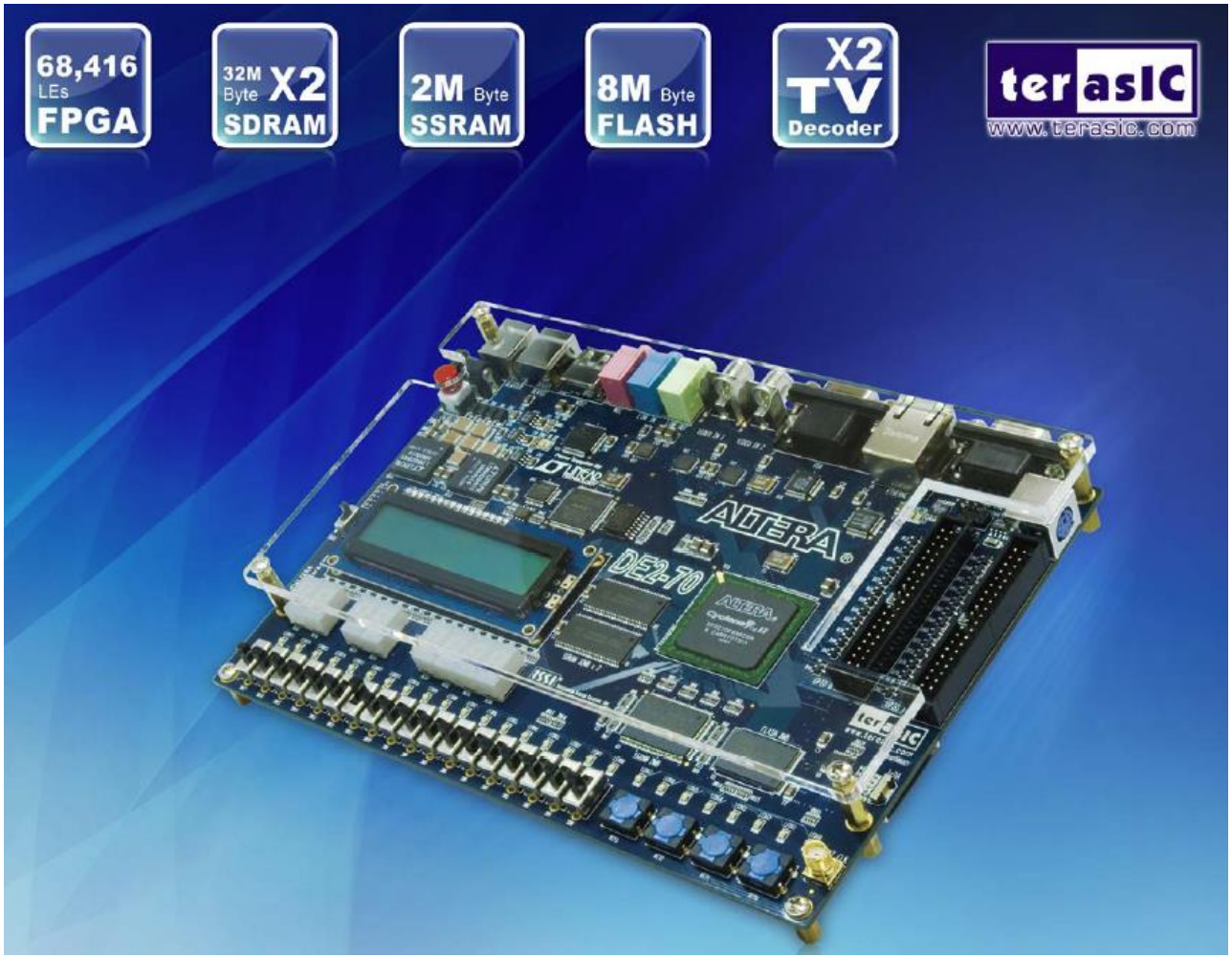

Digital Systems Design Using VHDL
Second Edition
Charles H. Roth, Jr.
Lizy Kurian John


Third Edition
Digital Systems Design Using VHDL
Charles H. Roth, Jr. | Lizy Kurian John

Experimental arrangement

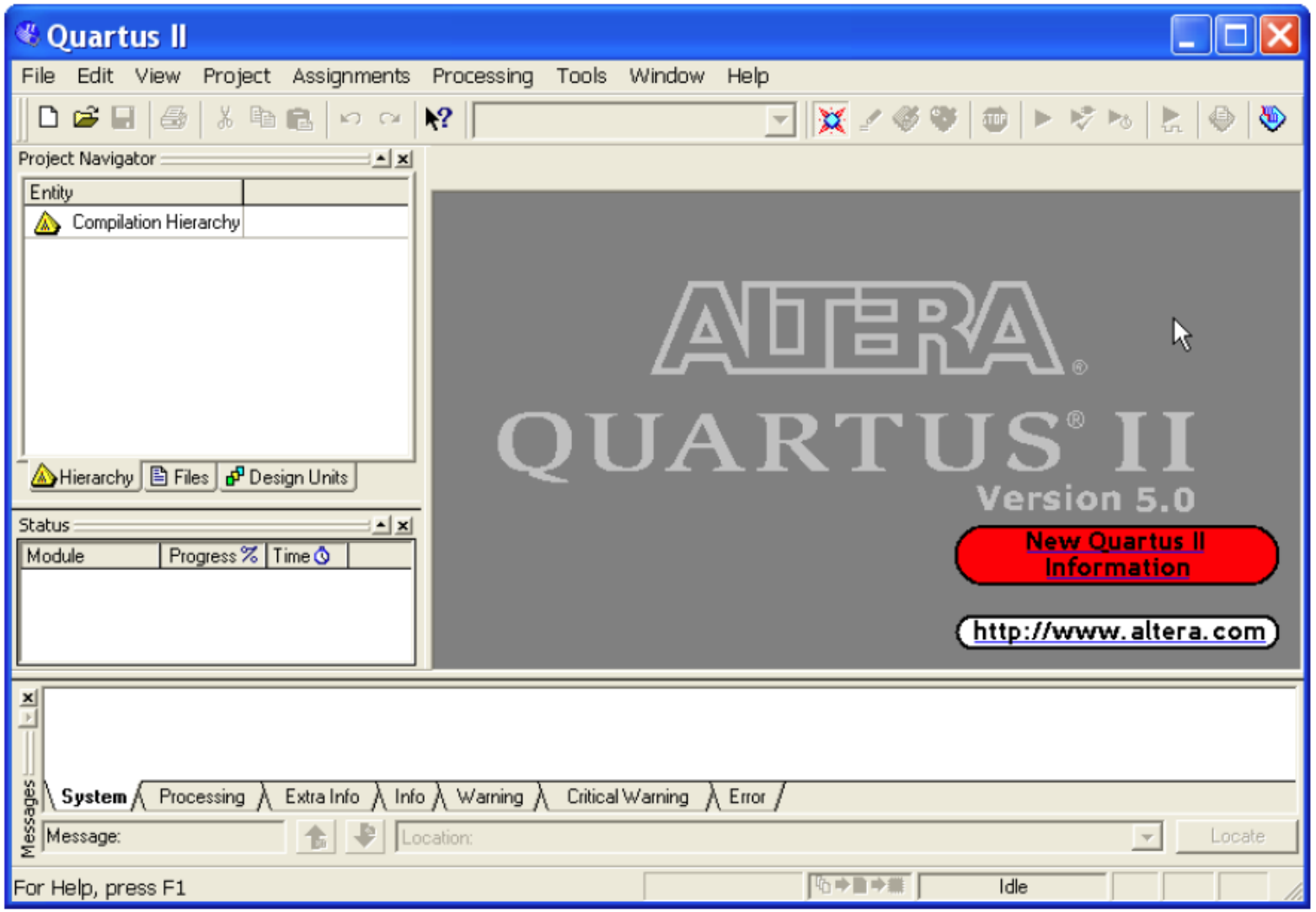
- Instructor: **ZHANG Jianglian（张建良）**
- Teaching Assistant: **ZHANG HANG (张航)**
- **Wednesday afternoon**
- **Lab0：熟悉实验软硬件**
- **每次实验(Lab1~6)之前必须带上纸质实验预习报告（检查但无需上交）**
- **从第二次实验开始，每次实验前上交前一次实验的纸质实验报告**
- **最后一次实验报告在期末考试前上交**

Lab equipment



FPGA实验指导书（pdf）

Quartus


Quartus II
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Compilation Hierarchy
Hierarchy Files Design Units
Status
Module Progress Time
ALTERA
QUARTUS II
Version 5.0
New Quartus II Information
http://www.altera.com
Messages
System Processing Extra Info Info Warning Critical Warning Error
Message:
Location:
Locate
For Help, press F1
Idle

Week	Date	Contents	Lab	Date
Week 1	11/14	Review of Logic Design Fundamentals: I	No Lab	11/16
	11/16	Review of Logic Design Fundamentals: II		
Week 2	11/21	Introduction to VHDL: I	Lab 0: Get Familiar with the Lab Equipment	11/23
	11/23	Introduction to VHDL: II		
Week 3	11/28	Introduction to VHDL: III	Lab 1: Switches, Lights, and Multiplexers	11/30
	11/30	Introduction to VHDL: IV		
Week 4	12/05	Introduction to FPGAs	Lab 2: Counters	12/07
	12/07	Design Examples: I		
Week 5	12/12	Design Examples: II	Lab 3: Numbers and Displays	12/14
	12/14	Design Examples: III		
Week 6	12/19	SM Charts and Microprogramming: I	Lab 4: Finite State Machines	12/21
	12/21	SM Charts and Microprogramming: II		
Week 7	12/26	Additional Topics in VHDL: I	Lab 5: Dice Game	12/28
	12/28	Additional Topics in VHDL: II		
Week 8	01/02	Additional Design Examples: I	Lab 6: Clocks and Timers	01/04
	01/04	Additional Design Examples: II + Review		
Week 10	01/18	Final Examination		

Grading

- Final exam 60%
  - One A4 paper allowed
  - 2023/01/18 14:00~16:00 @ 教7-306
  - 填空，选择，判断，程序设计
  - No Q&A
- Others 40%
  - Lab performance, Lab reports
  - Attendance, Class performance

A few reminders

- Do not late for class
- Avoid no show
- Do not play phone, pad etc. during lecture
- Actively involved, ask your questions