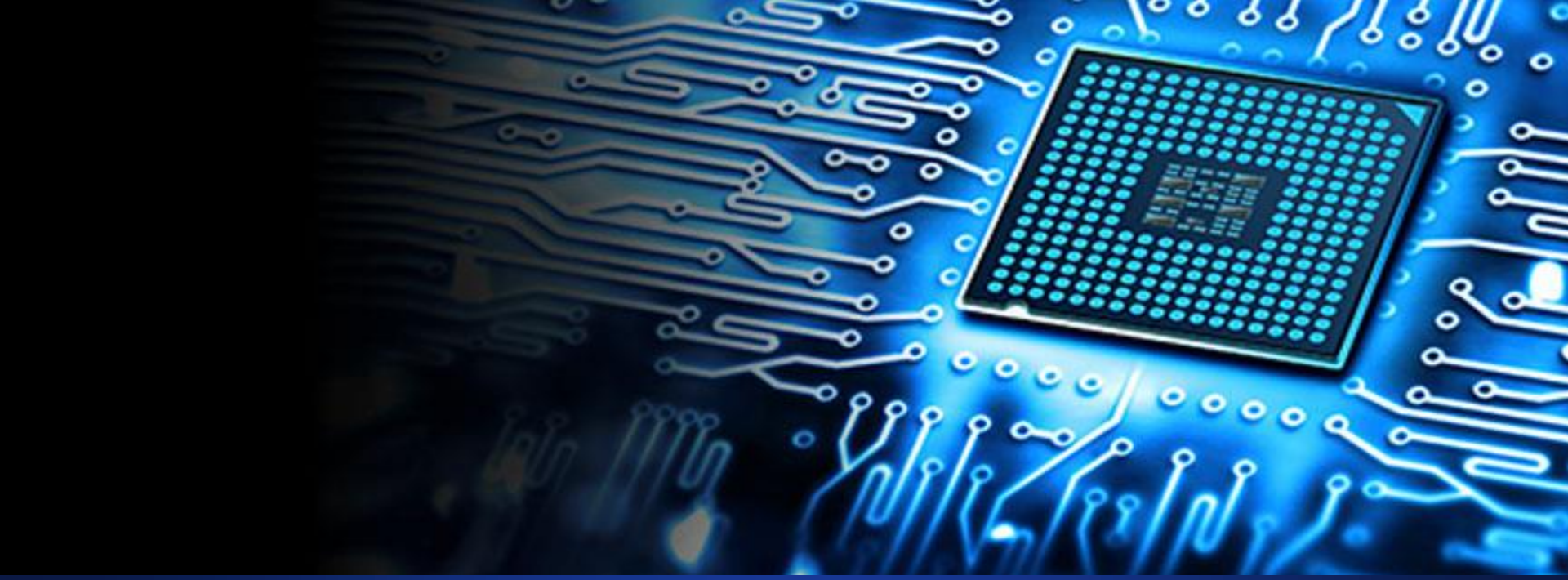
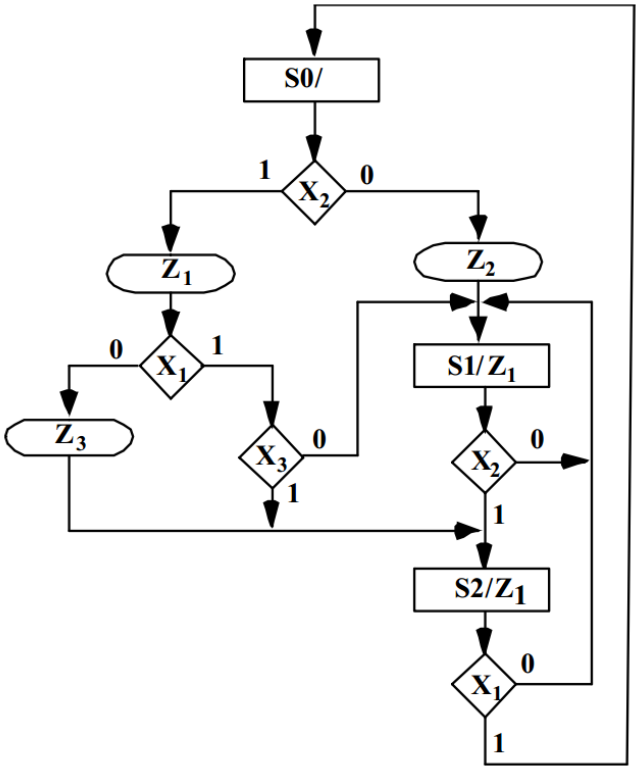


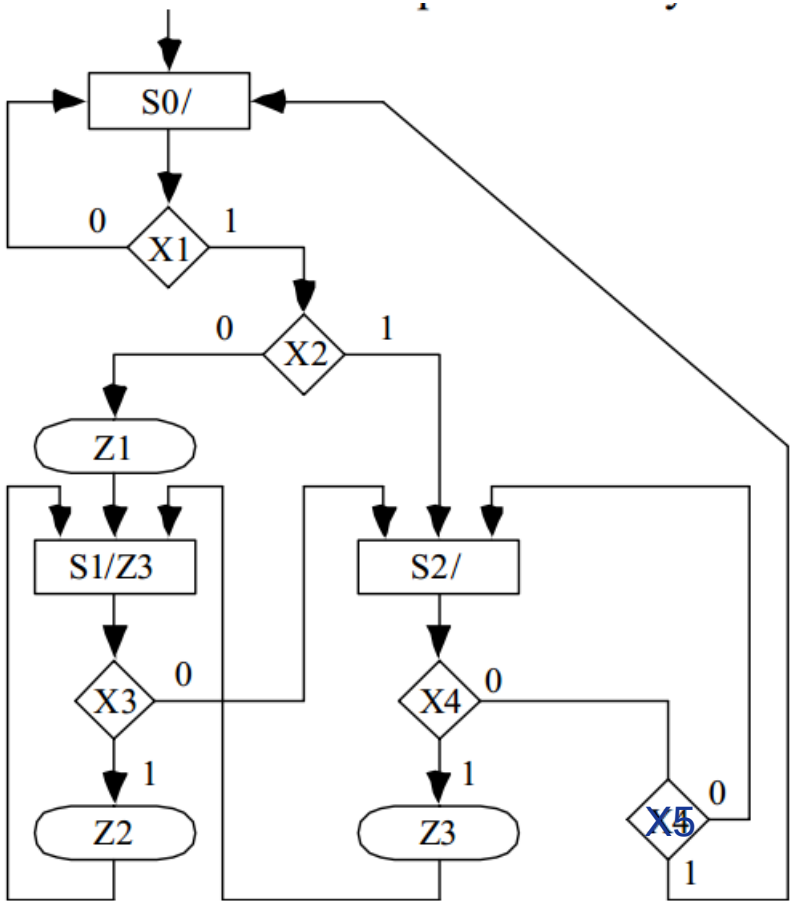
Chapter 5: Exercises

Version: 2023/12/19

1. For the following SM chart: Draw a timing chart that shows the clock, the state (S0, S1, or S2), the inputs (X1, X2 and X3) and the outputs. The input sequence is X1 X2 X3 = 011, 101, 111, 010, 110, 101, 001. Assume that all state changes occur on the rising edge of the clock, and the inputs change on the falling edge of the clock.



2. For the given SM chart: Write a VHDL description of the system.



2. The block diagram for an elevator controller for a building with two floors is shown below. The inputs FB1 and FB2 are floor buttons in the elevator. The inputs CALL1 and CALL2 are call buttons in the hall. The inputs FS1 and FS2 are floor switches that output a 1 when the elevator is at the first or second floor landing. Outputs UP and DOWN control the motor, and the elevator is stopped when UP = DOWN = 0. N1 and N2 are flip-flops that indicate when the elevator is needed on the first or second floor. R1 and R2 are signals that reset these flip-flops. DO = 1 causes the door to open, and DC = 1 indicates that the door is closed. Draw an SM chart for the elevator controller (four states).