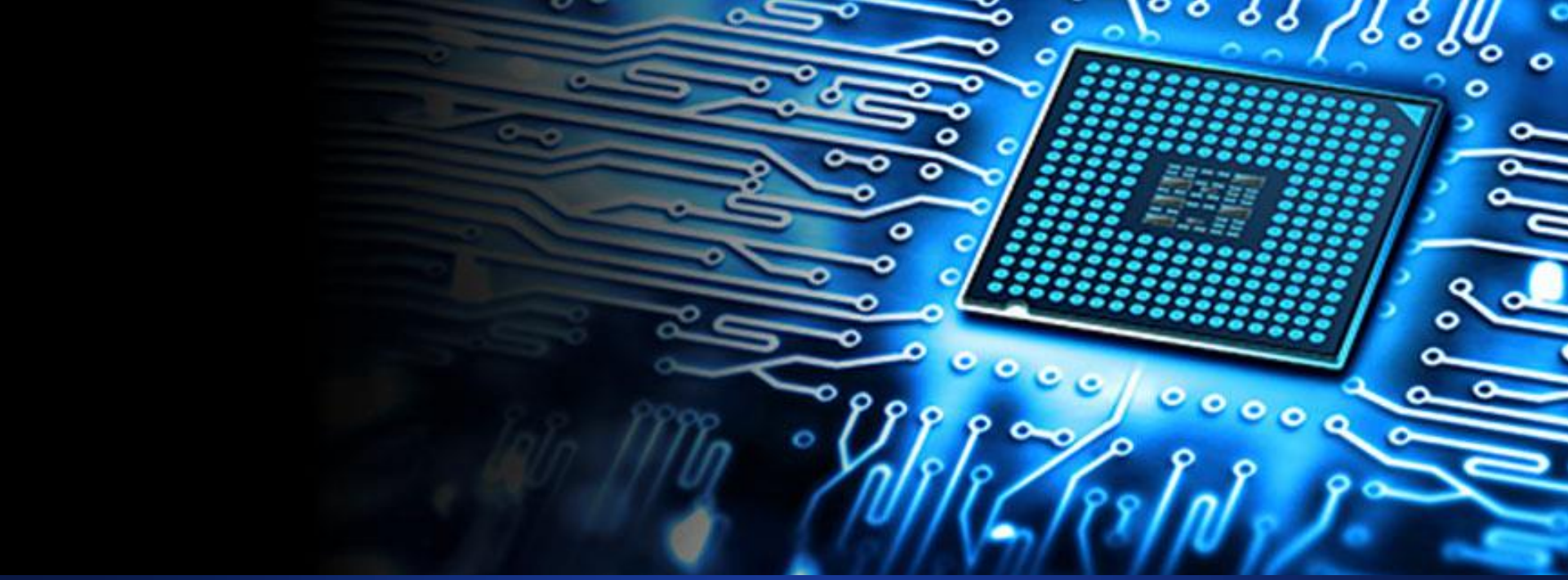
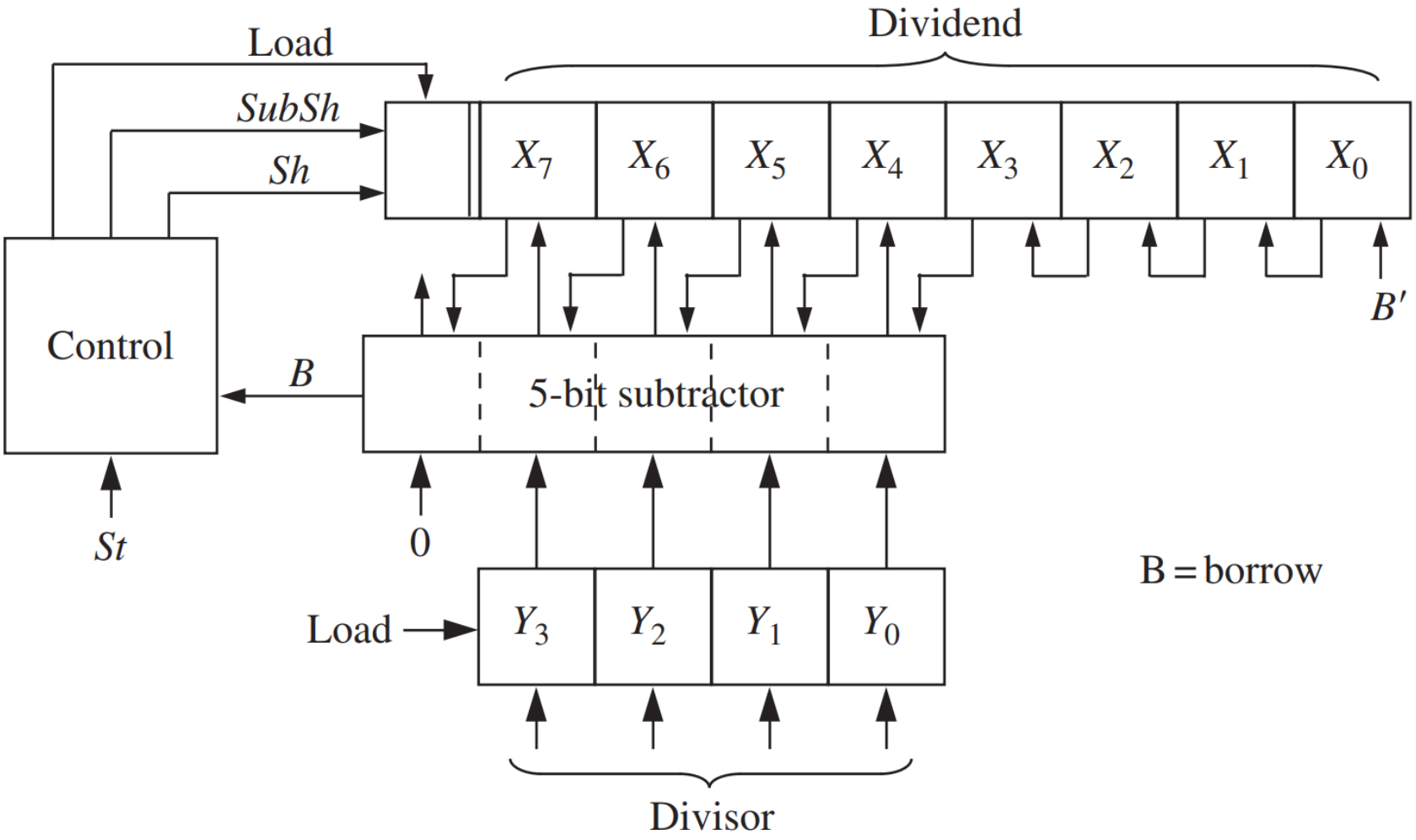


Chapter 4: Exercises

Version: 2023/12/13

1. A block diagram for a divider that divides an 8-bit unsigned number by a 4-bit unsigned number to give a 4-bit quotient is shown subsequently. Note that the X_i inputs to the subtractors are shifted over one position to the left. This means that the shift-and-subtract operation can be completed in one clock time instead of two. Depending on the borrow from the subtractor, a shift or shift-and-subtract operation occurs at each clock time, and the division can always be completed in four clock times after the registers are loaded. Ignore overflow. When the start signal (*St*) is 1, the *X* and *Y* registers are loaded. Assume that the start signal (*St*) is 1 for only one clock time. *Sh* causes *X* to shift left with 0 fill. *SubSh* causes the subtractor output to be loaded into the left part of *X* and at the same time the rest of *X* is shifted left.


Load
Dividend
SubSh
Sh
X_7
X_6
X_5
X_4
X_3
X_2
X_1
X_0
B'
Control
B
5-bit subtractor
St
0
B = borrow
Load
Y_3
Y_2
Y_1
Y_0
Divisor

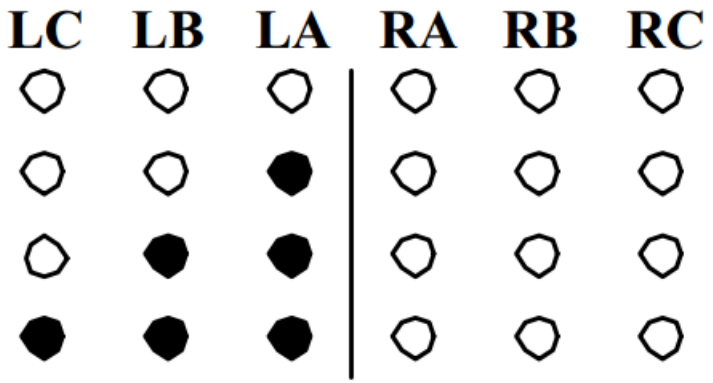
(a) Draw a state graph for the controller (five states).
(b) Complete the VHDL code that follows. Registers and signals should be of type unsigned so that overloaded operators may be used. Write behavioral code that uses a single always block.

```
library IEEE;
use IEEE.numeric_bit.all

entity divu is
    port(dividend: in unsigned(7 downto 0);
         divisor: in unsigned(3 downto 0);
         St, clk: in bit;
         quotient: out unsigned(3 downto 0));
end entity divu;

architecture div of divu is
```

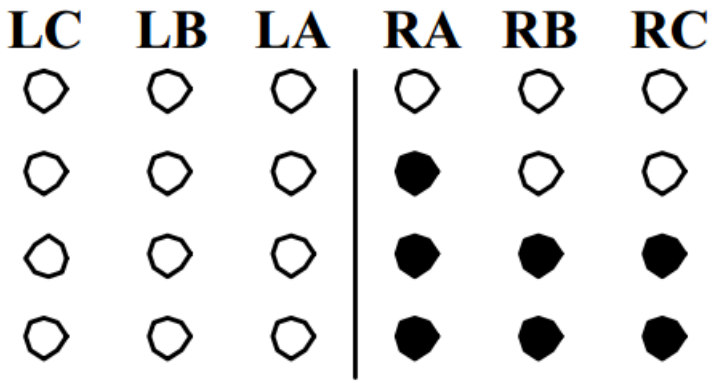
2. An older-model Thunderbird car has three left and three right tail lights, which flash in unique patterns to indicate left and right turns.

Design a Moore sequential network to control these lights. The network has three inputs, LEFT, RIGHT, and HAZ. LEFT and RIGHT come from driver's turn signal switch and cannot be 1 at the same time. When LEFT = 1, the lights flash in a pattern LA on , LA and LB on, LA, LB, and LC on and all off; then the sequence repeats. When RIGHT = 1, the light sequence is similar. IF a switch from LEFT to RIGHT (or vice versa) occurs in the middle of a flashing sequence, the network should immediately go to the IDLE state (lights off) and then start the new sequence. HAZ comes from the hazard switch, and when HAZ = 1, all six lights flash on and off in union. HAZ taks precedence if LEFT or RIGHT is also on. Assume the a clock signal is available with a frequency equal to the desired flashing rate.

Left-turn pattern:



Right-turn pattern:



(a) Draw the state graph (8 states)

(b) Write VHDL code for the controller.