University of Hawai'i Manoa
Instrumentation Development Laboratory

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TARGET5

16-channel, GSPS Transient Waveform Recorder with Self-Triggering and Fast, Selective Window Readout

General Description

The fifth-generation TeV Array with GSa/s sampling and Experimental Trigger (TARGET5) ASIC is a 16-channel transient waveform recorder initially designed to monolithically and inexpensively instrument large deployments of highly pixellated photon detectors for large neutrino and muon detectors. The very general nature of the signal recording, the narrow digitization selection window, and fast signal conversion make it useful in a number of applications. In order to support large arrays, self-triggering capabilities have been incorporated to permit event-of-interest identification as well as data sparsification.

Intended for detectors needing sampling rates of 0.4 - 1 Giga-samples per second (GSPS), triggered readout rates of up to 100kHz are possible, depending upon occupancy, number of bits of resolution and sustainable readout rate of the companion Field Programmable Gate Array. Each of the channels has 32 samples in 8 rows of 512 storage cells, or 16,384 storage samples available.

Features

- → High density (16 channels)
- → Good timing performance
- → 9-10 bits of resolution
- → Fast conversion (<5us/512 samples)
- → Random access to individual samples
- → Flexible operating modes
- → All biases set with internal DACs

Key Specifications

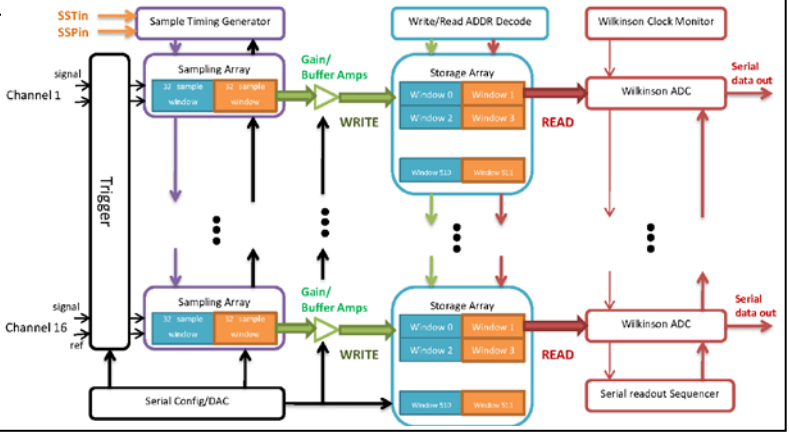
- → Low power (<10mW/channel quiescent)
- → Giga-sample per second recording
- → Selective (windowed) readout
- → 16,384 storage samples/channel

Applications

- ➔ Large scintillator-based muon/neutrino detectors
- ➔ Low-cost, highly integrated systems
- ➔ Collider Detector instrumentation
- ➔ Portable/pocket oscilloscope

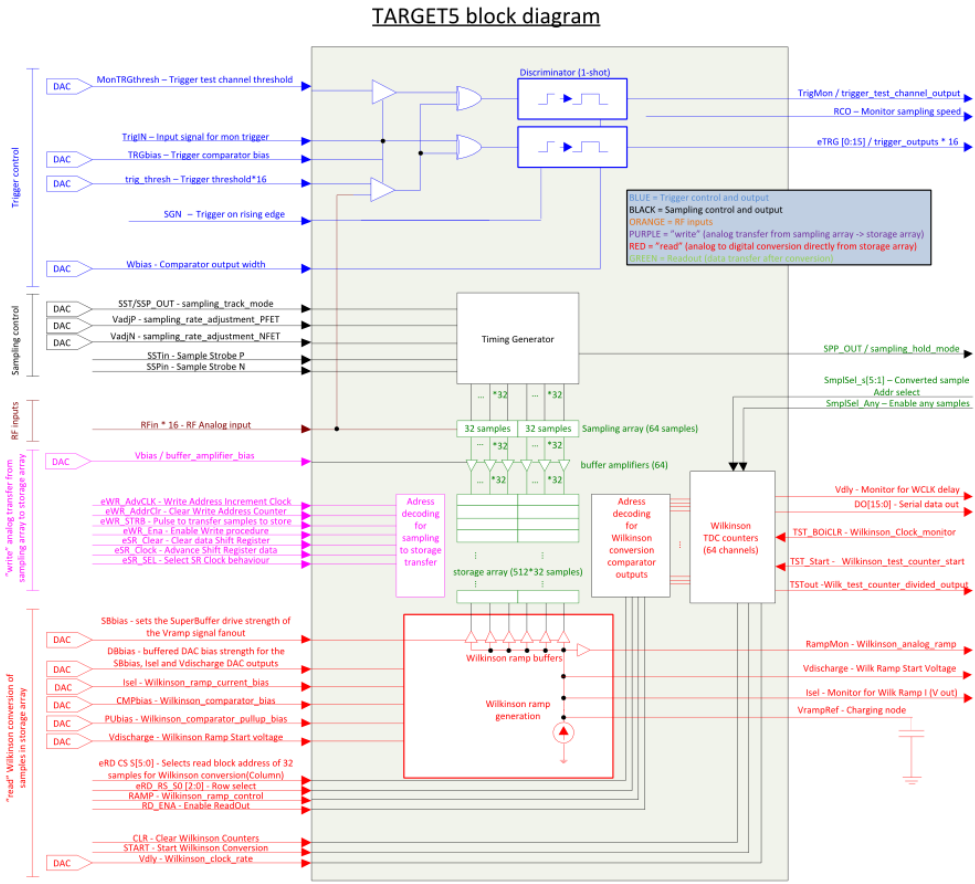
Block Diagram

Overview of the major functional blocks of the TARGET5 ASIC: Triggering, Sampling, Storage and ADC. Configuration of control features and DACs done via a Serial – Parallel interface.



TARGET5 A 16-channel, GSPS, Transient Waveform Recorder with Triggering

Overview Diagram



TARGET5 Overview block diagram, with the various functional components illustrated using different colors. As seen, there are 6 major elements associated with control and operation of the TARGET5 ASIC. In **blue** are controls associated with the trigger functionality of the chip. In order to reduce clutter in this section, details regarding the amplification and gain adjust in the trigger signal pathways are deferred to a more detailed discussion in the Trigger section. In **black** are elements associated with the sampling rate operations. In **magenta** are elements associated with control of stored samples (in **green**) into the larger, randomly-accessible storage array. Writing to and reading from this storage (in **green**) is done in groups of 32 samples on all 16 channels in parallel. In **red** are control signals associated with the read samples select, digitization and readout. Each major functional section is described in detail in separate sections that follow.

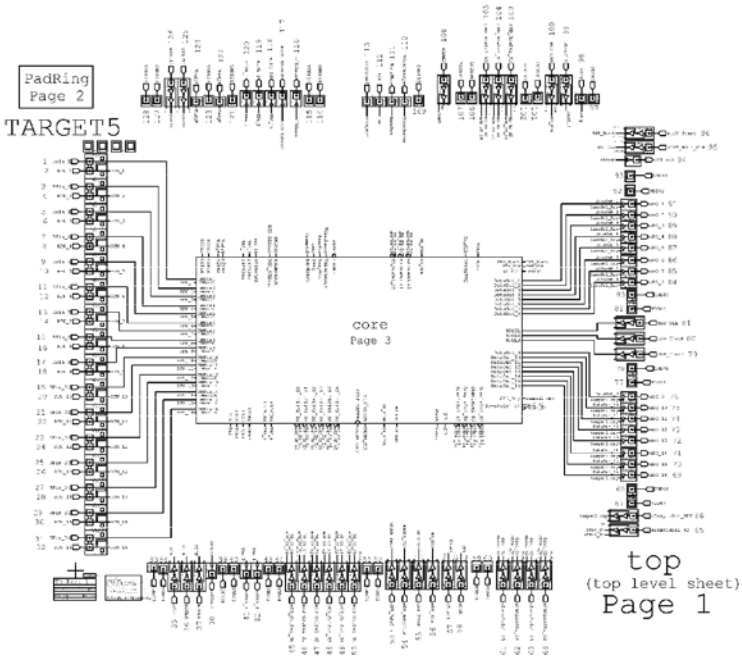
Pin-out Functional Listing

A detailed list of pin numbers corresponding to the symbol on the preceding page. Color coding has been used to clarify signal type and group by functionality. Additional comments are provided to indicate relationships, function, or suggested interconnect values. All purple signals correspond to analog signals and set via internal DAC and are primarily for monitoring, except for VrampRef (external capacitor).

TARGET5 ASIC pinout 30-Jan-13 GSV

Pin #	Pin Name	Connection type	Comments
1	RFin_1	PMT input Ch. 1	termination R
2	RFN_1	Termination ref input Ch. 1	external, between pins
3	RFin_2	PMT input Ch. 2	termination R
4	RFN_2	Termination ref input Ch. 2	external, between pins
5	RFin_3	PMT input Ch. 3	termination R
6	RFN_3	Termination ref input Ch. 3	external, between pins
7	RFin_4	PMT input Ch. 4	termination R
8	RFN_4	Termination ref input Ch. 4	external, between pins
9	RFin_5	PMT input Ch. 5	termination R
10	RFN_5	Termination ref input Ch. 5	external, between pins
11	RFin_6	PMT input Ch. 6	termination R
12	RFN_6	Termination ref input Ch. 6	external, between pins
13	RFin_7	PMT input Ch. 7	termination R
14	RFN_7	Termination ref input Ch. 7	external, between pins
15	RFin_8	PMT input Ch. 8	termination R
16	RFN_8	Termination ref input Ch. 8	external, between pins
17	RFin_9	PMT input Ch. 9	termination R
18	RFN_9	Termination ref input Ch. 9	external, between pins
19	RFin_10	PMT input Ch. 10	termination R
20	RFN_10	Termination ref input Ch. 10	external, between pins
21	RFin_11	PMT input Ch. 11	termination R
22	RFN_11	Termination ref input Ch. 11	external, between pins
23	RFin_12	PMT input Ch. 12	termination R
24	RFN_12	Termination ref input Ch. 12	external, between pins
25	RFin_13	PMT input Ch. 13	termination R
26	RFN_13	Termination ref input Ch. 13	external, between pins
27	RFin_14	PMT input Ch. 14	termination R
28	RFN_14	Termination ref input Ch. 14	external, between pins
29	RFin_15	PMT input Ch. 15	termination R
30	RFN_15	Termination ref input Ch. 15	external, between pins
31	RFin_16	PMT input Ch. 16	termination R
32	RFN_16	Termination ref input Ch. 16	external, between pins
33	GND33	0V power (GND = VSS)	
34	VDD34	2.5V power (VDD)	
35	eSin	Serial input data	all bits, last = first
36	eSCLK	Serial clock advance	shift in each bit
37	ePCLK	Parallel clock load	transfer shifted data
38	eSHout	Serial Shift Out	monitor output
39	GND39	0V power (GND = VSS)	
40	VDD40	2.5V power (VDD)	
41	eTRG_3	Trigger output #3	Ch. 9-12
42	eTRG_4	Trigger output #4	Ch. 13-16
43	GND43	0V power (GND = VSS)	
44	VDD44	2.5V power (VDD)	
45	eRD_CS_S0	Read Column Select Addr. 0	Selects Read
46	eRD_CS_S1	Read Column Select Addr. 1	Block
47	eRD_CS_S2	Read Column Select Addr. 2	of 32
48	eRD_CS_S3	Read Column Select Addr. 3	samples
49	eRD_CS_S4	Read Column Select Addr. 4	for Wilkinson
50	eRD_CS_S5	Read Column Select Addr. 5	Conversion
51	GND51	0V power (GND = VSS)	
52	VDD52	2.5V power (VDD)	
53	eWR_AdvClk	Write Address Increment Clock	Counter to select
54	eWR_AddrClr	Clear Write Address Counter	group of 32 to write
55	eWR_STRB	Pulse to transfer samples to store	H=track/L=hold
56	eWR_Ena	Enable Write procedure	global
57	eStart	Start Wilkinson Conversion	16 Ch. X 32 samples
58	eCLR	Clear Wilkinson Counters	prior new event
59	GND59	0V power (GND = VSS)	
60	VDD60	2.5V power (VDD)	
61	eSmplSel_S5	Converted sample Addr select #5	Most significant bit
62	eSmplSel_S4	Converted sample Addr select #4	
63	eSmplSel_S3	Converted sample Addr select #3	
64	eSmplSel_S2	Converted sample Addr select #2	
65	eSmplSel_S1	Converted sample Addr select #1	Least signif bit
66	eSmplSl_Any	Enable any samples	off during conv!!
67	VDD67	2.5V power (VDD)	
68	GND68	0V power (GND = VSS)	
69	eDO_16	Serial Data Out Ch. 16	MSB to LSB
70	eDO_15	Serial Data Out Ch. 15	
71	eDO_14	Serial Data Out Ch. 14	MSB to LSB
72	eDO_13	Serial Data Out Ch. 13	
73	eDO_12	Serial Data Out Ch. 12	MSB to LSB
74	eDO_11	Serial Data Out Ch. 11	
75	eDO_10	Serial Data Out Ch. 10	MSB to LSB
76	eDO_9	Serial Data Out Ch. 9	
77	VDD77	2.5V power (VDD)	
78	GND78	0V power (GND = VSS)	
79	eSR_Clear	Clear data Shift Reg	not required
80	eSR_Clock	Advance Shift Register data	or load, depending:
81	eSR_SEL	Select SR_Clock behaviour	L=SR; H=Load
82	VDD82	2.5V power (VDD)	
83	GND83	0V power (GND = VSS)	
84	eDO_8	Serial Data Out Ch. 8	MSB to LSB
85	eDO_7	Serial Data Out Ch. 7	
86	eDO_6	Serial Data Out Ch. 6	MSB to LSB
87	eDO_5	Serial Data Out Ch. 5	
88	eDO_4	Serial Data Out Ch. 4	MSB to LSB
89	eDO_3	Serial Data Out Ch. 3	
90	eDO_2	Serial Data Out Ch. 2	MSB to LSB
91	eDO_1	Serial Data Out Ch. 1	
92	VDD92	2.5V power (VDD)	
93	GND93	0V power (GND = VSS)	
94	eTSTout	Wilkinson clock monitor	WCLK/2^12
95	eTST_BOiCLR	Overloaded Boin and CLR	WCLK monitor
96	eTST_Start	Start Wilkinson clock monitor	
97	VDD97	2.5V power (VDD)	
98	Vdly	Monitor for WCLK delay	set by int. DAC
99	RegCLR	Global Registers Clear	clear all registers
100	eRD_ENA	Enable ReadOut	off = no comp
101	GND101	0V power (GND = VSS)	
102	VDD102	2.5V power (VDD)	
103	eRD_RS_S2	Select Row Read Addr #2	MSB
104	eRD_RS_S1	Select Row Read Addr #1	
105	eRD_RS_S0	Select Row Read Addr #0	LSB
106	GND106	0V power (GND = VSS)	
107	VDD107	2.5V power (VDD)	
108	eRamp	Wilkinson Ramp control	H=Ramp; L=Vdisc
109	GND109	0V power (GND = VSS)	
110	Vdischarge	Wilkinson Ramp Start voltage	set by int. DAC
111	RampMon	Buffered copy of Wilk Ramp	direct observation
112	ISEL	Monitor for Wilk Ramp I (V out)	set by int. DAC
113	VrampRef	Charging node	50-100pF typ
114	GND114	0V power (GND = VSS)	
115	VDD115	2.5V power (VDD)	
116	eTRGmon	Monitor trigger channel output	pulse output
117	eRCO_SSPout	RCO or SSPout for timebase	monitoring
118	eTRG_16	Trigger output -- any channel	Ch. 1-16
119	eTRG_2	Trigger output #2	Ch. 5-8
120	eTRG_1	Trigger output #1	Ch. 1-4
121	GND121	0V power (GND = VSS)	
122	VadjN	Sampling NMOS current Adj	int/ext
123	VDD123	2.5V power (VDD)	
124	VadjP	Sampling PMOS current Adj	int/ext
125	eSSPin	Sample Strobe P	arm -- tracking
126	eSSTin	Sample Strobe T	trigger -- hold
127	GND127	0V power (GND = VSS)	
128	VDD128	2.5V power (VDD)	

Connection Diagram



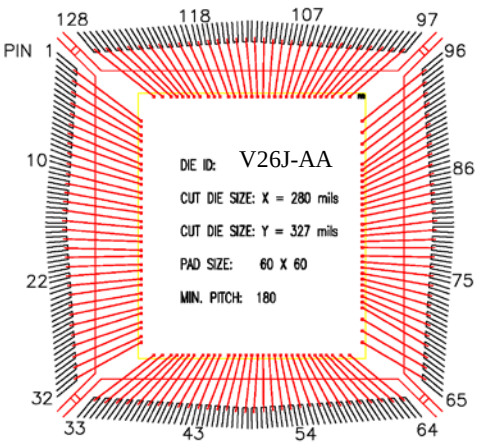
Available Packaging

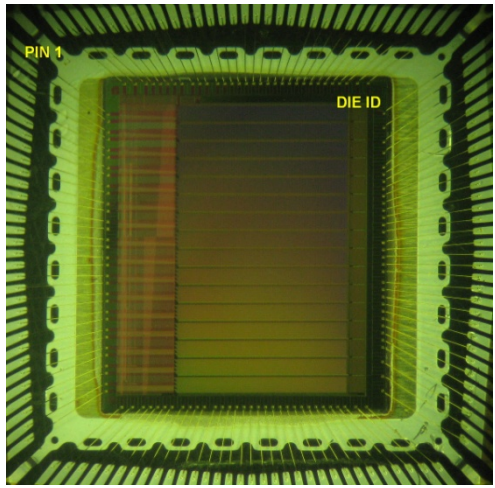
The currently available TARGET5 devices are available in a standard TQFP-128 package.

Die Overview

The TARGET5 die is 6.99mm x 8.16mm.

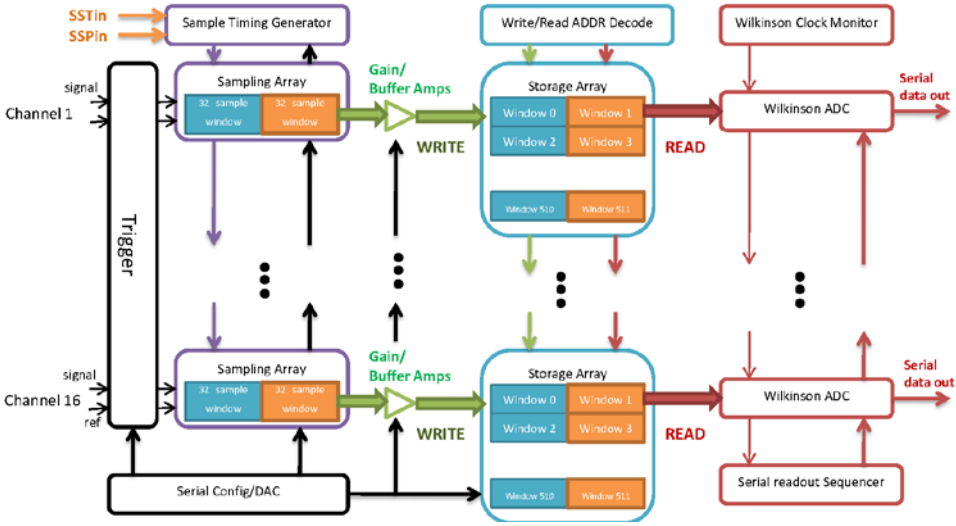
Bonding Diagram





Operational Overview

The figure below outlines the key functional blocks of the TARGET5 ASIC. External to this ASIC it is assumed that any gain required is provided externally. While the input is consistent with a low impedance one, external termination is expected to turn any current output device into an input voltage.



TARGET5 is a 16-channel device where both a signal and its reference signal are input to the ASIC, to provide a modest amount of common-mode noise rejection, as well as reference for the trigger path gain.

Control of the timing samples is provided by a timing generator that is driven by the **SSTin** and **SSPin** signals, as described in detail in the **Sample Timing Generator** section. In order to provide continuous sampling, sampling and transfer to a much larger storage array is performed on groups of 32. When acquisition occurs in one group of 32, the other group of 32 are being buffered by **Buffer Amps** and then written into the **Storage Array**. Independent Write and Read controls permit multi-hit functionality and addressing is described in the **Write/Read ADDR Decode** section.

Utilizing all 512 atomic storage groups of 32 samples, a depth of 16,384 samples is available for either multi-event buffering or up to 16μs of trigger latency. Groups of 32 are randomly accessible for readout. Once selected, the 32 storage cells in all 16 channels are powered up for Wilkinson ADC conversion. The **Wilkinson Ramp Generator** block (not shown) generates and broadcasts a ramp to all channels. At a separately controlled time a counter is started for each channel. In order to reduce power while allowing for a fast clock speed, separate oscillators are provided for each counter. When the voltage ramp crosses the comparator threshold the counter stops and the count then represents the time (ADC code) corresponding to the voltage held in the storage cell. In order to maintain a constant Wilkinson clock rate as a function of temperature, a separate, identical Wilkinson counter is provided inside the **Wilkinson Clock Monitor** block.

Digitized samples are selected (again randomly accessible) and then serial transferred on all 16 channels in parallel. Address decoding and sequencing is performed inside the Serial Readout Sequencer block.

Finally, to simply implementation and external board component requirements, many configuration bits and biases are set via on-chip 12-bit DACs. These are detailed in the **Serial Config/DAC** block.

Absolute Maximum Ratings

Supply Voltage (VDD)	-0.4V to +3.6V
Voltage Input Digital lines	-0.3V to +3.3V
Voltage Input Signal pins[1]	+0.4 to +2.8V
Voltage any output pin	TBD
Input Current (non-power)	TBD
Package Input Current	TBD
Max Junction Temperature	TBD
Thermal Resistance	TBD
Package Dissipation	TBD
+ Many other specs	TBD
Storage temperature[2]	-65C to +150C

Note 1: Minimal input protection diode structure
Note 2: Soldering process must comply with ASAT Technologies Reflow Temperature Profile Specifications

Operating Ratings

Operating Temperature	-0.4V to +3.6V
Supply Voltage	-0.3V to +3.3V
Output Signal Levels	+0.4 to +2.8V
TSA strobe jitter	TBD
RCO Duty Cycle	TBD
Analog Input Pins	TBD
Vped	+0.4V to +2.8V

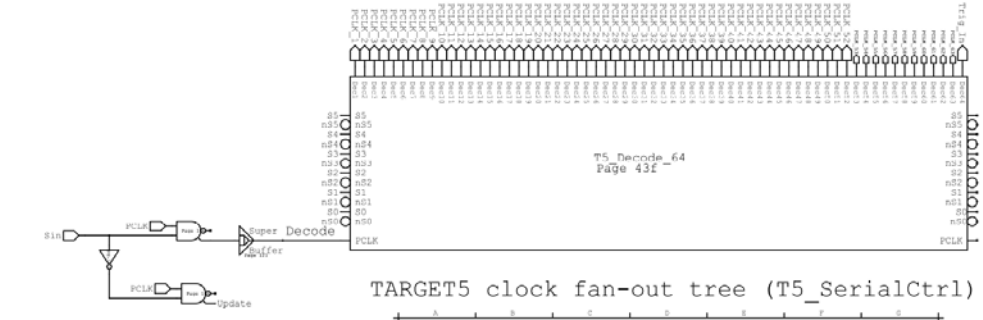
Converter Electrical Characteristics

Stored samples in the TARGET5 are converted into output digital code using a Wilkinson technique, where a ramp converts the analog value into a binary output time. These time intervals, from the beginning of ramp until the count time is latched using a fast ripple counter, is proportional to the stored analog value. By changing the ISEL (ramp rate) and VrampRef (external capacitor), the conversion ramp time slope can be manipulated. Performance and number of bits of resolution depend upon Vramp slope and Wilkinson counter clock rate, which is adjusted by the **Vdly** parameter.

Symbol	Parameter	Conditions	Typ.	Limits	Units
INL	Integral Non-linearity	Full scale input	TBD	TBD	Bits (min)
DNL	Differential Non-linearity	Full scale input	TBD	TBD	Bits (min)
Tacq	Conv. Cycle time	32x in parallel	1	0.5	us
ENC	Equivalent Noise	No signal	TBD	TBD	Bits (min)

Internal Programming

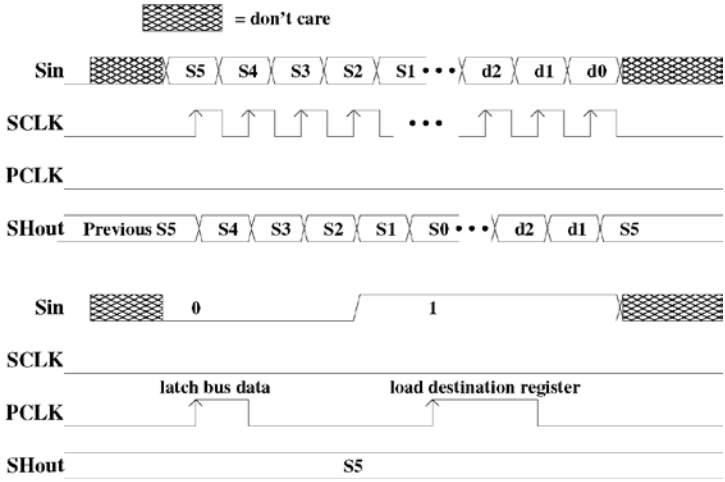
A number of adjustable parameters inside the TARGET5 ASIC can be set via an 18-bit serial shift register. The shift register schematic and decoding circuit for selecting the destination register to program is shown below.



The upper 6 bits of the serial-shifted data correspond to the target address, with the lower 12-bits corresponding to the data word. To avoid changing bus-lines during shift in, or when only want an addressing mode command, the 12-bit data bus is registered. An address map is provided on the next page.

TARGET5 Data Loading

3 phase loading: 1) Serial shift in; 2) latch bus register; 3) decode PCLKn update



Due to their physical co-location, the serial register should be able to operate at >50 MHz. Bus settling time determines minimum programming cycle time – TBD.

Update of the bus register is accomplished when Sin=0 and PCLK is asserted. Transfer of the bus value into the destination register is accomplished for Sin=1 and PCLK

Serial Config/DAC

TARGET5 has 52 configurable registers. As noted in the previous page, these are loaded via a serial data protocol into a shift register via data input pin **SIN** whose data is advanced on the rising edge of the **SCLK** pin. Confirmation of correct loading can be done via the **SHout** pin. Once all values have been serially loaded, the actual control registers are updated using the parallel clock (**PCLK**) signal, as described in the timing diagram of the previous page. A register reset pin (**RegCLR)** is provided though not normally needed. A map of the programming addresses is provided below.

Configuration Register Definition

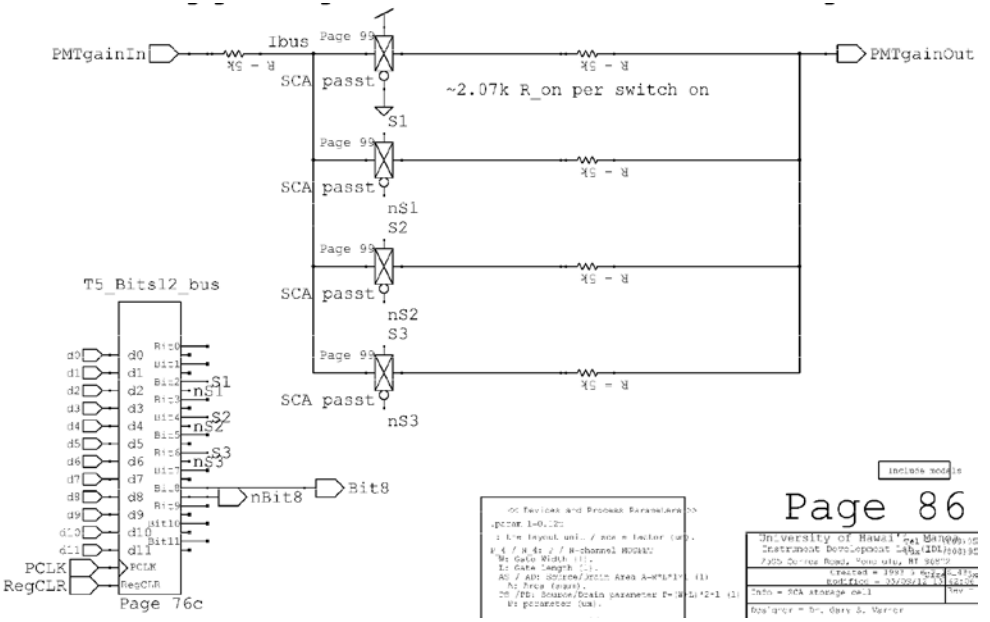
Items associated with Trigger Gain adjustments are in black, bias/adjustment control DACs are in red, Trigger control parameters are in green, and digital register in maroon.

PCLK #	Name	Function	Suggest. Value
1	Ch1_gain	Gain trim Channel 1 [see Gain_adj Table]	1:1
2	Ch2_gain	Gain trim Channel 2 [see Gain_adj Table]	
3	Ch3_gain	Gain trim Channel 3 [see Gain_adj Table]	
4	Ch4_gain	Gain trim Channel 4 [see Gain_adj Table]	
5	Ch5_gain	Gain trim Channel 5 [see Gain_adj Table]	
6	Ch6_gain	Gain trim Channel 6 [see Gain_adj Table]	
7	Ch7_gain	Gain trim Channel 7 [see Gain_adj Table]	
8	Ch8_gain	Gain trim Channel 8 [see Gain_adj Table]	
9	Ch9_gain	Gain trim Channel 9 [see Gain_adj Table]	
10	Ch10_gain	Gain trim Channel 10 [see Gain_adj Table]	
11	Ch11_gain	Gain trim Channel 11 [see Gain_adj Table]	
12	Ch12_gain	Gain trim Channel 12 [see Gain_adj Table]	
13	Ch13_gain	Gain trim Channel 13 [see Gain_adj Table]	
14	Ch14_gain	Gain trim Channel 14 [see Gain_adj Table]	
15	Ch15_gain	Gain trim Channel 15 [see Gain_adj Table]	
16	Ch16_gain	Gain trim Channel 16 [see Gain_adj Table]	
17	ITbias	DAC buffer bias: TRGGbias - Wbias	0.6V
18	TRGGbias	Trigger Input amp bias	0.6V
19	Vbias	Sample -> Storage buffer amp bias	0.6V
20	TRGsumbias	Trigger Sum Amp bias	0.7V
21	TRGbias	Discriminator comparator bias	0.8V
22	Wbias	Discriminator output width adjust	Table XX
23	TTbias[4]	DAC buffer bias: PMTref[4], THResh[4]	0.6V
24	PMTref4[4]	Summing Amp adjustable offset	~Vped
25	THResh[4]	Summed trigger threshold [4]	Threshold
26	TTbias[3]	DAC buffer bias: PMTref[3], THResh[3]	0.6V
27	PMTref4[3]	Summing Amp adjustable offset	~Vped
28	THResh[3]	Summed trigger threshold [3]	Threshold
29	TTbias[2]	DAC buffer bias: PMTref[2], THResh[2]	0.6V
30	PMTref4[2]	Summing Amp adjustable offset	~Vped
31	THResh[2]	Summed trigger threshold [2]	Threshold
32	TTbias[1]	DAC buffer bias: PMTref[1], THResh[1]	0.6V
33	PMTref4[1]	Summing Amp adjustable offset	~Vped
34	THResh[1]	Summed trigger threshold [1]	Threshold
35	TTbias[16]	DAC buffer bias: PMTref[16], THResh[16]	0.6V
36	PMTref4[16]	Summing Amp adjustable offset	~Vped
37	THResh[16]	Summed trigger threshold [16]	Threshold
38	SBbuff	DAC buffer bias: SBbias, MonTRGthresh	0.6V
39	SBbias	Vramp super-buffer bias	0.6V
40	MonTRGthresh	Trigger Monitor channel threshold	Threshold
41	WCbuff	DAC buffer bias: CMPbias, Pubias	0.6V
42	CMPbias	Wilkinson comparator current mirror	see p. XX
43	Pubias	Wilkinson comparator Pull-Up bias	see p. XY
44	DigiReg	SGN, Cload, MUX_SSX, MUX_RCO	Table XY
45	VAbuff	DAC buffer bias: VadjN, VadjP	0.6V
46	VadjN	Timing Adjust Delay N	see p. YY
47	VadjP	Timing Adjust Delay P	see p. YZ
48	DBbias	DAC buffer bias: Isel, Vdischarge	0.6V
49	Isel	Wilkinson ramp programming current	see p. Z1
50	Vdischarge	Wilkinson ramp starting voltage	see p. Z2
51	PRObias	DAC buffer bias: Vdly	0.6V
52	Vdly	Wilkinson counter speed adjust	see p. Z3

Trigger Control…

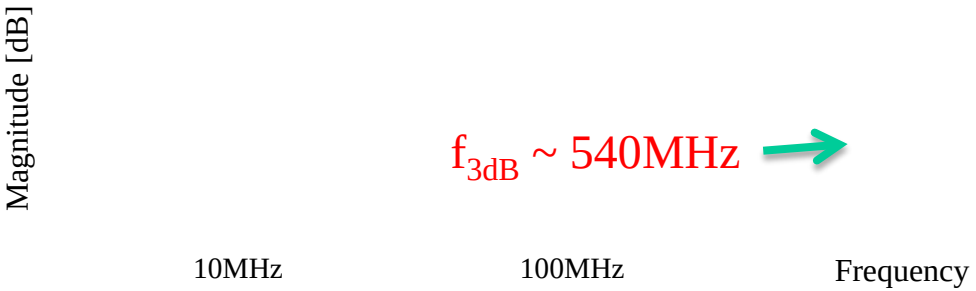
Trigger Gain Path

In order to uniquely determine….



Input Coupling

To permit the highest possible input frequency response that TARGET5 has been designed with a reference signal, tied to an input pedestal voltage (Vped) and used for common mode rejection, to complement the raw input signal. This reference is provided with high ESD protection. The raw high-frequency input is not. Therefore it is highly recommended that a fast, low capacitance RF-rated input protection diode be used on these inputs. The basics of this RF input structure have been evaluated previously and the expected performance is simulated below.



Due to the active elements in the amplification path, the SPICE simulated input frequency is expected to be more like 500MHz for the gain shown on the next page. Unlike TARGET, because the amplifier is on the storage sample output, instead of the input, the gain-bandwidth of the amplifier does not significantly degrade the large amplitude response.

Trigger Functionality

Trigger Encoding

In order to uniquely determine….

Encoding/decoding table for TARGET5 trigger 5-Nov-11 GSV

In general, there should be 3 possible trigger states to decode:

1 trigger bit ON	unique, single hit assignment	25% of time
2 trigger bits ON	use the TRG16 bit to resolve ambiguity	
3 or more bits ON	rare, multi-hit = read everything	

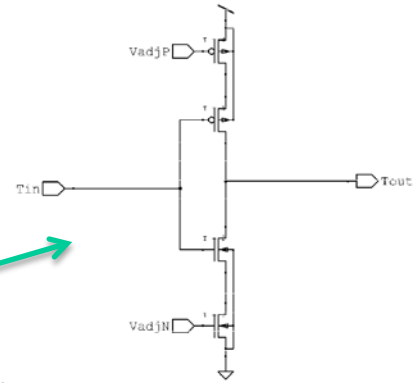
Ch. # hit		G1	G2	G3	G4	S1	S2	S3	S4	TRG1 M1	TRG2 M2	TRG3 M3	TRG4 M4	TRG16		OR6
0	0000	1	0	0	0	1	0	0	0	1	0	0	0	0	unique	
1	0001	1	0	0	0	0	1	0	0	1	1	0	0	0	x	
2	0010	1	0	0	0	0	0	1	0	1	0	1	0	0	x	
3	0011	1	0	0	0	0	0	0	1	1	0	0	1	0	x	
4	0100	0	1	0	0	1	0	0	0	1	1	0	0	1	G2&S1	1
5	0101	0	1	0	0	0	1	0	0	0	1	0	0	0	unique	
6	0110	0	1	0	0	0	0	1	0	0	1	1	0	0	x	
7	0111	0	1	0	0	0	0	0	1	0	1	0	1	0	x	
8	1000	0	0	1	0	1	0	0	0	1	0	1	0	1	G3&S1	1
9	1001	0	0	1	0	0	1	0	0	0	1	1	0	1	G3&S2	1
10	1010	0	0	1	0	0	0	1	0	0	0	1	0	0	unique	
11	1011	0	0	1	0	0	0	0	1	0	0	1	1	0	x	
12	1100	0	0	0	1	1	0	0	0	1	0	0	1	1	G4&S1	1
13	1101	0	0	0	1	0	1	0	0	0	1	0	1	1	G4&S2	1
14	1110	0	0	0	1	0	0	1	0	0	0	1	1	1	G4&S3	1
15	1111	0	0	0	1	0	0	0	1	0	0	0	1	0	unique	

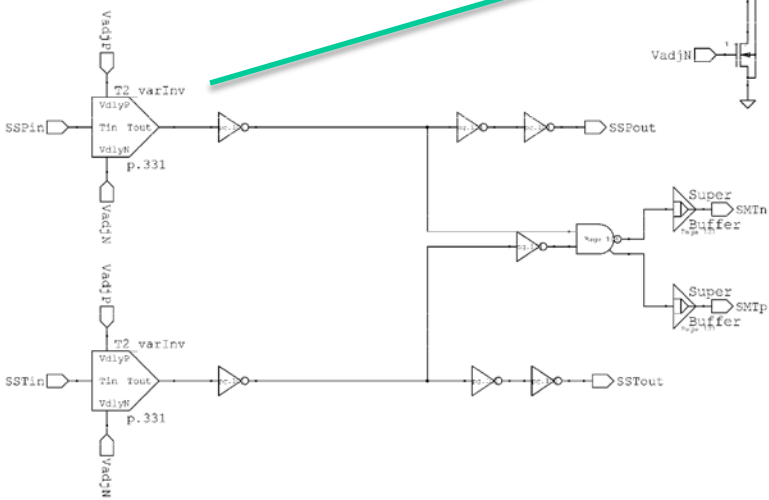
Decoding Table

TRG16	TRG4	TRG3	TRG2	TRG1	status	
0	0	0	0	0	-----	no hits
0	0	0	0	1	Ch. 0	
0	0	0	1	0	Ch. 5	
0	0	0	1	1	Ch. 1	
0	0	1	0	0	Ch. 10	
0	0	1	0	1	Ch. 2	
0	0	1	1	0	Ch. 6	
0	0	1	1	1	all	Ch. 0 - 11
0	1	0	0	0	Ch. 15	
0	1	0	0	1	Ch. 3	
0	1	0	1	0	Ch. 7	
0	1	0	1	1	all	Ch. 0-7; 12-15
0	1	1	0	0	Ch. 11	
0	1	1	0	1	all	Ch. 0-3; 8-15;
0	1	1	1	0	all	Ch. 4 - 15
0	1	1	1	1	all	channels
1	0	0	0	0	invalid	
1	0	0	0	1	invalid	
1	0	0	1	0	invalid	
1	0	0	1	1	Ch. 4	
1	0	1	0	0	invalid	
1	0	1	0	1	Ch. 8	
1	0	1	1	0	Ch. 9	
1	0	1	1	1	all	Ch. 0 - 11
1	1	0	0	0	invalid	
1	1	0	0	1	Ch. 12	
1	1	0	1	0	Ch. 13	
1	1	0	1	1	all	Ch. 0-7; 12-15
1	1	1	0	0	Ch. 14	
1	1	1	0	1	all	Ch. 0-3; 8-15;
1	1	1	1	0	all	Ch. 4 - 15
1	1	1	1	1	all	channels

Sample Timing Generator

The sampling speed of the TARGET5 is controlled by adjusting the **VadjP** and **VadjN** voltage lines. Internally, the base delay element is a current-starved inverter, as indicated at the right. A normal inverter regenerative stage is used in between to restore the voltage value between stages, and super buffers drive the sampling switches.





Schematic of the base timing generator cell. Quiescent, both SSPin and SSTin are low. Sampling begins with SSPin being asserted. Because of the additional inverter, when the output of the delayed copy of SSPin (SSPout) reaches the NAND gate, the switches for this time step close and the SCA goes into tracking mode. At a later time, when SSTin is asserted high, the switches then open and the instantaneous value at the input to the switch is then stored on the sampling capacitors. As long as SSPin is asserted sufficiently far in advance (sampling speed dependent but typically 8ns or more), and stays valid until after SSTin has passed, SSPin itself is not timing critical. Therefore the rising edge of SSTin is the defining timing signal and every effort should be made to maintain its integrity.

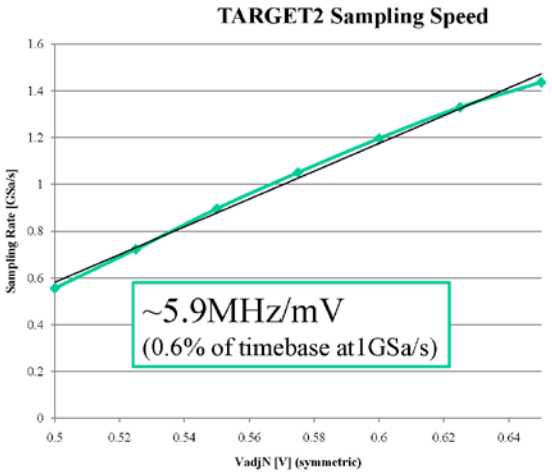
Sampling Speed Stabilization

It is known that the sampling speed of these delay timing generators is temperature dependent, typically with a value determined to be something like 0.2%/degree C. In order to compensate for this effect, there are 2 mechanisms available. A continuous ring oscillator copy of the delay time generator (with one additional inverter and that output fed back to the input is available as the **RCO** signal. The **SSPout** for the last stage of the delay chain is also made available for monitoring and feedback. A number of means can be employed to determine and lock the net delay and they will be updated as testing proceeds.

Sampling Speed Adjustment

As seen at the left, by adjusting the VadjN signal we are able to easily cover 0.5-1.5 GSa/s sampling in SPICE simulation. Very conservative values were used for the parasitic capacitances of the timing generator structure and 20% faster operation has been seen in similar ASICs using essentially the same delay generator circuitry, which indicates operation to just over 2 GSa/s may be possible. Multiple methods are available for locking this sampling frequency, as discussed on the preceding page. Sensitivity for a target operating point of 1 GSa/s is presented in the figure below.

Example tuning sensitivity for maintaining stable timebase.

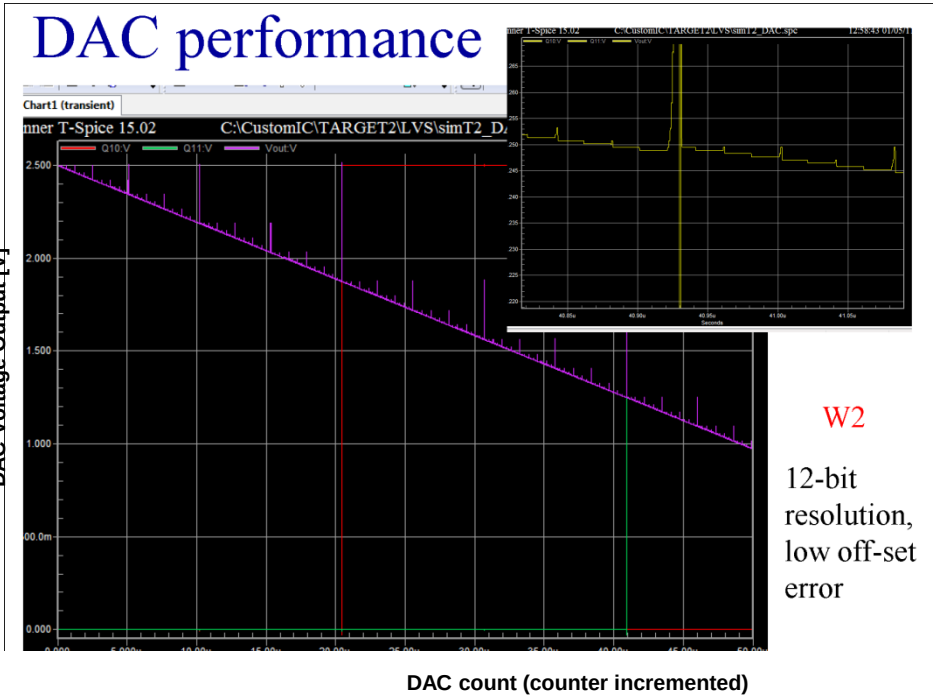


Sampling Speed Measurement

As this is one of the easiest of the adjustments, space reserved for this measurement

12-bit DACs

A large number of 12-bit DACs are provided for being able to tune a number of adjustable parameters. They are all based upon a class R-2R ladder design, and the typical output response versus DAC code is provided in the figure below. Inset is the transition seem of the most significant bit of the counter. Note that DAC response is inverted with respect to input code: 000000000000b = 2.5V, 111111111111b (4095) = 0.0V.



12-bit DAC Settings

Following sequentially through the programming chain the meaning and suggested operating points/trends of these various settings are discussed in the following pages.

TRGSumbias

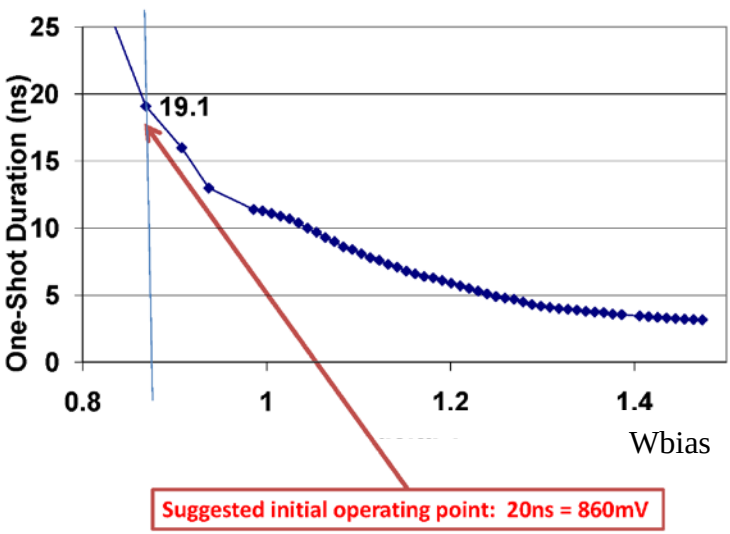
This is the amplifier bias for the Trigger Sum OTA. As it is not driving a heavy load, it need not be driven hard and is governed by the current draw curve for **Vbias,** which is shown on page 7.

TRGbias

This is the amplifier bias for the Trigger Comparator OTA itself. As the circuit is identical to that of TRGSumbias, its response is also shown on page 7.

Wbias

Adjustment of the WBIAS control voltage can be used to tune the 1-shot output width as seen in the figure at left. A comparison with a couple of SPICE reference points indicate that, apart from an observed threshold shift (in part due to level translation offset of an internal buffer amplifier, the same width dependence on WBIAS setting is observed. While narrow output signals can be reliably set, without feedback, temperature dependence is a concern. In future variants the ability to feedback lock using a reference signal will be an important enhancement.



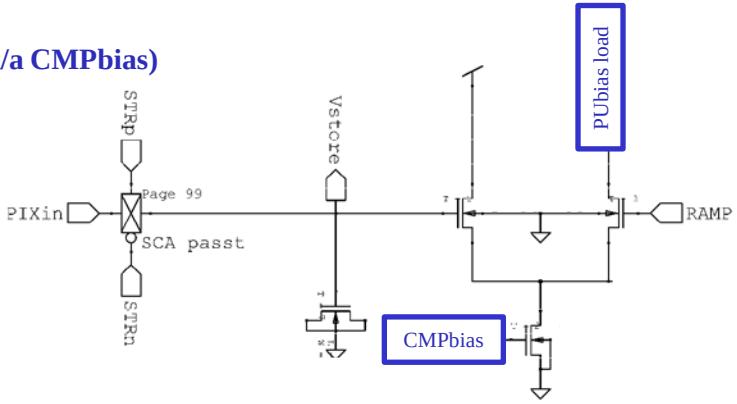
A more comprehensive SPICE simulation of the expected output width as a function of the discharge current, which is independent of the threshold offset observed above.

Temperature Dependence

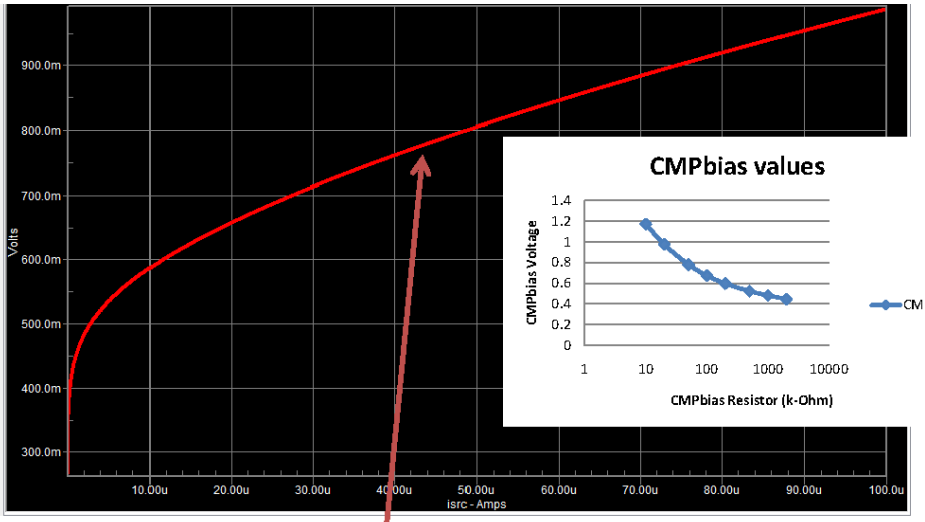
It has been observed that the trigger output width is temperature dependent. Some feedback control is likely to be needed, for which the **TRGin** and **TRGout** (output monitor) signals are provided.

CMPbiasIn (a/k/a CMPbias)

As shown in the circuit at the right is the base storage cell, where two biases are work in opposition to each other through the differential pair to compare the Vstore value with the Ramp voltage. Shout is pulled low to end Wilkinson conversion.



Optimal noise performance is expected to be for about a 4-5x stronger CMPbias than PUbias.



Suggested initial operating point: ~50kΩ = 781mV

TRGGbias

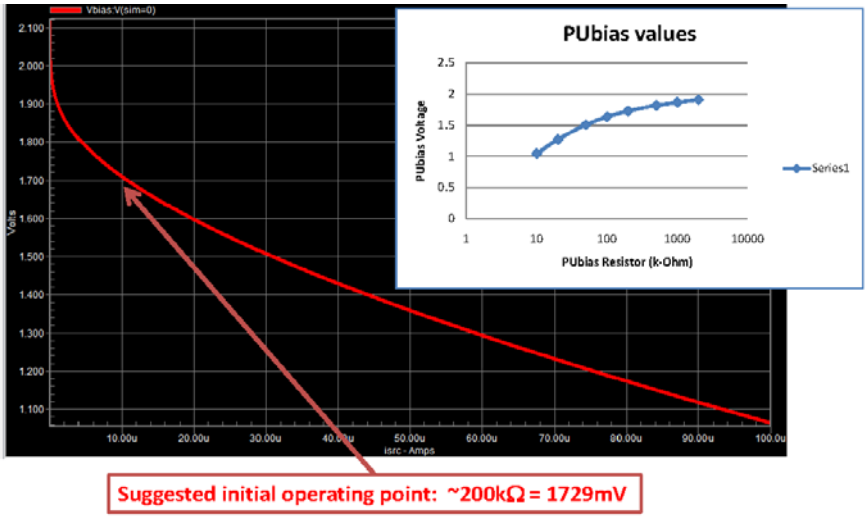
This is the amplifier bias for the Trigger Amplifier OTA, on the input path of every channel. As the circuit is identical to that of TRGSumbias, its response is also shown on page 7.

Sampbias1, Sampbias2 (a/k/a Vbs1, Vbs2)

These are the bias currents for the OTAs that perform the analog gain and transfer as discussed on page 7. For historical reasons they are also known as **Vbs1** and **Vbs2**.

PUbias

As indicated in the diagram on page 14, PUbias works in opposition to CMPbias to enable the differential pair of the compact storage cell to work as a wire-OR ooutput comparator. Something like a 4x-5x stronger CMPbias is suggested for optimum noise performance, though this needs to be studied systematically.



TRGthresh

These thresholds represent the actual thresholds applied to the comparators of the 4 quad trigger outputs, as well the threshold common to all 16 channels.

VdlyN, VdlyP (a/k/a VadjN, VadjP)

These DAC outputs control the sampling timebase adjustment as discussed in detail on page 8.

MonTRGthresh

This DAC sets the monitor trigger channel threshold (typically VDD/2 if using FPGA output as monitor input **[TRGin]** for continuously monitoring trigger width via **TRGout** width tracking.

DBbias

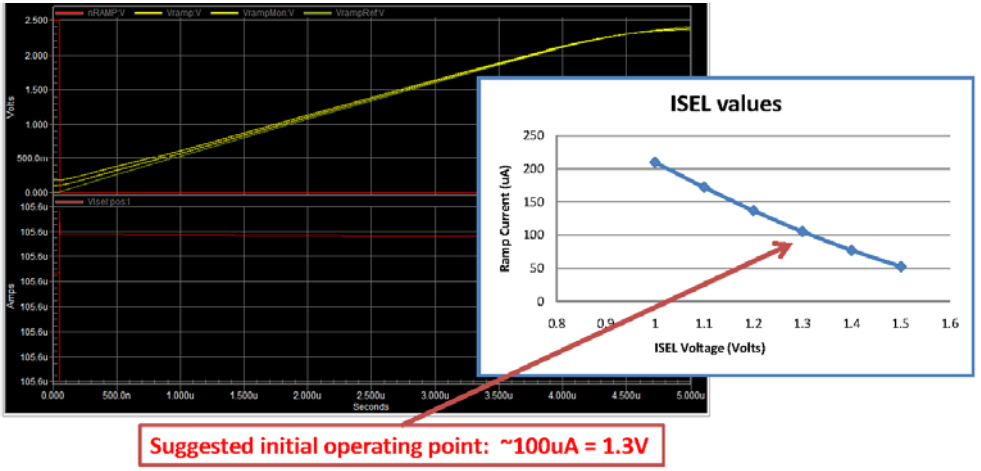
This DAC sets buffered DAC bias strength for the **SBbias**, **Isel** and **Vdischarge** DAC outputs.

SBbias

This DAC sets the SuperBuffer drive strength of the **Vramp** signal fanout.

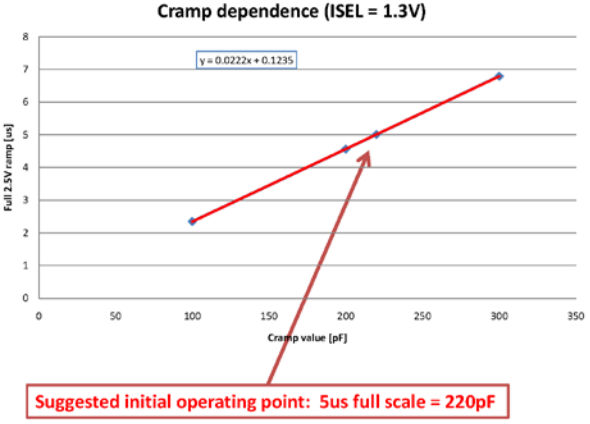
Isel Voltage Ramp Adjustment and Vdischarge Ramp offset

The Wilkinson ramp slew rate is adjusted by varying the capacitor charging current, denoted **ISEL**, or by changing the ramping capacitor (Cramp). For large values of ISEL, non-linearities in the ramp have been observed. For very fast ramping times, a small capacitor is preferred. A typical value of 200pF is normally used, corresponding to the current values and typical discharge time shown. Note that both the ramp slew rate and Wilkinson clock rate may be adjusted to set the Conversion Gain (mV/count), though with some restrictions. The ramp starting location is set via the **Vdischarge** DAC.



This is the Wilkinson Ramp slope adjustment
Simulation is for 200pF Cramp

Ramping Capacitor [Cramp] dependence

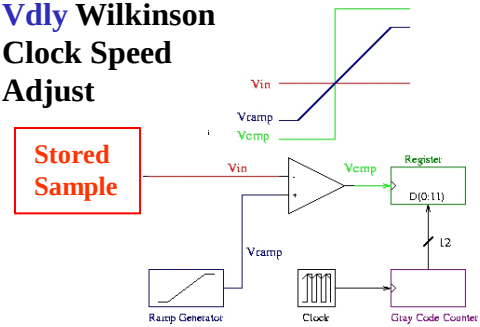


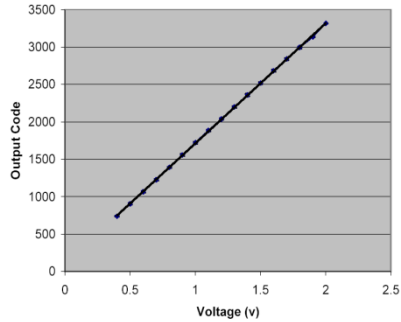
This is the Wilkinson ramp slope adjustment
Quite linear response over this range: 22ns per pF

To complete the discussion of what input ramping capacitance to use, at left is shown the dependence of the full ramping voltage as a function of the Cramp value chosen.

For CTA applications, taking the nominal **ISEL** value set above, about 40pF is the appropriate value for a 1us **Vramp** time.

Vdly Wilkinson Clock Speed Adjust



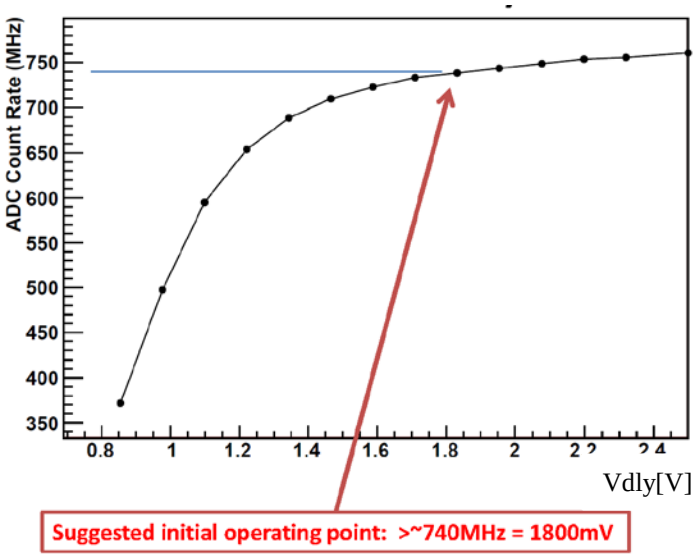


TARGET5 uses a classical Wilkinson architecture, where the comparator, Clock, and digital registers are provided inside the ASIC.

Operational Aspects

The previous pages indicated the bias conditions for the other building blocks of the Wilkinson ADC. A comparator is used to convert the stored sample voltage into a time that a voltage ramp, of known slew rate, exceeds the level of the stored voltage. This time is measured using a clock, of an adjustable rate, and a counter. Adjustable parameters associated with the voltage ramp generation and buffering have been presented. The final element that determines the gain (mV/count) of the Wilkinson ADC is the clock speed adjustment , as described below.

Wilkinson Clock speed adjustment [Vdly]



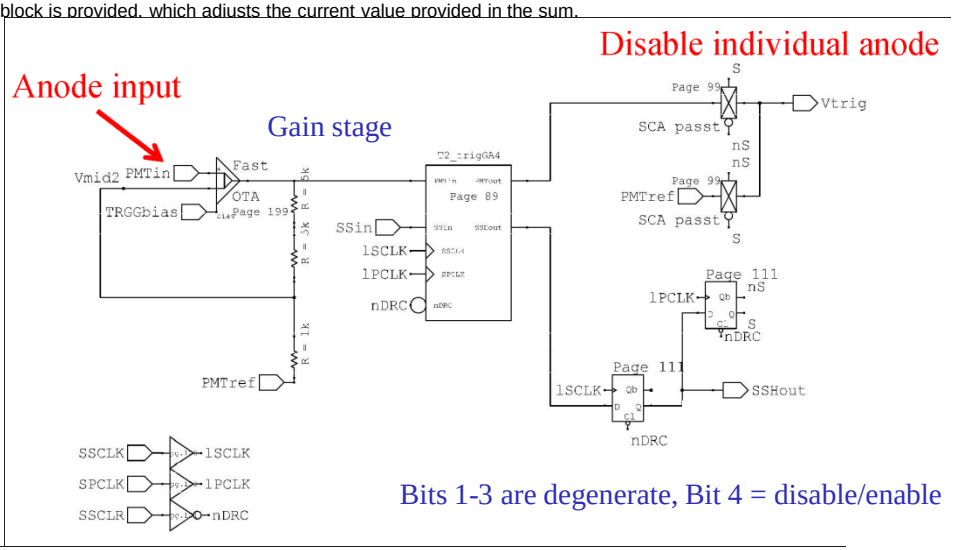
This is the Wilkinson clock adjustment

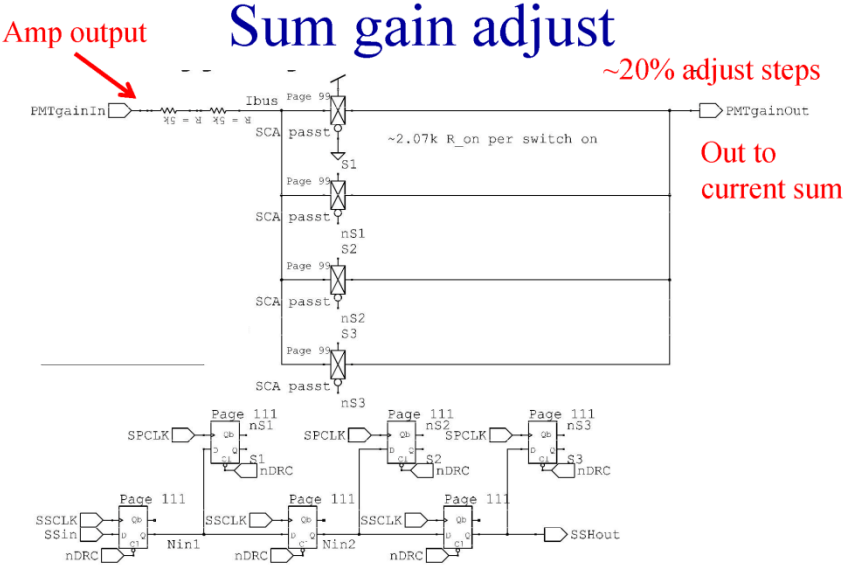
A dedicated, 513th Wilkinson counter is provided for monitoring this counting rate. A separate start/clear are provided and this counter can be left running continuously, as a divide by 13 stages output is provided for monitoring in the companion FPGA to lock in this clock frequency.

As the same temperature dependent effects are expected, this should be servo-looped.

Gain (4-bit register) Trigger Operation

Representative of the desired, extended flexibility in forming triggers with TARGET5, below is a schematic of the trigger path of a single input channel. The select bits shown below determine the gain and the ability to analog disable the sum from an individual anode. To account for differential gain across the face of the PMT, a gain block is provided, which adjusts the current value provided in the sum.

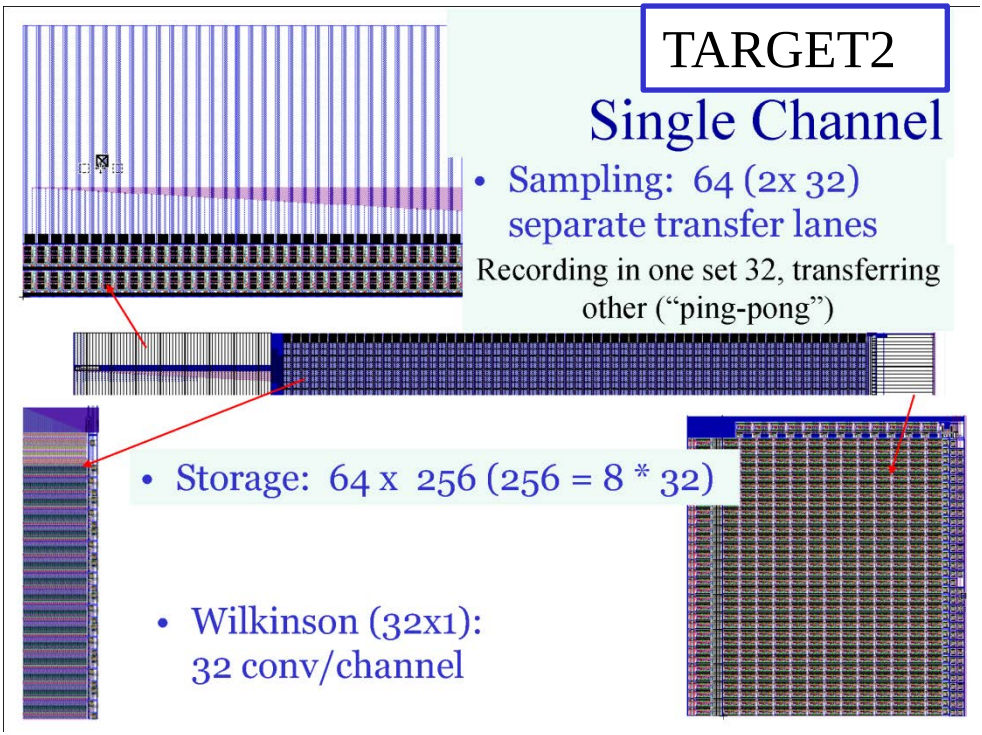




Storage array addressing

The 64 input samples are partitioned into 2 group of 32 sample writes, which are “ping-ponged” between, allowing continuous sampling. These atomic groups of 32 samples are written into an array that is 512 of such 32 samples deep. Due to wiring restrictions, each input group of 32 samples can only be written to 256 of these 512. This is illustrated in the block diagram on the first page of this datasheet. Another wiring limitation is that the samples are written into the rows in groups, such that bit 0 is not the least significant bit of addressing, though this can be treated as a simple pin redefinition.

Reading is performed completely independently of writing, to allow multi-hit buffering inside the array. Samples in groups of 32 are converted in parallel for each channel . The actual stored analog voltages are left inside the storage cell and interrogated in place, using a very simple and compact comparator inside each storage cell. The rest of the Wilkinson ADC (clock, ramp and counter) are described later, with the 32 registers holding the converted 32 samples is seen at the right of the array.

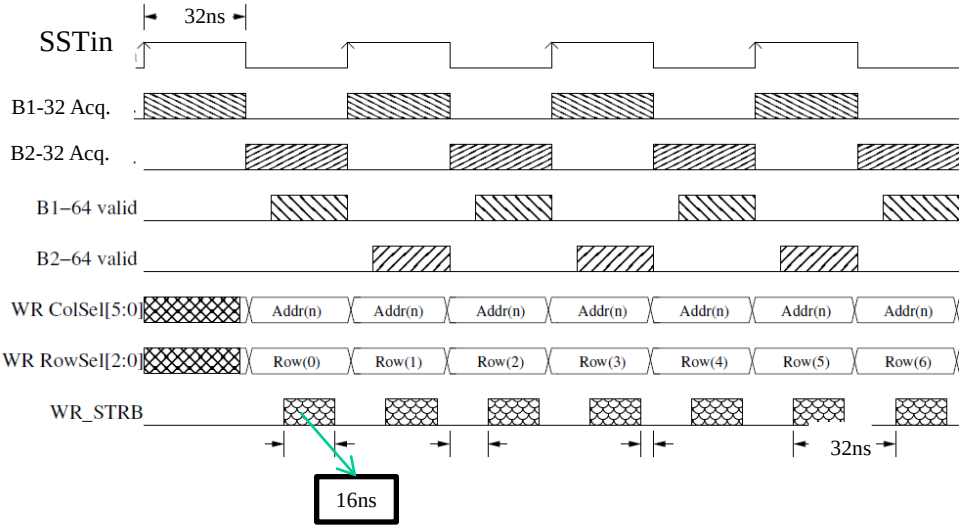


Storage Settling Time

Compared with the analog bandwidth required to couple the analog value into the sampling array, that required for the storage array is greatly reduced. Each buffer amplifier is driving 256 nodes, and simulations indicate settling to 10 bits of resolution in just less than 16ns, which is sufficient for continuous operation at 1GSa/s of the TARGET5 for 32 sample transfer during storage.

Continuous Sampling

In order to provide seamless sampling, the strobes **SSPin** and **SSTin** must be repeated, with a sequential selecting of the Write addresses and transfer of those signals into storage with the Write Strobe (**WR_STRB**) signal. Below is an example timing diagram for acquision at 1GSa/s.



TARGET5

Required state machine

Sampling timing generation and readout requires at least one, or two state machines to perform the sequence of timing strobes and address selects to access the correct addresses with stored samples, convert those values to digital intervals and then broadcast the conversion samples to a data acquisition of some kind. A set of reference firmware for the initial …..

At right is the top-level symbol reflecting the logic needed to implement the requisite state machine. Further information on this logic functionality and required resources will be described in a companion Application Note.

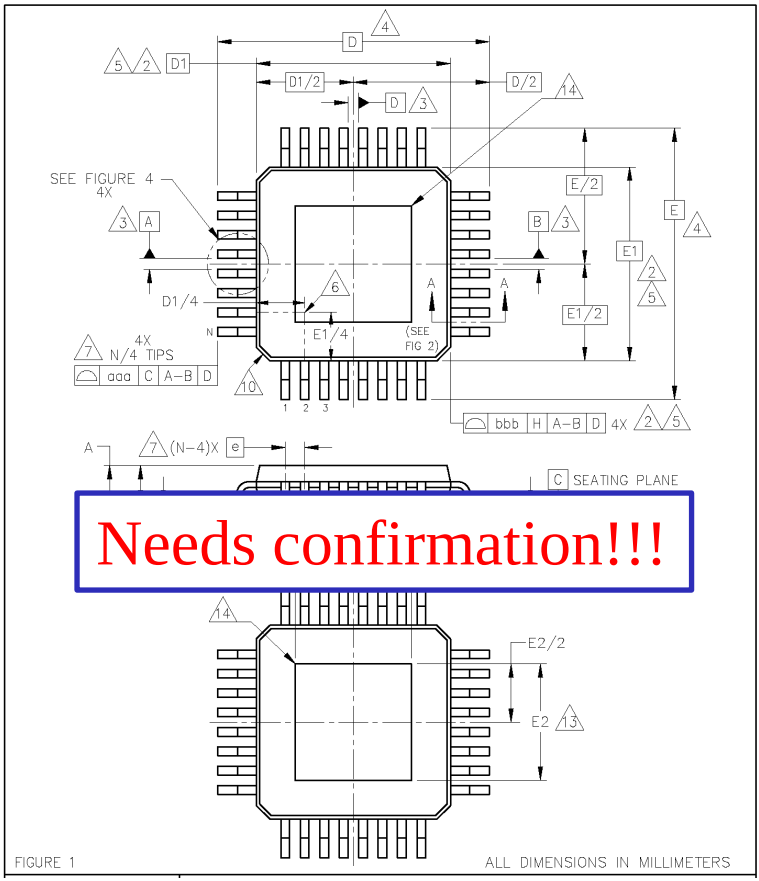
TARGET5 Evaluation Board

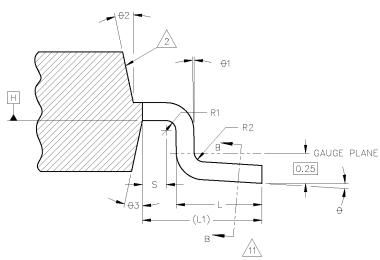
In order to speed development and to gain experience with using the TARGET5 ASIC, an evaluation board is being developed at SLAC….

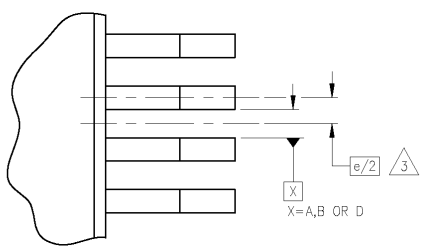
Replace with picture of new TARGET5_eval board

Packaging Mechanics

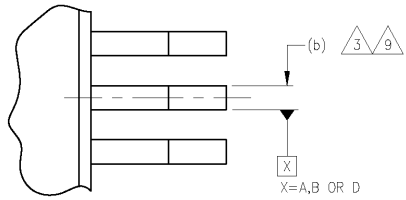
Mechanical drawing details are provided for the package used.







Package Details (cont'd).



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
θ	0°	3.5°	7°	
θ1	0°	–	–	
θ2	11°	12°	13°	
θ3	11°	12°	13°	
C	0.09	–	0.20	11
C1	0.09	–	0.16	11
D2	2.00	–	–	13
E2	2.00	–	–	13
L	0.45	0.60	0.75	
L1	1.00 REF			
R1	0.08	–	–	
R2	0.08	–	0.20	
S	0.20	–	–	
TOLERANCES OF FORM AND POSITION				
aaa	0.20			
bbb	0.20			
NOTE	1,8			
REF				
ISSUE				

14 X 14	1.00	52	AEA	AEA–HU / AEA–HD
14 X 14	0.80	64	AEB	AEB–HU / AEB–HD
14 X 14	0.65	80	AEC	AEC–HU / AEC–HD
14 X 14	0.50	100	AED	AED–HU / AED–HD
14 X 14	0.40	120	AEE	AEE–HU / AEE–HD

120-pin package relevant variation diagram is AEE.

Needs confirmation!!!

SYMBOL	AEC SQUARE			NOTE	AED SQUARE			NOTE	AEE SQUARE			NOTE
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	–	–	1.20	14	–	–	1.20	14	–	–	1.20	14
A1	0.05	–	0.15	12	0.05	–	0.15	12	0.05	–	0.15	12
A2	0.95	1.00	1.05	14	0.95	1.00	1.05	14	0.95	1.00	1.05	14
b	0.22	0.32	0.38	9,11	0.17	0.22	0.27	9,11	0.13	0.18	0.23	9,11
b1	0.22	0.30	0.33	11	0.17	0.20	0.23	11	0.13	0.16	0.19	11
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
e	0.65 BSC				0.50 BSC				0.40 BSC			
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	80				100				120			
TOLERANCES OF FORM AND POSITION												
ccc	0.10				0.08				0.08			
ddd	0.13				0.08				0.07			
NOTE	1,8,15				1,8,15				1,8,15			
REF	11–411				11–411				11–411			
ISSUE	A				A				A			

Mechanical drawing details are provided for the leadframe used to package TARGET5.