Target 5 Camera module interface write-up
2/27/2014
For version 0x31

1 Memory Map Demo Board:

1.1 Master Board FPGA Memory Map

Registers:

0. FpgaVersion
1. Detector ID
2. Serial ID LSW
3. Serial ID MSW
4. Status register
5. Latched Status register
6. FIFO Status register ASIC0
7. Latched FIFO Status register ASIC 0
8. FIFO Status register ASIC1
9. Latched FIFO Status register ASIC 1
10. FIFO Status register ASIC2
11. Latched FIFO Status register ASIC 2
12. FIFO Status register ASIC3
13. Latched FIFO Status register ASIC 3
14. Trigger FIFO Status register
15. Trigger statistics
16. TACK statistic
17. FIFO statistics
18. Packet statistics
19. Command/Ramp count statistics
20. ADC_control_reg
21. ADC_config_reg
22. Time register
23. Control register 0
24. Control register 1
25. Trigger control register 0
26. Trigger control register 1
27. Row/Column control/status
28. Number of samples to read
29. Serial data idelay control register
30. Configuration waveform register
31. Mics Test Register
32. SST FB PLL alignments register
33. SST FB idelay alignments register Status
34. SST FB idelay alignments register Control
35. Spare
36. ROVDD feedback control ASIC 0
37. ROVDD feedback control ASIC 1
38. ROVDD feedback control ASIC 2
39. ROVDD feedback control ASIC 3
40. VDEL feedback control ASIC 0
41. VDEL feedback control ASIC 1
42. VDEL feedback control ASIC 2
43. VDEL feedback control ASIC 3
44. VDEL/ROVDD calculated values ASIC 0
45. VDEL/ROVDD calculated values ASIC 1
46. VDEL/ROVDD calculated values ASIC 2
47. VDEL/ROVDD calculated values ASIC 3
48. VPED DAC control ASIC 0

49. VPED DAC control ASIC 1
50. VPED DAC control ASIC 2
51. VPED DAC control ASIC 3
52. VDELNP DAC control ASIC 0
53. VDELNP DAC control ASIC 1
54. VDELNP DAC control ASIC 2
55. VDELNP DAC control ASIC 3
56. DC_IN DAC control
57. HV DAC control
58. Zero suppression config
59. ADC measurement reg 0
60. ADC measurement reg 1
61. ADC measurement reg 2
62. ADC measurement reg 3
63. ADC measurement reg 4
64. ADC measurement reg 5
65. ADC measurement reg 6
66. ADC measurement reg 7
67. ADC measurement reg 8
68. ADC measurement reg 9
69. ADC measurement reg 10
70. ADC measurement reg 11
71. ADC measurement reg 12
72. Trigger Efficiency Cntl 0
73. Trigger Efficiency Cntl 1
74. Trigger Efficiency Input Cntr
75. Trigger Efficiency Cntr
76. Software reset register
77. Channel enable register 0
78. Channel enable register 1
79. Spare/Test
80. Write Target register
81. Read 0 Target register
82. Read 1 Target register
83. Dead-time control

FPGA version: Address 0x0

Bits	Function	R/W	Default
31-0	Assigned value of 0xFED000030, assigned in Firmware to highlight and track incremental changes in firmware. Incremented with every firmware revision	R	0

Figure 1: FPGA Version: Address 0x0

Detector ID: Address 0x1

Bits	Function	R/W	Default
31-16	Any value for control software, does not have effect on any FPGA logic	RW	0
15-8	Detector ID, fill Detector ID field of reported event	RW	0
7-0	CTA ID, fill CTA ID field of reported event	RW	0

Figure 2: Scratch pad: Address 0x1

Serial number LSW: Address 0x2

Bits	Function	R/W	Default
31-0	Serial number the least significant word	R	0

Figure 3: Serial number LSW: Address 0x2

Serial number MSW: Address 0x3

Bits	Function	R/W	Default
31-0	Serial number the most significant word	R	0

Figure 4 : Serial number MSW: Address 0x3

Status register: Address 0x4

Bits	Function	R/W	Default
31-16	Unused, always 0	R	0
15-12	Status of backplane lines from bp4 to bp7 (also, bp5 is reset and will not be available due to board reset)	R	0
11	Unused, always 0	R	0
10	mgt_AVCC_OK is OK, 1- OK, 0 – is not	R	0
9	+1_8V is OK, 1- OK, 0 – is not	R	0
8-2	Unused, always 0	R	0
1	Underflow on summary FIFO of event data	R	0
0	overflow on summary FIFO of event data	R	0

Figure 5: Status register: Address 0x4

Latched Status register: Addressw 0x5

Bits	Function	R/W	Default
31-16	Unused, always 0	R	0
15-12	Status of backplane lines from bp4 to bp7 (also, bp5 is reset and will not be available due to board reset)	R*	0
11	Unused, always 0	R	0
10	mgt_AVCC_OK is OK, 1- OK, 0 – is not	R*	0
9	+1_8V is OK, 1- OK, 0 – is not	R*	0
8-2	Unused, always 0	R	0
1	Underflow on summary FIFO of event data	R*	0
0	Overflow on summary FIFO of event data	R*	0

Figure 6: Latched Status register: Address 0x5

* - Writing one will reset corresponding bit

FIFO Status register ASIC 0: Address 0x6

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 7: FIFO Status register ASIC 0: Address 0x6

Latched FIFO Status register ASIC 0: Address 0x7

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 8: Latched FIFO Status register ASIC 0: Address 0x7

* - Writing one will reset corresponding bit

FIFO Status register ASIC 1: Address 0x8

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 9: FIFO Status register ASIC 1: Address 0x8

Latched FIFO Status register ASIC 1: Address 0x9

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 10: Latched FIFO Status register ASIC 1: Address 0x9

* - Writing one will reset corresponding bit

FIFO Status register ASIC 2: Address 0xa

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 11: FIFO Status register ASIC 2: Address 0xa

Latched FIFO Status register ASIC 2: Address 0xb

Bits	Function	R/W	Default

31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 12: Latched FIFO Status register ASIC 2: Address 0xb

* - Writing one will reset corresponding bit

FIFO Status register ASIC 3: Address 0xc

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 13: FIFO Status register ASIC 3: Address 0xc

Latched FIFO Status register ASIC 3: Address 0xd

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 14: Latched FIFO Status register ASIC 3: Address 0xd

* - Writing one will reset corresponding bit

Trigger FIFO Status register: Address 0xe

Bits	Function	R/W	Default
31-0	Free running time counter value set by sync over TACK pass 32 MSB	R	0

Figure 15: Trigger FIFO Status register: Address 0xe

* - Writing one will reset corresponding bit

Trigger statistics: Address 0xf

Bits	Function	R/W	Default
31-16	Count number of good Sync verification TACKs.	RW*	0
15-0	Count number of TACKs received	RW*	0

Figure 16: Trigger statistics: Address 0xf

* Writing any value into this register will reset all counters in registers 0xF, 0x10, 0x11, 0x12 and some on 0x13

Tack statistics: Address 0x10

Bits	Function	R/W	Default

31-24	Count sync errors. Time sync verification failed. Counter is reset by writing any value into register 0xF	R	0
23-16	Count of range error over Tack. Counter is reset by writing any value into register 0xF	R	0
15-8	Same as count in bits 7-0. Count Tack Parity errors	R	0
7-0	Count Tack Parity errors. Counter is reset by writing any value into register 0xF	R	0

Figure 17: Tack statistics: Address 0x10

FIFO statistics: Address 0x11

Bits	Function	R/W	Default
31-16	Count all enabled for counting (bits 31 of register 0x17) built packets on all incoming channels. Counter is reset by writing any value into register 0xF	R	0
15-0	Count all built packets on all incoming channels. Counter is reset by writing any value into register 0xF	R	0

Figure 18: FIFO statistics: Address 0x11

Packet statistics: Address 0x12

Bits	Function	R/W	Default
31-16	Internal Arbiter Counter, count all packet forwarded from internal storage to MAC. Counter is reset by writing any value into register 0xF	R	0
15-0	MAC Counter, count all transmitted packet by MAC. Counter is reset by writing any value into register 0xF	R	0

Figure 19: Packet statistics: Address 0x12

Ramp count statistics: Address 0x13

Bits	Function	R/W	Default
31-16	Count command issued to Camera module. Counter is reset by writing any value into register 0xF	R	0
15-0	Count number of event processed. Counter is reset by writing any value into register 0xF	R	0

Figure 20: Ramp count statistics: Address 0x13

ADC mode: Address 0x14

Bits	Function	R/W	Default
31-2	Unused	R	0

1	Select ADC mode for T5 module ADC 1(0 – acquire data continuously after start in reg 0x15, 1 – acquire just once after start in reg 0x15)	RW	0
0	Select ADC mode for T5 module ADC 0(0 – acquire data continuously after start in reg 0x15, 1 – acquire just once after start in reg 0x15)	RW	0

Figure 21: ADC mode: Address 0x14

ADC configuration Register: Address 0x15

Bits	Function	R/W	Default
31	ADC 1 logic, Writing one into this bit will start ADC acquisition immediately.	RW	0
30-26	Unused	R	0
25-23	ADC 1 logic, Select averaging and number of averages http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf 0xx – perform one conversion for each result 100 - perform four conversions and return average for each result 101 - perform eight conversions and return average for each result 110 - perform 16 conversions and return average for each result 111 - perform 32 conversions and return average for each result	RW	0
22-19	ADC 1 logic, Channel select bits, Set to b1011 to read all 12 channels http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf **Must be set to b1011**	RW	0
18	Unused	R	0
17	ADC 1 logic, Select scan mode, bit 0 of scan bits http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf 0- Select readout of channels from 0 through N, 1- from N to highest numbered channel. **Must be set to 0**	RW	0
16	Unused	R	0
15	ADC 0 logic, Writing one into this bit will start ADC acquisition immediately.	RW	0
14-10	Unused	R	0
9-7	ADC 0 logic, Select averaging and number of averages http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf 0xx – perform one conversion for each result 100 - perform four conversions and return average for each result 101 - perform eight conversions and return average for each result 110 - perform 16 conversions and return average for each result 111 - perform 32 conversions and return average for each result	RW	0
6-3	ADC 0 logic, Channel select bits, Set to b1011 to read all 12 channels http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf	RW	0

	Must be set to b1011		
2	Unused	R	0
1	ADC 0 logic, Select scan mode, bit 0 of scan bits http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf 1- Select readout of channels from 0 through N, 1- from N to highest numbered channel. **Must be set to 0**	RW	0
0	Unused	R	0

Figure 22: ADC configuration Register: Address 0x15

- - Good value to load into register 0x15 is 0x80588058, for example

Time register: Address 0x16

Bits	Function	R/W	Default
31-0	Free running time counter value set by sync over TACK pass 32 LSB	R	0

Figure 23: Time register: Address 0x16

Control register 0: Address 0x17

Bits	Function	R/W	Default
31	Enable packet count in register 0x10, bits 31-16	RW	0
30-24	Maximum Ethernet packet size parameter. Indicate how many channels out of available 64 can be shipped in one packet. Value of 0 and 1 indicate one channel per network packet, 2 – channels per packet, and … Careful attention need to be taken to set this parameter. First of all user need to know type of network card host system will have and if it support Jumbo packets. In any case maximum size of acceptable network packet need to be compared with expected event size and properly divided into packets. Default value of 0 (or 1) always process just one channel per packet and works in all cases but will generate maximum number of packets (64). This parameter help to reduce number of packets and related overhead for packet header and trailer to optimize system performance.	RW	0
23-19	Select output type for ASIC Test output. 0x0 - 62.5MHz 0x1… - TBD	RW	0
19	Enable Test Output to ASICs channel 15	RW	0
18-8	Specify ramp signal duration to Target	RW	0
7-3	Ramp start delay after trigger, in system clocks (8 ns)	RW	0
2	Offset usage enable (1). In order to optimize 48 samples readout relatively to trigger position, logic implement option to sync readout to 8 sample bins (4 bins per buffer). Setting bit to one will enable this feature. Otherwise buffer readout always start from beginning. Should be noted that that setting number of readout buffer to more then 2(Bits 23-20) will disable offset usage. And for software buffer this feature disabled as well (bit 9 of 0x1b)	RW	0
1	Unused	RW	0

0	Enable bit, 1- enable analog sampling, after proper Sync command issued	R	0

Figure 24: Control register 0: Address 0x17

Control register 1: Address 0x18

Bits	Function	R/W	Default
31-30	Unused, Spare control bits to Target ASIC 3	RW	0
29	VdlyN feedback on (1)/off(0) control ASIC 3	RW	0
28	Vdly feedback on (1)/off(0) control ASIC 3	RW	0
27	Directly control tst_start input to Target ASIC 3, set to 1	RW	0
26	Directly control tst_boiclr input to Target ASIC 3, set to 0	RW	0
25	Directly control clr_reg input to Target ASIC 3	RW	0
24	Power up ASIC 3 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0
23-22	Unused, Spare control bits to Target ASIC 2	RW	0
21	VdlyN feedback on (1)/off(0) control ASIC 2	RW	0
20	Vdly feedback on (1)/off(0) control ASIC 2	RW	0
19	Directly control tst_start input to Target ASIC 2, set to 1	RW	0
18	Directly control tst_boiclr input to Target ASIC 2, set to 0	RW	0
17	Directly control clr_reg input to Target ASIC 2	RW	0
16	Power up ASIC 2 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0
15-14	Unused, Spare control bits to Target ASIC 1	RW	0
13	VdlyN feedback on (1)/off(0) control ASIC 1	RW	0
12	Vdly feedback on (1)/off(0) control ASIC 1	RW	0
11	Directly control tst_start input to Target ASIC 1, set to 1	RW	0
10	Directly control tst_boiclr input to Target ASIC 1, set to 0	RW	0
9	Directly control clr_reg input to Target ASIC 1	RW	0
8	Power up ASIC 1 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0
7-6	Unused, Spare control bits to Target ASIC 0	RW	0
5	VdlyN feedback on (1)/off(0) control ASIC 0	RW	0
4	Vdly feedback on (1)/off(0) control ASIC 0	RW	0
3	Directly control tst_start input to Target ASIC 0, set to 1	RW	0
2	Directly control tst_boiclr input to Target ASIC 0, set to 0	RW	0
1	Directly control clr_reg input to Target ASIC 0	RW	0
0	Power up ASIC 0 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0

Figure 25: Control register 1: Address 0x18

Trigger control register 0: Address 0x19

Bits	Function	R/W	Default
31-18	Trigger delay, to compensate for time between trigger arrival and trigger decision making, need to be found experimentally. Count in 1ns steps	RW	0
17-14	Unused	RW	0
13-0	Trigger delay alternative, to compensate for time between trigger arrival and trigger decision making, need to be found experimentally. Count in 1ns steps	RW	0

Figure 26: Trigger control register 0: Address 0x19

Trigger control register 1: Address 0x1a

Bits	Function	R/W	Default
31-1	Unused	RW	0
0	Select phase of clock to sample TACK from BP (0 – rising edge, 1 - falling edge)	RW	0

Figure 27: Trigger control register 1: Address 0x1a

Row/Column control/status: Address 0x1b

Bits	Function	R/W	Default
31-30	Unused	RW	0
31-29	Latched by latest trigger value of row counter	R	0
28-23	Latched by latest trigger value of column counter	R	0
22-19	Latched by latest trigger value of sample value (only 4 MSB)	R	0
18-16	Free running current row value to simulate sampling buffer write row pointer	R	0
15-10	Free running current column value to simulate sampling buffer write column pointer	R	0
9	Unused, Old function of enabling software triggering managed by TACK command type. See TACK format	RW	0
8-3	Specify column for readout when Software trigger mode selected by TACK command.	RW	0
2-0	Specify row for readout when Software trigger mode selected by TACK command.	RW	0

Figure 28: Row/Column control/status: Address 0x1b

: Number of samples to read: Address 0x1c

Bits	Function	R/W	Default
31-20	Unused	R	0
19-16	Specify number of alternative buffer for readout, with 0 corresponding to 1 buffers	RW	0

	With 1- 2 buffers With 13 and more15- 14 buffers (maximum)		
15-9	Unused	R	0
8-4	Number of samples on partial buffer, from 0 to 31, to enable flexible readout of any number of desirable samples. At the moment value of 1 -> 16 samples, 0 – 0 samples. Optimized for 48 sample event	RW	0
3-0	Specify number of buffer for readout, with 0 corresponding to 1 buffers With 1- 2 buffers With 13 and more15- 14 buffers (maximum)	RW	0

Figure 29: Number of samples to read: Address 0x1c

Serial data idelay control register: Address 0x1d

Bits	Function	R/W	Default
31-14	Unused	R	0
13-8	Unused	RW	0
7	Unused	R	0
6-0	Unused	RW	0x20

Figure 30: Serial data idelay control register: Address 0x1d

Configuration waveform register: Address 0x1e

Bits	Function	R/W	Default
31-24	PCLK width plus 1 when SIN high, need to be set to 0x3	RW	3
23-16	SIN settling time after PCLK plus 1, need to set to 1	RW	1
15-8	SIN settling time before PCLK plus 1, need to set to 1	RW	1
7-0	PCLK width plus 1 when SIN low, need to be set to 0x7	RW	7

Figure 31: Configuration waveform register: Address 0x1e

Misc test register: Address 0x1f

Bits	Function	R/W	Default
31-22	Unused	RW	0
21-20	Special mode, must be 0	RW	0
19-16	Unused	RW	0
11-8	Select clock phase for input data (0- sampled on falling edge, 1 – sampled on rising edge), 0 – looks like right selection. One bit per ASIC. Bit 8 – ASIC 0, Bit 9 – ASIC 1, ….	RW	0
7-2	Unused	RW	0

1	Select if SR_SEL pulse signal asserted all time (1) or only actual event readout process	RW	0
0	Unused	RW	0

Figure 32: Misc test register: Address 0x1f

SST FB PLL alignments register : Address 0x20

Bits	Function	R/W	Default
31	RCO sampled with PLL clock and re-sampled with system clock to find proper edge (low to high), ignore of high to low. ASIC 3	R	0
30	RCO sampled with PLL clock and re-sampled with system clock to find proper edge (low to high), ignore of high to low. ASIC 2	R	0
29	RCO sampled with PLL clock and re-sampled with system clock to find proper edge (low to high), ignore of high to low. ASIC 1	R	0
28	RCO sampled with PLL clock and re-sampled with system clock to find proper edge (low to high), ignore of high to low. ASIC 0	R	0
27-25	Spare	R	0
24-16	Value recorded into PLL delay (previous value)	R	0
15-11	Spare	R	0
10-9	Select ASIC to address SST setup : 00 - ASIC0, 01 – ASIC1, 10 – ASIC2, 11 – ASIC3	RW	0
8-0	PLL setup value to shift sampling clock timing to align with SST input (from Target) for proper SST type feedback control. Actual value range is from 0 to 0xFF. Each step is about 125ps (estimate)	RW	0

Figure 33: SST FB PLL alignments register : Address 0x20

SST FB idelay alignments register control: Address 0x21

Bits	Function	R/W	Default
31-16	Spare	R	0
15-12	Select destination Idelay. Bit 8 – ASIC 0, Bit 9 - ASIC1, Bit 10 – ASIC 2, Bit 11 – ASIC3	RW	0
11-9	Spare	R	0
8	Idel setup value to shift direction. Every update to this register will shift in proper direction for proper amount specified in bits 21-16.	RW	0
7-0	Idelay setup value to shift sampling clock timing to align with SST input (from Target) for proper setup. Actual value range is from 0 to 0xff. Each step is about 70ps (estimate). Set to midrange at power up to make correction in both directions. Generally it is not used. Need for secondary feedback loop if implemented. For now just register control.	RW	0

Figure 34: SST FB idelay alignments register control: Address 0x21

SST FB idelay alignments register status: Address 0x22

Bits	Function	R/W	Default
31-24	Value recorded into Idelay delay ASIC 3	R	0
23-16	Value recorded into Idelay delay ASIC 2	R	0
15-8	Value recorded into Idelay delay ASIC 1	R	0
7-0	Value recorded into Idelay delay ASIC 0	R	0

Figure 35: SST FB idelay alignments register status: Address 0x22

Spare: Address 0x23

Bits	Function	R/W	Default
31-0	Spare	0	0

Figure 36: Spare: Address 0x23

ROVDD feedback control ASIC 0: Address 0x24

Bits	Function	R/W	Default
31-20	Set VDD value for ROVDD feedback loop, this value should be as close as possible to final desired sampling frequency. But from practical point only VdlyN control sampling frequency, so we should use only VdlyN to control RCO frequency to adjust sampling. Default value for 1GHz sampling is 0x910, therefore to control VdlyN we need to invert this value to 0x911(TBD) as starting RCO feedback value. Similarly for 400MHz sampling we have 0xBC0, so we have to set feedback initial value to 0xBC1(TBD). VdlyN Feedback enabled by bit 5 of the register 0x18.	RW	0
19-0	Bit in this field are interpreted on base of the ASIC configuration bit which are stored in reg. 0x2c bit 30. If bit set to 1: Compare value for ROVDD feedback loop. This is actual value which effect RCO final frequency. To find rough value we need to multiply desired RCO period in ns by 256. It is a little tricky task, because RCO runs faster than desired sampling frequency, so we need to target slower value of RCO frequency to get desired frequency. To have 1GHz sampling we need to set RCO roughly to 1GHz/128 = `7.8MHz(or period of 128ns), however in practice real 1GHz sampling achieved at 5.95MHZ (or 168ns) given that VdlyP set to value of 0x680 (to make RCO closer to 50% duty cycle). In this case value of this register need to be set 168*256=43008 (or 0xa800). Similarly for 400MHz sampling we need to set this value to about 1.88MHz(531ns) or value of 256*531= ~0x212f0 (need to be verified for 400MHz sampling) If bit set to 0: Then this field divided into 2: - bits 19-10 specify computational compare value for feedback control, nominally should be 0x200 - bits 9-0 specify computational compare hysteresis value for feedback control. Value to TBD	RW	0

Figure 37: ROVDD feedback control ASIC 0: Address 0x24

ROVDD feedback control ASIC 1: Address 0x25

Bits	Function	R/W	Default
31-20	Set VDD value for ROVDD feedback loop, this value should be as close as possible to final desired sampling frequency. But from practical point only VdlyN control sampling frequency, so we should use only VdlyN to control RCO frequency to adjust sampling. Default value for 1GHz sampling is 0x910, therefore to control VdlyN we need to invert this value to 0x911(TBD) as starting RCO feedback value. Similarly for 400MHz sampling we have 0xBC0, so we have to set feedback initial value to 0xBC1(TBD). VdlyN Feedback enabled by bit 13 of the register 0x18.	RW	0
19-0	Bit in this field are interpreted on base of the ASIC configuration bit which are stored in reg. 0x25d bit 30. If bit set to 1: Compare value for ROVDD feedback loop. This is actual value which effect RCO final frequency. To find rough value we need to multiply desired RCO period in ns by 256. It is a little tricky task, because RCO runs faster than desired sampling frequency, so we need to target slower value of RCO frequency to get desired frequency. To have 1GHz sampling we need to set RCO roughly to 1GHz/128 = `7.8MHz(or period of 128ns), however in practice real 1GHz sampling achieved at 5.95MHZ (or 168ns) given that VdlyP set to value of 0x680 (to make RCO closer to 50% duty cycle). In this case value of this register need to be set 168*256=43008 (or 0xa800). Similarly for 400MHz sampling we need to set this value to about 1.88MHz(531ns) or value of 256*531= ~0x212f0 (need to be verified for 400MHz sampling) If bit set to 0: Then this field divided into 2: - bits 19-10 specify computational compare value for feedback control, nominally should be 0x200 - bits 9-0 specify computational compare hysteresis value for feedback control. Value to TBD	RW	0

Figure 38: ROVDD feedback control ASIC 1: Address 0x25

ROVDD feedback control ASIC 2: Address 0x26

Bits	Function	R/W	Default
31-20	Set VDD value for ROVDD feedback loop, this value should be as close as possible to final desired sampling frequency. But from practical point only VdlyN control sampling frequency, so we should use only VdlyN to control RCO frequency to adjust sampling. Default value for 1GHz sampling is 0x910, therefore to control VdlyN we need to invert this value to 0x911(TBD) as starting RCO feedback value. Similarly for 400MHz sampling we have 0xBC0, so we have to set feedback initial value to 0xBC1(TBD). VdlyN Feedback enabled by bit 21 of the register 0x18.	RW	0
19-0	Bit in this field are interpreted on base of the ASIC configuration bit which are stored in reg. 0x2e bit 30. If bit set to 1: Compare value for ROVDD feedback loop. This is actual value which effect RCO final frequency. To find rough value we need to multiply desired RCO	RW	0

	period in ns by 256. It is a little tricky task, because RCO runs faster than desired sampling frequency, so we need to target slower value of RCO frequency to get desired frequency. To have 1GHz sampling we need to set RCO roughly to 1GHz/128 = `7.8MHz(or period of 128ns), however in practice real 1GHz sampling achieved at 5.95MHZ (or 168ns) given that VdlyP set to value of 0x680 (to make RCO closer to 50% duty cycle). In this case value of this register need to be set 168*256=43008 (or 0xa800). Similarly for 400MHz sampling we need to set this value to about 1.88MHz(531ns) or value of 256*531= ~0x212f0 (need to be verified for 400MHz sampling) If bit set to 0: Then this field divided into 2: - bits 19-10 specify computational compare value for feedback control, nominally should be 0x200 - bits 9-0 specify computational compare hysteresis value for feedback control. Value to TBD		

Figure 39: ROVDD feedback control ASIC 2: Address 0x26

ROVDD feedback control ASIC 3: Address 0x27

Bits	Function	R/W	Default
31-20	Set VDD value for ROVDD feedback loop, this value should be as close as possible to final desired sampling frequency. But from practical point only VdlyN control sampling frequency, so we should use only VdlyN to control RCO frequency to adjust sampling. Default value for 1GHz sampling is 0x910, therefore to control VdlyN we need to invert this value to 0x911(TBD) as starting RCO feedback value. Similarly for 400MHz sampling we have 0xBC0, so we have to set feedback initial value to 0xBC1(TBD). VdlyN Feedback enabled by bit 29 of the register 0x18.	RW	0
19-0	Bit in this field are interpreted on base of the ASIC configuration bit which are stored in reg. 0x2f bit 30. If bit set to 1: Compare value for ROVDD feedback loop. This is actual value which effect RCO final frequency. To find rough value we need to multiply desired RCO period in ns by 256. It is a little tricky task, because RCO runs faster than desired sampling frequency, so we need to target slower value of RCO frequency to get desired frequency. To have 1GHz sampling we need to set RCO roughly to 1GHz/128 = `7.8MHz(or period of 128ns), however in practice real 1GHz sampling achieved at 5.95MHZ (or 168ns) given that VdlyP set to value of 0x680 (to make RCO closer to 50% duty cycle). In this case value of this register need to be set 168*256=43008 (or 0xa800). Similarly for 400MHz sampling we need to set this value to about 1.88MHz(531ns) or value of 256*531= ~0x212f0 (need to be verified for 400MHz sampling) If bit set to 0: Then this field divided into 2: - bits 19-10 specify computational compare value for feedback control, nominally should be 0x200 - bits 9-0 specify computational compare hysteresis value for feedback control. Value to TBD	RW	0

Figure 40: ROVDD feedback control ASIC 3: Address 0x27

VDEL feedback control ASIC 0: Address 0x28

Bits	Function	R/W	Default
31-20	Set VDD value for VDEL feedback loop. Need to be set as close as possible to desired Wilkinson sampling control voltage DAC value. It is roughly 0x900. VdlyN Feedback enabled by bit 4 of the register 0x18.	RW	0
19-0	Compare value for VDEL feedback loop. This is value which effect final Vdly and related Wilkinson sampling frequency. It is computed by multiplying Wilkinson sampling period by 65536 (2^16). So, for example, for 700Mhz sampling we have period of 1.42ns. 1.42*65536 = 93623(16DB6).Also in practical sense we can measure frequency of Vdly*4096 on output pin. So to set this value we need just multiply desired observed period by 16.	RW	0

Figure 41: VDEL feedback control ASIC 0: Address 0x28

VDEL feedback control ASIC 1: Address 0x29

Bits	Function	R/W	Default
31-20	Set VDD value for VDEL feedback loop. Need to be set as close as possible to desired Wilkinson sampling control voltage DAC value. It is roughly 0x900. VdlyN Feedback enabled by bit 12 of the register 0x18.	RW	0
19-0	Compare value for VDEL feedback loop. This is value which effect final Vdly and related Wilkinson sampling frequency. It is computed by multiplying Wilkinson sampling period by 65536 (2^16). So, for example, for 700Mhz sampling we have period of 1.42ns. 1.42*65536 = 93623(16DB6).Also in practical sense we can measure frequency of Vdly*4096 on output pin. So to set this value we need just multiply desired observed period by 16.	RW	0

Figure 42: VDEL feedback control ASIC 1: Address 0x29

VDEL feedback control ASIC 2: Address 0x2a

Bits	Function	R/W	Default
27-16	Set VDD value for VDEL feedback loop. Need to be set as close as possible to desired Wilkinson sampling control voltage DAC value. It is roughly 0x900. Vdly Feedback enabled by bit 20 of the register 0x18.	RW	0
15-0	Compare value for VDEL feedback loop. This is value which effect final Vdly and related Wilkinson sampling frequency. It is computed by multiplying Wilkinson sampling period by 65536 (2^16). So, for example, for 700Mhz sampling we have period of 1.42ns. 1.42*65536 = 93623(16DB6).Also in practical sense we can measure frequency of Vdly*4096 on output pin. So to set this value we need just multiply desired observed period by 16.	RW	0

Figure 43: VDEL feedback control ASIC 2: Address 0x2a

VDEL feedback control ASIC 3: Address 0x2b

Bits	Function	R/W	Default
31-20	Set VDD value for VDEL feedback loop. Need to be set as close as possible to desired Wilkinson sampling control voltage DAC value. It is roughly 0x900. VdlyN Feedback enabled by bit 28 of the register 0x18.	RW	0
19-0	Compare value for VDEL feedback loop. This is value which effect final Vdly and related Wilkinson sampling frequency. It is computed by multiplying Wilkinson sampling period by 65536 (2^16). So, for example, for 700Mhz sampling we have period of 1.42ns. 1.42*65536 = 93623(16DB6).Also in practical sense we can measure frequency of Vdly*4096 on output pin. So to set this value we need just multiply desired observed period by 16.	RW	0

Figure 44: VDEL feedback control ASIC 3: Address 0x2b

VDEL/ROVDD calculated values ASIC 0: Address 0x2c

Bits	Function	R/W	Default
31	Unused	R	0
30	Captured at FPGA ASIC 0 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
29	Captured at FPGA ASIC 0 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0
28	Captured at FPGA ASIC 0 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0
27-16	Computed VdelN voltage, computed other by RCO FB(bit 30 = 1), or SST PLL based FB(0)	R	0
15-12	Unused	R	0
11-0	Computed VDEL DAC value	R	0

Figure 45: VDEL/ROVDD calculated values ASIC 0: Address 0x2c

VDEL/ROVDD calculated values ASIC 1: Address 0x2d

Bits	Function	R/W	Default
31	Unused	R	0
30	Captured at FPGA ASIC 1 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
29	Captured at FPGA ASIC 1 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0
28	Captured at FPGA ASIC 1 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0

27-16	Computed VdelN voltage, computed other by RCO FB(bit 30 = 1), or SST PLL based FB(0)	R	0
15-12	Unused	R	0
11-0	Computed VDEL DAC value	R	0

Figure 46: VDEL/ROVDD calculated values ASIC 1: Address 0x2d

VDEL/ROVDD calculated values ASIC 2: Address 0x2e

Bits	Function	R/W	Default
31	Unused	R	0
30	Captured at FPGA ASIC 2 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
29	Captured at FPGA ASIC 2 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0
28	Captured at FPGA ASIC 2 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0
27-16	Computed VdelN voltage, computed other by RCO FB(bit 30 = 1), or SST PLL based FB(0)	R	0
15-12	Unused	R	0
11-0	Computed VDEL DAC value	R	0

Figure 47: VDEL/ROVDD calculated values ASIC 2: Address 0x2e

VDEL/ROVDD calculated values ASIC 3: Address 0x2f

Bits	Function	R/W	Default
31	Unused	R	0
30	Captured at FPGA ASIC 3 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
29	Captured at FPGA ASIC 3 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0
28	Captured at FPGA ASIC 3 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0
27-16	Computed VdelN voltage, computed other by RCO FB(bit 30 = 1), or SST PLL based FB(0)	R	0
15-12	Unused	R	0
11-0	Computed VDEL DAC value	R	0

Figure 48: VDEL/ROVDD calculated values ASIC 3: Address 0x2f

VPED DAC control ASIC 0: Address 0x30

Bits	Function	R/W	Default
31-12	Unused	RW	0
11-0	VPED value from 0 to 2.5V (Max value enforced in hardware is 0xB6C ~2.5V)	RW	0

Figure 49: VPED DAC control ASIC 0: Address 0x30

VPED DAC control ASIC 1: Address 0x31

Bits	Function	R/W	Default
31-12	Unused	RW	0
11-0	VPED value from 0 to 2.5V (Max value enforced in hardware is 0xB6C ~2.5V)	RW	0

Figure 50: VPED DAC control ASIC 1: Address 0x31

VPED DAC control ASIC 2: Address 0x32

Bits	Function	R/W	Default
31-12	Unused	RW	0
11-0	VPED value from 0 to 2.5V (Max value enforced in hardware is 0xB6C ~2.5V)	RW	0

Figure 51: VPED DAC control ASIC 2: Address 0x32

VPED DAC control ASIC 3: Address 0x33

Bits	Function	R/W	Default
31-12	Unused	RW	0
11-0	VPED value from 0 to 2.5V (Max value enforced in hardware is 0xB6C ~2.5V)	RW	0

Figure 52: VPED DAC control ASIC 3: Address 0x33

VDELNP DAC control ASIC 0: Address 0x34 (not implemented – space holder)

Bits	Function	R/W	Default
31	Update VdlyP value	RW	0
30-28	Unused	RW	0
27-16	VdlyP value from 0 to 2.5V	RW	0
15	Update VdlyN value	RW	0
14-12	Unused	RW	0
11-0	VdlyN value from 0 to 2.5V	RW	0

Figure 53: VDELNP DAC control ASIC 0: Address 0x34

VDELNP DAC control ASIC 1: Address 0x35 (not implemented – space holder)

Bits	Function	R/W	Default

31	Update VdlyP value	RW	0
30-28	Unused	RW	0
27-16	VdlyP value from 0 to 2.5V	RW	0
15	Update VdlyN value	RW	0
14-12	Unused	RW	0
11-0	VdlyN value from 0 to 2.5V	RW	0

Figure 54: VDELNP DAC control ASIC 1: Address 0x35

VDELNP DAC control ASIC 2: Address 0x36 (not implemented – space holder)

Bits	Function	R/W	Default
31	Update VdlyP value	RW	0
30-28	Unused	RW	0
27-16	VdlyP value from 0 to 2.5V	RW	0
15	Update VdlyN value	RW	0
14-12	Unused	RW	0
11-0	VdlyN value from 0 to 2.5V	RW	0

Figure 55: VDELNP DAC control ASIC 2: Address 0x36

VDELNP DAC control ASIC 3: Address 0x37 (not implemented – space holder)

Bits	Function	R/W	Default
31	Update VdlyP value	RW	0
30-28	Unused	RW	0
27-16	VdlyP value from 0 to 2.5V	RW	0
15	Update VdlyN value	RW	0
14-12	Unused	RW	0
11-0	VdlyN value from 0 to 2.5V	RW	0

Figure 56: VDELNP DAC control ASIC 3: Address 0x37

DC_IN DAC control all ASIC: Address 0x38

Bits	Function	R/W	Default
31-12	Unused	RW	0
11-0	DC_IN to bias input voltage value from 0 to 2.047V - Unused	RW	0

Figure 57: DC_IN DAC control all ASIC : Address 0x38

HV DAC control: Address 0x39

Bits	Function	R/W	Default
31-12	Unused	RW	0
11-0	HV setup voltage value from 0 to 2.047V , correspond to specific selected HV supply	RW	0

Figure 58: HV DAC control: Address 0x39

Zero-suppression control register: Address 0x3a

Bits	Function	R/W	Default
31	Enable zero suppression algorithm. This algorithm discard all suppressed channels	RW	0
30	Test zero-suppression reporting. Configure system return only enabled channels regarding zero-suppression logic	RW	0
29-24	Unused	RW	0
23-12	Set overflow value to properly handle overflow	RW	0
11-0	Set threshold value to compare. Discard if all values under threshold.	RW	0

Figure 59: Zero-suppression control register: Address 0x3a

ADC 0 Data: Address 0x3b

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, Temperature measured by ADC 1, conversion is T,C = value*0.125, C	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, Temperature measured by ADC 0,conversion is T,C = value*0.125, C	R	0

Figure 60: ADC 0 Data: Address 0x3b

ADC 1 Data: Address 0x3c

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, Unused	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0

11-0	ADC 0, Unused	R	0

Figure 61: ADC 1 Data: Address 0x3c

ADC 2 Data: Address 0x3d

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 +2.5V Voltage, conversion is V = value*5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 3 +2.5V Voltage, conversion is V = value*5/4096,V	R	0

Figure 62: ADC 2 Data: Address 0x3d

ADC 3 Data: Address 0x3e

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 VPED Voltage, conversion is V = value*5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 3 VPED Voltage, conversion is V = value*5/4096,V	R	0

Figure 63: ADC 3 Data: Address 0x3e

ADC 4 Data: Address 0x3f

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 Temperature in K = ADC_value *2500/4095/2.94 K	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 3 Temperature in K = ADC_value *2500/4095/2.94 K	R	0

Figure 64: ADC 4 Data: Address 0x3f

ADC 5 Data: Address 0x40

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 SUM of DISCHARGE and ISEL Voltage, conversion is V = value*7.5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 3 SUM of DISCHARGE and ISEL Voltage, conversion is V = value*7.5/4096,V	R	0

Figure 65: ADC 5 Data: Address 0x40

ADC 6 Data: Address 0x41

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, Unused	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, Unused	R	0

Figure 66: ADC 6 Data: Address 0x41

ADC 7 Data: Address 0x42

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 0 +2.5V Voltage, conversion is V = value*5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 1 +2.5V Voltage, conversion is V = value*5/4096,V	R	0

Figure 67: ADC 7 Data: Address 0x42

ADC 8 Data: Address 0x43

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 0 VPED Voltage, conversion is V = value*5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 1 VPED Voltage, conversion is V = value*5/4096,V	R	0

Figure 68: ADC 8 Data: Address 0x43

ADC 9 Data: Address 0x44

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 0 Temperature in K = ADC_value *2500/4095/2.94 K	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 1 Temperature in K = ADC_value *2500/4095/2.94 K	R	0

Figure 69: ADC 9 Data: Address 0x44

ADC 10 Data: Address 0x45

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 0 SUM of DISCHARGE AND ISEL Voltage, conversion is V = value*7.5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, ASIC 1 DISCHARGE AND ISEL Voltage, conversion is V = value*7.5/4096,V	R	0

Figure 70: ADC 10 Data: Address 0x45

ADC 11 Data: Address 0x46

Bits	Function	R/W	Default

31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30-28	Unused	R	0
27-16	ADC 1, MGT Supply Voltage, conversion is V = value*5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, 1.2V FPGA Voltage (2.5V), conversion is V = value*5/4096,V	R	0

Figure 71: ADC 11 Data: Address 0x46

ADC 12 Data: Address 0x47

Bits	Function	R/W	Default
31	ADC 1, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
30- 28	Unused	R	0
27-16	ADC 1, 1.8V FPGA Voltage , conversion is V = value*5/4096,V	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	RW	0
14-12	Unused	R	0
11-0	ADC 0, 2.5V FPGA Voltage , conversion is V = value*5/4096,V	R	0

Figure 72: ADC 12 Data: Address 0x47

Trigger efficiency control 0 register: Address 0x48

Bits	Function	R/W	Default
31-0	Unused	R	0

Figure 73: Trigger efficiency control 0 register: Address 0x48

Trigger efficiency control 1 register: Address 0x49

Bits	Function	R/W	Default
31-0	Unused	R	0

Figure 74: Trigger efficiency control 1 register: Address 0x49

Trigger input counter register: Address 0x4a

Bits	Function	R/W	Default
31-0	Unused	R	0

Figure 75: Trigger input counter register: Address 0x4a

Trigger efficiency counter register: Address 0x4b

Bits	Function	R/W	Default
31-0	Unused	RW	0

Figure 76: Trigger efficiency counter register: Address 0x4b

Software reset register: Address 0x4c

Bits	Function	R/W	Default
31-0	Writing value of 0xBECEDACE will start reset of FPGA logic, but keep values programmed into register. Also, write to this register does not generate command response due to transmitter logic reset as well	RW	0

Figure 77: Software reset register: Address 0x4c

Channel enable register 0: Address 0x4d

Bits	Function	R/W	Default
31-0	Channel enable register bits 31-0. Channel 15-0 on ASIC 0, Channel 31-16 on ASIC 1. One bit per channel. 0 – disable, 1 - enable	RW	0

Figure 78: Channel enable register 0: Address 0x4d

Channel enable register 1: Address 0x4e

Bits	Function	R/W	Default
31-0	Channel enable register bits 31-0. Channel 15-0 on ASIC 0, Channel 31-16 on ASIC 1. One bit per channel. 0 – disable, 1 - enable	RW	0

Figure 79: Channel enable register 1: Address 0x4e

Spare/test: Address 0x4f – Not for normal operation

Bits	Function	R/W	Default
31-12	Unused	R	0
11	Special mode for sr_clk. 0 – sr_clk run continuously, 1 – sr_clk run when only needed	RW	0
10	Special trigger mode. When set to 1 enable J5 output generate pulse on every sampling buffer turn for 10 event and stop. To reactivate need to bring it back to 0, if 0 - trigger sync command generated ~ at 1kHz	RW	0
9	To control direction of External Trigger IO, 0 – input, 1 - output	RW	0
8-0	Unused	R	0

Figure 80: Spare/test: Address 0x4f

1.1.1 Target 5 ASIC related registers

Write Target register: Address 0x50

Bits	Function	R/W	Default
31-24	Unused	R	0
23	Enable (1) write/read operation to ASIC 3	RW	0
22	Enable (1) write/read operation to ASIC 2	RW	0
21	Enable (1) write/read operation to ASIC 1	RW	0
20	Enable (1) write/read operation to ASIC 0	RW	0
19	If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	RW	0
18	Define if data latching on Target is required. 0 – latching is required, 1 – no latching.	RW	0
17-12	Target register address to write. See Target 5 documentation for specific register address map. Need to be noted that if Target register 0x2b is addresses than write will be forced to all target registers regardless of bits 23-20 in this register to force all ASIC to be in the same state.	RW	0
11-0	Target register value to write. See Target 5 documentation for specific registers and bit allocation	RW	0

Figure 81: Write Target register: Address 0x50

*-Writing to register 0x2b of ASIC will always write to all 4 ASICs regardless of state of bits 23-20.

Read 0 target register: Address 0x51

Bits	Function	R/W	Default
31	Unused	RW	0
30	Captured at FPGA ASIC 1 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
29	Captured at FPGA ASIC 1 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0
28	Captured at FPGA ASIC 1 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0
27-16	Read back value from ASIC 1. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0
15	Unused	RW	0
14	Captured at FPGA ASIC 0 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
13	Captured at FPGA ASIC 0 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0

12	Captured at FPGA ASIC 0 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0
11-0	Read back value from ASIC 0. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0

Figure 82: Read 0 target register: Address 0x51

Read 1 target register: Address 0x52

Bits	Function	R/W	Default
31	Unused	RW	0
30	Captured at FPGA ASIC 3 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
29	Captured at FPGA ASIC 3 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0
28	Captured at FPGA ASIC 3 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0
27-16	Read back value from ASIC 3. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0
15	Unused	RW	0
14	Captured at FPGA ASIC 2 configuration bits. Captured bit of Target 5 configuration, Select output between SST/SSP (0) and RCO(1)	R	0
13	Captured at FPGA ASIC 2 configuration bits. Captured bit of Target 5 configuration, Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	R	0
12	Captured at FPGA ASIC 2 configuration bits. Captured bit of Target 5 configuration, Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	R	0
11-0	Read back value from ASIC 2. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0

Figure 83: Read 1 target register: Address 0x52

1.2 Packet data word

Modification for new loopback format

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
ZS_e	SizeOfPacket (7 bits). Indicate how many channels included into this packet. 0 –							Size(6 bits). Indicate number of 16 words group in event. Value					First sub-		Last sub-

n (1 bit) Copy of reg setup	indicate that all events are zero-suppressed. Maximum 0x40 or all 64 channels in event. This field controlled by combination of zero-suppressed logic and parameter of Maximum packet size in register 0x17 bit 30-24						of 0x3 indicate 48 data words, value of 0x4 – 64 words per channel. This value related to Number of buffers in event (register 0x17, bits 23-20). Total packet size in bytes will be = (size*32 + 2) * SizeOfPacket+20	packet of event packet	packet of event packet
NEW-> TACK LOOP BACK TIME bits 15-0									
CTA ID (8 bits) (value loaded into register 0x1, bits 7-0)							Detector ID (8bits)) (value loaded into register 0x1, bits 15-8)		
Event sequence number (8bit) Sequence number, number incremented in each sequential packet. Cleared only by reset.							Detector unique tag (8 LSB of 64 bit ID tag) Tag bits (Unique 8 LSB of serial ID which can be read from register 2 bits 7-0)		
NEW-> TACK LOOP BACK TIME bits 31-16									
NEW-> TACK LOOP BACK TIME bits 47-32									
NEW-> TACK LOOP BACK TIME bits 63-48									
Zero-suppression enabled (1b)	Stale data(read more than once without update or TACK with error(1bit)			Starting column location of buffers read 6 bits)			Starting row location of buffers read (3 bits)	Starting quadrant location of buffers read (5 bits)	
1	ASIC ID (2 bits)		Channel ID (4 bits)		Error flags (1b)	NEW->TACK mode bits 65-64		Size(6 bits). Size of 16 bit word groups	
0	0	0	0	ADC value of sample 0 (12 bits)					
0	0	0	1	ADC value of sample 1 (12 bits)					
0	n	n	N	-----					
0	1	1	1	ADC value of sample n (12 bits)					
1	ASIC ID (2 bits)		Channel ID (4 bits)		Error flags (1b)	Not Zero-suppression = 1 (1b)	0	Size(6 bits). Size of 16 bit word groups	
0	0	0	0	ADC value of sample 0 (12 bits)					
0	0	0	1	ADC value of sample 1 (12 bits)					
0	n	n	N	-----					
0	1	1	1	ADC value of sample n (12 bits)					

1	ASIC ID (2 bits)		Channel ID (4 bits)		Error flags (1b)	Not Zero-suppression = 1 (1b)	0	Size(6 bits). Size of 16 bit word groups	

0	0	0	0	ADC value of sample 0 (12 bits)
0	0	0	1	ADC value of sample 1 (12 bits)
0	n	n	N	-----
0	1	1	1	ADC value of sample n (12 bits)
CRC on above words				
MBZ(14 bits)			Timeout	Error

2 Command Input data format:

Word #	Byte 1								Byte 0								Type
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	DNC																UDP/PGP
1	DNC														MBZ		UDP/PGP
2	OC 00read 01write		DNC						Address MSB								UDP/PGP
3	Address LSW																UDP/PGP
4	Data MSW, write – actual word, read - 0																UDP/PGP
5	DATA LSW, write – actual word, read - 0																UDP/PGP
6	DNC																
7	DNC																

Table 1: Command input packet format

Formatted according to PGP requirements to deal with dual board usage (UDP and PGP)

3 Response output data format:

Word #	Byte 1								Byte 0								Type
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	0x7				Feedback command header word												UDP/PGP
1	Feedback command header word														MBZ		UDP/PGP
2	OC 00read 01write		0x0						Address MSB								UDP/PGP
3	Address LSW																UDP/PGP
4	Data MSW, write – feedback written word, read – actual read word																UDP/PGP
5	DATA LSW, – feedback written word, read – actual read word																UDP/PGP
6	MBZ														Timeout error	Other Error	UDP/PGP
7	MBZ																UDP/PGP

Table 2: Response output packet format

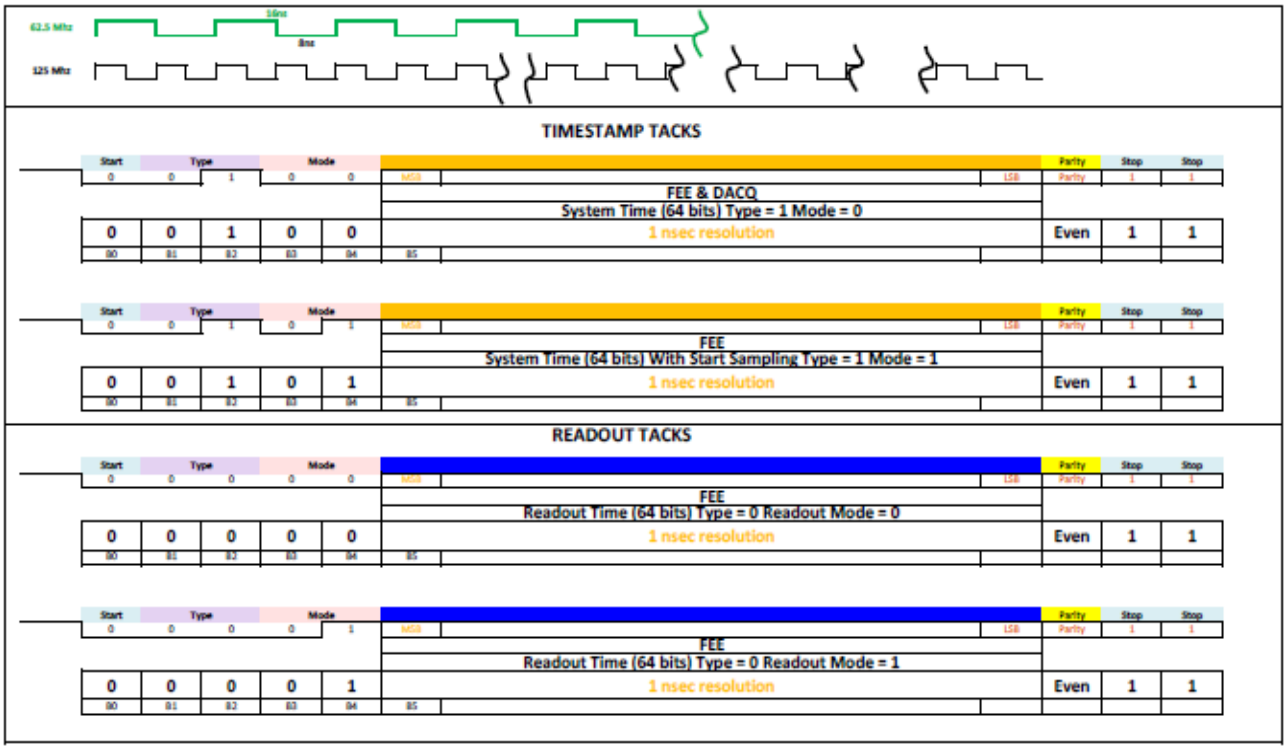
4 TACK command format:

Trigger command consist of 72 bits described in this table

#	Bits						
	0	1-2	3-4	5-68	69	70-71	Comments
	Start	Type	Mode	TACK command load	Even parity	Stop	
0	0	01	00	System Time (64 bits) Type = 1 Mode = 0. 1ns resolution Can be issued only once at the start of operation, set all timing to sync base. The 3 LSB must be 000, since camera module has only 8ns in time counter. Need to be verified by checking Enable bit 0, of register 0x17. Sync while module synced will not have effect on operation	X	11	SYNC
1	0	01	01	System Time (64 bits) Type = 1 Mode = 1. 1ns resolution Re-sync command, can be sent at any time with proper time load. The 3 LSB must be 000, since camera module has only 8ns in time counter. This is passive command, payload just compared with current time counter value and counted as good re-sync (register 0xF bits 31-16), or counted as error in register 0x10. Every issued re-sync need to be verified	X	11	RE_SYNC
2	0	01	10	Stop Sync command, Payload ignored. Need to be verified by checking Enable bit 0, of register 0x17. For follow-up sync, camera module need to be reset before new Sync attempted.	X	11	Stop Sync
3	0	01	11	TBD	X	11	Unused
4	0	00	00	System Time (64 bits) Type = 0 Mode = 0. 1ns resolution, indicate actual time of trigger, so camera module can calculate how far in time it needs to go to extract proper waveforms. It is set 0, and use related trigger delay time (Register 0x19, bits 31-18) and number of buffers to read (Register 0x19, bits 3-0)	X	11	TACK, set 0
5	0	00	01	System Time (64 bits) Type = 0 Mode = 1. 1ns resolution, indicate actual time of trigger, so camera module can calculate how far in time it needs to go to extract proper waveforms. It is set 1, and use related trigger delay time (Register 0x19, bits 13-0) and number of buffers to read (Register 0x19, bits 19-16)	X	11	TACK, set 1
6	0	00	10	Software trigger command. Will read data from buffer specified in register 0x1b, bits 8-0	X	11	Software forced trigger
1	0	10	XX	TBD	X	11	Unused
1	0	11	XX	TBD	X	11	Unused

Table 3: TACK packet format

From ICD to backplane



5 IP and MAC address specification:

Each camera module should have unique IP and MAC addresses. This address is extracted from unique and at first unknown serial ID from IC loaded on camera module. This serial ID reflected in registers 0x2 and 0x3. The following rules defined to build IP and MAC address:

IP address-> 192.168.0.[Bits 15:8 of low IP address at register 0x2]

MAC address-> Stanford_MAC_assignment(08:00:56):00:03:[Bits 15:8 of low IP address at register 0x2]

Camera module is using port number 8105

In addition to its specific IP, camera module will respond to its broadcast address: 192.168.0.255

By using this IP used can read register 0x2 and find actual IP and MAC address of camera module

After initial discovery sticker with proper IP will be attached to camera module for user convenience.

Warning: This method does not guaranty 100% uniqueness of IP address. Need to be seen if production run will meet this criteria.