Target 5 Register Map
7/23/2012

1 Memory Map:

1.1 Target 5 Memory Map

Registers:

1. Channel 0 Trigger configuration register
2. Channel 1 Trigger configuration register
3. Channel 2 Trigger configuration register
4. Channel 3 Trigger configuration register
5. Channel 4 Trigger configuration register
6. Channel 5 Trigger configuration register
7. Channel 6 Trigger configuration register
8. Channel 7 Trigger configuration register
9. Channel 8 Trigger configuration register
10. Channel 9 Trigger configuration register
11. Channel 20 Trigger configuration register
12. Channel 11 Trigger configuration register
13. Channel 12 Trigger configuration register
14. Channel 13 Trigger configuration register
15. Channel 14 Trigger configuration register
16. Channel 15 Trigger configuration register
17. ITbias, control supply bias for 5 voltages : TRGGbias, Vbias, TRGsumBias, TRGbias, Wbials
18. TRGGbias, control supply bias for the first preamp of the Trigger input
19. Vbias, control supply bias for the first preamp of the Data input
20. TRGsumBias, control supply bias for the second summing amp of the 4 Trigger inputs
21. TRGbias, control supply bias for the analog to digital conversion buffer
22. Wbials, control width of digital trigger output
23. TTbias, control supply bias for the 2 voltages related to the FOURTH group of four: PMTref4 and Thresh
24. PMTref4, reference voltage for summing amp supplied by TRGsumBias, FOURTH group
25. Thresh, reference voltage for activating digital one-shot, supplied by TRGbias, FOURTH group
26. TTbias, control supply bias for the 2 voltages related to the THIRD group of four: PMTref4 and Thresh
27. PMTref4, reference voltage for summing amp supplied by TRGsumBias, THIRD group
28. Thresh, reference voltage for activating digital one-shot, supplied by TRGbias, THIRD group
29. TTbias, control supply bias for the 2 voltages related to the SECOND group of four: PMTref4 and Thresh

30. PMTref4, reference voltage for summing amp supplied by TRGsumBias, SECOND group
31. Thresh, reference voltage for activating digital one-shot, supplied by TRGbias, SECOND group
32. TTbias, control supply bias for the 2 voltages related to the FIRST group of four: PMTref4 and Thresh
33. PMTref4, reference voltage for summing amp supplied by TRGsumBias, FIRST group
34. Thresh, reference voltage for activating digital one-shot, supplied by TRGbias, FIRST group
35. TTbias, control supply bias for the 2 voltages related to the Sum of 16 group of four: PMTref4 and Thresh
36. PMTref4, reference voltage for summing amp supplied by TRGsumBias, Sum of 16
37. Thresh, reference voltage for activating digital one-shot, supplied by TRGbias, Sum of 16
38. Sbuff, control supply bias for 2 voltages : SBbias and MonTRGthresh
39. SBbias, control supply bias for ramp bufer
40. MonTRGthresh, reference voltage (threshold) for digital trigger input. Since digital trigger will always have same amplitude, is not clear what is function of this register
41. WCbuff, control supply bias for 2 voltages : CMPbias and PUbias
42. CMPbias, control current through ramp comparator logic
43. PUbias, control load of pull-up of ramp comparator logic, and as result control relative voltage switch point
44. Random Bits (SGN, CloadP/N, MUX_SSX,MUX_RCO)
45. WAbuff, control supply bias for 2 voltages : VadjN and VadjP
46. VadjN, (old VdlyN) control delay on low to high transition of sampling delay circuit
47. VadjP, (old VdlyP) control delay on high to low transition of sampling delay circuit
48. DBbias, control supply bias for 2 voltages : Isel and Vdischarge
49. Isel, control current to ramp slope circuit
50. Vdischarge, control starting voltage of ramp
51. PRObuff, control supply bias for 1 voltages : Vdly
52. Vdly, control speed of Wilkinson ADC
53. Unused
54. Unused
55. Unused
56. Unused
57. Unused
58. Unused
59. Unused
60. Unused
61. Unused
62. Unused
63. Unused

64. Start digital trigger-in signal

To store data in preliminary buffer register Sin = 0 and PCLK pulse.

To store data in destination register Sin = 1 and PCLK pulse.

Channel 0(1,2,..15) Trigger configuration register: Address 0x0 (0x1, 0x2, .. 0x15)

Bits	Function	R/W	Default
11-9	Unused	RW	0
8	Select source of trigger output 0 – PMTref, 1- gain adjusted channel input	RW	0
7	Unused	RW	0
6	Select trigger gain. Nominal resistor 5K, when set to 1 and bits 2 and 4 set to 1, Nominal resistor 5K/4	RW	0
5	Unused	RW	0
4	Select trigger gain. Nominal resistor 5K, when set to 1 and bit 2 set to 1, Nominal resistor 5K/3	RW	0
3	Unused	RW	0
2	Select trigger gain. Nominal resistor 5K, when set to 1, Nominal resistor 5K/2	RW	0
1-0	Unused	RW	0

Figure 1: Channel 0(1,2,..15) Trigger configuration register: Address 0x0 (0x1, 0x2, .. 0x15)

ITbias, control supply bias: Address 0x10

Bits	Function	R/W	Default
11-0	DAC value, supply voltage for TRGGbias, Vbias, TRGsumBias, TRGbias, Wbials buffers	RW	0

Figure 2: ITbias, control supply bias, 0x10

TRGGbias, control supply bias: Address 0x11

Bits	Function	R/W	Default
11-0	DAC value, supply voltage for the first preamp of the Trigger input	RW	0

Figure 3: TRGGbias, control supply bias: Address 0x11

Vbias, control supply bias: Address 0x12

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for the first preamp of the Data input	RW	0

Figure 4: Vbias, control supply bias: Address 0x12

TRGsumBias, control supply bias: Address 0x13

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for the second summing amp of the 4	RW	0

	Trigger inputs		

Figure 5: TRGsumBias, control supply bias: Address 0x13

TRGbias, control supply bias: Address 0x14

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for the analog to digital conversion buffer	RW	0

Figure 6: TRGbias, control supply bias: Address 0x14

Wbials, control supply bias: Address 0x15

Bits	Function	R/W	Default
11-0	DAC value, control width of digital trigger output	RW	0

Figure 7: Wbials, control supply bias: Address 0x15

TTbias_3, control supply bias: Address 0x16

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 voltages related to the FOURTH group (channels12-15) of four: PMTref4 and Thresh	RW	0

Figure 8: TTbias_3, control supply bias, 0x16

PMTref4_3, control supply bias: Address 0x17

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TRGsumBias, FOURTH group (channels 12-15)	RW	0

Figure 9: PMTref4_3, control supply bias: Address 0x17

Thresh_3, control supply bias: Address 0x18

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TRGbias, FOURTH group(channels 12-15)	RW	0

Figure 10: Thresh_3, control supply bias: Address 0x18

TTbias_2, control supply bias: Address 0x19

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 voltages related to the THIRD group (channels8-11) of four: PMTref4 and Thresh	RW	0

Figure 11: TTbias_2, control supply bias, 0x19

PMTref4_2, control supply bias: Address 0x1A

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TRGsumBias, THIRD group (channels 8-11)	RW	0

Figure 12: PMTref4_2, control supply bias: Address 0x1A

Thresh_2, control supply bias: Address 0x1B

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TRGbias, THIRD group(channels 8-11)	RW	0

Figure 13: Thresh_2, control supply bias: Address 0x1B

TTbias_1, control supply bias: Address 0x1C

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 voltages related to the SECOND group (channels4-7) of four: PMTref4 and Thresh	RW	0

Figure 14: TTbias_1, control supply bias, 0x1C

PMTref4_1, control supply bias: Address 0x1D

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TRGsumBias, SECOND group (channels 4-7)	RW	0

Figure 15: PMTref4_1, control supply bias: Address 0x1D

Thresh_1, control supply bias: Address 0x1E

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TRGbias, SECOND group(channels 4-7)	RW	0

Figure 16: Thresh_1, control supply bias: Address 0x1E

TTbias_0, control supply bias: Address 0x1F

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 voltages related to the FIRST group (channels0-3) of four: PMTref4 and Thresh	RW	0

Figure 17: TTbias_0, control supply bias, 0x1F

PMTref4_0, control supply bias: Address 0x20

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TRGsumBias, FIRST group (channels 0-3)	RW	0

Figure 18: PMTref4_0, control supply bias: Address 0x20

Thresh_0, control supply bias: Address 0x21

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TRGbias, FIRST group(channels 0-3)	RW	0

Figure 19: Thresh_0, control supply bias: Address 0x21

TTbias_Summory, control supply bias: Address 0x22

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 voltages related to the sum of all 16 channels: PMTref4 and Thresh	RW	0

Figure 20: TTbias_Summory, control supply bias, 0x22

PMTref4_ Summory, control supply bias: Address 0x23

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TRGsumBias, sum of all 16 channels	RW	0

Figure 21: PMTref4_Summory, control supply bias: Address 0x23

Thresh_Summory, control supply bias: Address 0x24

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TRGbias, sum of all 16 channels	RW	0

Figure 22: Thresh_Summory, control supply bias: Address 0x24

Sbuff, control supply bias: Address 0x25

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 : SBbias and MonTRGthresh	RW	0

Figure 23: Sbuff, control supply bias: Address 0x25

SBbias, control supply bias: Address 0x26

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for ramp buffer	RW	0

Figure 24: SBbias, control supply bias: Address 0x26

MonTRGthresh, control supply bias: Address 0x27

Bits	Function	R/W	Default
11-0	DAC value reference voltage (threshold) for digital trigger input. Since digital trigger will always have same amplitude, is not clear what is function of this register	RW	0

Figure 25: MonTRGthresh, control supply bias: Address 0x27

WCbuff, control supply bias: Address 0x28

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 : CMPbias and PUbias	RW	0

Figure 26: WCbuff, control supply bias: Address 0x28

1. CMPbias, control supply bias: Address 0x29

Bits	Function	R/W	Default
11-0	DAC value, control current through ramp comparator logic	RW	0

Figure 27: CMPbias, control supply bias: Address 0x29

2. PUbias, control supply bias: Address 0x2a

Bits	Function	R/W	Default
11-0	DAC value, control load of pull-up of ramp comparator logic, and as result control relative voltage switch point	RW	0

Figure 28: PUbias, control supply bias: Address 0x2a

Random bit register: Address 0x2b

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select output between SST/SSP (0) and RCO(1)	RW	0
6	Unused	RW	0
5	Select output between SST and SSP , 0 – SST, 1 – SSP | 0 – SSP_RCO, 1 – SSt_RCO	RW	0
4	Unused	RW	0
3	Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 400MHz sampling	RW	0
2	Unused	RW	0
1	SGN bit, select sign bit of trigger edge, 0 – rising edge, 1 - falling	RW	0
0	Unused	RW	0

Figure 29: Random bit register: Address 0x2b

VAbuff, control supply bias: Address 0x2C

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 : VadjN and VadjP	RW	0

Figure 30: VAbuff, control supply bias: Address 0x2c

VadjN, control supply bias: Address 0x2D

Bits	Function	R/W	Default
11-0	DAC value, (old VdlyN) control delay on low to high transition of sampling delay circuit	RW	0

Figure 31: VadjN, control supply bias: Address 0x2D

VadjP, control supply bias: Address 0x2E

Bits	Function	R/W	Default
11-0	DAC value, (old VdlyP) control delay on high to low transition of	RW	0

	sampling delay circuit comparator logic, and as result control relative voltage switch point		

Figure 32: VadjP, control supply bias: Address 0x2E

DBbias, control supply bias: Address 0x2F

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 2 : : Isel and Vdischarge	RW	0

Figure 33: DBbias, control supply bias: Address 0x2F

Isel, control supply bias: Address 0x30

Bits	Function	R/W	Default
11-0	DAC value, control current to ramp slope circuit	RW	0

Figure 34: Isel, control supply bias: Address 0x30

Vdischarge, control supply bias: Address 0x31

Bits	Function	R/W	Default
11-0	DAC value, control starting voltage of ramp	RW	0

Figure 35: Vdischarge, control supply bias: Address 0x31

PRObuff, control supply bias: Address 0x32

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for 1 voltages : Vdly	RW	0

Figure 36: DBbias, control supply bias: Address 0x32

Vdly, control supply bias: Address 0x33

Bits	Function	R/W	Default
11-0	DAC value, control speed of Wilkinson ADC	RW	0

Figure 37: Vdly, control supply bias: Address 0x33

Unused, Address 0x34-0x3e

Bits	Function	R/W	Default
11-0	Unused	RW	0

Figure 38: Unused, Address 0x34-0x3e

Start digital trigger-in signal, control supply bias: Address 0x3f

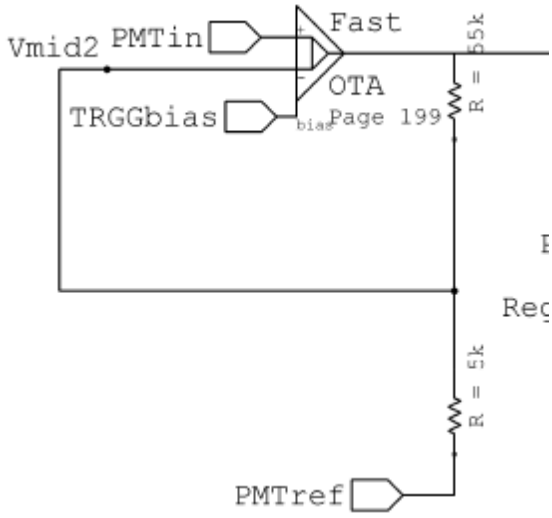
Bits	Function	R/W	Default
11-0	Unused, Only write to this register generate inter trigger signal	RW	0

Figure 39: Start digital trigger-in signal, control supply bias: Address 0x3f

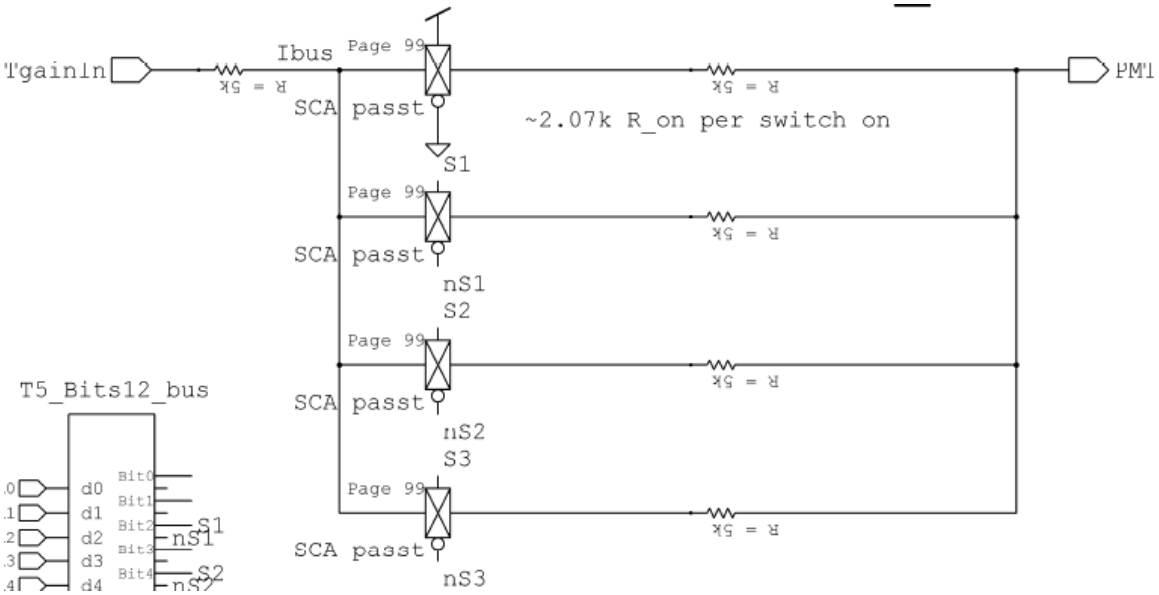
2 Trigger Gain Estimate:

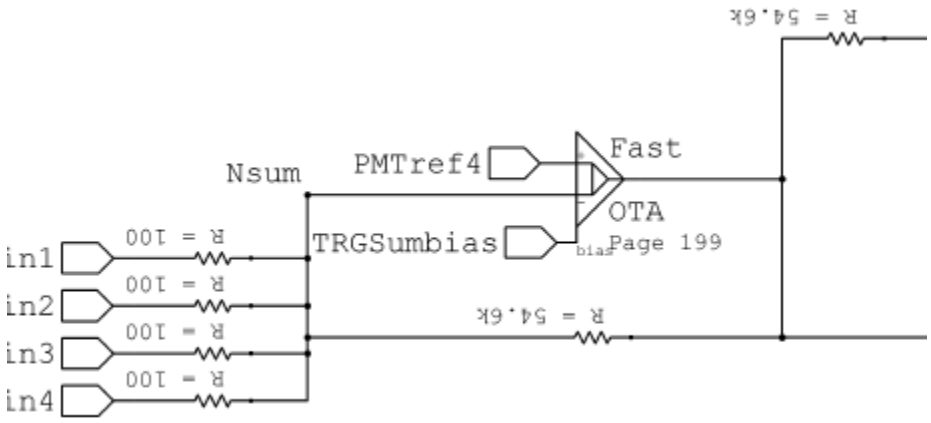
2.1 Gain Amp 0

V2=V+=Vin
V1= V-=VrefN
Rfb=55K, R1=5K
Vout0 = [(55+10)/10]Vin –(55/10) VrefN= 6.5Vin – 5.5VrefN
So, if VrefN = Vin, Vout0 = Vin
Or is we want Vout0=0, and Vin = 1.5V then VrefN = 1.772
dV = 0.010V => Vout0 = 0.069V



2.2 Gain Amp 1





V2=V+=Vref4
V1= V-= Vout0
Rfb =54.6K
R1 = 10K, or 7.5K, or 6.67K, or 6.25K (gain selection)
Vout = [(54.6+10)/10]Vref4 – (54.6/10)[Vout0_0 + Vout0_1 + Vout0_2 + Vout0_3]

Example:

I. Vin_1= Vin_2 = Vin_3 = Vin_0 = Vin=VrefN_0
Vout_1, Vout_2, Vout_3 = 0
Vout1 = 6.46Vref4 - 5.46*(4*Vin)
Assume Vout1 = 0 => Vref4 = 5V is not possible

II. Vin_1= Vin_2 = Vin_3 = Vin_0 = Vin = 1.5V, VrefN = 1.772 => Vout0 =0
And if Vref4 = 0, then Vout1 = 0
With dV on one channel Vout1 = 0 – 5.46*0.069 = 0.373V (if dV is negative transition.
With dV on all 4 channels Vout1 = 0 – 4*5.46*0.069 = 1.5V (if dV is negative transition)
For positive transition we need to set Vout to Maximum, or 2.5/6.46 = 0.387V.

3 Modification on Evaluation board:

1. TRGin was replaced by RCO. So RCO on pin 117
2. RCO was replaced by VdlyN. So VdlyN on pin 122
3. SSPout was replaced by VdlyP. So VdlyP on pin 124
4. RegClr on pin 38 exchanged with Shout on pin 99. So Shout now on pin 38, and RegClr on pin 99.

To run external VdlyP/N if required the following mods need to be done:

1. Disconnect Vped wire from TP29 and TP30
2. Connect TP29 to TP26 for VdlyN
3. Connect TP30 to TP23 for VdlyP
4. Add decupling caps
5. Change firmware to control external DAC for VdlyN and VdlyP
6. Disable output buffer by forcing output buffer bias on both signals to 0 at location 0x2C (VAbuff). Could enforced through firmware.