Target 7 Register Map
1/29/2014

1 Memory Map:

1.1 Target 5 Memory Map

Registers:

1. Channel 0 Trigger configuration register A
2. Channel 0 Trigger configuration register B
3. Channel 1 Trigger configuration register A
4. Channel 1 Trigger configuration register B
5. Channel 2 Trigger configuration register A
6. Channel 2 Trigger configuration register B
7. Channel 3 Trigger configuration register A
8. Channel 3 Trigger configuration register B
9. Channel 4 Trigger configuration register A
10. Channel 4 Trigger configuration register B
11. Channel 5 Trigger configuration register A
12. Channel 5 Trigger configuration register B
13. Channel 6 Trigger configuration register A
14. Channel 6 Trigger configuration register B
15. Channel 7 Trigger configuration register A
16. Channel 7 Trigger configuration register B
17. Channel 8 Trigger configuration register A
18. Channel 8 Trigger configuration register B
19. Channel 9 Trigger configuration register A
20. Channel 9 Trigger configuration register B
21. Channel 10 Trigger configuration register A
22. Channel 10 Trigger configuration register B
23. Channel 11 Trigger configuration register A
24. Channel 11 Trigger configuration register B
25. Channel 12 Trigger configuration register A
26. Channel 12 Trigger configuration register B
27. Channel 13 Trigger configuration register A
28. Channel 13 Trigger configuration register B
29. Channel 14 Trigger configuration register A
30. Channel 14 Trigger configuration register B
31. Channel 15 Trigger configuration register A
32. Channel 15 Trigger configuration register B

33. TTbias_0, control supply
34. PMTref4_0, reference voltage
35. Thresh_0, reference voltage
36. Wbias_0, reference voltage
37. TTbias_1, control supply
38. PMTref4_1, reference voltage
39. Thresh_1, reference voltage
40. Wbias_1, reference voltage
41. TTbias_2, control supply
42. PMTref4_2, reference voltage
43. Thresh_2, reference voltage
44. Wbias_2, reference voltage
45. TTbias_3, control supply
46. PMTref4_3, reference voltage
47. Thresh_3, reference voltage
48. Wbias_3, reference voltage
49. SBbias, ,control supply
50. Vdischarge, reference voltage
51. Isel, control ramp current
52. DBbias, control supply
53. Qbias
54. Vqbuff
55. VtrimT
56. Random bit register 0
57. VadjP
58. VAPbuff
59. VadjN
60. VANbuff
61. TRGsumbias
62. Vbias
63. TRGGbias
64. ITbias
65. SSP Leding Edge Timing bit register
66. SSP Trailing Edge Timing bit register
67. WR_ADDR_INC1 Leding Edge Timing bit register
68. WR_ADDR_INC1 Trailing Edge Timing bit register
69. WR_STRB1 Leding Edge Timing bit register

70. WR_ STRB1 Trailing Edge Timing bit register
71. WR_ADDR_INC2 Leding Edge Timing bit register
72. WR_ADDR_INC2 Trailing Edge Timing bit register
73. WR_STRB2 Leding Edge Timing bit register
74. WR_ STRB2 Trailing Edge Timing bit register
75. Random bit register 1
76. SST_FB Timing bit register
77. CMPbias
78. PUbias
79. CMPbias
80. Test Output register
81. 81 to 128 - unused

To store data in preliminary buffer register Sin = 0 and PCLK pulse.

To store data in destination register Sin = 1 and PCLK pulse.

Channel 0(1,2,..15) Trigger configuration register A: Address 0x0 (0x2, 0x4, .. 0x1e)

Bits	Function	R/W	Default
11-0	DAC value, reference voltage to control Vofs1 value of selected channel to compensate the first stage amplifier offset	RW	0

Figure 1: Channel 0(1,2,..15) Trigger configuration register A: Address 0x0 (0x2, 0x4, .. 0x1e)

Channel 0(1,2,..15) Trigger configuration register B: Address 0x1 (0x3, 0x5, .. 0x1f)

Bits	Function	R/W	Default
11-0	DAC value, reference voltage to control Vofs2 value of selected channel to compensate the second stage amplifier offset	RW	0

Figure 2: Channel 0(1,2,..15) Trigger configuration register B: Address 0x1 (0x3, 0x5, .. 0x1f)

TTbias_0, control supply bias: Address 0x20

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 3 voltages related to the FIRST group (channels0-3) of four: PMTref4, Thresh, and Wbias	RW	0

Figure 3: TTbias_0, control supply bias, 0x20

PMTref4_0, control supply bias: Address 0x21

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TTbias_0, FIRST group (channels 0-3)	RW	0

Figure 4: PMTref4_0, control supply bias: Address 0x21

Thresh_0, control supply bias: Address 0x22

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TTbias_0, FIRST group(channels 0-3)	RW	0

Figure 5: Thresh_0, control supply bias: Address 0x22

Wbias_0, control supply bias: Address 0x23

Bits	Function	R/W	Default
11-0	DAC value, control width of digital trigger output, supplied by TTbias_0, FIRST group(channels 0-3)	RW	0

Figure 6: Wbias_0, control supply bias: Address 0x23

TTbias_1, control supply bias: Address 0x24

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 3 voltages related to the Second group (channels4-7) of four: PMTref4, Thresh, and Wbias	RW	0

Figure 7: TTbias_1, control supply bias, 0x24

PMTref4_1, control supply bias: Address 0x25

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TTbias_1, Second group (channels4-7)	RW	0

Figure 8: PMTref4_1, control supply bias: Address 0x25

Thresh_1, control supply bias: Address 0x26

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TTbias_1, Second group (channels4-7)	RW	0

Figure 9: Thresh_1, control supply bias: Address 0x26

Wbias_1, control supply bias: Address 0x27

Bits	Function	R/W	Default
11-0	DAC value, control width of digital trigger output, supplied by TTbias_1, Second group (channels4-7)	RW	0

Figure 10: Wbias_1, control supply bias: Address 0x27

TTbias_2, control supply bias: Address 0x28

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 3 voltages related to the Third group (channels8-11) of four: PMTref4, Thresh, and Wbias	RW	0

Figure 11: TTbias_2, control supply bias, 0x28

PMTref4_2, control supply bias: Address 0x29

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TTbias_2, Third group (channels8-11)	RW	0

Figure 12: PMTref4_2, control supply bias: Address 0x29

Thresh_2, control supply bias: Address 0x2A

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TTbias_2, Third group (channels8-11)	RW	0

Figure 13: Thresh_2, control supply bias: Address 0x2A

Wbias_2, control supply bias: Address 0x2B

Bits	Function	R/W	Default
11-0	DAC value, control width of digital trigger output, supplied by TTbias_2, Third group (channels8-11)	RW	0

Figure 14: Wbias_2, control supply bias: Address 0x2B

TTbias_3, control supply bias: Address 0x2C

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 3 voltages related to the Fourth group (channels12-15) of four: PMTref4, Thresh, and Wbias	RW	0

Figure 15: TTbias_3, control supply bias, 0x2C

PMTref4_3, control supply bias: Address 0x2D

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for summing amp supplied by TTbias_3, Fourth group (channels12-15)	RW	0

Figure 16: PMTref4_3, control supply bias: Address 0x2D

Thresh_3, control supply bias: Address 0x2E

Bits	Function	R/W	Default
11-0	DAC value, reference voltage for activating digital one-shot, supplied by TTbias_3, Fourth group (channels12-15)	RW	0

Figure 17: Thresh_3, control supply bias: Address 0x2E

Wbias_3, control supply bias: Address 0x2F

Bits	Function	R/W	Default
11-0	DAC value, control width of digital trigger output, supplied by TTbias_3, Fourth group (channels12-15)	RW	0

Figure 18: Wbias_3, control supply bias: Address 0x2F

SBbias, control supply bias: Address 0x30

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for ramp buffer and all compactor biases CMPbias, CMPbias2 and PUbias, supplied by DBbias	RW	0

Figure 19: SBbias, control supply bias: Address 0x30

Vdischarge, control supply bias: Address 0x31

Bits	Function	R/W	Default
11-0	DAC value, control starting voltage of ramp, supplied by DBbias	RW	0

Figure 20: Vdischarge, control supply bias: Address 0x31

Isel, control supply bias: Address 0x32

Bits	Function	R/W	Default
11-0	DAC value, control current to ramp slope circuit, supplied by DBbias	RW	0

Figure 21: Isel, control supply bias: Address 0x32

DBbias, control supply bias: Address 0x33

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for the 3 : SBbias, Isel, and Vdischarge	RW	0

Figure 22: DBbias, control supply bias: Address 0x33

Qbias, control supply bias: Address 0x34

Bits	Function	R/W	Default
11-0	DAC value, control supply for charge pump of DLL, supplied by Vqbuff. Generate VadjN	RW	0

Figure 23: Qbias, control supply bias: Address 0x34

Vqbuff, control supply bias: Address 0x35

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for the 2 : Qbias and VtrimT. If external source of VadjN or external FB for VadjN source selected disable Vqbuff supply by setting to 0	RW	0

Figure 24: Vqbuff, control supply bias: Address 0x35

VtrimT, control supply bias: Address 0x36

Bits	Function	R/W	Default
11-0	DAC value, control N-side of buffer in SST_FB pass, supplied by Vqbuff	RW	0

Figure 25: VtrimT, control supply bias: Address 0x36

Random bit register 0: Address 0x37

Bits	Function	R/W	Default
11-10	Unused	RW	0
9- 4	Analog Mux Select bits (VS5-VS0): 000000 - Channel 0, Trigger Pass First Amp Output 000001 - Channel 0, Trigger Pass Second Amp Output 000010 - Channel 1, Trigger Pass First Amp Output 000011 - Channel 1, Trigger Pass Second Amp Output 000100 - Channel 2, Trigger Pass First Amp Output 000101 - Channel 2, Trigger Pass Second Amp Output 000110 - Channel 3, Trigger Pass First Amp Output 000111 - Channel 3, Trigger Pass Second Amp Output 001000 - Channel 4, Trigger Pass First Amp Output 001001 - Channel 4, Trigger Pass Second Amp Output 001010 - Channel 5, Trigger Pass First Amp Output 001011 - Channel 5, Trigger Pass Second Amp Output 001100 - Channel 6, Trigger Pass First Amp Output 001101 - Channel 6, Trigger Pass Second Amp Output 001110 - Channel 7, Trigger Pass First Amp Output 001111 - Channel 7, Trigger Pass Second Amp Output 010000 - Channel 8, Trigger Pass First Amp Output 010001 - Channel 8, Trigger Pass Second Amp Output 010010 - Channel 9, Trigger Pass First Amp Output 010011 - Channel 9, Trigger Pass Second Amp Output 010100 - Channel 10, Trigger Pass First Amp Output 010101 - Channel 10, Trigger Pass Second Amp Output 010110 - Channel 11, Trigger Pass First Amp Output 010111 - Channel 11, Trigger Pass Second Amp Output 011000 - Channel 12, Trigger Pass First Amp Output 011001 - Channel 12, Trigger Pass Second Amp Output 011010 - Channel 13, Trigger Pass First Amp Output 011011 - Channel 13, Trigger Pass Second Amp Output 011100 - Channel 14, Trigger Pass First Amp Output 011101 - Channel 14, Trigger Pass Second Amp Output 011110 - Channel 15, Trigger Pass First Amp Output 011111 - Channel 15, Trigger Pass Second Amp Output 100000 - Channel 0-3, Trigger Pass Summing Amp Output 100001 - Channel 4-7, Trigger Pass Summing Amp Output 100010 - Channel 8-11, Trigger Pass Summing Amp Output	RW	0

	100011 - Channel 12-15, Trigger Pass Summing Amp Output 100100 – 111111 - unused		
3-1	Unused	RW	0
0	SGN bit, select sign bit of trigger edge, 0 – rising edge, 1 - falling	RW	0

Figure 26: Random bit register 0: Address 0x37

VadjP, control supply bias: Address 0x38

Bits	Function	R/W	Default
11-0	DAC value, control delay on high to low transition of sampling delay circuit comparator logic, and as result control relative voltage switch point, Supplied by VAPbuff	RW	0

Figure 27: VadjP, control supply bias: Address 0x38

VAPbuff, control supply bias: Address 0x39

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for VadjP, If external source of VadjP selected disable VAPbuff supply by setting to 0	RW	0

Figure 28: VAPbuff, control supply bias: Address 0x39

VadjN, control supply bias: Address 0x3A

Bits	Function	R/W	Default
11-0	DAC value, control delay on low to high transition of sampling delay circuit, Supplied by VANbuff	RW	0

Figure 29: VadjN, control supply bias: Address 0x3A

VANbuff, control supply bias: Address 0x3B

Bits	Function	R/W	Default
11-0	DAC value, , control supply bias for VadjN, , If external source of VadjN or internal DLL source selected disable VANbuff supply by setting to 0	RW	0

Figure 30: VANbuff, control supply bias: Address 0x3B

TRGsumBias, control supply bias: Address 0x3C

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for the summing amp of the 4 Trigger inputs and for the monitoring buffer of the summing amp output of the 4 Trigger inputs, Supplied by ITbias	RW	0

Figure 31: TRGsumBias, control supply bias: Address 0x3C

Vbias, control supply bias: Address 0x3D

Bits	Function	R/W	Default
11-0	DAC value, control supply bias for the first preamp of the Data input,	RW	0

	Supplied by ITbias		

Figure 32: Vbias, control supply bias: Address 0x3D

TRGGbias, control supply bias: Address 0x3E

Bits	Function	R/W	Default
11-0	DAC value, supply voltage for the comparator between amplified signal and trigger threshold value, Supplied by ITbias	RW	0

Figure 33: TRGGbias, control supply bias: Address 0x3E

ITbias, control supply bias: Address 0x3F

Bits	Function	R/W	Default
11-0	DAC value, supply voltage for TRGGbias, Vbias, for TRGsumBias buffers	RW	0

Figure 34: ITbias, control supply bias, 0x3F

SSP Leading Edge Timing bit register: Address 0x40

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select leading rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 35: SSP Leading Edge Timing bit register: Address 0x40

SSP Trailing Edge Timing bit register: Address 0x41

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select Trailing rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 36: SSP Trailing Edge Timing bit register: Address 0x41

WR_ADDR_INCR1 Leading Edge Timing bit register: Address 0x42

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select leading rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 37: WR_ADDR_INCR1 Leading Edge Timing bit register: Address 0x42

WR_ADDR_INCR1 Trailing Edge Timing bit register: Address 0x43

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select Trailing rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 38: WR_ADDR_INCR1 Trailing Edge Timing bit register: Address 0x43

WR_STRB1 Leading Edge Timing bit register: Address 0x44

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select leading rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 39: WR_ STRB1 Leading Edge Timing bit register: Address 0x44

WR_ STRB1 Trailing Edge Timing bit register: Address 0x45

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select Trailing rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 40: WR_ STRB1 Trailing Edge Timing bit register: Address 0x45

WR_ADDR_INCR2 Leading Edge Timing bit register: Address 0x46

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select leading rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 41: WR_ADDR_INCR2 Leading Edge Timing bit register: Address 0x46

WR_ADDR_INCR2 Trailing Edge Timing bit register: Address 0x47

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select Trailing rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 42: WR_ADDR_INCR2 Trailing Edge Timing bit register: Address 0x47

WR_STRB2 Leading Edge Timing bit register: Address 0x48

Bits	Function	R/W	Default
11-8	Unused	RW	0

7	Select leading rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 43: WR_ STRB2 Leading Edge Timing bit register: Address 0x49

WR_ STRB2 Trailing Edge Timing bit register: Address 0x49

Bits	Function	R/W	Default
11-8	Unused	RW	0
7	Select Trailing rising edge (0) or falling edge(1)	RW	0
6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 44: WR_ STRB2 Trailing Edge Timing bit register: Address 0x49

Random bit register 1: Address 0x4a

Bits	Function	R/W	Default
11-8	Unused	RW	0
7- 4	Timing Mux Select bits (nSel3- nSel0): 0000 – SSPout 0001 – SSTout 0010 – SSToutFB 0011 – SSPin 0100 – Wr_Strb1 0101 – Wr1_Addr_Incr 0110 – Wr_Strb2 0111 – Wr2_Addr_Incr 1000 – 1111 – RCO	RW	0
3	nRipSST, Disable RCO generation (0) /enable 1	RW	0
2	Select additional load capacitor for sampling logic, 0 – 1GHz sampling, 1 – 500MHz sampling	RW	0

1-0	Unused	RW	0

Figure 1: Random bit register 1z: Address 0x4a

SST_FB Timing bit register: Address 0x4b

Bits	Function	R/W	Default
11-6	Unused	RW	0
5-0	Timing Mux Select bits (LE_nTS5- LE_nTS0): 000000 – minimum delay …….. 111111 – maximum delay	RW	0

Figure 45: SST_FB Timing bit register: Address 0x4b

CMPbias2, control supply bias: Address 0x4c

Bits	Function	R/W	Default
11-0	DAC value, control current through ramp comparator logic, Supplied by SBbias	RW	0

Figure 46: CMPbias2, control supply bias: Address 0x4c

PUbias, control supply bias: Address 0x4d

Bits	Function	R/W	Default
11-0	DAC value, control load of pull-up of ramp comparator logic, and as result control relative voltage switch point, Supplied by SBbias	RW	0

Figure 47: PUbias, control supply bias: Address 0x4d

CMPbias, control supply bias: Address 0x4e

Bits	Function	R/W	Default
11-0	DAC value, control current through ramp comparator logic, Supplied by SBbias	RW	0

Figure 48: CMPbias, control supply bias: Address 0x4e

Address 0x4f

Bits	Function	R/W	Default
11-0	Test output value, sent instead of data if select_any signal is 0	RW	0

Figure 49: Test Output register: Address 0x4f