Target 7 Camera Module interface write-up
10/16/2014

1 PURPOSE

This document describes the user interface for the Target 5 Camera Module with communication over Ethernet UDP protocol

2 SCOPE

This document gives an overview of the user interface of the Target 5 Camera Module

3 INTRODUCTION

Target 5 Camera Module is designed to communicate and control acquisitions in current version using standard 1Gbit Ethernet connection. It uses UDP protocol to send and receive packets. Also, for image data it can send packets (one packet per image pixel) with maximum size smaller then Jumbo packet.(No support for Jumbo packets required)

4 Requirements:

1. Support Processing Command/Image data from four Target 7 ASIC.
2. TBD.

5 Memory Map Demo Baord:

5.1 Master Board FPGA Memory Map

Registers:

0. FpgaVersion
1. Detector ID
2. Serial ID LSW
3. Serial ID MSW
4. Status register
5. Latched Status register
6. FIFO Status register ASIC0
7. Latched FIFO Status register ASIC 0
8. FIFO Status register ASIC1
9. Latched FIFO Status register ASIC 1
10. FIFO Status register ASIC2
11. Latched FIFO Status register ASIC 2
12. FIFO Status register ASIC3
13. Latched FIFO Status register ASIC 3
14. Trigger FIFO Status register
15. Trigger statistics
16. TACK statistic
17. FIFO statistics
18. Packet statistics
19. Command/Ramp count statistics
20. Time Adjust register
21. ADC_config_reg (For MAX1230 ADC measuring current)
22. Time register
23. Control register 0
24. Control register 1
25. Trigger control register 0
26. Trigger control register 1
27. Row/Column control/status

28. Number of samples to read
29. Monitor control register (For internal ADC measuring Target voltages)
30. Configuration waveform register
31. ADC MAX11611 control register (For MAX11616 to measure HV cur/volt and spare)
32. HV control
33. Peltier uC control
34. Peltier uC data to uC
35. Peltier uC data from uC
36. Flash memory write
37. Flash memory control
38. Flash memory read
39. Zero suppression config
40. Monitor results register
41. MAX11616 ADC 0 Data (Temperature)
42. MAX11616 ADC 1 Data (HV Current/Voltage)
43. MAX11616 ADC 2 Data (spare)
44. MAX11616 ADC 3 Data (spare)
45. MAX11616 ADC 4 Data (spare)
46. MAX11616 ADC 5 Data (spare)
47. MAX11616 ADC 6 Data (spare)
48. VPED DAC control ASIC
49. TACK simulator LSW
50. TACK simulator MSW
51. TACK simulator Special word
52. MAX1230 ADC 0 Data (Temperature)
53. MAX1230 ADC 1 Data (Currents n and n+32)
54. MAX1230 ADC 2 Data (Currents n and n+32)
55. MAX1230 ADC 3 Data (Currents n and n+32)
56. MAX1230 ADC 4 Data (Currents n and n+32)
57. MAX1230 ADC 5 Data (Currents n and n+32)
58. MAX1230 ADC 6 Data (Currents n and n+32)
59. MAX1230 ADC 7 Data (Currents n and n+32)
60. MAX1230 ADC 8 Data (Currents n and n+32)
61. MAX1230 ADC 9 Data (Currents n and n+32)
62. MAX1230 ADC 10 Data (Currents n and n+32)
63. MAX1230 ADC 11 Data (Currents n and n+32)
64. MAX1230 ADC 12 Data (Currents n and n+32)
65. MAX1230 ADC 13 Data (Currents n and n+32)
66. MAX1230 ADC 14 Data (Currents n and n+32)
67. MAX1230 ADC 15 Data (Currents n and n+32)
68. MAX1230 ADC 16 Data (Currents n and n+32)
69. MAX1230 ADC 17 Data Data (Temperature)
70. MAX1230 ADC 18 Data (Currents n and n+32)
71. MAX1230 ADC 19 Data (Currents n and n+32)
72. MAX1230 ADC 20 Data (Currents n and n+32)
73. MAX1230 ADC 21 Data (Currents n and n+32)
74. MAX1230 ADC 22 Data (Currents n and n+32)
75. MAX1230 ADC 23 Data (Currents n and n+32)
76. MAX1230 ADC 24 Data (Currents n and n+32)
77. MAX1230 ADC 25 Data (Currents n and n+32)
78. MAX1230 ADC 26 Data (Currents n and n+32)
79. MAX1230 ADC 27 Data (Currents n and n+32)
80. MAX1230 ADC 28 Data (Currents n and n+32)
81. MAX1230 ADC 29 Data (Currents n and n+32)
82. MAX1230 ADC 30 Data (Currents n and n+32)
83. MAX1230 ADC 31 Data (Currents n and n+32)

84. MAX1230 ADC 32 Data (Currents n and n+32)
85. MAX1230 ADC 33 Data (Currents n and n+32)
86. Trigger Efficiency Cntl 0
87. Trigger Efficiency Cntl 1
88. Trigger Efficiency Input Cntr
89. Trigger Efficiency Cntr
90. Software reset register
91. Channel enable register 0
92. Channel enable register 1
93. Trigger statistic 1
94. Special feature register
95. Dead-time control (unused)
96. Write Target register
97. Read 0 Target register
98. Read 1 Target register

FPGA version: Address 0x0

Bits	Function	R/W	Default
31-0	Assigned value of 0xFED700001, assigned in Firmware to highlight and track incremental changes in firmware. Incremented with every firmware revision	R	0

Figure 1: FPGA Version: Address 0x0

Detector ID: Address 0x1

Bits	Function	R/W	Default
31-16	Any value for control software, does not have effect on any FPGA logic	RW	0
15-8	Detector ID, fill Detector ID field of reported event	RW	0
7-0	CTA ID, fill CTA ID field of reported event	RW	0

Figure 2: Scratch pad: Address 0x1

Serial number LSW: Address 0x2

Bits	Function	R/W	Default
31-0	Serial number the least significant word	R	0

Figure 3: Serial number LSW: Address 0x2

Serial number MSW: Address 0x3

Bits	Function	R/W	Default
31-0	Serial number the most significant word	R	0

Figure 4 : Serial number MSW: Address 0x3

Status register: Address 0x4

Bits	Function	R/W	Default

31-28	Status of backplane lines from bp4 to bp7 (also, bp5 is reset and will not be available due to board reset)	R	0
27-22	Unused, always 0	R	0
21	Underflow on summary FIFO of event data	R	0
20	overflow on summary FIFO of event data	R	0
19	State of event Done bit ASIC 3	R	0
18	State of event Done bit ASIC 2	R	0
17	State of event Done bit ASIC 1	R	0
16	State of event Done bit ASIC 0	R	0
15-14	Unused	R	0
13	mgt_AVTT_OK is OK, 1- OK, 0 – is not	R	0
12	mgt_AVCC_OK is OK, 1- OK, 0 – is not	R	0
11	mgt_AVCC_OK is OK, 1- OK, 0 – is not	R	0
10	+1_8V is OK, 1- OK, 0 – is not	R	0
9	+5_2V for Peltier and Preamp OK, 1- OK, 0 – is not	R	0
8	OT (Over-Temperature alarm) from FPGA monitoring, see FPGA monitoring section	R	0
7	EOS from FPGA monitoring, This signal transitions to active High when the measurement data from the last channel in an automatic channel sequence is written to the status registers,see FPGA monitoring section	R	0
6	EOC from FPGA monitoring, This signal transitions to an active High at the end of an ADC conversion when the measurement is written to the status registers, see FPGA monitoring section	R	0
5	DRDYfrom FPGA monitoring, see FPGA monitoring section	R	0
4	BUSY from FPGA monitoring, ADC busy signal. This signal transitions High during an ADC conversion. This signal also transitions High for an extended period during an ADC or sensor calibration,.see FPGA monitoring section	R	0
3	USER_TEMP_ALARM_OUTfrom FPGA monitoring, see FPGA monitoring section(Vccbram)	R	0
2	USER_TEMP_ALARM_OUTfrom FPGA monitoring, see FPGA monitoring section(Vccaux)	R	0
1	VCCINT_ALARM_OUT from FPGA monitoring, see FPGA monitoring section(Vccint)	R	0
0	VCCAUX_ALARM_OUT from FPGA monitoring, see FPGA monitoring section (temperature)	R	0

Figure 5: Status register: Address 0x4

Latched Status register: Addressw 0x5

Bits	Function	R/W	Default
31-28	Status of backplane lines from bp4 to bp7 (also, bp5 is reset and will not be available due to board reset)	RW*	0

27-22	Unused, always 0	RW*	0
21	Underflow on summary FIFO of event data	RW*	0
20	overflow on summary FIFO of event data	RW*	0
19	State of event Done bit ASIC 3	RW*	0
18	State of event Done bit ASIC 2	RW*	0
17	State of event Done bit ASIC 1	RW*	0
16	State of event Done bit ASIC 0	RW*	0
15-14	Unused	RW*	0
13	mgt_AVTT_OK is OK, 1- OK, 0 – is not	RW*	0
12	mgt_AVCC_OK is OK, 1- OK, 0 – is not	RW*	0
11	mgt_AVCC_OK is OK, 1- OK, 0 – is not	RW*	0
10	+1_8V is OK, 1- OK, 0 – is not	RW*	0
9	+5_2V for Peltier and Preamp OK, 1- OK, 0 – is not	RW*	0
8	OT (Over-Temperature alarm) from FPGA monitoring, see FPGA monitoring section	RW*	0
7	EOS from FPGA monitoring, This signal transitions to active High when the measurement data from the last channel in an automatic channel sequence is written to the status registers,see FPGA monitoring section	RW*	0
6	EOC from FPGA monitoring, This signal transitions to an active High at the end of an ADC conversion when the measurement is written to the status registers, see FPGA monitoring section	RW*	0
5	DRDYfrom FPGA monitoring, see FPGA monitoring section	RW*	0
4	BUSY from FPGA monitoring, ADC busy signal. This signal transitions High during an ADC conversion. This signal also transitions High for an extended period during an ADC or sensor calibration,.see FPGA monitoring section	RW*	0
3	USER_TEMP_ALARM_OUTfrom FPGA monitoring, see FPGA monitoring section(Vccbram)	RW*	0
2	USER_TEMP_ALARM_OUTfrom FPGA monitoring, see FPGA monitoring section(Vccaux)	RW*	0
1	VCCINT_ALARM_OUT from FPGA monitoring, see FPGA monitoring section(Vccint)	RW*	0
0	VCCAUX_ALARM_OUT from FPGA monitoring, see FPGA monitoring section (temperature)	RW*	0

Figure 6: Latched Status register: Address 0x5

* - Writing one will reset corresponding bit

FIFO Status register: Address 0x6

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 7: FIFO Status register: Address 0x6

Latched FIFO Status register: Address 0x7

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 8: Latched FIFO Status register: Address 0x7

* - Writing one will reset corresponding bit

FIFO Status register ASIC 1: Address 0x8

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 9: FIFO Status register ASIC 1: Address 0x8

Latched FIFO Status register ASIC 1: Address 0x9

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 10: Latched FIFO Status register ASIC 1: Address 0x9

* - Writing one will reset corresponding bit

FIFO Status register ASIC 2: Address 0xa

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 11: FIFO Status register ASIC 2: Address 0xa

Latched FIFO Status register ASIC 2: Address 0xb

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 12: Latched FIFO Status register ASIC 2: Address 0xb

* - Writing one will reset corresponding bit

FIFO Status register ASIC 3: Address 0xc

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	R	0

Figure 13: FIFO Status register ASIC 3: Address 0xc

Latched FIFO Status register ASIC 3: Address 0xd

Bits	Function	R/W	Default
31-0	Data Storage FIFO underflow(bits 1,3,5,7,..) and overflow (0,2,4,..) errors. Two bits per acquisition channel. Channel 0 errors reported in bits 0(underflow) and 1(overflow), channel 1 in bits 2 and 3,….	RW*	0

Figure 14: Latched FIFO Status register ASIC 3: Address 0xd

* - Writing one will reset corresponding bit

Trigger FIFO Status register: Address 0xe

Bits	Function	R/W	Default
31-0	Free running time counter value set by sync over TACK pass 32 MSB	R	0

Figure 15: Trigger FIFO Status register: Address 0xe

* - Writing one will reset corresponding bit

Trigger statistics: Address 0xf

Bits	Function	R/W	Default
31-16	Count number of good Sync verification TACKs.	RW*	0
15-0	Count number of TACKs received	RW*	0

Figure 16: Trigger statistics: Address 0xf

* Writing any value into this register will reset all counters in registers 0xF, 0x10, 0x11, 0x12 and some on 0x13

Tack statistics: Address 0x10

Bits	Function	R/W	Default
31-24	Count sync errors. Time sync verification failed. Counter is reset by writing any value into register 0xF	R	0
23-16	Count of range error over Tack. Counter is reset by writing any value into register 0xF	R	0
15-8	Same as count in bits 7-0. Count Tack Parity errors	R	0
7-0	Count Tack Parity errors. Counter is reset by writing any value into	R	0

	register 0xF		

Figure 17: Tack statistics: Address 0x10

FIFO statistics: Address 0x11

Bits	Function	R/W	Default
31-16	Count all enabled for counting (bits 0 of register 0x30) built packets on all incoming channels. Counter is reset by writing any value into register 0xF	R	0
15-0	Count all built packets on all incoming channels. Counter is reset by writing any value into register 0xF	R	0

Figure 18: FIFO statistics: Address 0x11

Packet statistics: Address 0x12

Bits	Function	R/W	Default
31-16	Copy of bits 15-0, Counter is reset by writing any value into register 0xF	R	0
15-0	MAC Counter, count all transmitted packet by MAC. Counter is reset by writing any value into register 0xF	R	0

Figure 19: Packet statistics: Address 0x12

Ramp count statistics: Address 0x13

Bits	Function	R/W	Default
31-16	Count command issued to Camera module. Counter is reset by writing any value into register 0xF	R	0
15-0	Count number of event processed. Counter is reset by writing value of 1 into bit 30 of register 0x1a	R	0

Figure 20: Ramp count statistics: Address 0x13

Time Adjust register: Address 0x14

Bits	Function	R/W	Default
31	Start time base writing 1 to this bit will start and restart time base. Time base always start from 0	RW	0
30-16	To correct TACK for proper time by taking in to account propagation and decision making (1 ns steps)	RW	0
15-8	Unused	RW	0
7-0	Time offset register, specify amount of clock cycles to adjust timebase between tester and camera module to start simultaneously (8 ns steps)	RW	0

Figure 21: Time Adjust register: Address 0x14

ADC configuration Register: Address 0x15

Bits	Function	R/W	Default
31	ADC start (1), non sticky, will start/restart reconfiguration and conversion	RW	0
30	ADC stop, will stop ADC update	RW	0
29-20	Unused	R	0
11-8	Select set of ADC enables, one bit per ADC (bit 4 – ADC 8 for ASIC 0, bit 9 – ADC 1 for ASIC 1, …, bit 11 – ADC 3 for ASIC 3	RW	0
7-5	ADC 0 logic, Select averaging and number of averages http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf 0xx – perform one conversion for each result 100 - perform four conversions and return average for each result 101 - perform eight conversions and return average for each result 110 - perform 16 conversions and return average for each result 111 - perform 32 conversions and return average for each result	RW	0
4-1	ADC 0 logic, Channel select bits, Set to b1111 to read all 16 channels http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf **Must be set to b1111**	RW	0
0	ADC 0 logic, Select scan mode, bit 0 of scan bits http://datasheets.maxim-ic.com/en/ds/MAX1227-MAX1231.pdf 0- Select readout of channels from 0 through N, 1- from N to highest numbered channel. **Must be set to 0**	RW	0

Figure 22: ADC configuration Register: Address 0x15

Time register: Address 0x16

Bits	Function	R/W	Default
31-0	Free running time counter value set by sync over TACK pass 32 LSB	R	0

Figure 23: Time register: Address 0x16

Control register 0: Address 0x17

Bits	Function	R/W	Default
31	Enable packet count in register 0x10, bits 31-16	RW	0
30-24	Maximum Ethernet packet size parameter. Indicate how many channels out of available 64 can be shipped in one packet. Value of 0 and 1 indicate one channel per network packet, 2 – channels per packet, and … Careful attention need to be taken to set this parameter. First of all user need to know type of network card host system will have and if it support Jumbo packets. In any case maximum size of acceptable network packet need to be compared with expected event size and properly divided into packets. Default value of 0 (or 1) always process just one channel per packet and works in all cases but will generate maximum number of packets (64). This parameter help	RW	0

	to reduce number of packets and related overhead for packet header and trailer to optimize system performance.		
23	Select options when buffer never incremented, stay same as start one	RW	0
22	Special mode for sr_clk. 0 – sr_clk run continuously, 1 – sr_clk run when only needed	RW	0
21	Select if SR_SEL pulse signal asserted all time (1) or only actual event readout process	RW	0
20-8	Specify ramp signal duration to Target	RW	0
7-3	Ramp start delay after trigger, in system clocks (8 ns)	RW	0
2	Offset usage enable (1). In order to optimize 48 samples readout relatively to trigger position, logic implement option to sync readout to 8 sample bins (4 bins per buffer). Setting bit to one will enable this feature. Otherwise buffer readout always start from beginning. Should be noted that that setting number of readout buffer to more then 2(Bits 23-20) will disable offset usage. And for software buffer this feature disabled as well (bit 9 of 0x1b)	RW	0
1	Unused	RW	0
0	Enable bit, 1- enable analog sampling, after proper Sync command issued	R	0

Figure 24: Control register 0: Address 0x17

Control register 1: Address 0x18

Bits	Function	R/W	Default
31-27	Unused, Spare control bits	RW	0
27-24	Select phase of clock to sample event data from ASICs, 1 per ASIC (0 – rising edge, 1 - falling edge) ASIC0 – bit 24, ASIC1 – bit 25, …, ASIC3 – bit 27	RW	0
23-22	Select Wilkinson clock frequency divided by 2: 00 – 104MHz 01 – 62.5MHZ 10 – 250MHz 11 – 250MHz	R/W	0
21	Select buffer enable logic. With current sampling timing this bit need to be set to 1. All odd buffers will get incremented earlier and as result special counting as increment by 3 and decrement by 1 need to be used (Set to 1)	R/W	0
20	Select if done signal is used to speed up conversion (1 – done is enabled)	R/W	0
19	Unused	R/W	0
18	Enable 2.7V distribution to Peltier Controller Aux board, 1- on, 0 – off	RW	0
17	Enable 5.2V distribution to Aux board, 1- on, 0 – off	RW	0
16	HV enable signal, 1- switch on distribution to FE, 0 disabled If overcurrent is detected, check voltage on MAX11616 ADC, to see if it still distributing to FE, otherwise, toggle bit to enable voltage again	RW	0

15-14	Unused, Spare control bits to Target ASIC 3	RW	0
13	Directly control clr_reg input to Target ASIC 3	RW	0
12	Power up ASIC 3 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0
11-10	Unused, Spare control bits to Target ASIC 2	RW	0
9	Directly control clr_reg input to Target ASIC 2	RW	0
8	Power up ASIC 2 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0
7-6	Unused, Spare control bits to Target ASIC 1	RW	0
5	Directly control clr_reg input to Target ASIC 1	RW	0
4	Power up ASIC 1 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0
3-2	Unused, Spare control bits to Target ASIC 0	RW	0
1	Directly control clr_reg input to Target ASIC 0	RW	0
0	Power up ASIC 0 bit. (0 –turn off 2.5V to ASIC, 1 - turn on 2.5V to ASIC)	RW	0

Figure 25: Control register 1: Address 0x18

Trigger control register 0: Address 0x19

Bits	Function	R/W	Default
31-18	Trigger delay, to compensate for time between trigger arrival and trigger decision making, need to be found experimentally. Count in 1ns steps	RW	0
17-14	Unused	RW	0
13-0	Trigger delay alternative, to compensate for time between trigger arrival and trigger decision making, need to be found experimentally. Count in 1ns steps	RW	0

Figure 26: Trigger control register 0: Address 0x19

Trigger control register 1: Address 0x1a

Bits	Function	R/W	Default
31	Unused -Software trigger, non sticky bit, need to be set to one to initiate software trigger, does not require to set to 0 to generate next trigger	RW	0
30	Trigger counter reset,	RW	0
29-26	Unused	RW	0
25-8	Enable trigger input contribution to trigger counter(register 0xF bits 31-16). Bits assigned as followed: 3-0 – Target ASIC 0 trigger bits, 7-4 – Target ASIC 1 trigger bits, 11-8 – Target ASIC 3 trigger bits, 15-12 – Target ASIC 3 trigger bits,16 – external hardware trigger, 17 – software trigger	RW	0
7-1	Unused	RW	0
0	Select phase of clock to sample TACK from BP (0 – rising edge, 1 - falling edge)	RW	0

Figure 27: Trigger control register 1: Address 0x1a

Row/Column control/status: Address 0x1b

Bits	Function	R/W	Default
31-29	Latched by latest trigger value of row counter	R	0
28-23	Latched by latest trigger value of column counter	R	0
22-19	Latched by latest trigger value of sample value (only 4 MSB)	R	0
18-16	Free running current row value to simulate sampling buffer write row pointer	R	0
15-10	Free running current column value to simulate sampling buffer write column pointer	R	0
9	Unused	RW	0
8-3	Specify column for readout when trigger received and activated by TACK Mode = "10" OR "11"	RW	0
2-0	Specify row for readout when trigger received and activated by TACK Mode = "10" OR "11"	RW	0

Figure 28: Row/Column control/status: Address 0x1b

Number of samples to read: Address 0x1c

Bits	Function	R/W	Default
31-20	Unused	R	0
19-16	Specify number of alternative buffer for readout, with 0 corresponding to 1 buffers With 1- 2 buffers With 13 and more15- 14 buffers (maximum)	RW	0
15-9	Unused	R	0
8-4	Number of samples on partial buffer, from 0 to 31, to enable flexible readout of any number of desirable samples. At the moment value of 1 -> 16 samples, 0 – 0 samples. Optimized for 48 sample event	RW	0
3-0	Specify number of buffer for readout, with 0 corresponding to 1 buffers With 1- 2 buffers With 15- 16 buffers (maximum)	RW	0

Figure 29: Number of samples to read: Address 0x1c

Monitor control register: Address 0x1D

Bits	Function	R/W	Default
31	Data write for FPGA monitoring interface, DWE on page 14 of http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf	RW	0
30-28	Unused	R	0
27-23	Unused	RW	0
22-16	Data address for FPGA monitoring interface, DADDR on page 14 of	RW	0

	http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf		
15-0	Input data for FPGA monitoring interface, DI on page 14 of http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf	RW	0

Figure 30: Monitor control register: Address 0x1D

Configuration waveform register: Address 0x1e

Bits	Function	R/W	Default
31-24	PCLK width plus 1 when SIN high, need to be set to 0x3	RW	3
23-16	SIN settling time after PCLK plus 1, need to set to 1	RW	1
15-8	SIN settling time before PCLK plus 1, need to set to 1	RW	1
7-0	PCLK width plus 1 when SIN low, need to be set to 0x7	RW	7

Figure 31: Configuration waveform register: Address 0x1e

ADC11616 control register: Address 0x1f

Bits	Function	R/W	Default
31	Setting to 1 will start ADC readout, non-sticky bit	R	0
30-17	Unused	R	0
16	Stop bit, to change configuration operation needs to be stopped and restarted again	RW	0
15-8	Setup byte for MAX11616, see configuration/setup bytes definitions, default 0xd2 http://datasheets.maximintegrated.com/en/ds/MAX11612-MAX11617.pdf (Table 1)	RW	0
7-0	Configuration byte for MAX11616, see configuration/setup bytes definitions, default 0x17 http://datasheets.maximintegrated.com/en/ds/MAX11612-MAX11617.pdf (Table 2)	RW	0

Figure 32: ADC11616 control register: Address 0x1f

HV control: Address 0x20

Bits	Function	R/W	Default
31-12	HV low side 0 to XX V. Direct Write to configuration space of MAX5715.	RW	0
11	Load Low voltage side DAC, need to be set to 1	RW	0
10-4	Unused	RW	0
3-0	Select DAC used for control operation 1 –enable control, 0 disable , Bit 0 for DAC 0 (ASIC 0), Bit 1 for DAC 1 (ASIC 1),.., Bit 3 for DAC 3 (ASIC 3)	RW	0

Figure 33: HV control: Address 0x20

To set MAX5715 need to do the following steps:

1. Write value of 0x71000c00 enable internal 2.5V reference (or 0x73000c00 for 4.096 ref)
2. Write value of 0x82800c00 load value of 1.25V(or 2.0V with 4.096 ref)
3. Optional to adjust termination 0x430f0c00

Peltier uC control: Address 0x21

Bits	Function	R/W	Default
31	Done bit. If mode bit (bit 1) set to 0 indicate completion of individual write operation, in programming mode (bit 1 set to 1), this bit indicate that programming to uC is enabled and can be followed with uC programming commands	RW	0
30-16	Unused	RW	0
15-8	Define clock period. Which will be equal Value * 256 (ns). For programming the blank device this value need to be set to 0x20 For normal operation in is function of many configuration parameters of actual code running on uC	RW	0
7-3	Unused	RW	0
2	Complement reset bit (invert) . In normal mode reset needs to be at high level (5v), so asserting this bit will assert reset (0V). And in programming mode reset needs to 0V (asserted), and this bit set to 1 will deassert reset (5v)	RW	0
1	Mode bit (0) normal operation, (1) programming mode. By setting this bit to 1 before bit 0 is set to 1, enable execution or programming enable instruction to uC. See http://www.atmel.com/Images/Atmel-8271-8-bit-AVR-Microcontroller-ATmega48A-48PA-88A-88PA-168A-168PA-328-328P_datasheet.pdf Page 300-301 for details	RW	0
0	Enable start of communication over SPI, 1 – start of operation. Need to be 1 for both programming and normal mode for SPI to work	RW	0

Figure 34: Peltier uC control: Address 0x21

Peltier uC data to uC: Address 0x22

Bits	Function	R/W	Default
31-0	32 bit value which need to be written to uC, Function of write to this registaer depend on normal or programming mode. Programming mode defined on page 301 of http://www.atmel.com/Images/Atmel-8271-8-bit-AVR-Microcontroller-ATmega48A-48PA-88A-88PA-168A-168PA-328-328P_datasheet.pdf For normal mode details of protocol will be specified by uC firmware implementer.	RW	0

Figure 35: Peltier uC data to uC: Address 0x22

Peltier uC data from uC: Address 0x23

Bits	Function	R/W	Default
31-0	Data captured from uC as response to communication to uC.	RW	0

	Again, programming mode defined on page 301 of http://www.atmel.com/Images/Atmel-8271-8-bit-AVR-Microcontroller-ATmega48A-48PA-88A-88PA-168A-168PA-328-328P_datasheet.pdf Normal is up to implementation		

Figure 36: Peltier uC data from uC: Address 0x23

Instruction on how to set programming mode:

1. Write value of 0x2002 into register 0x2f
2. Write value of 0x2003 into register 0x2f
3. Read both registers 0x2f, it should have value of 0x80002003 and register 0x31 with value of 0x5300. If both is true programing got enable, and other programming command can be issued
4. Now it is up to user to deal with programming
5. Example I did just to understand interface
    - Wrote 0x30 = 0x500000ab (0xab is just random selection, can be anything)
    - Read 0x31 -> 0xab500062
    - Wrote 0x30 = 0xaca00022 (to enable internal clock output on pin 12)
    - Read 0x31 -> 0xabac0000
    - Wrote 0x30 = 0x500000ab (0xab is just random selection, can be anything)
    - Read 0x31 -> 0xab500022
    - Write 0x2f = 0x2007 (to remove reset signal) as recommended by uC manual
    - Power cycled and observed clock on pin 12

To write Bootloader to flash memory the following steps need to take:

1. Write value of 0x2002 into register 0x2f
2. Write value of 0x2003 into register 0x2f
3. Read both registers 0x2f, it should have value of 0x80002003 and register 0x31 with value of 0x5300. If both is true programing got enable, and other programming command can be issued
4. Flash Memory divided into pages (64 16bits words, 256 pages), Flash section start depend on Bootsz1/0 bits. With current selection "11" it start at location of 0x3f00 (Register Extended Fuse, bits 2-1). Also in hex file it is byte addressing so we need to convert from byte addressing to word addressing by dividing by 2 and round down.
5. There are command for lower byte and higher byte in the word. Order load lower byte and then higher byte
6. Wrote 0x30 = 0x40000085 Load lower byte, and 0x30 = 0x480000E0
7. …. Write full page (64 16-bit words)
8. Store page by write page command 0x30 = 0x4c3f0000
9. Write 0x2f = 0x2007 (to remove reset signal) as recommended by uC manual
10. Power cycle and verify writing by reading locations
    0x203f0000
    0x283f0000

Flash memory write: Address 0x24

Bits	Function	R/W	Default
31	Write to this bit (1) start operation of writing to flash command intermediate storage	RW	0
30-27	Unused	R	0
26	MSB Address , select flash 0(0), or 1(1)	RW	0
25-16	Address of flash intermediate command data storage for write.	RW	0
15-0	Value to be written to flash intermediate storage at location specified in bits	R	0

	25-16.		

Figure 37: Flash memory write: Address 0x24

Flash memory control: Address 0x25

Bits	Function	R/W	Default
31	Write to this bit (1) start flash 1 command pre-stored in flash intermediate storage programmable in register 0x24. If command involve read operation data will be stored in intermediate storage accessible from register 0x26	RW	0
30	Write to this bit (1) start flash 0 command pre-stored in flash intermediate storage programmable in register 0x24. If command involve read operation data will be stored in intermediate storage accessible from register 0x26	RW	0
29-25	Unused	R	0
24-16	Size of read operation in bytes to be to be stored into intermediate read store, 0x0 – no read required	RW	0
15-10	Unused	R	0
9	If set to 1, flash chip select will not be asserted16	R	0
8-0	Size of command in bytes to be played from intermediate command store	RW	0

Figure 38: Flash memory control: Address 0x25

Flash memory read: Address 0x26

Bits	Function	R/W	Default
31	Write to this bit (1) start operation of reading which can be completed on follow up read	RW	0
30	Done bit, indicate that flash command is completed	RW	0
29-27	Unused	R	0
26	MSB Address , select flash 0(0), or 1(1)	RW	0
25-16	Address of flash intermediate data storage to read.	RW	0
15-0	Value read from flash intermediate storge at location specified in bits 25-16.	R	0

Figure 39: Flash memory re56: Address 0x26

Zero-suppression control register: Address 0x27

Bits	Function	R/W	Default
31	Enable zero suppression algorithm. This algorithm discard all suppressed channels	RW	0
30	Test zero-suppression reporting. Configure system return only enabled channels regarding zero-suppression logic	RW	0
29-24	Unused	RW	0
23-12	Set overflow value to properly handle overflow	RW	0
11-0	Set threshold value to compare. Discard if all values under threshold.	RW	0

Figure 40: Zero-suppression control register: Address 0x27

Monitor results register: Address 0x28

Bits	Function	R/W	Default
31	Always 1	R	0
30-28	Unused	R	0
27-23	Unused	R	0
22-16	Data address for FPGA monitoring interface, DADDR on page 14 of http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf	R	0
15-0	Output data for FPGA monitoring interface, DO on page 14 of http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf	R	0

Figure 41: Monitor results register: Address 0x28

MAX11616 ADC 0 Data: Address 0x29

Bits	Function	R/W	Default
31	ADC, Valid data bit, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	MAX11616 ADC, HV voltage ,conversion is V,V = 21*value/1000, V	R	0
15	ADC, Valid data bit, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	MAX11616 ADC, HV current ,conversion is I,mA = value/10, mA	R	0

Figure 42: MAX11616 ADC 0 Data: Address 0x29

MAX11616 ADC 1 Data: Address 0x2a

Bits	Function	R/W	Default
31	ADC, Valid data bit, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	MAX11616 ADC, unused	R	0
15	ADC, Valid data bit, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	MAX11616 ADC, unused	R	0

Figure 43: MAX11616 ADC 1 Data: Address 0x2a

MAX11616 ADC 2 Data: Address 0x2b

Bits	Function	R/W	Default

31-28	Unused	R	0
27-16	MAX11616 ADC 3, Unused	R	0
15-12	Unused	R	0
11-0	MAX11616 ADC 2, Unused	R	0

Figure 44: MAX11616 ADC 2 Data: Address 0x2b

MAX11616 ADC 3 Data: Address 0x2c

Bits	Function	R/W	Default
31-28	Unused	R	0
27-16	MAX11616 ADC 5, Unused	R	0
15-12	Unused	R	0
11-0	MAX11616 ADC 4, Unused	R	0

Figure 45: MAX11616 ADC 3 Data: Address 0x2c

MAX11616 ADC 4 Data: Address 0x2d

Bits	Function	R/W	Default
31-28	Unused	R	0
27-16	MAX11616 ADC 7, Unused	R	0
15-12	Unused	R	0
11-0	MAX11616 ADC 6, Unused	R	0

Figure 46: MAX11616 ADC 4 Data: Address 0x2d

MAX11616 ADC 5 Data: Address 0x2e

Bits	Function	R/W	Default
31-28	Unused	R	0
27-16	MAX11616 ADC 9, Unused	R	0
15-12	Unused	R	0
11-0	MAX11616 ADC 8, Unused	R	0

Figure 47: MAX11616 ADC 5 Data: Address 0x2e

MAX11616 ADC 3 Data: Address 0x2f

Bits	Function	R/W	Default
31-28	Unused	R	0
27-16	MAX11616 ADC 11, Unused	R	0
15-12	Unused	R	0
11-0	MAX11616 ADC 10, Unused	R	0

Figure 48: MAX11616 ADC 3 Data: Address 0x2f

VPED DAC control Address 0x30

Bits	Function	R/W	Default
31-12	Unused	RW	0
11-0	VPED value from 0 to 2.5V (Max value enforced in hardware is 0xB6C ~2.5V)	RW	0

Figure 49: VPED DAC : Address 0x30

TACK simulator LSW: Address 0x31

Bits	Function	R/W	Default
31-0	Bits 0 to 31 of TACK command (see section 8), Write to register 0x33 initiate this command application	RW	0

Figure 50: TACK simulator LSW: Address 0x31

TACK simulator MSW: Address 0x32

Bits	Function	R/W	Default
31-0	Bits 32 to 63 of TACK command (see section 8), Write to register 0x33 initiate this command application	RW	0

Figure 51: TACK simulator MSW: Address 0x32

TACK simulator Special word: Address 0x33

Bits	Function	R/W	Default
31	Software trigger, if software trigger enable, it is treated as random trigger, otherwise, it sent command specified in TACK register and TACK mode registers	RW	0
30	Parity of TACK, 0- even parity, 1 – odd parity, TBD	RW	0
29	RE-sync trigger, take current time on tester board and send to camera module. Correct Trigger mode need to be used	RW	0
28-22	Unused	RW	0
28-22	Trigger dead time, after trigger detected and processed module will ignore the next trigger for number of ns specified in these bits. Asserted deadtime = Value * 256*8ns.	RW	0
21-20	Trigger mode: 00 – regular trigger 01 – sync related operation 10 - unused 11 - unused	RW	0
19-18	Trigger type: for trigger mode 00 00 – TACK with number of buffers and trigger delay for set 0 01 – TACK with number of buffers and trigger delay for set 1 10 – software trigger 11 - unused	RW	0

	for trigger mode 01 00 – Initial sync command, can be done only once for proper operation, can be reassured after stop sync command (trigger type 10) 01 – Re-sync command, passive command, checked on camera module do detect if any difference between time base on camera module and tester board 10 – stop sync command, after stop sync command, to operate triggering on camera module sync command need to be reissued 11 - unused		
17-0	Enable trigger input. Bits assigned as followed: 0 –trigger bit 0, 1 –trigger bit 1, …, 15 – trigger bit 15 ,16 – external hardware trigger, 17 – software trigger	RW	0

Figure 52: TACK simulator Special word: Address 0x33

MAX1230 ADC 0 Data: Address 0x34

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC , Temperature measured by ADC 2, conversion is T,C = value*0.125, C	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC , Temperature measured by ADC 0,conversion is T,C = value*0.125, C	R	0

Figure 53: MAX1230 ADC 0 Data: Address 0x34

MAX1230 ADC 1 Data: Address 0x35

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 0 current(32), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 0 current (0), conversion is I = value/2, uA	R	0

Figure 54: MAX1230 ADC 1 Data: Address 0x35

MAX1230 ADC 2 Data: Address 0x36

Bits	Function	R/W	Default

31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 1 current (33), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 1 current(1), conversion is I = value/2, uA	R	0

Figure 55: MAX1230 ADC 2 Data: Address 0x36

MAX1230 ADC 3 Data: Address 0x37

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 2 current(34), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 2 current (2), conversion is I = value/2, uA	R	0

Figure 56: MAX1230 ADC 3 Data: Address 0x37

MAX1230 ADC 4 Data: Address 0x38

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 3 current (35), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 3 current(3), conversion is I = value/2, uA	R	0

Figure 57: MAX1230 ADC 4 Data: Address 0x38

MAX1230 ADC 5 Data: Address 0x39

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0

30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 4 current(36), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 4 current (4), conversion is I = value/2, uA	R	0

Figure 58: MAX1230 ADC 5 Data: Address 0x39

MAX1230 ADC 6 Data: Address 0x3a

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 5 current (37), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 5 current(5), conversion is I = value/2, uA	R	0

Figure 59: MAX1230 ADC 6 Data: Address 0x3a

MAX1230 ADC 7 Data: Address 0x3b

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 6 current(38), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 6 current (6), conversion is I = value/2, uA	R	0

Figure 60: MAX1230 ADC 7 Data: Address 0x3b

MAX1230 ADC 8 Data: Address 0x3c

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 7 current (39), conversion is I = value/2, uA	R	0

15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 7 current(7), conversion is I = value/2, uA	R	0

Figure 61: MAX1230 ADC 8 Data: Address 0x3c

MAX1230 ADC 9 Data: Address 0x3d

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 8 current(40), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 8 current (8), conversion is I = value/2, uA	R	0

Figure 62: MAX1230 ADC 9 Data: Address 0x3d

MAX1230 ADC 10 Data: Address 0x3e

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 9 current (41), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 9 current(9), conversion is I = value/2, uA	R	0

Figure 63: MAX1230 ADC 10 Data: Address 0x3e

MAX1230 ADC 11 Data: Address 0x3f

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 10 current(42), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0

14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 10 current (10), conversion is I = value/2, uA	R	0

Figure 64: MAX1230 ADC 11 Data: Address 0x3f

MAX1230 ADC 12 Data: Address 0x40

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 11 current (43), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 11 current(11), conversion is I = value/2, uA	R	0

Figure 65: MAX1230 ADC 12 Data: Address 0x40

MAX1230 ADC 13 Data: Address 0x41

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 12 current(44), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 12 current (12), conversion is I = value/2, uA	R	0

Figure 66: MAX1230 ADC 13 Data: Address 0x41

MAX1230 ADC 14 Data: Address 0x42

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 13 current (45), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 13 current(13), conversion is I = value/2, uA	R	0

Figure 67: MAX1230 ADC 14 Data: Address 0x42

MAX1230 ADC 15 Data: Address 0x43

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 14 current(46), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 14 current (14), conversion is I = value/2, uA	R	0

Figure 68: MAX1230 ADC 15 Data: Address 0x43

MAX1230 ADC 16 Data: Address 0x44

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 15 current (47), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 15 current(15), conversion is I = value/2, uA	R	0

Figure 69: MAX1230 ADC 16 Data: Address 0x44

MAX1230 ADC 17 Data: Address 0x45

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC , Temperature measured by ADC 3, conversion is T,C = value*0.125, C	R	0
15	ADC 0, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC , Temperature measured by ADC 1,conversion is T,C = value*0.125, C	R	0

Figure 70: MAX1230 ADC 17 Data: Address 0x45

MAX1230 ADC 18 Data: Address 0x46

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 3 channel 0 current(48), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 1 channel 0 current (16), conversion is I = value/2, uA	R	0

Figure 71: MAX1230 ADC 18 Data: Address 0x46

MAX1230 ADC 19 Data: Address 0x47

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 3 channel 1 current (49), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 1 channel 1 current(17), conversion is I = value/2, uA	R	0

Figure 72: MAX1230 ADC 19 Data: Address 0x47

MAX1230 ADC 20 Data: Address 0x48

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 2 current(50), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 2 current (18), conversion is I = value/2, uA	R	0

Figure 73: MAX1230 ADC 20 Data: Address 0x48

MAX1230 ADC 21 Data: Address 0x49

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in	R	0

	conversion.		
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 3 current (51), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 3 current(19), conversion is I = value/2, uA	R	0

Figure 74: MAX1230 ADC 21 Data: Address 0x49

MAX1230 ADC 22 Data: Address 0x4a

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 4 current(52), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 4 current (20), conversion is I = value/2, uA	R	0

Figure 75: MAX1230 ADC 22 Data: Address 0x4a

MAX1230 ADC 23 Data: Address 0x4b

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 5 current (53), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 5 current(21), conversion is I = value/2, uA	R	0

Figure 76: MAX1230 ADC 23 Data: Address 0x4b

MAX1230 ADC 24 Data: Address 0x4c

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0

27-16	ADC 1, ASIC 2 channel 6 current(54), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 6 current (22), conversion is I = value/2, uA	R	0

Figure 77: MAX1230 ADC 24 Data: Address 0x4c

MAX1230 ADC 25 Data: Address 0x4d

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 7 current (55), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 7 current(23), conversion is I = value/2, uA	R	0

Figure 78: MAX1230 ADC 25 Data: Address 0x4d

MAX1230 ADC 26 Data: Address 0x4e

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 8 current(56), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 8 current (24), conversion is I = value/2, uA	R	0

Figure 79: MAX1230 ADC 26 Data: Address 0x4e

MAX1230 ADC 27 Data: Address 0x4f

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 9 current (57), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in	R	0

	conversion.		
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 9 current(25), conversion is I = value/2, uA	R	0

Figure 80: MAX1230 ADC 27 Data: Address 0x4f

MAX1230 ADC 28 Data: Address 0x50

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 10 current(58), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 10 current (26), conversion is I = value/2, uA	R	0

Figure 81: MAX1230 ADC 28 Data: Address 0x50

MAX1230 ADC 29 Data: Address 0x51

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 11 current (59), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 11 current(27), conversion is I = value/2, uA	R	0

Figure 82: MAX1230 ADC 29 Data: Address 0x51

MAX1230 ADC 30 Data: Address 0x52

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 12 current(60), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0

11-0	ADC 1, ASIC 0 channel 12 current (28), conversion is I = value/2, uA	R	0

Figure 83: MAX1230 ADC 30 Data: Address 0x52

MAX1230 ADC 31 Data: Address 0x53

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 13 current (61), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 13 current(29), conversion is I = value/2, uA	R	0

Figure 84: MAX1230 ADC 31 Data: Address 0x53

MAX1230 ADC 32 Data: Address 0x54

Bits	Function	R/W	Default
31	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 14 current(62), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 14 current (30), conversion is I = value/2, uA	R	0

Figure 85: MAX1230 ADC 32 Data: Address 0x54

MAX1230 ADC 33 Data: Address 0x55

Bits	Function	R/W	Default
31	ADC, Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
30-28	Unused	R	0
27-16	ADC 1, ASIC 2 channel 15 current (63), conversion is I = value/2, uA	R	0
15	ADC , Valid data bit, if bit 0 of register 14 set 0, 1 indicate data valid, 0 – is in conversion.	R	0
14-12	Unused	R	0
11-0	ADC 1, ASIC 0 channel 15 current(31), conversion is I = value/2, uA	R	0

Figure 86: MAX1230 ADC 33 Data: Address 0x55

Trigger efficiency control 0 register: Address 0x56

Bits	Function	R/W	Default
31	Indicate completion of counting	RW	0
30-0	Specify duration of trigger statistic collection in 8ns. So, full value is ~8.5 seconds	RW	0

Figure 87: Trigger efficiency control 0 register: Address 0x56

- Write to this register will start time interval counting in system clock cycles (8ns)
- Value of this register indicate time interval when trigger statistic collected after start (write operation)

Trigger efficiency control 1 register: Address 0x57

Bits	Function	R/W	Default
31-16	Unused	R	0
15-0	Enable for trigger inputs into efficiency counters in register 0x4b. One bit per trigger input	RW	0

Figure 88: Trigger efficiency control 1 register: Address 0x57

Trigger input counter register: Address 0x58

Bits	Function	R/W	Default
31	Indicate completion of counting	RW	0
30	Number of trigger low to high transitions counted	RW	0

Figure 89: Trigger input counter register: Address 0x58

Trigger efficiency counter register: Address 0x59

Bits	Function	R/W	Default
31	Indicate completion of counting	RW	0
30	Number of trigger low to high transitions counted	RW	0

Figure 90: Trigger efficiency counter register: Address 0x59

Software reset register: Address 0x5a

Bits	Function	R/W	Default
31-0	Writing value of 0xBECEDACE will start reset of FPGA logic, but keep values programmed into register. Also, write to this register does not generate command response due to transmitter logic reset as well	RW	0

Figure 91: Software reset register: Address 0x5a

Channel enable register 0: Address 0x5b

Bits	Function	R/W	Default
31-0	Channel enable register bits 31-0. Channel 15-0 on ASIC 0, Channel 31-16 on	RW	0

	ASIC 1. One bit per channel. 0 – disable, 1 - enable		

Figure 92: Channel enable register 0: Address 0x5b

Channel enable register 1: Address 0x5c

Bits	Function	R/W	Default
31-0	Channel enable register bits 31-0. Channel 15-0 on ASIC 0, Channel 31-16 on ASIC 1. One bit per channel. 0 – disable, 1 - enable	RW	0

Figure 93: Channel enable register 1: Address 0x5c

Trigger statistic 1: Address 0x5d

Bits	Function	R/W	Default
31-16	Count trigger low to high transitions on all enabled for counting (bits 17-0 of register 0x1a) incoming triggers (16 from four Target ASICs, 1 software trigger(bit 31 of register 0x1a), and 1 external hardware trigger). Trigger transition observed on same clock transition counted as one trigger. Counter is reset by writing value of 1 into bit 30 of register 0x1a	RW*	0
15-0	Count trigger low to high transitions on all incoming triggers (16 from four Target ASICs, 1 software trigger(bit 31 of register 0x1a), and 1 external hardware trigger). Trigger transition observed on same clock transition counted as one trigger. Counter is reset by writing value of 1 into bit 30 of register 0x1a	RW*	0

Figure 94: Trigger statistic 1: Address 0x5d

Special feature register: Address 0x5e (only expert usage)

Bits	Function	R/W	Default
31-16	Unused, TBD	R/W	0
15	To study drooping effect of sample 31(32nd) we can read samples in increasing (0) or decreasing (1) order.	RW	0
14-8	Adjust event serial data input delay to make sure all channels properly clock input data	RW	0
7	Special trigger mode. When set to 1 enable J5 output generate pulse on every sampling buffer turn for 10 event and stop. To reactivate need to bring it back to 0, if 0 - trigger sync command generated ~ at 1kHz	RW	0
6	To control direction of External Trigger IO, 0 – input, 1 - output	RW	0
5-0	Unused , TBD	RW	0

Figure 95: Special feature register: Address 0x5e

Dead-time control (unused): Address 0x5f

Bits	Function	R/W	Default
31-16	Duration of trigger deadtime, in 8ns steps	RW	0
15	Enable deadtime logic	RW	0
14	Unused	RW	0

13-0	Delay after readout start to assert trigger deadtime, in 8ns steps	RW	0

Figure 96 Dead-time control(unused): Address 0x5f

5.1.1 Target 7 related registers

Write Target register: Address 0x60

Bits	Function	R/W	Default
31-25	Unused	R	0
24	Enable (1) write/read operation to ASIC 3	RW	0
23	Enable (1) write/read operation to ASIC 2	RW	0
22	Enable (1) write/read operation to ASIC 1	RW	0
21	Enable (1) write/read operation to ASIC 0	RW	0
20	If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	RW	0
19	Define if data latching on Target is required. 0 – latching is required, 1 – no latching.	RW	0
18-12	Target register address to write. See Target 7 documentation for specific register address map.	RW	0
11-0	Target register value to write. See Target 7 documentation for specific registers and bit allocation	RW	0

Figure 97: Write Target register: Address 0x60

Read 0 target register: Address 0x61

Bits	Function	R/W	Default
31-28	Unused	RW	0
27-16	Read back value from ASIC 1. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0
15-12	Unused	RW	0
11-0	Read back value from ASIC 0. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0

Figure 98: Read 0 target register: Address 0x61

Read 1 target register: Address 0x62

Bits	Function	R/W	Default
31-28	Unused	RW	0
27-16	Read back value from ASIC 3. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0
15-12	Unused	RW	0

11-0	Read back value from ASIC 2. Updated after Target ASIC operation enabled in register 0x40(bit 20). If bit 19 is set (1) read back followed immediately after write. Otherwise, read of previously written register	R	0

Figure 99: Read 1 target register: Address 0x62

5.2 Packet data word

Packet for Buffer 0, channel 0:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Size. Real size = size * 8 in bytes.								Sequence number per ID							
Time Stamp[15:0] at time of TACK arrival, 8ns resolution															
Read Sft (1b)	Use offset (1b)	*Current column of buffer at time of sampling (6 bits)*						*Current row of buffer at time of sampling(3 bits)*					Current sample offset (5 bits)		
Sample offset (2bits)		Contributing triggers(6 bits)						Number of buffers(4bits) as specified in Reg0xF(bits19-16)					ID of serial data connection (4 bits)		
Indicate Stale Data(1) – if data read from same buffer more than once with sampling update		MBZ(5)						Adjusted sample delay due to trigger time and selected trigger delay(5)					Partial number of samples(5) as specified in Reg0x16(bits4-0)		
MBZ(1)		Total number of samples in event (10 bits)											Total number of buffers digitized(5 bits)		
MBZ(2)								Time Stamp[23:16] at time of TACK arrival, 8ns resolution							
MBZ(16)															
MBZ(3)		Trigger delay (8 bits)													
Sample ID (only 4 bits) Samples 0 and 16 look same. First enabled sample of buffer 0								12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.							
Sample ID (only 4 bits) Samples 0 and 16 look same,. Second enabled sample of buffer 0								12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.							
…								…							
Sample ID (only 4 bits) Samples 0 and 16 look								12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample							

same. Last enabled sample of buffer 0	ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.		
Sample ID (only 4 bits) Samples 0 and 16 look same. First enabled sample of buffer 1	12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.		
Sample ID (only 4 bits) Samples 0 and 16 look same,. Second enabled sample of buffer 1	12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.		
…	…		
Sample ID (only 4 bits) Samples 0 and 16 look same. Last enabled sample of buffer 1	12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.		
…			
Sample ID (only 4 bits) Samples 0 and 16 look same. First enabled sample of Last buffer.	12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.		
Sample ID (only 4 bits) Samples 0 and 16 look same,. Second enabled sample of Last buffer	12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.		
…	…		
Sample ID (only 4 bits) Samples 0 and 16 look same. Last enabled sample of Last buffer	12 bit ADC value for sample ID indicated. Even so, sample ID is limited to 4 bits, information can be easily restored from list of enabled samples. Sample ID start from 0 to 31(63). Buffers are going in order as well after all samples collected.		
CRC on above words			
0xbeef - This is filler words to keep size at multiple of 8 bytes and is function of actual enabled samples (see above). Up to 3 words possible			
MBZ(14 bits)		Timeout	Error
MBZ			

6 Command Input data format:

Word #	Byte 1								Byte 0								Type
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	DNC																PGP
1	DNC														MBZ		PGP
2	OC 00read 01write		DNC						Address MSB								PGP
3	Address LSW																PGP
4	Data MSW, write – actual word, read - 0																PGP
5	DATA LSW, write – actual word, read - 0																PGP
6	DNC																
7	DNC																

Table 1: Command input packet format

Formatted according to PGP requirements to deal with double board usage (UDP and PGP)

7 Response output data format:

Word #	Byte 1								Byte 0								Type
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0	Feedback command header word																PGP
1	Feedback command header word														MBZ		PGP
2	OC 00read 01write		0x0						Address MSB								PGP
3	Address LSW																PGP
4	Data MSW, write – feedback written word, read – actual read word																PGP
5	DATA LSW, – feedback written word, read – actual read word																PGP
6	MBZ														Timeout error	Other Error	PGP
7	MBZ																PGP

Table 2: Response output packet format

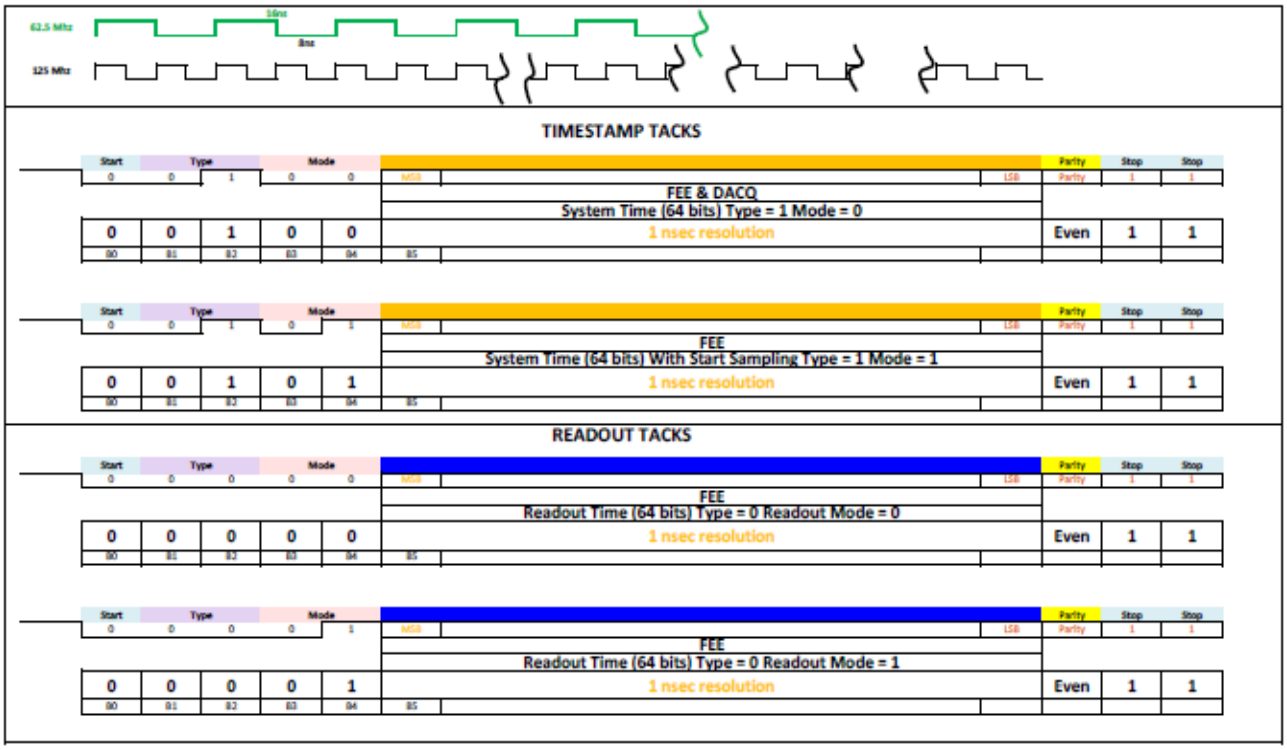
8 TACK command format:

Trigger command consist of 72 bits described in this table

#	Bits						
	0	1-2	3-4	5-68	69	70-71	Comments
	Start	Type	Mode	TACK command load	Even parity	Stop	
0	0	01	00	System Time (64 bits) Type = 1 Mode = 0. 1ns resolution Can be issued only once at the start of operation, set all timing to sync base. The 3 LSB must be 000, since camera module has only 8ns in time counter. Need to be verified by checking Enable bit 0, of register 0x17. Sync while module synced will not have effect on operation	X	11	SYNC
1	0	01	01	System Time (64 bits) Type = 1 Mode = 1. 1ns resolution Re-sync command, can be sent at any time with proper time load. The 3 LSB must be 000, since camera module has only 8ns in time counter. This is passive command, payload just compared with current time counter value and counted as good re-sync (register 0x10 bits 31-16). Every issued re-sync need to be verified	X	11	RE_SYNC
2	0	01	10	Stop Sync command, Payload ignored. Need to be verified by checking Enable bit 0, of register 0x17. For follow-up sync, camera module need to be reset before new Sync attempted.	X	11	Stop Sync
3	0	01	11	TBD	X	11	Unused
4	0	00	00	System Time (64 bits) Type = 0 Mode = 0. 1ns resolution, indicate actual time of trigger, so camera module can calculate how far in time it needs to go to extract proper waveforms. It is set 0, and use related trigger delay time (Register 0x19, bits 31-18) and number of buffers to read (Register 0x19, bits 3-0)	X	11	TACK, set 0
5	0	00	01	System Time (64 bits) Type = 0 Mode = 1. 1ns resolution, indicate actual time of trigger, so camera module can calculate how far in time it needs to go to extract proper waveforms. It is set 1, and use related trigger delay time (Register 0x19, bits 13-0) and number of buffers to read (Register 0x19, bits 19-16)	X	11	TACK, set 1
6	0	00	10	Software trigger command. Will read data from buffer specified in register 0x1b, bits 8-0	X	11	Software forced trigger
1	0	10	XX	TBD	X	11	Unused
1	0	11	XX	TBD	X	11	Unused

Table 3: TACK packet format

From ICD to backplane



9 Artix-7 FPGA System Monitoring

User guide for Artix-7 FPGA system monitoring can be found under

http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf

T7EV implement readout of 16 VAUX channels.

VAUX channel definition table

Signal	Function	Conversion formula, V=,V
VAUX0	ASIC 0 Amon, Monitoring output from Target-7. For detail of selection of specific voltage see Target-7 documentation	Value*3/1024
VAUX1	ASIC 0, Vped voltage	Value*3/1024
VAUX2	ASIC 0 , ISEL voltage	Value*3/1024
VAUX3	ASIC 0, 2_5V supply	Value*3/1024
VAUX4	ASIC 1 Amon, Monitoring output from Target-7. For detail of selection of specific voltage see Target-7 documentation	Value*3/1024
VAUX5	ASIC 1, Vped voltage	Value*3/1024
VAUX6	ASIC 1 , ISEL voltage	Value*3/1024

VAUX7	ASIC 1, 2_5V supply	Value*3/1024
VAUX8	ASIC 2 Amon, Monitoring output from Target-7. For detail of selection of specific voltage see Target-7 documentation	Value*3/1024
VAUX9	ASIC 2, Vped voltage	Value*3/1024
VAUX10	ASIC 2 , ISEL voltage	Value*3/1024
VAUX11	ASIC 2, 2_5V supply	Value*3/1024
VAUX12	ASIC 3 Amon, Monitoring output from Target-7. For detail of selection of specific voltage see Target-7 documentation	Value*3/1024
VAUX13	ASIC 3, Vped voltage	Value*3/1024
VAUX14	ASIC 3 , ISEL voltage	Value*3/1024
VAUX15	ASIC 3, 2_5V supply	Value*3/1024

Figure 100: VAUX channel definition table

To read any register used in FPGA monitoring interface the following sequence need to be executed:

1. Write value of 0xAA0000, where AA is FPGA monitoring register address into T7EV register number 0x1D
2. Read T7EV register 0x28, the 16 LS bits will have register value

To write any register used in FPGA monitoring interface the following sequence need to be executed:

1. Write value of 0x80AA0000, where AA is FPGA monitoring register address into T7EV register number 0x1D
2. Read T7EV register 0x28, the 16 LS bits will have updated (written) register value

Example of reading temperature in register 0:

1. Write value of 0 into T7EV register 0x1D
2. Read register 0x28 and extract ADC value = (Reg0x28 & 0xffff) >> 4
3. Calculate by T,C = (ADCValue x 503.975)/4096 – 273.15

Example of reading VCCINT in register 1:

4. Write value of 0x10000 into T7EV register 0x1D
5. Read register 0x28 and extract ADC value = (Reg0x28 & 0xffff) >> 4
6. Calculate by Voltage, V = (ADCValue x 3)/4096

Example of reading VAUX0 in register 1:

7. Write value of 0x100000 into T7EV register 0x1D
8. Read register 0x28 and extract ADC value = (Reg0x28 & 0xffff) >> 4
9. Calculate by Voltage, V = (ADCValue*3)/4096 – formula from table 47

Artix-7 FPGA monitoring interface include many options for operation, for basic operation all registers is configured at power up and will not require additional configuration. For expert usage need to consult

http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf

10 UDP requirements and setups:

T7EV support UDP communication through external network connections. There are set of limitations that need to be considered when interface to T7EV is designed:

1. T7EV board has Fiber-optic Ethernet interface. As result in order to talk to any regular PC there are two possible solutions:
    - Use NIC card supporting Fiber-optic interface. Possible NIC card which was tested with this interface is Hewlett-Packard-HP-NC373F-Mltfunc-PCI-E-1000SX-GbEth-ADP-NC373F
    - Use Fiber Transceiver to convert from FO Ethernet to 1Gbit copper connection. Adapter used is FIB1-1000TS
2. Any 1Gbit NIC card will support communication with evaluation board
3. T7EV hardwired to IP address 192.168.0.173
4. T7EV hardwired to port 8105
5. T7EV responds to only ARP and UDP packet with IP192.168.0173 and port 8105, does not responds to ping
6. On Linux core in order to keep up with flood of packets command

    sudo /sbin//sysctl -w net/core/rmem_max=2000000

    need to be executed to increase kernel buffering for incoming data. Value of 2000000 need to be verified. Window version of this setup is not known at this point.
7. The following Python command used to set and talk to T7EV
    - from socket import *
    - UDPSock = socket(AF_INET,SOCK_DGRAM)
    - UDPSock.bind((HOST0,PORT0))
    - UDPSock.settimeout(1)
    - UDPSock.sendto(buffer,(HOST,PORT))
    - data,addr = UDPSock.recvfrom(buffer)
    - UDPSock.close()
8. For each command sent to T7EV there are response (each command is acknowledged)