EE 3613: Computer Organization

Homework #3

Due Date: (blackboard) Wednesday April 21

Problem 1 (15 Points):
We wish to implement the instruction **sw** (store word) in the attached figure.

Problem 2 (15 Points):
We wish to add the instruction **jr** (jump register) to the single cycle-datapath described in class. Add any necessary datapaths and control signals to the single-cycle datapath and show the additions in the attached figure.

Problem 3 (15 Points):
This question is similar to Problem 1, except that we wish to add the instruction **sll** (shift left logical) and show the additions in the attached figure.

Problem 4 (**20 Points**): Show the forwarding paths needed to execute the following 4 instructions:

```
add $3, $4, $6
sub $5, $3, $2
lw $7, 100($5)
add $8, $7, $2
```

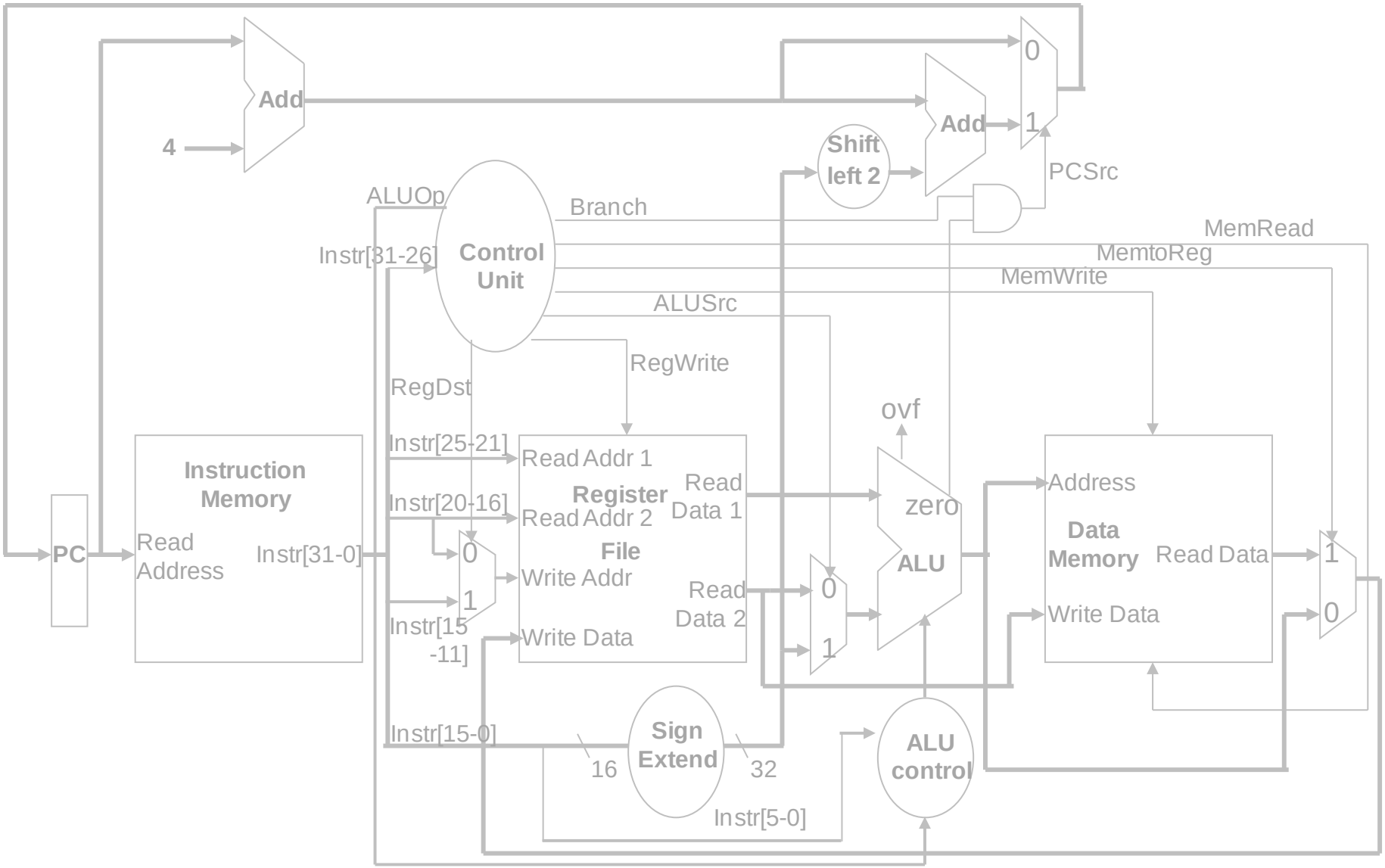
Problem 5 (**15 Points**): Identify all of the data dependencies in the following code. Which dependencies are data hazards that will be resolved via forwarding? Which dependencies are data hazards that will cause a stall?

```
add $3, $4, $2
sub $5, $3, $1
lw $6, 200($3)
add $7, $3, $6
```

Problem 6 (**20 Points**): Consider executing the following code on the pipelined datapath:

```
add $2, $3, $1
sub $4, $3, $5
add $5, $3, $7
add $7, $6, $1
add $8, $2, $6
```

At the end of the 5th cycle of execution, which registers are being read and which are being written? What are the *forwarding unit* and *hazard detection* units doing during the 5th cycle of execution, if any comparisons are being made, mention them.


Add
4
Add
Shift
left 2
0
1
PCSrc
ALUOp
Branch
MemRead
MemtoReg
MemWrite
ALUSrc
RegWrite
RegDst
Instr[31-26]
Control
Unit
ovf
Instruction
Memory
Read
Address
Instr[31-0]
PC
Instr[25-21]
Instr[20-16]
Instr[15
-11]
Instr[15-0]
Instr[5-0]
Read Addr 1
Read Addr 2
Register
File
Write Addr
Write Data
Read
Data 1
Read
Data 2
zero
ALU
Address
Data
Memory
Read Data
Write Data
Sign
Extend
16
32
ALU
control