Experiment 12: Sub-threshold Characteristics of N-channel MOSFET

Electronic Devices Lab
Department of Electrical Engineering, IIT Bombay

Jatin Kumar
Roll No: 22B3922

Contents

Aim of the Experiment

The main objectives of this experiment are:

1. To obtain the sub-threshold I_d *vs* V_{gs} characteristics of NMOS using a low-noise OP-AMP, and to analyze and compare the resulting plots.
2. To verify the continuity of I_d *vs* V_{gs} characteristics beyond the sub-threshold region.
3. To design and test a Common Source Amplifier using an NMOS in the sub-threshold region.

Chapter 1

Background Theory

1.1 Overview of N-channel MOSFET

An N-channel MOSFET is a Field Effect Transistor with four terminals: Drain, Gate, Source, and Body. For an NMOS to turn ON, the Gate-to-Source voltage, V_{gs}, must exceed a threshold voltage, V_{th}. However, even when $V_{gs} < V_{th}$, a small current flows, termed as sub-threshold current, due to diffusion mechanisms.

The equation governing the drain current (I_d) in the sub-threshold region is given by:

$$I_d = I_0 e^{\left(\frac{V_{gs}-V_{th}}{\eta V_t}\right)} \left(1 - e^{\frac{-V_{ds}}{\eta V_t}}\right) \tag{1.1}$$

where

- $I_0 = \mu_n C_{ox} \frac{W}{L} V_t^2 (\eta - 1)$,
- V_t is the thermal voltage,
- μ_n is the electron mobility,
- C_{ox} is the gate oxide capacitance,
- $\eta = 1 + \frac{C_d}{C_{ox}}$ (Sub-threshold Slope Factor).

Chapter 2

Experimental Setup and Approach

2.1 Components

- ALD1106 NMOS IC
- TLV9161 OP-AMP
- Keithley Power Supply
- 10 MΩ and 1 MΩ resistors
- 100 Ω Potentiometer
- 3 Digital Multimeters (DMMs)

2.2 Design Approach

To simplify the I_d equation, we assume $V_{ds} = 2V$, allowing the exponential term to approach 1, simplifying to:

$$I_d \approx I_0 e^{\left(\frac{V_{gs}-V_{th}}{\eta V_t}\right)} \tag{2.1}$$

where η is assumed initially as 10. This will be verified post-experiment by calculating the sub-threshold slope, S, as:

$$S = \frac{dV_{gs}}{d(\log_{10} I_d)} \tag{2.2}$$

Chapter 3

Experimental Procedure and Results

3.1 Part 1: Transfer Characteristics of NMOS

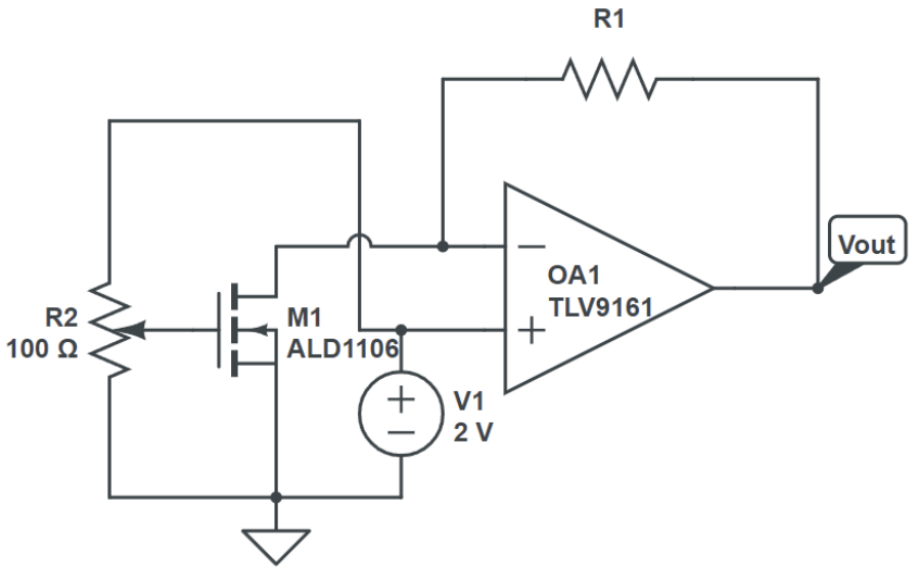

Figure 3.1: Circuit for Part1

3.1.1 Measurement of I_d vs V_{gs} for 10 MΩ Resistor

1. Connect the circuit as per the TLV9161 and ALD1106 pinouts.
2. Vary V_{gs} from 0V until V_{out} of OP-AMP saturates, with a step size of 0.02V.
3. Record V_{out} and calculate I_d using:

$$I_d = \frac{V_{out} - V_{inv}}{10 \times 10^6} \tag{3.1}$$

Table 3.1: I_d vs V_{gs} for 10 MΩ

V_{gs} (V)	V_{out} (V)	I_d (μA)
0.00	1.99	-0.001
0.24	2.01	0.001
0.26	2.01	0.001
0.28	2.01	0.001
0.30	2.02	0.002
0.32	2.04	0.004
0.34	2.06	0.006
0.36	2.15	0.015
0.38	2.21	0.021
0.40	2.30	0.03
0.42	2.55	0.055
0.44	2.82	0.082
0.46	3.44	0.144
0.48	4.18	0.218
0.50	5.11	0.311
0.52	7.13	0.513
0.54	8.00	0.6

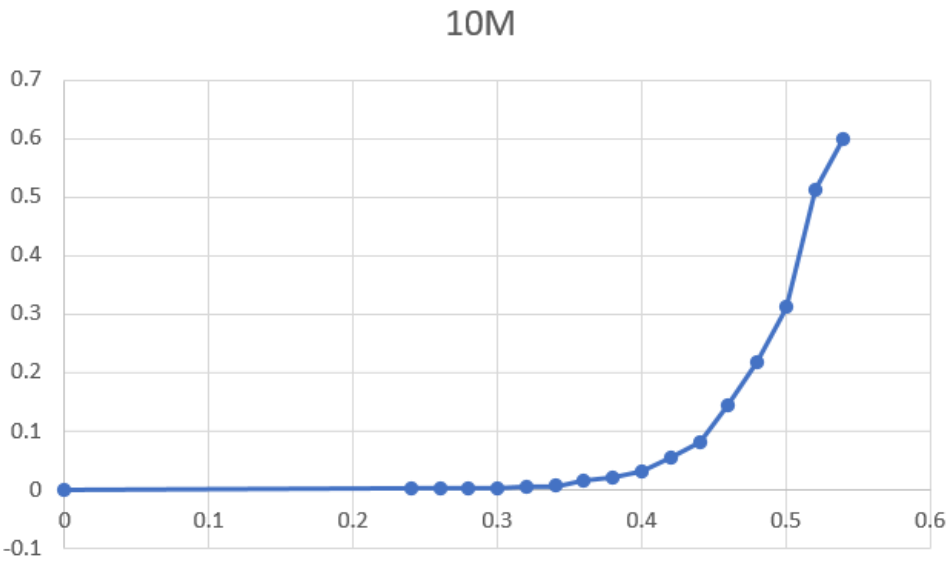

Figure 3.2: Plot for Id vs Vgs for 10MOhms

3.1.2 Measurement of I_d vs V_{gs} for 1 MΩ Resistor

Table 3.2: I_d vs V_{gs} for 1 MΩ

V_{gs} (V)	V_{out} (V)	I_d (μA)
0.56	3.01	1.01
0.58	3.62	1.62
0.60	4.33	2.33
0.62	5.03	3.03
0.64	5.91	3.91
0.66	7.12	5.12
0.68	8.00	6.00

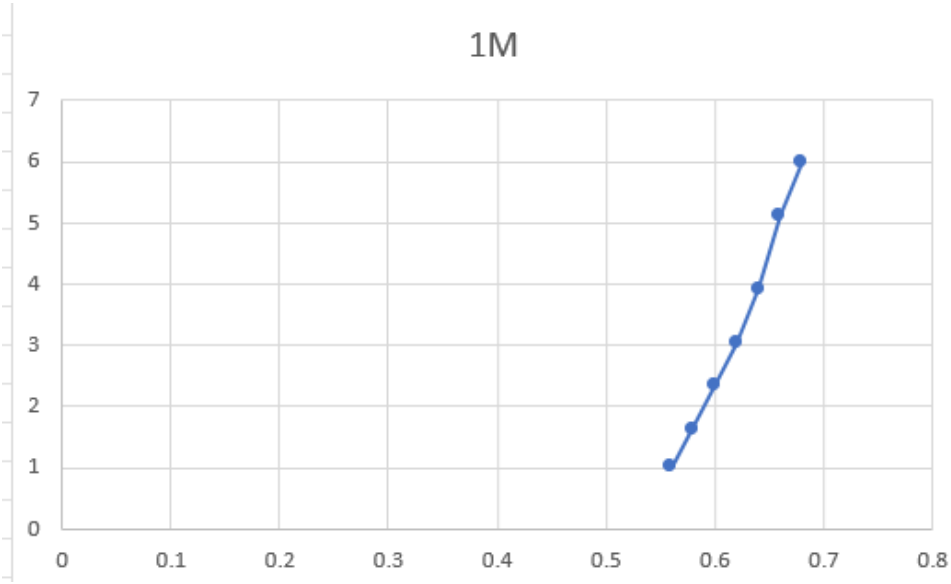

Figure 3.3: Plot for Id vs Vgs for 1MOhms

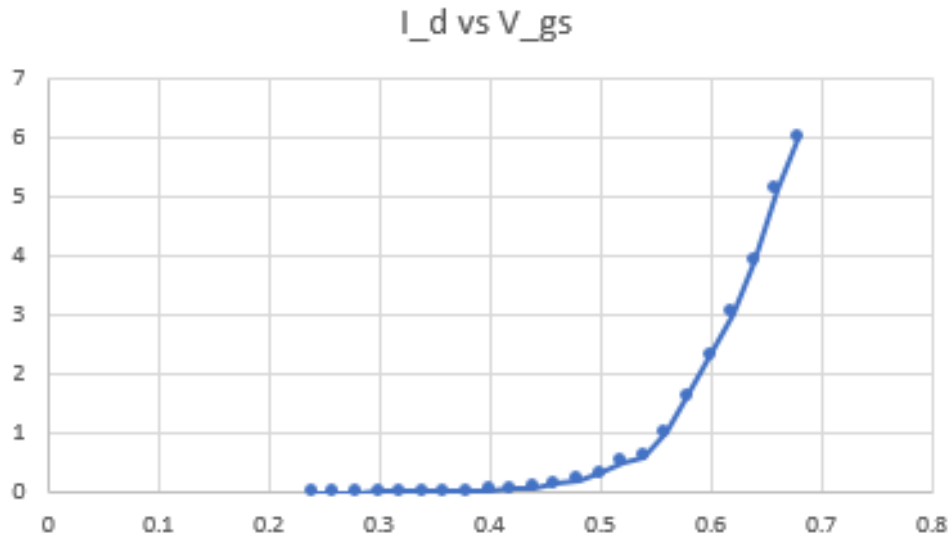

Figure 3.4: Plot for Id vs Vgs for Concatenated

Table 3.3: Values of I_d vs V_{gs} Concatenated

V_{gs} (V)	I_d (μA)	log(I_d)
0.00	–	-3
0.24	0.001	-3
0.26	0.001	-3
0.28	0.001	-3
0.30	0.002	-2.698970004
0.32	0.004	-2.397940009
0.34	0.006	-2.22184875
0.36	0.015	-1.823908741
0.38	0.021	-1.677780705
0.40	0.030	-1.522878745
0.42	0.055	-1.259637311
0.44	0.082	-1.086186148
0.46	0.144	-0.841637508
0.48	0.218	-0.661543506
0.50	0.311	-0.507239611
0.52	0.513	-0.289882635
0.54	0.600	-0.22184875
0.56	1.010	0.004321374
0.58	1.620	0.209515015
0.60	2.330	0.367355921
0.62	3.030	0.481442629
0.64	3.910	0.592176757
0.66	5.120	0.709269961
0.68	6.000	0.77815125

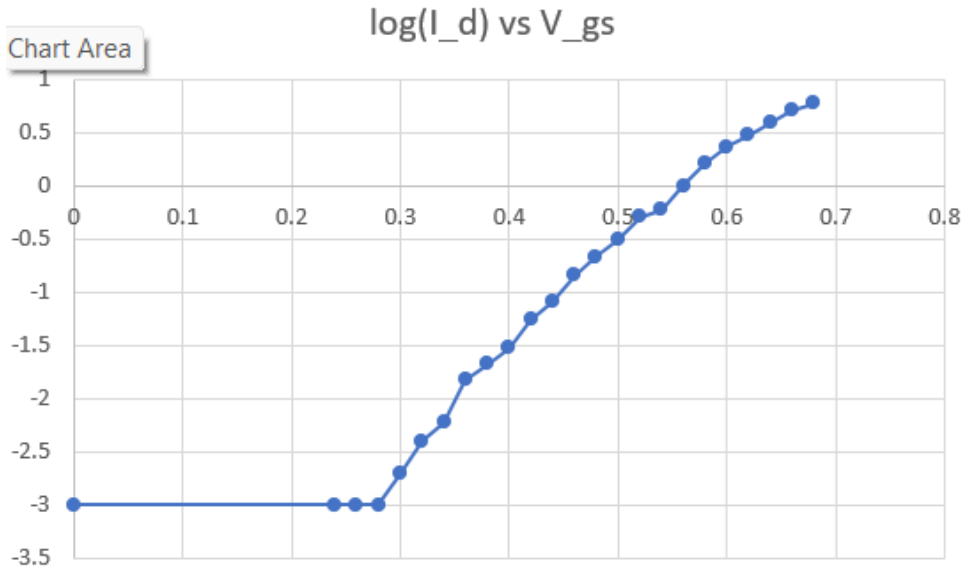

Figure 3.5: Plot for logId vs Vgs for Concatenated

3.1.3 Results Part 1

Step 1: Plot $\log_{10}(I_d)$ vs V_{gs}

We need to plot $\log_{10}(I_d)$ on the y-axis and V_{gs} on the x-axis. The slope of this plot will help us determine the Subthreshold Swing S.

Step 2: Find the Slope of $\log_{10}(I_d)$ vs V_{gs}

To find the slope $\frac{d(\log_{10} I_d)}{dV_{gs}}$, we use two points in the subthreshold region:

$$(V_{gs} = 0.3\,V,\ \log_{10}(I_d) = -2.699) \quad \text{and} \quad (V_{gs} = 0.6\,V,\ \log_{10}(I_d) = 0.367)$$

The slope is calculated as follows:

$$\text{Slope} = \frac{\Delta(\log_{10} I_d)}{\Delta V_{gs}} = \frac{0.367 - (-2.699)}{0.6 - 0.3}$$

$$\text{Slope} = \frac{3.066}{0.3} = 10.221$$

Step 3: Calculate Subthreshold Swing S

The Subthreshold Swing S is given by the inverse of the slope:

$$S = \frac{1}{\text{Slope}} = \frac{1}{10.221} = 0.09786\,\text{V/decade} = 97.86\,\text{mV/decade}$$

Step 4: Comparison with Ideal Value

For a long-channel transistor, $S \approx 60\,\text{mV/decade}$. Our calculated value of $S = 97.86\,\text{mV/decade}$ suggests a different value of η.

Step 5: Calculate η

The relationship for S in terms of η is:

$$S = 60\eta \,\text{mV/decade}$$

Solving for η:

$$\eta = \frac{S}{60} = \frac{97.86}{60} = 1.631$$

Conclusion

Since $\eta < 10$, the assumed value of $\eta \approx 1.6$ is confirmed, and no changes to V_{ds} are necessary.

3.2 Part 2: Verification of Continuity in Sub-threshold Region

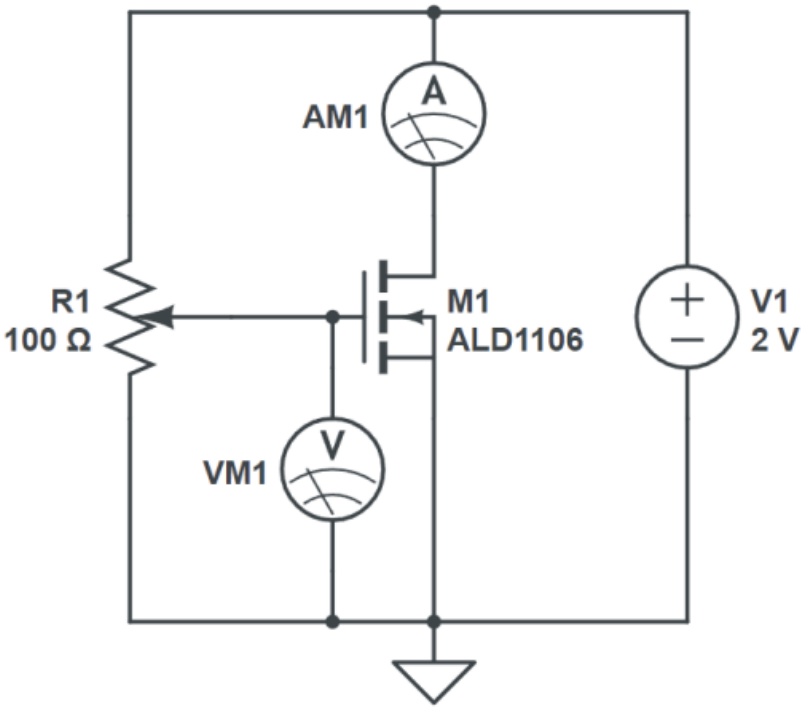

Figure 3.6: Circuit for Part2

The following results show the V_{gs} versus I_d and $\log(I_d)$:

Table 3.4: Continuity of I_d vs V_{gs}

V_{gs} (V)	I_d (μA)	$\log(I_d)$
0.00	–	-3
0.24	0.001	-3
0.26	0.001	-3
0.28	0.001	-3
0.30	0.002	-2.698970004
0.32	0.004	-2.397940009
0.34	0.006	-2.22184875
0.36	0.015	-1.823908741
0.38	0.021	-1.677780705
0.40	0.030	-1.522878745
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0.54	0.600	-0.22184875
0.56	1.010	0.004321374
0.58	1.620	0.209515015
0.60	2.330	0.367355921
0.62	3.030	0.481442629
0.64	3.910	0.592176757
0.66	5.120	0.709269961
0.68	6.000	0.77815125
0.78	19.000	1.278753601
0.88	33.000	1.51851394
0.98	62.000	1.792391689
1.08	95.000	1.977723605
1.18	135.000	2.130333768
1.29	199.000	2.298853076
1.38	242.000	2.383815366
1.48	291.000	2.463892989
1.59	382.000	2.582063363
1.69	455.000	2.658011397
1.78	521.000	2.716837723
1.88	591.000	2.771587481

Continuity of Characteristics

For V_{gs} beyond the sub-threshold region (approximately 0.7V to 1.9V), the following observations were made:

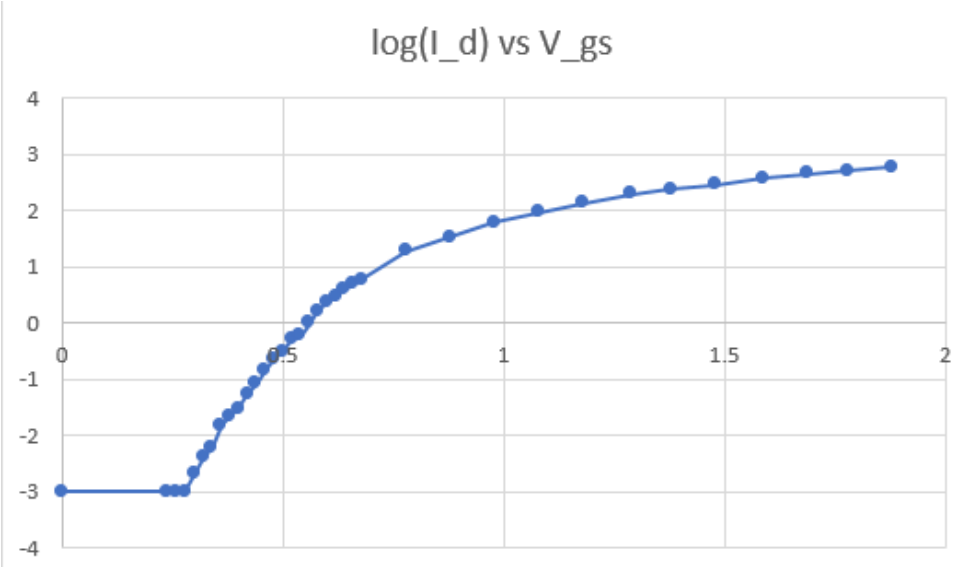

Figure 3.7: Plot of Subthreshold and Saturation Log(Id) vs Vgs

3.2.1 Results Part 2

1. **Measurement of V_{gs} and Corresponding I_d**:

   The values of V_{gs} were systematically increased in steps of 0.1V, starting from 0V and continuing until approximately 1.9V. The corresponding drain current (I_d) was recorded at each increment.

2. **Trend Analysis**:

   For V_{gs} values ranging from 0V to around 1V, the drain current I_d remains very low, indicating that the NMOS transistor is operating in the **subthreshold region**. The increase in I_d is gradual, reflecting the typical behavior of an NMOS in this region, where the current is controlled by the gate voltage but remains below the threshold.

3. **Transition to Strong Inversion**:

   Once V_{gs} exceeds 1V, a noticeable increase in I_d is observed. For example, at $V_{gs} = 1.0V$, I_d increases to 95 µA, and further increases in V_{gs} lead to significant jumps in I_d. This sharp increase signifies that the NMOS is transitioning from the subthreshold region into the **saturation or triode region**, where the device is fully turned on and exhibits a strong inversion characteristic. In this region, the channel is enhanced significantly, allowing a larger current to flow through the transistor.

4. **Final Readings**:

   At $V_{gs} = 1.9V$, the recorded current is 591 µA, demonstrating that the NMOS is well into the saturation region, confirming that it can effectively conduct higher currents.

5. **Conclusion**:

The data shows that as V_{gs} crosses the threshold of 1V, the NMOS no longer operates in the subthreshold region. Instead, it is clearly in the **saturation region**, where the current flow is governed by the gate-source voltage. This is an important consideration in the design and application of NMOS transistors in circuits.

3.3 Part 3: Common Source Amplifier Gain Calculation

Table 3.5: Common Source Amplifier Gain

$V_{out(pp)}$ (mV)	$V_{in(pp)}$ (mV)	Gain
125	52	2.404

3.3.1 Results Part 3

1. **Gain Analysis**:

   The calculated gain of the basic common source amplifier operating in the sub-threshold region is approximately 2.40. This gain, while lower than what is typically observed in the saturation region, is still sufficient for practical amplification purposes. The relationship between input and output signals can be expressed as:

   $$\text{Gain} = \frac{V_{out(pp)}}{V_{in(pp)}} = \frac{125 \text{ mV}}{52 \text{ mV}} \approx 2.40$$

   This indicates that even in the sub-threshold region, the amplifier can provide a meaningful level of amplification.

2. **Current Characteristics**:

   It is important to note that the currents in the sub-threshold region of operation are typically in the order of a few nanoamperes (nA). This significantly restricts the current-driving capability of the amplifier when compared to devices operating in the saturation region. As a result, amplifiers in the sub-threshold region are not suitable for applications that require high current outputs, as their performance is limited by these low current levels.

3. **Practical Implications**:

   Despite the limitations in current driving capacity, the gain observed is respectable, making the sub-threshold amplifier viable for specific applications, particularly in low-power or low-frequency contexts. However, for high-power applications, it is advisable to utilize amplifiers operating in the saturation region where higher gains and current capabilities can be achieved.

Conclusion

In this experiment, we successfully obtained the sub-threshold characteristics of NMOS and confirmed the continuity beyond sub-threshold. The Common Source Amplifier in sub-threshold region provided a gain of approximately 2.40.