Control of a Single-Stage Three-Phase Boost Power Factor Correction Rectifier

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***Abstract* - Advances in power electronics are enabling More Electric Aircrafts (MEAs) to replace pneumatic systems with electrical systems. Active power factor correction (PFC) rectifiers are used in MEAs to rectify the output voltage of the three-phase AC-DC boost converter, while maintaining a unity input power factor. Many existing control strategies implement PI compensators, with slow response times, in their voltage and current loops. Alternatively, computationally expensive non-linear controllers can be chosen to generate input currents with high power factor and low total harmonic distortion (THD), but they may need to be operated at high switching frequencies due to relatively slower execution of control loop. In this work, a novel control strategy is proposed for a three-phase, single-stage boost-type rectifier that is capable of tight and fast regulation of the output voltage, while simultaneously achieving unity input power factor, without constraining the operating switching frequency. The proposed control strategy is implemented, using one voltage-loop PI controller and a linearized transfer function of duty-ratio to input current, for inner loop current control. A 1.5 kW three-phase boost PFC prototype is designed and developed to validate the proposed control algorithm. The experimental results show that an input power factor of 0.992 and a tightly regulated DC link voltage with 3% ripple can be achieved.**

I. INTRODUCTION

Traditional three-phase variable voltage and variable frequency AC/DC rectification topologies in airplane generators utilize passive diode bridges and large DC link capacitors. Passive diode-bridge based rectifiers generate higher harmonics in the input current, have poor input power factor, create input voltage source disturbances, and lack output voltage regulation [1]. To alleviate these problems, recent progresses in high-speed, power semiconductor devices have facilitated the development of active switched-mode AC/DC converters that are controlled by pulse width modulation (PWM) techniques. The dominant topologies for active, single-stage PWM-based AC/DC conversion are boost-type [1-4], buck-type [5-6] and buck-boost type rectifiers [7-8]. Three-phase, boost-type power factor correction (PFC) converters have received attention due to their simple structure with less number of power semiconductor devices, less passive components and more importantly capability of continuous current conduction mode operation. Besides, three-phase buck-boost-type and buck-type AC-DC converter have drawbacks such as operation with discontinuous current conduction mode, higher amount of power semiconductor devices, and lower conversion efficiencies [7-9].

In addition to the fact that these aforementioned topological constraints limit the performance of several power converters, there is a significant and effective role, played by novelty of control methodology in enhancing the performance of any AC-DC converter. Implemented control algorithm acts as a crucial factor in governing power quality of the input current by limiting harmonics content of the PFC stage and also enhancing the conversion efficiency. A novel and noteworthy strategy, proposes a vectorial sliding mode input current control technique for a three-phase AC-DC buck-boost-type PFC [10], which is also applicable for a boost-type AC-DC rectifier with the objective of improving its power quality. Although the simplified vectorial control method is fast and offers robust control; however, considering non-idealities would lead to a computationally time expensive technique, which would limit the operational feasibility of the converter in high-end switching frequencies.

To improve upon existing strategies, and to offer a novel solution without any of the previously mentioned drawbacks, this paper proposes a new control strategy utilizing the input currents and output voltage of the converter. The main objective of the control strategy is to make the input current controller as fast and as robust as possible; to produce high quality input currents (low THD percentage and unity power factor). Instead of using a conventional control loop, that performs Park Transforms from the three-phase (abc) reference frame to the dq0 reference frame [11], our research thrust proposes an input current control structure that manipulates the reference duty ratio of each switch, in order to maintain an appropriate/desired input current shape. The final duty ratio value is derived from a weighted, cross-coupled sum of required change in duty ratios, which are obtained from both active and reactive power controller outputs. This control structure excels in two separate areas: (1) obtaining a fast and robust input current response (with high power factor quality); and (2) achieving a steady state response in a significantly less amount of settling time, under a step change in load or reference output voltage, as compared to conventional PI current compensators. Simply put, the

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control strategy put forth in this research thrust is simple, fast, and reliable – and is perfectly suited for implementation in the active three-phase boost rectifiers.

This paper is organized as follows. Section II introduces the three-phase AC-DC boost rectifier topology and explains the details of the proposed control strategy. Device selection details and their specifications are provided in Section III. In Section IV, the simulation and experimental results of the designed converter, which is controlled with proposed control strategy, considering some of the specifications for regulated transformer rectifier unit (RTRU) applications in MEAs, are presented and analyzed. Section V evaluates the power loss and efficiency calculation of the converter. Finally, Section VI puts forward conclusions with relevant discussions.

II. Topology And Control Of A Three-Phase Active Boost Rectifier

A. Topology

The overall structure of a three-phase active boost-type rectifier is shown in Fig. 1. In this topology, there are three inductances in series with the AC source. These inductances help to boost the input AC voltage and filter the input current, thus reducing the harmonic contents. The top and bottom set of MOSFETs are switched in a complementary fashion with a fixed deadband. In order to reduce the forward conduction losses, three pairs of diodes are placed in anti-parallel combination with the power MOSFETs. These three external diodes are chosen to be of Schottky type, with less ON-state resistance than existing internal body diodes of the MOSFETs. Thus, the effective path resistance while forward conduction reduces.

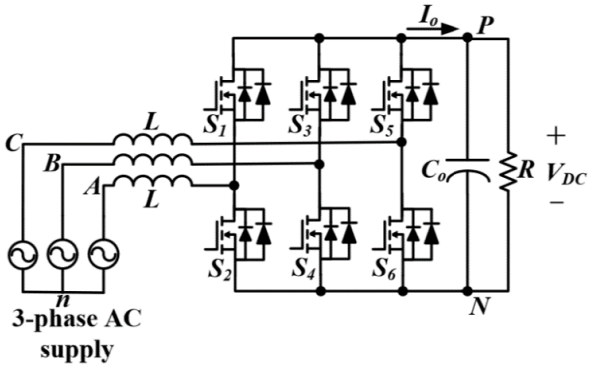


Fig. 1. Three phase boost-type rectifier.

B. Control Strategy

The nomenclatures used in this paper are summarized in Table I.

TABLE I: List of nomenclatures

Symbol	Description
D	Duty ratio
C_o	Output capacitor value
V_{DC}	Output voltage
I	RMS current through inductor L
V_{DC_min}	Minimum possible output DC link voltage in this topology
i_d	Direct current
i_q	Reactive current
i_m^* *or* v_m^*	Reference current or reference voltage for m^{th} term; (i_a, i_b, i_c) are the input phase 'a', 'b', 'c' currents, respectively

This paper proposes a linear control technique, which uses small signal transfer functions of the converter, derived from the state-space averaging techniques, applied on different modes of operations. State-space averaging techniques allow for reduced computational efforts, and linearize systems around certain operating points. The state-space averaging method is chosen to control the rectification process, due to the fact that the voltage and current transients reach steady state with less oscillation than other methods; zero-order approximations, as an example, are more oscillatory [13]. Using state-space averaging, the small signal transfer function of the three-phase boost-type rectifier [1, 10], shown in Fig. 1, can be derived as shown in eq. (1).

$$T(s) = G_{vd}(s) = \frac{v_o(s)}{d(s)} = \frac{(ILR)s - R(1-D)(V_{DC} - V_{DC\_\min})}{RLC_o s^2 + Ls + R(1-D)^2} \quad (1)$$

The transfer function in eq. (1) has a zero, shown in Eq. (2).

$$s = \frac{V_{DC}(1-D) + V_{DC\_\min}(D-1)}{LI} \quad (2)$$

Due to the existence of a right half zero, this AC/DC converter acts as a non-minimum phase system [1]. The zero is located in the right half plane because $V_{DC} > V_{DC\_min}$, where V_{DC_min} is the output voltage of the uncontrolled diode-bridge configuration of three-phase active boost rectifier. If any system contains a right-half zero, the dynamic response in output voltage and input current is significantly slower, in comparison to a system with a left-half-plane zero and equivalent gain response [8]. Due to the characteristics of the zero, tuning the control circuit of the rectifier becomes difficult and is best suited for operation only in a particular region. However, since filter components of the converter must be designed to allow for faster input current dynamics, rather than output voltage dynamics, it is obligatory to segregate the dynamics of the input current from the output voltage. Moreover, a cascaded control system can be implemented on a system with separated dynamics [10]. Considering these facts, a suitable control structure is proposed in this paper.

The control goal for the three-phase boost rectifier is to generate sinusoidal input currents in phase with the input voltages, and regulate the DC output voltage. To operate with unity power factor, the reference reactive power should

be set as 0 and active power should be set as the total nominal power of the converter. It also implies that in dq control method, the projection of input line current should be 0 on the quadrature axis and its entire projection should lie on direct axis. Thus, the real power and reactive power can be regulated by controlling direct current (i_d) and quadrature current (i_q), respectively. Utilizing Park transforms, as part of our control effort, allows the input line currents, $\{i_a, i_b, i_c\}$ to be transformed into the dq-domain currents, $\{i_d, i_q\}$, as demonstrated in eq. (3) and eq. (4).

$$i_d = -\frac{2}{3}[i_a \cos(\omega t) + i_b \cos(\omega t - 2\pi/3) + i_c \cos(\omega t + 2\pi/3)] \quad (3)$$

$$i_q = -\frac{2}{3}[i_a \sin(\omega t) + i_b \sin(\omega t - 2\pi/3) + i_c \sin(\omega t + 2\pi/3)] \quad (4)$$

Applying derivative on both sides of eq. (3) and (4), we get:

$$\partial i_d = -\partial i_a \cos(\omega t) + \frac{1}{\sqrt{3}}(\partial i_a + 2\partial i_b)\sin(\omega t)] \quad (5)$$

$$\partial i_q = -\partial i_a \sin(\omega t) + \frac{1}{\sqrt{3}}(\partial i_a + 2\partial i_b)\cos(\omega t)] \quad (6)$$

In order to achieve unity input power factor, reference quadrature component of line current, i_q, is set to zero. The DC-bus voltage is regulated by controlling the real power through controlling the direct component of line current, i_d. The instantaneous output power of the converter can be presented by eq. (7).

$$P = v_a i_a + v_b i_b + v_c i_c \quad (7)$$

Assuming the converter to be ideal, we can derive eq. (8) using the input and output power balance, considering a resistive output load.

$$v_o^2 = R(v_a i_a + v_b i_b + v_c i_c) \quad (8)$$

Considering a balanced 3-phase system, i.e. $v_a+v_b+v_c=0$, eq. (8) can be written as:

$$v_o^2 = R \cdot [i_a(v_b + 2v_a) + i_b(v_a + 2v_b)] \quad (9)$$

Differentiating both sides of the equality in eq. (9) with respect to time, leads to the following relationship in eq. (10).

$$2v_o \frac{\partial v_o}{\partial t} = R[\frac{\partial i_a}{\partial t} \times (v_b + 2v_a) + i_a \times (\frac{\partial v_b}{\partial t} + 2\frac{\partial v_a}{\partial t}) + \frac{\partial i_b}{\partial t} \times (v_a + 2v_b) + i_b \times (\frac{\partial v_a}{\partial t} + 2\frac{\partial v_b}{\partial t})] \quad (10)$$

Replacing $v_a=k_1 i_a$, $v_b=k_2 i_b$, and $v_c=k_3 i_c$; assuming PFC operation of the converter (where k_1, k_2, k_3 are zero-phase constants), eq. (11) and eq. (12) can be derived.

$$\frac{\partial i_a}{\partial d} = \frac{\partial v_o / \partial d}{\partial v_o / \partial i_a} = \frac{T(s)}{R \cdot [4k_1 i_a + (k_1 + k_2) i_b]} \quad (11)$$

$$\frac{\partial i_b}{\partial d} = \frac{\partial v_o / \partial d}{\partial v_o / \partial i_b} = \frac{T(s)}{R \cdot [4k_2 i_b + (k_1 + k_2) i_a]} \quad (12)$$

The output of the voltage compensator generates a direct current reference, i_d corresponding to active power. The direct component error, of the line current, followed by an equivalent linearized transfer function of $\delta d/\delta i_d$, generates the required change of duty ratio to control the active power, Δd_d. The error in the quadrature component of the line current, followed by an equivalent linearized transfer function of $\delta d/\delta i_q$, generates the required change of duty ratio to control the reactive power, Δd_q .

$$\Delta d = \frac{\partial d}{\partial i_d}(\Delta i_d) + \frac{\partial d}{\partial i_q}(\Delta i_q) \quad (13)$$

The two obtained perturbations in the duty ratios, Δd_d and Δd_q, followed by two gains G_1 (d-loop) and G_2 (q-loop), respectively, add together and generate the total change in the reference duty ratio, Δd, to achieve the reference input

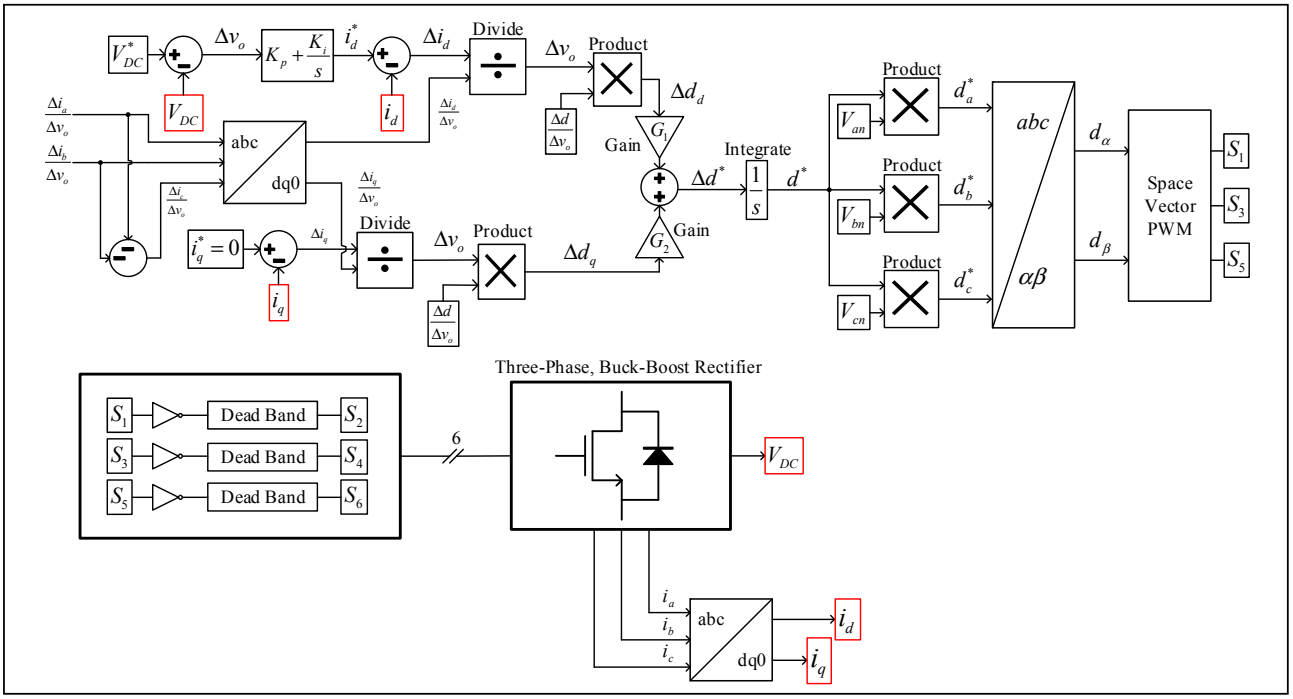


Fig. 2. Control Structure of the Single-Stage, Three-Phase Boost AC/DC Converter.

currents. Taking the integral of the change in the reference duty ratio, Δd, followed by a saturation block (0 to 1), gives the amplitude of the operating duty ratio, from which the phase duty ratios are derived. The individual phase duty ratios are followed by an ABC to αβ transformation. The duty ratios in the $\alpha\beta$ reference frame, $\{d_\alpha, d_\beta\}$, are then fed to a Space Vector PWM block, which generates switching pulses for the converter.

III. Device Selection

The selection of MOSFETs and power diodes depends on input voltages, output DC link voltage, and the converter power rating. Considering 208V RMS (line-line), 400Hz input AC supply, the derived output voltage boundary, between buck and boost mode operations for the converter, is the line-to-line peak voltage; i.e. $208\sqrt{2} = 295V$. Hence, the minimum possible DC link voltage generated by this boost PFC topology is 295V, using SVPWM switching technique. The application in this paper mainly focuses on a RTRU unit inside a MEA, which typically has the second stage of an isolated DC-DC resonant converter. With a higher DC link voltage, the second stage isolated converter would need a transformer with high step-down ratio and hence, more number of turns, which could potentially increase the size of the transformer and the magnetic core loss. In addition, at a higher DC link voltage, the voltage stresses across switches would be higher and result in degrading the efficiency due to more switching losses. Therefore, DC link voltage is regulated at 400V, which leads to a modulation index of 0.74. The reference value of DC link voltage would appear across the parallel combination of a MOSFET and a diode pair. Hence, the maximum voltage stress (V_{SW}) across each MOSFET is 400V.

Under specified DC link voltage ripple requirement, output capacitance (C_o) can be obtained from the fact that capacitor current is the difference between sum of top-leg phase currents and load current, which is provided in eq. (14):

$$\sum_{\substack{i,j=A,B,C \\ i\neq j}} (I_i + I_j) - \frac{V_o}{R} = \frac{\Delta Vo}{\Delta T} C_o \qquad (14)$$

where, ΔT is ON period of a lower leg MOSFET of any phase in a switching cycle and I_i, I_j represent currents of the phases, whose upper leg switches are conducting at any time. An output capacitance of 100 μF ensures an output voltage ripple of less than 0.8% (peak-peak). But an output capacitor less than 100 μF results in large undershoot (>15%) during a load step up transient of 100% at the output.

The absolute maximum voltage rating of the power MOSFETs have been chosen based on the fact that it must never be exceeded during operation, irrespective of any fluctuation in input voltage or load transient. A sudden drop in load current could potentially create an overshoot as high as twice of DC link voltage. Therefore, typically the rating should be chosen at least twice of DC link reference voltage. Though 800V Si-based MOSFET satisfies our requirements, its power loss is more than 1.2 kV SiC MOSFETs at high-end switching frequency operation, which is required for improving the power quality of the converter. Hence, APT40SM120B (1.2 kV, SiC MOSFET) has been selected. Furthermore, 1.2 kV SiC Schottky diode C2D05120 has been chosen, because it satisfies the current and voltage stress requirements with low forward voltage drop and also incurs lower reverse recovery loss. On a nutshell, all the discussed key parameters and power devices of the prototype are listed in Table II.

TABLE II: Component details of boost PFC design

Symbol	Device	Part number
S_1-S_6	SiC Power MOSFET	APT40SM120B
D_1-D_6	SiC Power Schottky diodes	C2D05120A
L	Input inductors	AS225-125A toroid core
C_o	DC link capacitor	DCP4P055009J (polypropylene film capacitor)

IV. Simulation And Experimental Results

The converter is simulated with an input AC voltage of 120V (phase-neutral RMS) at 400 Hz for avionics applications; these specifications are chosen, as they are consistent with the specifications of some of the RTRUs in future MEAs. The simulations are performed in MATLAB-Simulink. The rated power of the simulated converter is 1.5 kW. Fig. 3 provides the simulation results of the converter in boost mode, and also validates the PFC operation with voltage regulation of the converter. The design parameters of the simulated converter include input inductor (L) of 0.3 mH, output capacitor (C_o) of 100 μF and switching frequency of 150 kHz. During the simulation, at 20 ms, the output load power is increased from 1.5kW to 2.25kW. The 2% settling time of the output DC voltage is 7 ms with proposed control, which is faster as compared to a PI compensator that takes 15 ms to reach 2% settling band. The proposed control is able to achieve a unity PFC operation, and 2.3% input current THD.

An experimental prototype of 1.5 kW, with control logic being implemented in DSP (TMS320F28335), is built as a proof-of-concept verification of theoretical analyses. Programmable DC electronic load (BK Precision 8512) has been used for load emulation in this PFC experiment. Photos of the three-phase-boost PFC board and entire experimental setup are shown in Fig. 4.

Table III represents the experimental specification details of the converter in terms of input voltage, output voltage, and load power.

TABLE III: Rating specifications of the PFC

Parameters	Specifications
Input voltage	3-phase 120V RMS (phase-neutral), 400Hz
DC link reference	400V
Load power	1.5kW

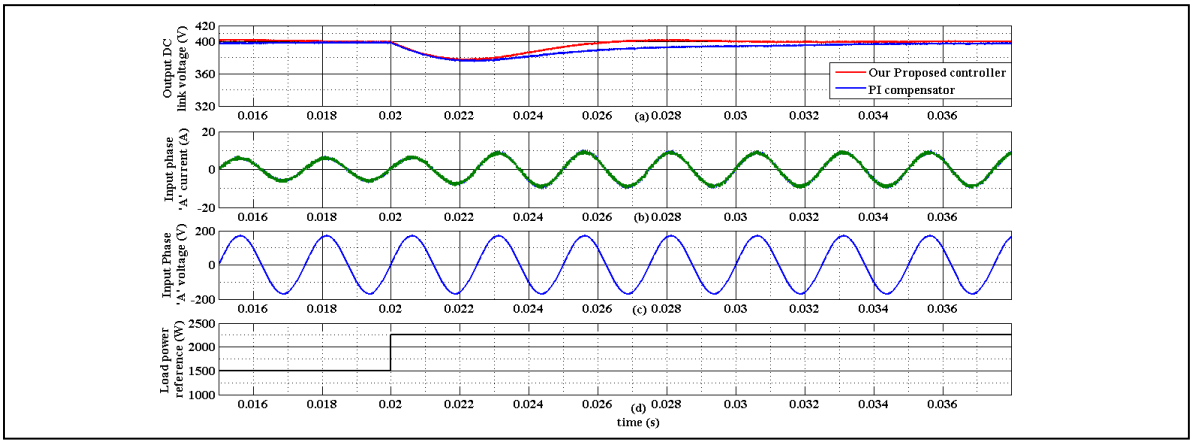


Fig. 3. (a) DC link voltage (V) with our proposed control and PI compensator; (b) Phase 'A' current (A) with our proposed control and PI compensator; (c) Phase 'A' input voltage (V) (d) Output power reference (W).

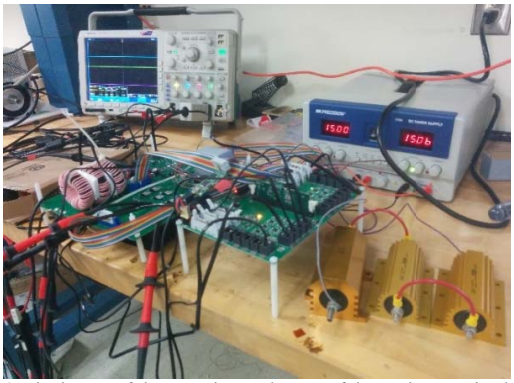


Fig. 4. The image of the experimental setup of three-phase active boost rectifier.

As Fig. 3 demonstrates, the Fig. 5 shows the boost mode operation of the PFC converter with proposed control logic and represents the stable and settled down output DC link voltage of the PFC. The DC link voltage is regulated at 400V with a ripple of ±2.5% (10V), as implied by Fig. 5(a). As shown in Fig. 5(b) and Fig. 5(c), the input phase current is in phase with the corresponding phase voltage and thus, demonstrates its PFC operation with an input power factor more than 0.99 and a THD below 5%. The output voltage spikes are caused by the acquisition inaccuracy of the voltage probe Tektronix-MDO3014. At 1.5 kW operation, THD and conversion efficiency are measured at 4.8% and 97.5%, respectively.

V. Loss And Efficiency Calculation

Total power loss in the closed loop PFC system arises from switching, MOSFET conduction and diode conduction voltage drop. The switching loss (P_{SW}) and diode loss (P_{diode_loss}) [1-2] are given by the equations (15) – (17):

$$P_{SW} = P_{SW_{ON}} + P_{SW_{OFF}} = \frac{I_D V_{DS} f_S (t_{on} + t_{off})}{6} \quad (15)$$

$$P_{diode\_loss} = V_f I_{d\_avg} \quad (16)$$

$$I_{d\_avg} = I_a \frac{6 + \sqrt{3}\pi M}{12\pi} \quad (17)$$

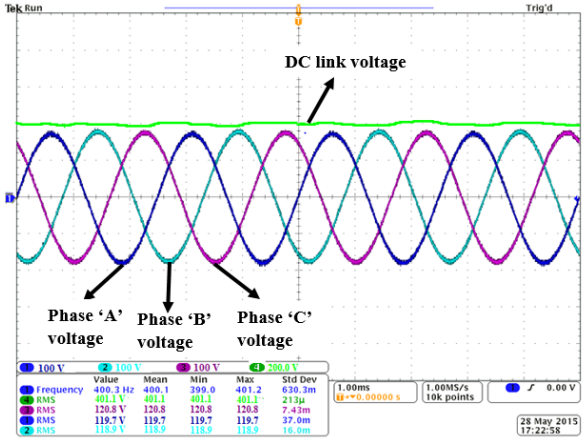
The switch conduction loss (P_{cond}) [2] is governed by the eq. (18) and eq. (19).

$$P_{cond} = I_{RMS}{}^2 R_{ON} \quad (18)$$

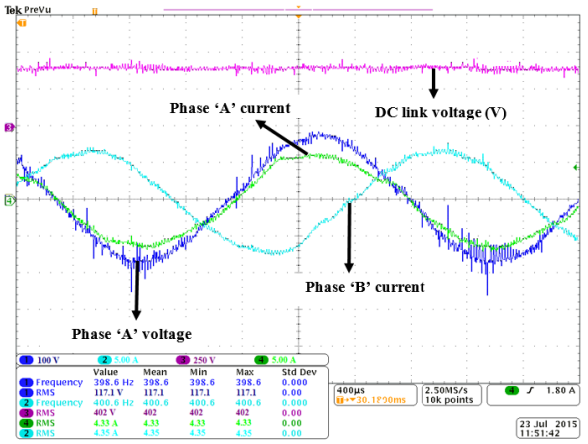
$$I_{RMS} = I_a \sqrt{\frac{4\pi + \sqrt{3}(3 + 4M)}{24\pi}} \quad (19)$$

In the above equations, t_{on} and t_{off} represent the turn-on and turn-off times for the MOSFET and 'M' is the modulation index; I_a is the RMS current of phase 'A'.

Total switching, conduction and diode loss are 15W, 7.5W, 3W respectively, as obtained from theoretical calculation. It leads to an expected efficiency of 98.3%. From the experimental data, total power loss is 40W and hence, obtained efficiency is 97.5%, which closely matches theoretical estimation. Thus, it proves an accurate modelling and precise implementation of our control logic.



(a)



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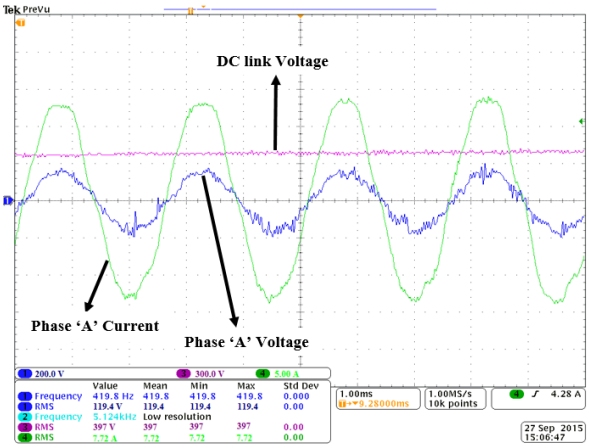

(c)

Fig. 5. Experimental waveforms of the converter (a) 3-phase input voltage and DC link voltage; (b) Phase 'A' voltage and current, Phase 'B' current, DC link voltage; (c) Phase 'A' voltage & current, DC link voltage

VI. CONCLUSION

In this paper, a novel control methodology, which sets forth a linearized transfer function of duty-ratio to input current, for inner loop control of a three-phase active boost rectifier, has been proposed, analyzed and developed. This strategy has the advantage of faster transient response and also is of less computational complexity than most of the conventional linear control algorithms. The feasibility, suitability and advantages of the proposed control method are discussed, and the design guidelines are provided through the theoretical analyses for a three-phase boost-type rectifier. As a case study, design considerations for a 1.5 kW PFC hardware prototype, which converts 70-120V, 400Hz AC to 400V DC, are provided.

The obtained experimental results demonstrate and verify that an efficiency of 97.5% at 150 kHz switching frequency, an input power factor of 0.993, a THD as low as 4.8% and a tight regulation of output DC link voltage of the converter within ±3% band can be achieved with the proposed control logic without constraining the operating switching frequency. Furthermore, the proposed control ensures the system dynamics and settling to be faster than conventional PI compensator, while undergoing a step change in load power. Hence, the proposed control strategy shows promising performance for 3-phase boost PFC and can be extended to be applied on other single and three phase AC-DC converters with similar plant characteristics for high-switching frequency applications.

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REFERENCES

[1] J. W. Kolar, M. Hartmann, and T. Friedli, "Three-phase PFC rectifier and AC-AC converter systems," Tutorial at the *26th Annual IEEE Applied Power Electronics Conference and Exposition*, Fort Worth, TX, USA, Mar. 2011.

[2] J. W. Kolar and T. Friedli, "The essence of three-phase PFC rectifier systems," in *Proc. IEEE International Telecommunications Energy Conference (INTELEC),* Amsterdam, Oct.2011.

[3] A. Mallik and A. Khaligh, "Comparative study of three-phase buck, boost and buck-boost rectifier topologies for regulated transformer rectifier units," in *Proc. IEEE Transportation Electrification Conference and Exposition*, Dearborn, MI, Jun. 2015.

[4] S. L. Sanjuan, "Voltage oriented control of three - phase boost PWM converters," Master of Science Thesis in Electric Power Engineering, Chalmers University of Technology, Sweden, May 2010.

[5] F. Xu, B. Guo, L.M. Tolbert, F. Wang, and B. J. Blalock, "Evaluation of SiC MOSFETs for a high efficiency three-phase buck rectifier," in *Proc. IEEE Applied Power Electronics Conference and Exposition* , Orlando, FL, Feb. 2012, pp.1762-1769.

[6] A. Stupar, T. Friedli, J. Minibo□ck, M. Schweizer, and J.W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400 V DC distribution systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition,* Fort Worth, TX, Mar. 2011, pp.505-512.

[7] C.T. Pan and T.C. Chen, "Step-up/down three-phase AC to DC converter with sinusoidal input current and unity power factor," *Proc. IEEE*, vol. 141, pp. 77-84, Mar. 1994.

[8] Y. Nishida, A. Maeda, and H. Tomita, "A new instantaneous-current controller for three-phase buck-boost and buck converters with PFC operation," in *Proc. IEEE Applied Power Electronics Conference and Exposition,* Dallas, TX, 1995, Mar. 1995, pp. 875-883.

[9] Y. Nishida and A. Maeda, "A simplified discontinuous-switching-modulation for three-phase current-fed PFC-converters and experimental study for the effects," in *Proc. IEEE Applied Power Electronics Conference and Exposition,* San Jose, CA, Mar. 1996, pp. 552-558.

[10] V. F. Pires, and J.F.A. Silva, "Single-stage three-phase buck-boost type AC-DC converter with high power factor," *IEEE Transactions on. Power Electron.*, vol.16, no.6, pp. 784-793, Nov. 2001.

[11] Z. Shen, M. Jaksic, B. Zhou, P. Mattavelli, D. Boroyevich, J. Verhulst, and M. Belkhayat, "Analysis of Phase Locked Loop (PLL) influence on DQ impedance measurement in three-phase AC systems," in *Proc. IEEE Applied Power Electronics Conference and Exposition,* Long Beach, CA, Mar. 2013, pp. 939-945.

[12] H. Wei and I. Batarseh, "Comparison of basic converter topologies for power factor correction," in *Proc. IEEE Southeastcon,* Orlando, FL, Apr. 1998, pp.348-353.

[13] J. Mahdavi, A. Emaadi, M. D. Bellar, and M. Ehsani, "Analysis of power electronic converters using the generalized state-space averaging approach," *IEEE Transactions Circuits Syst. I, Reg. Papers*, vol.44, no.8, pp.767-770, Aug. 1997.

[14] Y. Lee, A. Khaligh, and A. Emadi, "A compensation technique for smooth-transitions in non-inverting buck-boost converter," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 1002-1015, Apr. 2009.