TFE4575: Fabrication of 675 nm wavelength LEDs

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Abstract

Light emitting diodes (LED) are widely used light producing electrical components. Producing LEDs is a micro- and nanotechnological processes. In this report, a premade multi-layered semiconductor wafer is used to produce LEDs. The wafer have been processed by strategically using photolithography, deposition, and etching. The LED have been characterized using an optical microscope, a scanning electron microscope, a profilometer, an ellipsometer and a SourceMeter. The characterizations revealed that some process steps resulted in minor defects. However, measurements of the IV-characteristics of the LEDs have been performed, and it confirmed that the LEDs are working as diodes. With voltage at 1.7 V and current at 30 mA the LEDs emits red light, which is the around the target wavelength of 675 nm.

Contents

1. Introduction

LEDs (Light Emitting Diode) are, as the name suggests, a type of electrical component producing light. They are widely used due to their low power consumption, long lifetime, small size, and fast switching [1]. LEDs are made up of strategically layered semiconductors and metals. Then, in order to produce a working diode, the layered stack needs to undergo several process steps. Some of these can be photolithography, etching, deposition, and annealing. After, the LEDs should be characterized and tested, e.g. by scanning electron microscopy (SEM), optical microscopy and current-voltage (IV) testing.

2. Theory

2.1. LED theory

In its most simple form, a LED is a p-type semiconductor (SC) in contact with a n-type SC, i.e. a pn-junction [2]. In the region close to the contact area of the two SC materials, electrons and holes will recombine. This leaves a negative charge on the p-type SC and a positive charge on the n-type SC, creating an electric field. The region where this electric field is present is called the depletion region, and will under normal conditions be depleted of charge carriers. When a voltage is applied over the pn-junction, electrons and holes are pushed into the depletion region where they recombine. This can either happen non-radiatively or radiatively, where the latter is the process that emits light.

2.2. Photolithography

This section is based on Quirk and Serda's book *Semiconductor Manufacturing Technology* [3].

Photolithography is used to print micro- and nanoscale structures on a substrate. This is done by coating the substrate in a light-sensitive photoresist and strategically exposing it to light. The photoresist will then either harden or dissolve depending on the type. Negative resist gets insolvable in the developer when exposed to light, while positive gets solvable. As a consequence, the mask used with a negative resist must be the inverse of the desired structure, while with positive resit, the structure must be identical. The process should be done in a cleanroom, as it is very sensitive to contaminations. The following list gives the name and purpose of the eight main steps in the photolithography process:

1. **Vapor prime**: Remove contamination from the substrate.
2. **Spin coating**: Spin coat the photoresist on the substrate.
3. **Soft bake**: Bake the photoresist to remove solvent.
4. **Exposure**: Align the mask and expose certain areas of the photoresist to light.
5. **Develop**: Develop the photoresist to remove the soluble parts.
6. **Post exposure bake**: Bake the photoresist to initiate resist reactions for deep UV resists and enhance adhesion.
7. **Hard bake**: Bake the photoresist to remove more solvent. Not often needed.
8. **Inspect**: Optical inspection of the photoresist to verify the quality of the pattern.

Lift-off is a technique used to remove the photoresist from the substrate after metallization. When doing lift-off, it is most common to use negative resist. This is because only negative resist can achieve an undercut resist profile, which can improve the metal edges.

Different photoresists need different baking parameters, spin speeds, developing times and exposure doses. The parameters can change for the same resist over time, e.g. when the resist is exposed to light, heat, humidity, or contaminations.

2.3. Contacts, etching and passivation

This subsection is based on the laboratory manual for TFE4575 [4].

LEDs need to have both a front and back metal contact. The purpose of the contacts are to provide a path so that current can be injected to the device. The back contact can simply be deposited on the whole back side of the wafer. The front contact however, needs to be patterned. In order to reduce absorption losses, the contact area needs to be minimized while keeping the spreading resistance as low as possible. It is important to carefully chose the contact material, as it affects the electrical properties of the device. Also, the front side contracts should be made first, as the following steps may damage the surface.

Etching is a process of chemically removing material from a surface. The process can be divided into two categories - wet etching and dry etching. Wet etching uses a liquid etchant, while dry etching uses a gas etchant. In LED fabrication, etching is an important process step. Here, etching is typically used to remove strongly light absorbing layers or to electrically isolate different parts of the device.

Exposed sides of the LED will result in high non-radiative recombination at the surface, which will reduce the efficiency of the LED. Also, exposed sided increases the risk of shorting the circuit. For those two reasons, it is necessary to coat the LED surface in a passivation material, e.g. Si_3N_4. The deposition of this layer should be done by an isotropic deposition method to ensure that the layer cover both horizontal and vertical edges. One such method is plasma enhanced chemical vapor deposition (PECVD). The thickness of the layer should be such that the optical path creates destructive interference at the wavelength of the emitted light λ. This relation is given by

$$2d = \frac{\lambda}{n}\frac{3}{2} \tag{1}$$

where d is the thickness and n is the refractive index.

2.4. Equipment

The theory and working principle behind the tools and instruments used in this lab is assumed to be known. The manufacturing equipment used were hot plate, spin coater, MLA (Maskless aligner) photolithography tool, PECVD, and annealing furnace. The characterization equipment used were optical microscope, SEM, profilometer, ellipsometer, and source meter.

3. Methods

The layered LED sample is shown in Figure 1 was grown by the staff of the course. To form working LEDs from the wafer, the following steps were done at NTNU NanoLab:

1. Front contact formation
2. GaAs contact layer etch
3. Backside contact formation
4. Mesa etch, PECVD passivation deposition, and contact annealing
5. Planarization and passivation layer etch
6. Pad metallization

Each step was first done with a GaAs dummy sample to check that the process was working as intended. After the last step, the IV-characteristics of the LEDs were inspected.

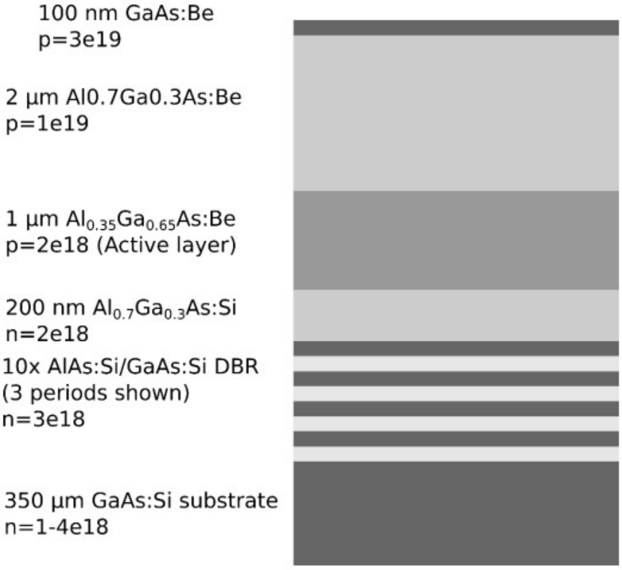


Figure 1: The layered LED sample made by the staff of the course. The layers were grown in the MBE, molecular beam epitaxy, machine at NTNU NanoLab. Figure borrowed from the lab manual [4].

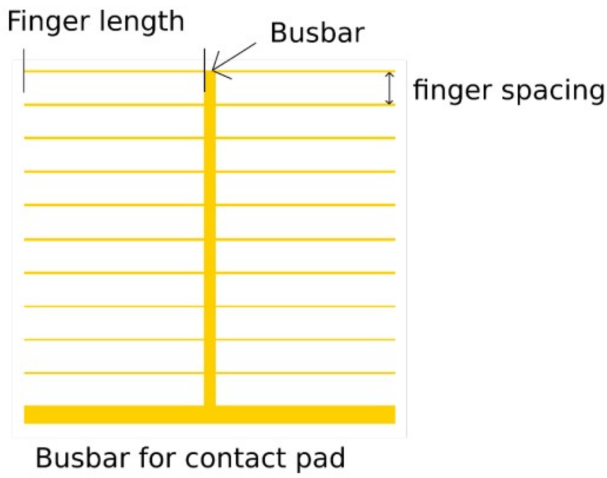


Figure 2: Schematic of the LED design. Figure borrowed from the lab manual.

3.1. LED design

Different finger spacings and finger widths were tested. An overview schematic of the LED design is shown in Figure 2. One LED was 1 mm x 1 mm. The bus bar for contact pad was 1 mm x 40 µm. The bus bar connecting the fingers was 1 mm x 30 µm. The fingers were 500 µm long, with widths at 4, 8, 12 and 16 µm, and finger spacings at 40, 60, 80 and 100 µm. The first lithography layer is shown in Figure 3. The second lithography layer, Figure 4, was equal to the first, but scaled with a 5 µm buffer everywhere to protect the fingers. The third lithography layer, Figure 5, was for the mesa etch, and was a box around each LED with a 6 µm buffer. The fourth lithography layer, Figure 6, was for the etch of the passivation layer, and was a 30 µm x 980 µm box on each bottom bus bar. The fifth and final lithography layer, Figure 7, was for the pad metallization, and was a 1000 µm x 800 µm box at the bottom of each LED connected to the bottom bus bar. Schematics of the different layers are shown in Figure 3 to Figure 7. Schematics of the alignment marks in layer 1 and layer 2 is shown in Figure 8.

3.2. Front contact formation

The bus bars and their fingers, i.e. the front contacts, were formed with lithography and lift-off. A dose test was done to find the optimal dose and developing time for the resist, ensuring an undercut. To verify this, both a SEM image and optical images of the sample were taken. The optimal dose for MAN 440 was 1300 mJ/cm^2 and the optimal developing time was 5 minutes. The hot plate temperatures are from the NanoLab hot plates in the student lab area, which have not been calibrated in a long time and can have some uncertainties. Negative photoresist was used, and the steps were done in the following order:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 150 °C for 5 minutes.
3. Spin coated MAN 440 resist at 4000 rpm for 30 seconds with 1000 rpm/s acceleration.
4. Cleaned the backside.
5. Soft baked at 95 °C for 1 minute.
6. Exposed the pattern at 1300 mJ/cm^2 in the MLA.
7. Developed in maD-332S developer for 5 minutes.
8. Optical inspected the pattern.
9. Teaching assistants metallized the wafer with a Pd/Ti/Pt/Au stack, referred to as the Au fingers.
10. Lift-off with acetone.

Unfortunately, a mix-up of the type of developer was done, and the process had to be repeated. The optical inspection before round number two showed some contamination on the wafer, which was probably caused by the wrong developer. The wafer was cleaned thoroughly with acetone and IPA before the second round, but some contamination might have been left behind.

Another problem was that the dose test were done with a resist that got emptied, and a newer resist had to be used for the actual process. When using the new resist the developer time was increased from 5 to 6 minutes, which gave an undercut but damaged the alignment marks and the thickest and closest fingers.

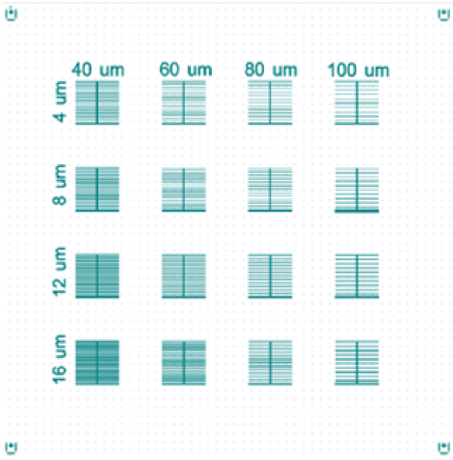


Figure 3: Layer 1. Numbers on the top is the spacing between the fingers in the LED matrix. Numbers on the left side is the width of the fingers in the LED matrix. Each LED is 1 mm x 1 mm. Alignment marks for layer 1 are in the corners.

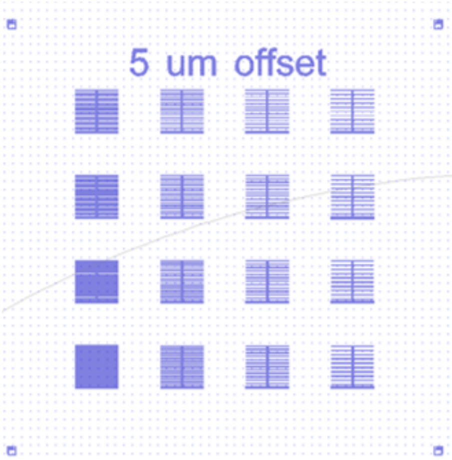


Figure 4: Layer 2. This is the same as layer 1, but with a 5 µm buffer on the whole pattern.

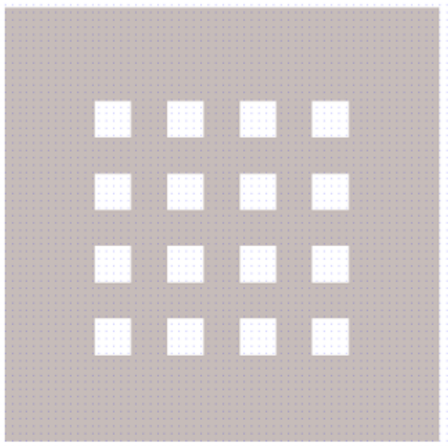


Figure 5: Layer 3. This is the mesa etch layer. The size of the box covering each LED is 1.012 mm x 1.012 mm.

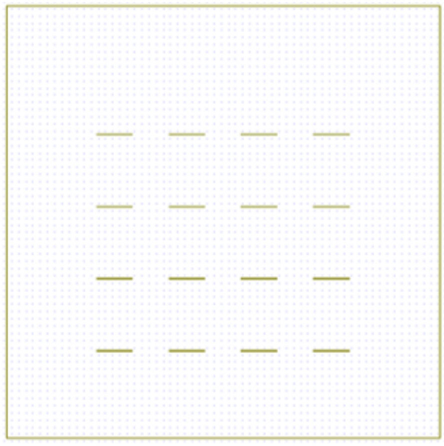


Figure 6: Layer 4. This is the HF etch layer. Each bar is covering a part of the bottom bus bar, with a size of 30 µm x 980 µm.

Figure 7: Layer 5. This is the pad metallization layer, where each box is 1 mm x 0.8 mm. The box is covering the bottom bus bar of each LED.

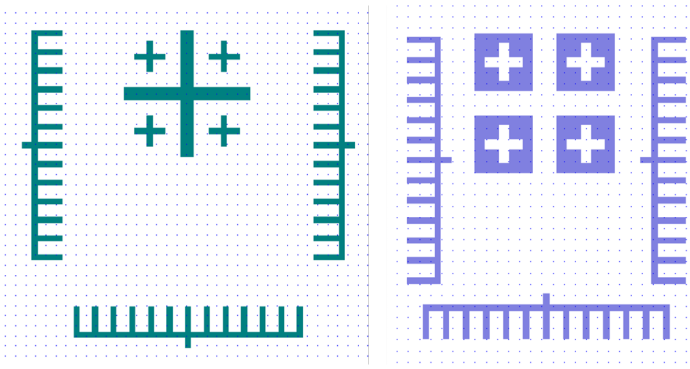


Figure 8: Alignment marks for layer 1 on the left and layer 2 on the right. The design allows quantification of the alignment error. These marks are the Verniers design.

3.3. GaAs contact layer etch

The heavily p-doped GaAs layer at the top of the metal stack was etched away to allow light to pass out of the LED. The deposited Au fingers were measured to be 250 nm high in the profilometer. Measuring the Au height was important for the later measurement of the etch depth of the 100 nm GaAs layer. The Au fingers were protected with a positive photoresist before the wet etch. Optimal dose for the positive photoresist was found to be 130 mJ/cm^2. The preperation was done with the following steps:

1. Cleaned the sample with IPA.
2. Dehydration baked at 115 °C for 5 minutes.
3. Spin coated SPR 700 resist at 4000 rpm for 34 seconds with 1000 rpm/s acceleration.
4. Soft baked at 95 °C for 1 minute.
5. Aligned the pattern in the MLA. The alignment marks were badly damaged, so the alignment was not perfect.
6. Exposed the pattern at 130 mJ/cm^2 in the MLA.
7. Post exposure baked at 115 °C for 1 minute.
8. Developed in maD-332S developer for 30 seconds.
9. Optical inspected the pattern to see if it covered the Au fingers.

Quantification of the misalignment with the Verniers were tried, but the Verniers were too badly damaged to get any number out. The wet etch was done at the chemical clanroom at NTNU NanoLab, with NH_3:H_2O_2:H_20 in 3:1:300 ratio. The ammonium hydroxide was 30%. The etch depth was tested on the GaAs dummy sample, and measured with the profilometer to figure out an etch time which would remove 100 nm of GaAs. The GaAs dummy was etched 50 nm at the first run, thus the time was doubled for the LED etch to achieve 100 nm. The etch steps were as follows:

1. 3 mL 30% NH_3 was added to the etch tank with 300 ml H_2O.
2. 1 mL H_2O_2 was added to the etch tank.
3. The sample was placed in the etch tank for 90 seconds.
4. The sample was rinsed with H_2O and cleaned on the backside.
5. The protective photoresist was removed with acetone and IPA before profilometer measurement.
6. The etch depth was measured with the profilometer.

3.4. Backside contact formation

The backside of the LED sample was metallized with a Pd/Ge/Ti/Pt/Au stack to form the backside contact. The positive photoresist SPR 700 was used to protect the frontside, using the following steps:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 115 °C for 5 minutes.
3. Spin coated SPR 700 resist at 4000 rpm for 34 seconds with 1000 rpm/s acceleration.
4. Soft baked at 95 °C for 1 minute.
5. No exposure was done, since the whole frontside needed to be protected.
6. Post exposure baked at 115 °C for 1 minute.
7. Developed in maD-332S developer for 30 seconds.
8. Optically inspected the pattern to see if the whole frontside was covered.
9. Backside metallization was done by the teaching assistants.

3.5. Mesa etch, PECVD passivation deposition, and contact annealing

In one session the the mesa was etched, the passivation layer deposited and the contacts annealed. The mesa etch was done with a wet etch with H_3PO_4:H_2O_2:H2O 5:5:15, with the goal of separating the 16 LEDs. The mesa etch had to get through the two p-doped $Al_{0.7}Ga_{0.3}As$ layers, i.e. had to be deeper than 3 µm. The preperation for the mesa etch was to add a positive photoresist mesa mask, which was done in the following steps:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 115 °C for 5 minutes.
3. Spin coated SPR 700 resist at 4000 rpm for 34 seconds with 1000 rpm/s acceleration.
4. Soft baked at 95 °C for 1 minute.
5. Aligned the pattern in the MLA.
6. Exposed the pattern at 130 mJ/cm^2 in the MLA.
7. Post exposure baked at 115 °C for 1 minute.
8. Developed in maD-332S developer for 30 seconds.
9. Optically inspected the pattern to see if it covered the LEDs.

The mesa etch and passivation deposition was done in parallel. The wet etch was first done on the GaAs dummy to test the etch time, where it was found that 1 minute 30 seconds would be sufficient to etch through the two p-doped layers. The thickness aim for the passivation layer was 253 nm. The following steps were done:

1. Deposited Si_3N_4 passivation layer on Si to find an optimal layer thickness. The recipe used was "(OPT) Si3N4" for 18 minutes and 35 seconds.
2. Wet etched the dummy to find a suitable etch time. This etch time was 1 minute 15 seconds, which was increased by 15 seconds for the LED etch.
3. The wet etch was done with H_3PO_4:H_2O_2:H2O 5:5:15 mL.
4. The resist was stripped of the dummy, and the etch depth was measured with the profilometer.
5. The inferometer was used to measure the passivation layer deposition thickness.
6. The LED was mesa wet etched as the dummy was, but with 1 minutes 30 seconds etch time.

7. The etch depth was controlled to be deeper than 3 µm in the profilometer.
8. PECVD passivation layer deposition was done on the LED and the dummy with the same recipe and time as the Si test, because the recipe was found to be good enough.
9. The last step was the contact annealing, which was done with warm up to 420 °C, and 30 seconds annealing at 420 °C, before cooling down to room temperature.

3.6. Planarization and passivation layer etch

The passivation layer HF etch was done by the teaching assistants. The planarization and preperation for the passivation layer etch was to add a thick positive photoresist with a mask opening on the bottom bus bar, and was done in the following steps:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 150 °C for 5 minutes.
3. Spin coated AZ5214E positive resist at 1000 rpm for 34 seconds with 250 rpm/s acceleration.
4. Soft baked at 95 °C for 1 minute.
5. Exposed the pattern at 80 mJ/cm^2 in the MLA.
6. Developed in 70:30 ma-D 332S:H_2O developer for 1 minute 30 seconds.
7. Hard baked at 175 °C for 15 minutes.
8. Optical inspection of the pattern.
9. Teaching assistants preformed HF etch to expose the Au in the bottom bus bar.

3.7. Pad metallization

Lithography on the LED sample was done to prepare for the pad metallization. The teaching assistants did the pad metallization. The preparation was to make a negative photoresist mask for the pad metallization, and was done in the following steps:

1. Cleaned the sample with IPA.
2. Dehydration baked at 115 °C for 5 minutes.
3. Spin coated MAN 440 resist at 4000 rpm for 30 seconds with 1000 rpm/s acceleration.
4. Soft baked at 95 °C for 1 minute.
5. Exposed the pattern at 1300 mJ/cm^2 in the MLA
6. Developed in maD-332S developer for 5 minutes.
7. Optical inspected the pattern to see if the pattern covered the bottom bus bar and an area below.
8. Handed in the sample to the teaching assistants, who did the pad metallization with Ti/Au, with 30 nm Ti and 500 nm Au.
9. Lift-off was done with acetone.

3.8. LED testing/characterization

The final LED sample was tested using a Keithley 2450 SourceMeter, a probe, and an optical microscope. Initially, there was no measured contact in the LED between the frontside and the backside. The voltage was then turned up to 10 V, which warmed up the LED and gave contact. Using the SourceMeter, the voltage was swept from -1 V to 3 V, while the measured current was recorded. The measuring was automatically stopped when a current of 30 mA was reached. The results were then plotted as an IV-curve. Two of the LEDs was measured this way.

The LED was turned on with 1.71 V and 30 mA, and images was taken with an iPhone.

4. Results

4.1. Photoresist profile

Figure 9 shows an SEM image of the photoresit profile of the dose test sample where undercut was most visible. This is the sample with a dose of 1300 mJ/cm^2 and 5 minutes developing time. The depth of the undercut, i.e. the difference between the top and bottom of the profile, is roughly 1 µm.

Figure 10a and Figure 10b show 100X magnification images of one LED where the focus is on the bottom and the top of the profile, respectively. This shows that the bottom area of the finger is smaller than the top area, again verifying that an undercut profile is obtained with a dose of 1300 mJ/cm^2 and 5 minutes developing time.

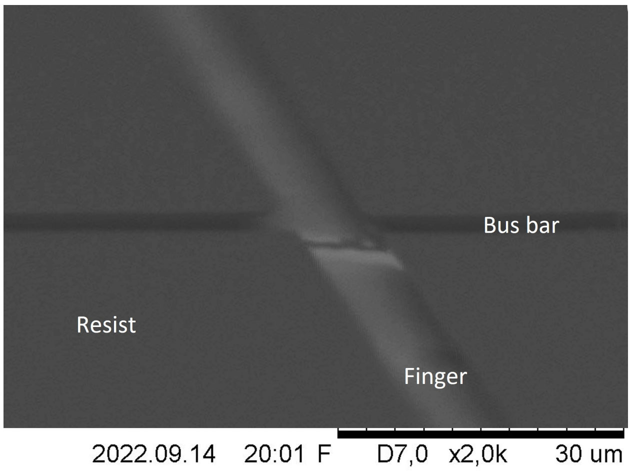
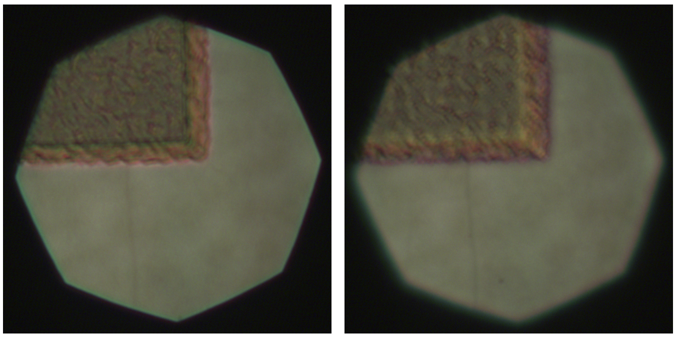


Figure 9: Secondary Electrons (SE) SEM image of the photoresist profile in the dose test sample where the best undercut profile was achieved. The optimal dose was 1300 mJ/cm^2 and the optimal developing time was 5 minutes. The exact undercut is not measured, but it is estimated to be around 1 µm. Acceleration voltage in the SE image was 5 kV. SEM image taken at the Hitachi TM3000 table top SEM at NTNU NanoLab.



(a) Focus on bottom of profile **(b)** Focus on top of profile

Figure 10: 100X magnification optical images of one finger on one LED. This illustrates that the photoresist profile is undercut.

4.2. Etching

The GaAs wet etch of the dummy was done for 45 seconds and gave a depth of 50 nm, thus the etching of the LED was done for twice as long at 90 seconds and gave a depth of 100 nm. This is an etch rate of 1.11 nm/s. The measured height of two fingers using the profilometer is shown in Figure 11. Measurements of other fingers gave similar results. Before the etch the Au fingers was measured to be 250 nm high. In the figure it is possible to see the etch edge, which is marked with the green line at 100 nm. The second green line is at 350 nm, which is the height of the finger after the etch. A profilometer artifact is shown in Figure 12.

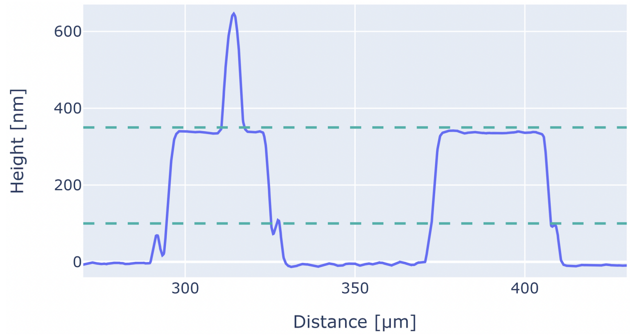


Figure 11: Profilometer data plot of the GaAs top layer etch. The etch was 100 nm deep, which is sufficient to get through the light absorbing layer. The plot shows an artifact on top of the finger to the left, but these were not examined further.

The deep AlGaAs wet etch for the mesas was done for 1 minute and 15 seconds on the dummy which gave 3000 - 3400 nm of etch depth, and thus the time was increased to 1 minute and 30 seconds for the LED, which gave 3100 - 3500 nm of etch depth. The deviation in etch depth is illustrated in Figure 13, where the devitaion is due to the fact that the profilometer data is not flat before and after the mesas. The etch rate was around 40 nm/s.

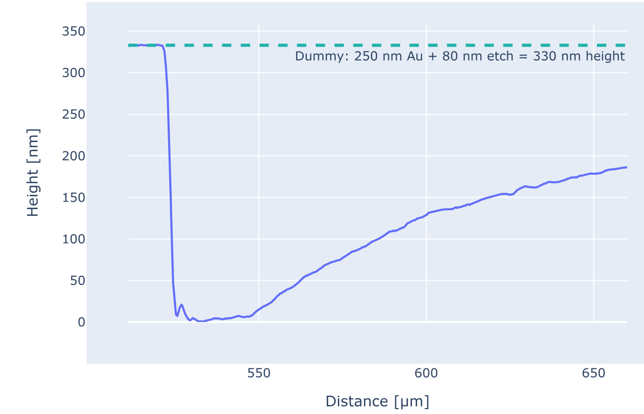


Figure 12: Profilometer data plot of GaAs dummy on the etch edge. The etch depth here was 80 nm, which was deeper that around the fingers. However, this plot shows an artifact in the profilometer, which is the curve starting at around 550 μm. The upwards curve continues upwards outside the plot till 350 nm, which is higher than the finger height.

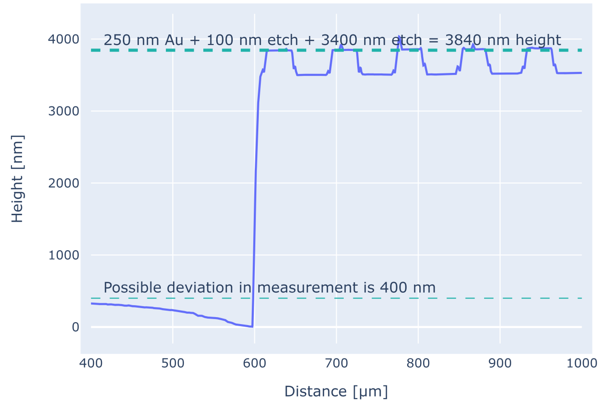


Figure 13: Profilometer data plot after the mesa etch of the LED sample. The etch is 3500 nm deep at the edges of the mesas, but the profile is not flat before and after each mesa. The data points outside the mesas flattened at 400 nm, which puts the etch depth between 3100 and 3500 nm. The height of the fingers are around 3840 nm, because of the GaAs layer and Au fingers on top of the AlGaAs.

4.3. PECVD

The result of the PECVD of Si_3N_4 was inspected using an ellipsometer. From this, the reflectance as a function of wavelength was obtained, as can be seen in Figure 14. The goodness of fit was 0.9926. The lowest measured reflectance was 0.29 % at 667.7 nm. At a wavelength of 675 nm, the reflectance was 0.42 %. From the ellipsometer, the thickness of the Si_3N_4 layer was measured to be 249.70 nm. Using Equation 1, with a refractive index n of 2.02 at $\lambda \approx$ 670 nm [5], the thickness is calculated to be 247.91 nm. These results are summarized in Table 1.

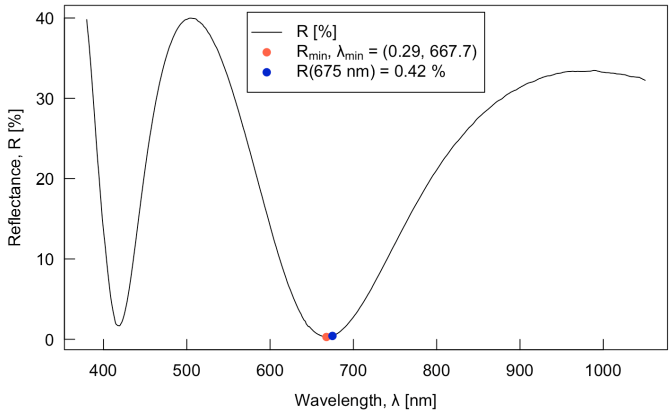


Figure 14: Reflectance as a function of wavelength for the PECVD Si_3N_4 film.

Table 1: Key parameters for the PECVD Si_3N_4 film obtained from the ellipsometer.

Parameter	Value
Lowest reflectance	0.29 %
Wavelength at lowest reflectance	667.7 nm
Reflectance at 675 nm	0.42 %
Measured thickness	249.70 nm
Calculated thickness	247.91 nm

4.4. Optical characterization of PECVD

After the PECVD and its finishing steps, an 10X optical image was taken of the LED. This image can be seen in Figure 15. From this, it can clearly be seen that the LED sample surface is not uniform. Visually, it seems that there are cracks and impurities present.

4.5. Final optical inspection

Using an optical microscope, the final LED sample was inspected. Figure 16a shows the visually best LED, which has an 80 µm period and a 4 µm finger width. Figure 16b shows the visually worst LED, which has a 40 µm period and a 16 µm finger width.

A final 50X magnification optical image were taken of all four alignment marks. The result can be seen in Figure 18. From these pictures, it is not possible to give a numerical estimate on the alignment accuracy

4.6. IV measurements

Using the sourcemeter, IV measurements were performed on two LEDs, one with 100 µm period and 16 µm finger width and one with 40 µm period and 4 µm finger width. Figure 17 shows the IV curve from -1 V to 0.5 V, while Figure 19 shows the IV-curve for the same LEDs from 0.5 V to 1.8 V.

Using a iPhone 13 Pro Max, a picture of the LED sample was taken while one LED was emitting light. The picture can be seen in Figure 20.

5. Discussion

5.1. Photolithography

All the lithography processes used in this work gave valuable experience. One of the experiences was how to do a dose test to get a sufficient undercut while using negative photoresist. The lab manual for the course [4] states that the undercut should be at least 1 µm deep, while the teaching assistant stated that 0.5-1 µm would be sufficient. Getting an exact measurement of the undercut was difficult with the Table Top SEM, because the tilting and rotation of the sample in the chamber is very restricted. Quantification of the undercut is problematic with the Table Top SEM, but the undercut is clearly visible in the SEM image in Figure 9. Estimating the undercut was easier when using the optical microscope. First it was assessed whether the slope visible in the optical images in

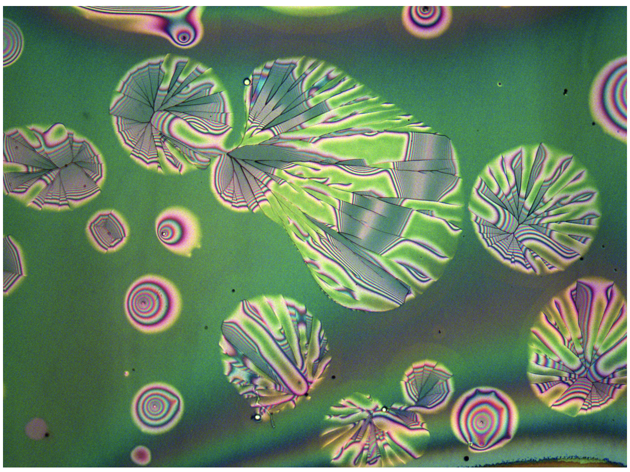


Figure 15: Optical overview 5X magnification image of the LED. The image shows cracks and impurities on the surface.

(a) Visually best LED. 80 µm period and 4 µm width.

(b) Visually worst LED. 40 µm period and 16 µm width.

Figure 16: 5X magnification optical images of the visually best and worst LEDs.

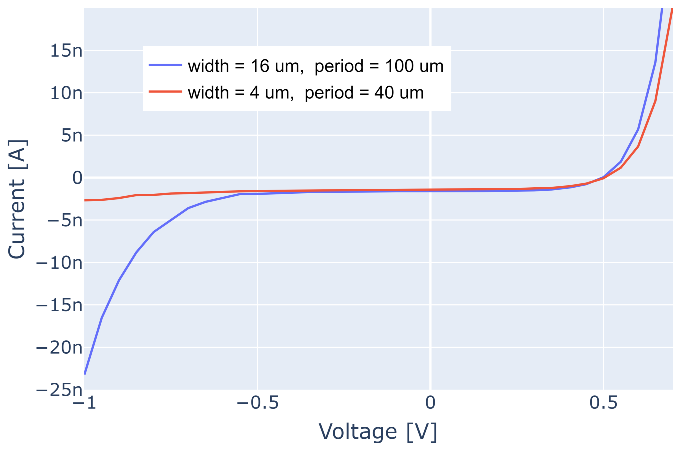


Figure 17: IV-curve for two LEDs, one with 100 µm period and 16 µm finger width and one with 40 µm period and 4 µm finger width.

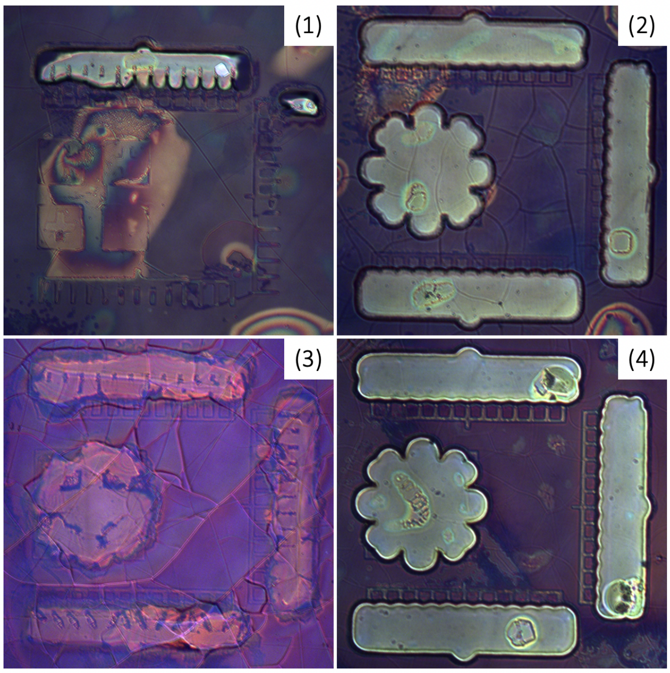


Figure 18: 50X magnification optical images of the four alignment marks.

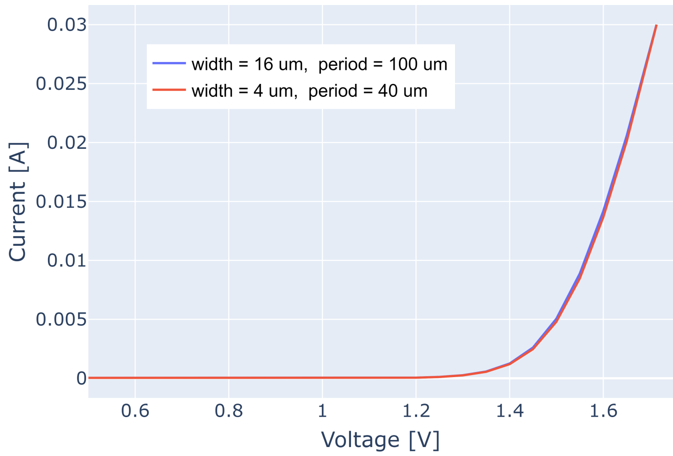


Figure 19: IV-curve for two LEDs, one with 100 µm period and 16 µm finger width and one with 40 µm period and 4 µm finger width.

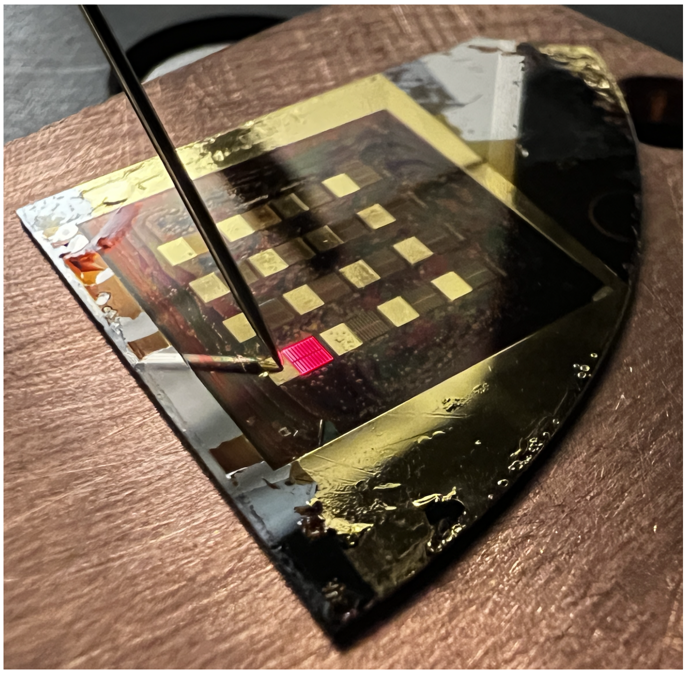


Figure 20: Image of the LED sample while one LED was emitting light. Taken with an iPhone 13 Pro Max.

Figure 10b and Figure 10a was an undercut or not. Over- and under focusing on the edge indicated that the slope was an undercut, and this was confirmed in the SEM. The quantification of the undercut was done by measuring the length of the slope and comparing this to the width of the finger. This is a crude approximation, but it confirmed that the undercut was in the range of 0.5-1.5 µm, assuming that the widest part of the finger was 4 µm wide.

If all the photolithography steps were done again, using only positive photoresist could have yielded better results. The first layer made with negative photoresist produced many defect fingers, while the second layer made with positive photoresist on top of the fingers did not have the same defects. Lift-off with positive photoresist is known to be possible with sufficiently large structures. Negative photoresist is normally used for lift-off, but results from this work suggests that trials with positive photoresist should be done for lift-off.

5.2. Etch

Etching of the two different layers gave some artifacts and had as expected different etch rates. The etch rate for the mesa was as intended higher, because the etch needed to be around 10 times deeper than the etch of the GaAs layer. Even though the etch solutions were different, it was expected that the mesa etch rate would be higher because the concentration of the etch solution was higher. Etch solution is not the only factor that affects the etch rate, but it is important.

The plots from the profilometer on the etches show that the surface after the etch is not perfectly flat. Three artifacts have been identified in the etch process.

One artifact is the contact loss shown in Figure 12. Here, the depth is measured to 330 nm, but this is uncertain since the contact is lost 20 µm after the etch edge. The contact loss can be countered with the right settings on the profilometer. The artifact could have been something else, but the contact loss is the most likely cause since the profilometer data outside the plot on the left side is flat and correct. The plot of the mesa etch could also have this artifact. To be sure that the etch depth was deeper than 3.1 µm in the mesa etch, the etch time was increased from the dummy to the LED sample to compensate for eventual profilometer contact loss.

A second artifact are on the vertical edges, where the etch is varying a lot. This is illustrated in Figure 11. The other vertical edges varied in other but similar ways. This could both be caused by the etch process and the profilometer. The profilometer might struggle to measure around vertical edges. The etch process could be affected by the increased area and by different etch rates on different crystallographic planes.

A third artifact is the squiggly surface, shown between the fingers in Figure 11. This artifact is caused by the etch process, and is present all over the wafer where the etch was done. The surface is varying around ± 5 nm, which is a lot for a 100 nm etch. This artifact could potentially block some of the light from the LED, but it is not clear how much of the light this could block.

5.3. Deposition of passivation layer

If all process steps are done correctly, the LED will emit light at 675 nm. For Si_3N_4, this corresponds to an optical thickness of around 253 nm. The optical thickness of Si_3N_4 was measured to be 249.70 nm and calculated to be 247.91 nm. A few nanometers difference between the measured and calculated thickness is expected, because the n in the calculation is an approximation. The values are very close to the target, which is good.

In order to adjust the thickness to get even closer to the target thickness, the deposition time could be adjusted. The deposition time was 18 minutes and 35 seconds. This corresponds to a deposition rate of 0.22 nm/sec, assuming that the deposition was linear and that the measured thickness is correct. Using these numbers, the deposition time could be adjusted to 18 minutes and 50 seconds, which would give an optical thickness of 253.06 nm, slightly closer to target value.

5.4. Surface artifact

The surface of the LED sample was far from perfect throughout the process. While alignment in the MLA was done, multiple surface impurities were visible. These impurities are probably what is seen as a high and abrupt peak in the profilometer data in Figure 11 around 320 µm. Peaks like this one are visible in all the profilometer data from the sample. The optical microscope images in Figure 15 show that the surface have many surface impurities which have cracked before, during or after annealing.

The annealing process made the surface artifacts and more visible. It is most likely that the surface impurities were present before the etch, and that the etch process has made the area around the impurities more susceptible to cracking and slightly different etch rates. The different etch rates are visible as different colors in the optical microscope images in Figure 15, which can arise due to different thicknesses. Another argument for the artifacts being a result of the etch process and not the annealing, is that the passivation layer totally covers the surface and protects it from damage.

5.5. IV-measurements

Initially, only a very low current was detected during the voltage swipe, in the order of pico amperes. Therefore, the voltage was briefly increased to 10 V. This caused the current to increase to the maximum allowed current, 30 mA. This behavior suggests that somewhere in the LED structure, minimum two layers were not in contact. The increased voltage will anneal the layers and make them diffuse into contact so that current can flow through them. One possible explanation of this behavior is that during the frontside contact metal deposition, the chamber was exposed to air between the titanium and gold layer. This can result in an oxide layer forming between them. An oxide layer can reduce the conductivity, and annealing can fix this problem. Annealing is probably what happened to the LEDs when the voltage was set to 10 V, because it fixed the contact problem.

While there are some differences between the IV-curves of the two LEDs, both show a typical diode behavior. At negative voltages, the LEDs show a low reverse current and one of the LEDs have a breakdown at between -0.5 and -1.0 V. The biggest difference between the two plotted IV-curves from two different LEDs, is that the 4 um width 40 um period LED does not have a breakdown as the 16 um width 100 um period LED does. The difference could come from the fact that the 4 um width 40 um period LED was more prone to finger defects, which could cause worse contact between the fingers and the wafer. At positive voltages, the two LEDs have the exponential increase in forward current from around 1.3 V.

In Figure 20, it can clearly be seen that the color of the emitted light from the LED is red. Red light has a wavelength between 620 and 720 nm [6]. The aim of this work was to make a LED emitting light at 675 nm. As we observed red light, we can therefore conclude that the target wavelength was roughly achieved.

6. Conclusion

Functioning LEDs have been produced by using a multi-layered semiconductor wafer. The wafer have been processed by strategically using photolithography, deposition, and etching. Producing the LEDs did not always go as planned, and some defects and artifacts were produced. However, characterization of the LEDs have been performed and the results show that the LEDs are working as a diode. With voltage at 1.7 V and current at 30 mA the LEDs emits red light, which is the around the target wavelength of 675 nm.

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