

TFE4575: LED lab

Brynjar Morka Mæhlum^a, Thord Niri Gjesdal Heggren^a

^aDepartment of Physics, Norwegian University of Science and Technology, 7491 Trondheim, Norway.

Abstract

make the abstract. (short)

Contents

1	Introduction	1
2	Theory	1
2.1	LED theory	1
2.2	Photolithography	1
2.3	Contact Formation	2
2.4	Etching	2
2.5	Passivation	2
2.6	Characterization equipment	2
3	Methods	2
3.1	LED design	2
3.2	Front contact formation	3
3.3	GaAs contact layer etch	3
3.4	Backside contact formation (step 3 or 4?)	3
3.5	Mesa etch, PECVD passivation deposition, and contact annealing	4
3.6	Planarization and passivation layer etch	4
3.7	Pad metallization	4
3.8	LED testing/characterization	5
4	Results	5
4.1	Photoresist Profile	5
4.2	PECVD	5
4.3	Optical Characterization of PECVD	6
4.4	Other Things	6
5	Discussion	6
5.1	Photolithography	6
5.2	Etch	7
5.3	Surface artifact	7
6	Conclusion	7

1. Introduction

LEDs (Light Emitting Diode) are, as the name suggests, a type of electrical component producing light. They are widely used due to their low power consumption, long lifetime, small size, and fast switching. LEDs are made up of strategically layered semiconductors and metals. Then,

in order to produce a working diode, the wafer needs to undergo several process steps. Some of these can be photolithography, etching, deposition, and annealing. After, the LEDs should be characterized and tested, e.g. by scanning electron microscopy (SEM), optical microscopy and current-voltage (IV) testing.

2. Theory

2.1. LED theory

LEDs are made of a PN junction, which is a semiconductor junction between a p-type and an n-type semiconductor. The p-type semiconductor is doped with a lot of holes, and the n-type semiconductor is doped with a lot of electrons. The junction is made by doping the semiconductor with impurities, which are atoms that are not part of the semiconductor crystal. The impurities are added to the semiconductor to change the electrical properties of the semiconductor. Light is emitted when an electron jumps from the n-type semiconductor to the p-type semiconductor. More on semiconductor physics can be found in [1].

2.2. Photolithography

Photolithography is used to make micro- and nanoscale structures on a substrate. The process is done in a cleanroom, where the air is filtered to remove dust and other particles. Small contamination can ruin the process by disturbing the resist. The photoresist is a polymer that is sensitive to light, which will either harden or dissolve depending on the type of photoresist. This is the steps of the process, and the reason for each step:

1. **Cleaning:** Remove any contamination from the substrate.
2. **Spin coating:** Spin coat the photoresist on the substrate.
3. **Soft bake:** Bake the photoresist to remove any solvent.
4. **Exposure:** Expose certain areas of the photoresist to light. Eventually with mask alignment.

5. **Develop:** Develop the photoresist to remove the softened parts.
6. **Post exposure bake:** Bake the photoresist to enhance adhesion. ??
7. **Hard bake:** Bake the photoresist to remove any solvent. Not often needed.
8. **Inspect:** Optical inspect the photoresist to see if it is good.

Negative photoresist are often used for lift-off, because negative photoresist can achieve an undercut which can improve the metallization edges. Photoresists needs different developing time and exposure doses, and they do change over time when the photoresist is exposed to light, heat, humidity, and time.

2.3. Contact Formation

LEDs need to have both a front and back metal contact. The purpose of the contacts are to provide a path so that current can be injected to the device. The back contact can simply be deposited on the whole back side of the wafer. The front contact however, needs to be patterned. This is because in order to reduce absorption losses, the contact area needs to be minimized while keeping the spreading resistance as low as possible. It is important to carefully chose the contact material, as it affect the electrical properties of the device. Also, the front side contracts should be made first, as the following steps may damage the surface.

2.4. Etching

Etching is a process of chemically removing material from a surface. The process can be divided into two categories - wet etching and dry etching. Wet etching uses a liquid etchant, while dry etching uses a gas etchant.

In LED fabrication, etching can be used e.g. to remove strongly light absorbing layers or to electrically isolate different parts of the device.

2.5. Passivation

Exposed sides of the LED will result in high non-radiative recombination at the surface, which will reduce the efficiency of the LED.

The Si_3N_4 has two main purposes in on the LED. Firstly, it acts as a passivation agent, reducing the surface non-radiative recombination. Secondly, it reduces the possibility of short-circuiting the diode by conduction on the sides of the etched mesa. The thickness of this layer should be such that it works as an antireflective coating, i.e. have an optical thickness of $(k/2 + 1/4)\lambda$.

2.6. Characterization equipment

The characterization equipment used in this lab was optical microscope, SEM, profilometer and IES-stuff to measure the LED efficiency. The theory behind these instruments and how they work are assumed to be known.

3. Methods

The LED sample with its metal layers shown in Figure 1 was grown by the staff of the course and given to the student group. To form a working LED from the metal layer sample, the following steps were done at NTNU NanoLab:

1. Front contact formation
2. GaAs contact layer etch
3. Backside contact formation
4. Mesa etch, PECVD passivation deposition, and contact annealing
5. Planarization and passivation layer etch
6. Pad metallization

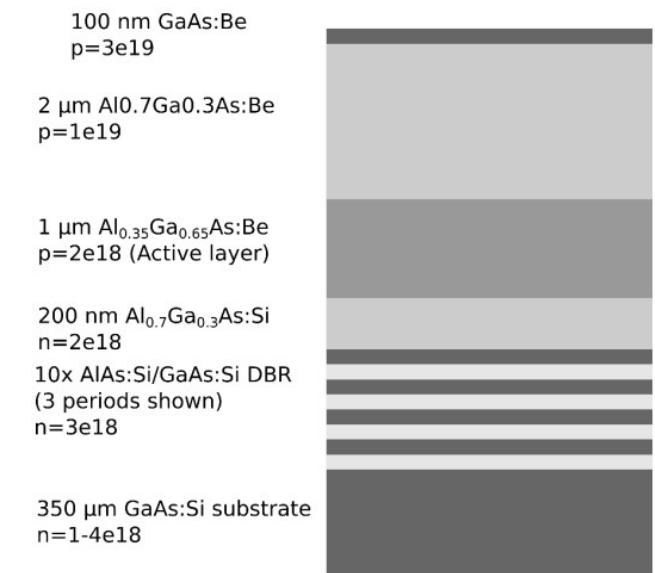


Figure 1: The metal layers the students got from the course staff to make the LED. The layers were grown in the MBE, molecular beam epitaxy, machine at NTNU NanoLab. Figure borrowed from the lab manual.

Each step was first done with a GaAs dummy sample to check that the process was working as intended. After the last step, the LED was ready for testing at a lab at IES, the Department of Electronic Systems at NTNU.

3.1. LED design

Different finger spacings and finger widths were tested. An overview schematic of the LED design is shown in Figure 2. One LED was 1 mm x 1 mm. The bus bar for contact pad was 1 mm x 300 μm. The bus bar connecting the fingers was 1 mm x 100 μm. The fingers were 450 μm long, with widths ranging from 50 μm to 100 μm and spacings ranging from 50 μm to 100 μm. **FIX THESE NUMBERS FIGURE WITH DIFFERENT FINGER WIDTHS AND SPACINGS?** CleWin stuff

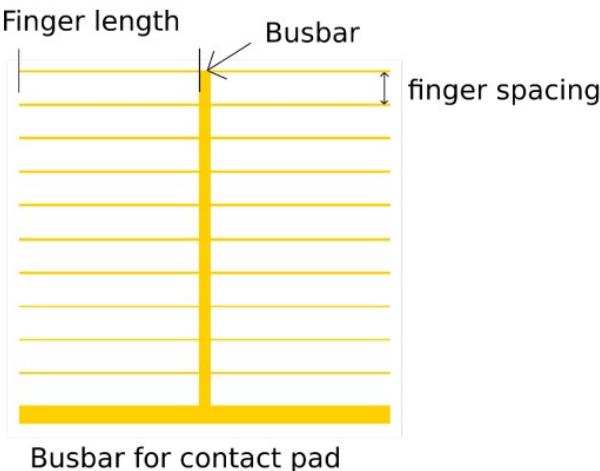


Figure 2: Schematic of the LED design. Figure borrowed from the lab manual.

3.2. Front contact formation

The bus bar and its fingers were formed with lithography and lift-off. A dose test was done to find the optimal dose and developing time for the resist, ensuring an undercut. To verify this, both a SEM image and optical images of the sample were taken. The optimal dose was 1300 mJ/cm^2 and the optimal developing time was 5 min. All temperatures are probably some degrees off, since the hot plates at NanoLab havt not been calibrated for many years. **FIX THESE NUMBERS** Negative photoresist was used, and the steps were done in the following order:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 110°C for 4 min. ??
3. Spin coated MAN 440 resist at 4000 rpm for 30 s with 1000 rpm/s acceleration.
4. Cleaned the backside.
5. Soft baked at 95°C for 5 min.
6. Exposed the pattern at 1300 mJ/cm^2 in the MLA.
7. Developed in maD-332S developer for 5 min.
8. Optical inspected the pattern.
9. Teaching assistants metallized the pattern with Au. **Au or Pd/Ti/Pt/Au?**
10. Lift-off with acetone.

Unfortunately, the students mixed up the developer with another group the first time, and had to start over. The optical inspection before round number two showed some bubbles on the wafer, which was probably caused by the wrong developer. The wafer was cleaned thoroughly with acetone and IPA before the second round, but some residue might have been left behind.

Another problem was that the dose test were done with a resist that got emptied, and the students had to use a new resist for the actual process. The new resist needed some more time in developer, which gave an undercut but damaged the alignment marks and the thinnest fingers. **Was this the new resist with a weird dev time?**

3.3. GaAs contact layer etch

The heavy p-doped GaAs layer at the top of the metal stack was etched away to allow light to pass through the LED. The deposited Au fingers were measured to be 250 nm high in the profilometer. Measuring the Au height was important for the later measurement of the etch depth of the 100 nm GaAs layer. The Au fingers were protected with a positive photoresist before the wet etch. Optimal dose for the positive photoresist was found to be 130 mJ/cm^2 . **True?** The preperation was done with the following steps:

1. Cleaned the sample with IPA.
2. Dehydration baked at 110°C for 4 min. ??
3. Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.
4. Soft baked at 95°C for 1 min.
5. Aligned the pattern in the MLA. The alignment marks were badly damaged, so the alignment was not perfect. See ??.
6. Exposed the pattern at 130 mJ/cm^2 in the MLA.
7. Post exposure baked at 115°C for 1 min.
8. Developed in maD-332S developer for 30 sec.
9. Optical inspected the pattern to see if it covered the Au fingers.

The students tried to use the Verniers to calculate the misalignment, but the Verniers were too badly damaged to get a number. The wet etch was done at the chemical clanroom at NTNU NanoLab, with $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ in 3:1:300 ratio. The etch depth was tested on the GaAs dummy sample, and measured with the profilometer to figure out a etch time which would remove 100 nm of GaAs. The GaAs dummy was etched 50 nm at the first run, thus the time was doubled for the LED etch to achieve 100 nm. The etch steps were as follows:

1. All equipment and chemicals were placed in the avtrekksskap. ???
2. 3 mL NH_3 was added to the etch tank with 300 ml H_2O .
3. 1 mL H_2O_2 was added to the etch tank.
4. The sample was placed in the etch tank for 60 sec. **True time?**
5. The sample was rinsed with H_2O and cleaned on the backside.
6. The protective photoresist was removed with acetone and IPA before profilometer measurement.
7. The etch depth was measured with the profilometer.

3.4. Backside contact formation (step 3 or 4?)

The backside of the LED wafer sample was metallized with Au to form the backside contact. The metallization was done by the teaching assistants, but the students had to protect the frontside with a photoresist. The student selected the positive photoresist SPR 700, since that one gave better results than MAN 440. **This is true? SPR 700 for protection?** The frontside protection was done with the following steps:

- Cleaned the sample with acetone and IPA.
- Dehydration baked at 110 °C for 4 min. ??
- Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.
- Soft baked at 95 °C for 1 min.
- No exposure was done, since the whole frontside needed to be protected.
- Post exposure baked at 115 °C for 1 min.
- Developed in maD-332S developer for 30 sec.
- Optically inspected the pattern to see if it covered the whole frontside.

3.5. Mesa etch, PECVD passivation deposition, and contact annealing

In one session the students did the mesa etch, passivation deposition and contact annealing. The mesa etch was done with a wet etch with H₃PO₄:H₂O₂:H₂O 5:5:15, with the goal of separating the 16 LEDs. The mesa etch had to get through the two p-doped Al_{0.7}Ga_{0.3}As layers, i.e. had to be deeper than 3 μm. The preparation for the mesa etch was to add a positive photoresist mesa mask, which was done in the following steps:

- Cleaned the sample with acetone and IPA.
- Dehydration baked at 110 °C for 4 min. ??
- Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.
- Soft baked at 95 °C for 1 min.
- Aligned the pattern in the MLA.
- Exposed the pattern at 80 mJ/cm² in the MLA.
- Post exposure baked at 115 °C for 1 min.
- Developed in maD-332S developer for 30 sec.
- Optically inspected the pattern to see if it covered the LEDs.

The mesa etch and passivation deposition was done in parallel at NTNU NanoLab. The wet etch was first done on the GaAs dummy to test the etch time, and the students figured out that 1 min 45 sec would be sufficient to etch through the two p-doped layers. The optimal thickness for the passivation layer was 253 nm to minimize reflection. The following steps were done:

- Deposited Si₃N₄ passivation layer on Si to find an optimal layer thickness. The recipe used was "(OPT) Si₃N₄" for 10 min.
- Wet etch of the dummy to find a suitable etch time. This etch time was 1 min 30 sec, which was increased by 15 sec for the LED etch.
- The wet etch was done with H₃PO₄:H₂O₂:H₂O 5:5:15 mL.
- The resist was stripped of the dummy, and the etch depth was measured with the profilometer.
- The inferometer was used to measure the passivation layer deposition thickness.

- The LED was mesa wet etched as the dummy was, but with 1 min 45 sec etch time.
- The etch depth was controlled to be deeper than 3 μm in the profilometer.
- PECVD passivation layer deposition was done on the LED and the dummy with the same recipe as the Si test, because the recipe was found to be good enough. **True?**
- The last step was the contact annealing, which was done with 70 sec warm up to 420 °C, and 60 sec annealing at 420 °C, before cooling down to room temperature.

3.6. Planarization and passivation layer etch

The planarization was done by the students, which the passivation layer etch was done by the teaching assistants. The planarization and preparation for the passivation layer etch was to add a thick positive photoresist with a mask opening on the bottom bus bar, and was done in the following steps:

- Cleaned the sample with acetone and IPA.
- Dehydration baked at 110 °C for 4 min. ??
- Spin coated AZ5214E positive resist at 1000 rpm for 34 sec with 250 rpm/s acceleration.
- Soft baked at 95 °C for 1 min.
- Exposed the pattern at 80 mJ/cm² in the MLA.
- Developed in 70:30 ma-D 332S:H₂O developer for 1 min 30 sec.
- Hard baked at 175 °C for 15 min.
- Optical inspection of the pattern.
- Teaching assistants performed HF etch to expose the Au in the bottom bus bar.

3.7. Pad metallization

The students did the preparation for the pad metallization, while the teaching assistants did the pad metallization. The lab manual said to use negative photoresist, but the students used positive photoresist, since that gave better results and does actually work for lift-off. The preparation was to make a positive photoresist mask for the pad metallization, and was done in the following steps:

- Cleaned the sample with IPA.
- Dehydration baked at 110 °C for 4 min. ??
- Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.
- Soft baked at 95 °C for 1 min.
- Exposed the pattern at 80 mJ/cm² in the MLA.
- Post exposure baked at 115 °C for 1 min.
- Developed in maD-332S developer for 30 sec.
- Optically inspected the pattern to see if it covered the bottom bus bar and an area below.
- Handed in the sample to the teaching assistants, who did the pad metallization with Au.
- The students did the lift-off of the resist with acetone.

3.8. LED testing/characterization

After all these steps the LED was ready for testing. Testing was done at IES, with ...

4. Results

4.1. Photoresist Profile

Figure 3 shows an SEM image of the photoresist profile of the dose test sample where undercut was most visible. This corresponds to a sample with a dose of 1300 mJ/cm^2 and 5 minutes developing time. The depth of the undercut, i.e. the difference between the top and bottom of the profile, is estimated to be roughly $1 \mu\text{m}$.

Figure 4a and **Figure 4b** show 100X magnification images of the LED where the focus is on the bottom and the top of the profile, respectively. This shows that the bottom area of the finger is smaller than the top area, again verifying that an undercut profile is obtained with a dose of 1300 mJ/cm^2 and 5 minutes developing time.

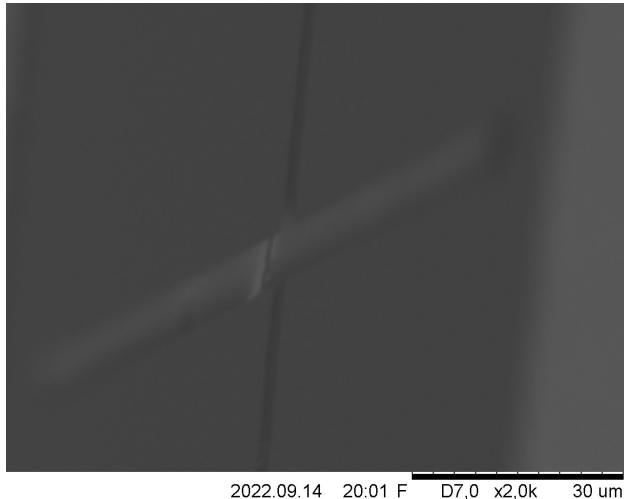
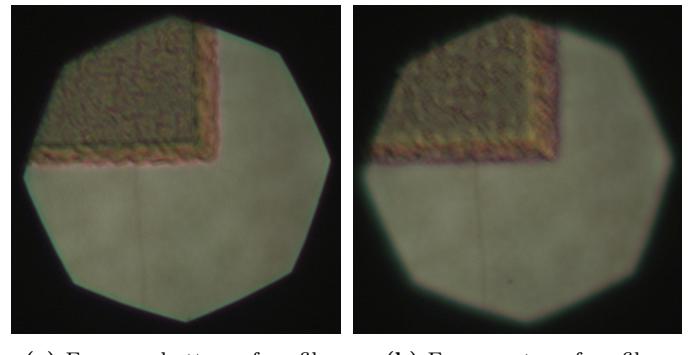


Figure 3: SE SEM image of the photoresist profile in the dose test where the best undercut profile was achieved. The optimal dose was 1300 mJ/cm^2 and the optimal developing time was 5 minutes. The exact undercut is not measured, but it is estimated to be around $1 \mu\text{m}$. Acceleration voltage in the SE image was 5 kV. SEM image taken at the Hitachi TM3000 table top SEM at NTNU NanoLab.

4.2. PECVD

The result of the PECVD of Si_3N_4 was inspected using an ellipsometer. From this, the reflectance as a function of wavelength was obtained, as can be seen in **Figure 5**. The goodness of fit was 0.9926. The lowest measured reflectance was 0.29 % at 667.7 nm. At a wavelength of 675 nm, the reflectance was 0.42 %. From the ellipsometer, the thickness of the Si_3N_4 layer was measured to be 249.70 nm. From the equation $2d = \lambda/n \cdot 3/2$, with a refractive index n of 2.02 [2], the thickness is calculated to be 247.91 nm. These results are summarized in **Table 1**.



(a) Focus on bottom of profile (b) Focus on top of profile

Figure 4: 100X magnification optical images of one finger on the LED. This illustrates the photoresist profile is undercut.

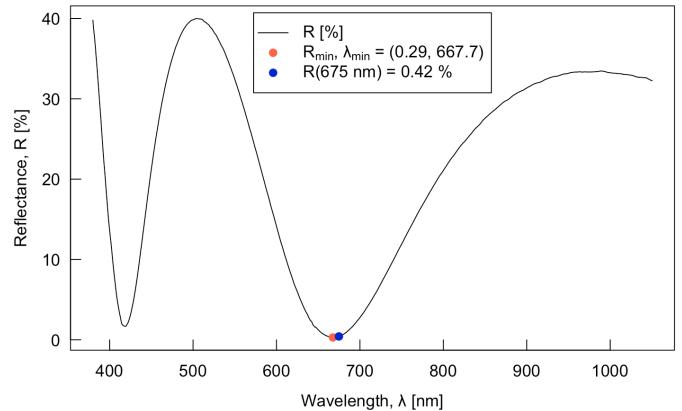


Figure 5: Reflectance as a function of wavelength for the PECVD Si_3N_4 film.

Table 1: Key parameters for the PECVD Si_3N_4 film obtained from the ellipsometer.

Parameter	Value
Lowest reflectance	0.29 %
Wavelength at lowest reflectance	667.7 nm
Reflectance at 675 nm	0.42 %
Measured thickness	249.70 nm
Calculated thickness	247.91 nm

4.3. Optical Characterization of PECVD

After the PECVD and its finishing steps, an 10X optical image was taken of the LED. This image can be seen in [Figure 6](#). From this, it can clearly be seen that the Si_3N_4 film is not uniform. Visually, it seems that the film has cracked and that there are some impurities present.

4.4. Other Things

We still need the following:

- [images of alingment marks](#)
- [IES test of LED. I-V curve](#)

Results we will list:

1. undercut in SEM image (done)
2. etch depth for GaAs etch, 100 nm (done)
3. alignment accuracy
4. etch depth for AlGaAs etch, 3 μm
5. PECVD Si_3N_4 thickness vs. deposition time, reflection curve vs. wavelength (or at least the reflection minima for the final thickness and the reflectivity at 675 nm).
6. Optical images of the sample after finishing steps in the PECVD independent work.
7. Optical image of final LED

The wet etch of the dummy was done for XX seconds and gave a depth of 50 nm, thus the etching of the LED was done for twice as long at XX seconds and gave a depth of 100 nm. This is an etch rate of ~~XXXXXXXX~~ nm/s. Two of the measured profilometer finger heights are shown in [Figure 7](#). The other measurements of the fingers gave similar results. Before the etch the Au fingers was measured to be 250 nm high. In the figure it is possible to see the etch edge, which is marked with the green line at 100 nm. The second green line is at 350 nm, which is the height of the finger after the etch. A profilometer artifact is shown in [Figure 8](#).

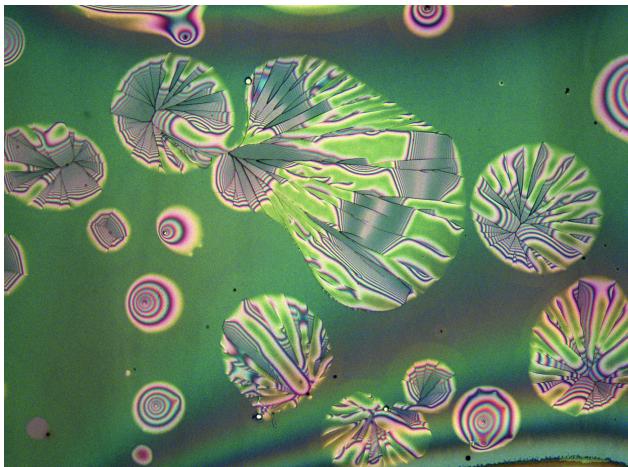


Figure 6: Optical image of the LED.

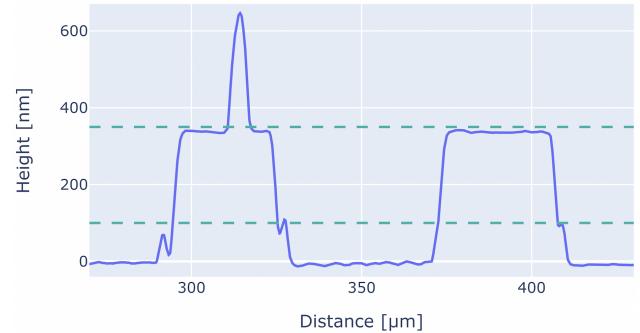


Figure 7: Profilometer data plot of the GaAs top layer etch. The etch was 100 nm deep, which is sufficient to get through the light absorbing layer. The plot shows an artifact on top of the finger to the left, but these were not examined further.

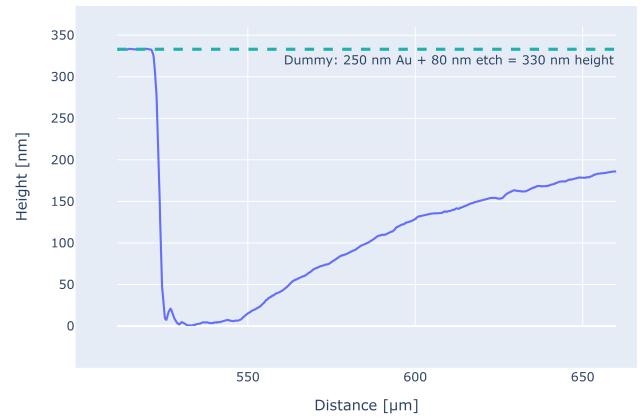


Figure 8: Profilometer data plot of GaAs dummy on the etch edge. The etch depth here was 80 nm, which was deeper than around the fingers. However, this plot shows an artifact in the profilometer, which is the curve starting at around 550 μm . The upwards curve continues upwards outside the plot till 350 nm, which is higher than the finger height.

The deep AlGaAs wet etch for the mesas was done for 1 minute and 45 seconds and gave a depth of 3.1 μm . The dummy was etched for 1 minute and 30 seconds and gave a depth of 2.9 μm , and thus the LED was etched for 15 more seconds. The profilometer data was not extracted to be plotted. However, the etch rate was measured to be 30 nm/s. **TODO: Should we plot the data???**

5. Discussion

5.1. Photolithography

All the lithography processes used in this work gave valuable experience. One of the experiences was how to do a dose test to get a sufficient undercut while using negative photoresist. The lab manual for the course [3] states that the undercut should be at least 1 μm deep, while the teaching assistant stated that 0.5-1 μm would be sufficient. Getting an exact measurement of the undercut was difficult with the Table Top SEM, because the tilting and

rotation of the sample in the chamber is very restricted. Quantification of the undercut with the Table Top SEM, but the undercut is clearly visible in the SEM image in [Figure 3](#). Estimating the undercut was easier when using the optical microscope. First it was assessed whether the slope visible in the optical images in [Figure 4b](#) and [Figure 4a](#) was an undercut or not. Over- and under focusing on the edge indicated that the slope was an undercut, and this was confirmed in the SEM. The quantification of the undercut was done by measuring the length of the slope and comparing this to the width of the finger. This is a crude approximation, but it confirmed that the undercut was in the range of 0.5-1.5 μm , assuming that the widest part of the finger was 5 μm wide.

If all the photolithography steps were done again from start, positive photoresist would have been preferred over negative photoresist to get the best possible results. All the steps with positive photoresist gave better results than with negative photoresist. One example of the bad Negative photoresist is supposed to be better to use for lift-off, because of the undercut, but it was concluded that the positive resist gave sufficiently good results and less edge problems when used in the lift-off process. One of the students did use positive photoresist for the lift-off process in his project thesis, and found there too that the positive resist gave good enough results.

5.2. Etch

The plots from the profilometer on the etches show that the etch is not perfectly flat. Three artifacts have been identified in the etch process, which are the cause of the non-flat etch.

One artifact is the contact loss shown in [Figure 8](#). Here the depth is measured to 80 nm, but this is uncertain since the contact is lost. The contact loss can be countered with the right settings on the profilometer. The artifact could have been something else, but the contact loss is the most likely cause since the profilometer data outside the plot on the left side is flat and correct.

A second artifact are on the vertical edges, where the etch is varying a lot. This is illustrated in [Figure 7](#). The other vertical edges varied in other but similar ways. This could both be caused by the etch process and the profilometer. The profilometer might struggle to measure around vertical edges. The etch process could be affected by the increased area and by different etch rates on different crystallographic planes.

A third artifact is the squiggly surface, shown between the fingers in [Figure 7](#). This artifact is caused by the etch process, and is present all over the wafer where the etch was done. The surface is varying around $\pm 5 \text{ nm}$, which is a lot for a 100 nm etch. This artifact could potentially block some of the light from the LED, but it is not clear how much of the light this could block.

Adding a passivation layer

If all process steps are done correctly, the LED will emit light at 675 nm.

5.3. Surface artifact

The surface of the LED was far from perfect throughout the process. While alignment in the MLA was done, multiple surface impurities were visible. These impurities are probably what is seen as a high and abrupt peak in the profilometer data in [Figure 7](#) around 320 μm . Peaks like this one are visible in all the profilometer data from the sample. The optical microscope images in [Figure 6](#) show that the surface have many surface impurities which have cracked before, during or after annealing.

The annealing process made the surface artifacts and more visible. It is most likely that the surface impurities were present before the etch, and that the etch process has made the area around the impurities more susceptible to cracking and slightly different etch rates. The different etch rates are visible as different colors in the optical microscope images in [Figure 6](#), which can arise due to different thicknesses. Another argument for the artifacts being a result of the etch process and not the annealing, is that the passivation layer totally covers the surface and protects it from damage.

6. Conclusion

References

- [1] B.G. Streetman and S. Banerjee. *Solid State Electronic Devices*. Pearson, 2015.
- [2] Filmetrics. Refractive index of si3n4, silicon nitride, sin, sion. <https://www.filmetrics.com/refractive-index-database/Si3N4/Silicon-Nitride-SiN-SiON>, 2022.
- [3] Tron Arne Nilsen and Bjørn-Ove Finland. Tfe4575 - overview information for photolithography and pecvd/dry etch modules, 2022.