TFE4575: LED lab

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Abstract

make the abstract. (short)

Contents

1. Introduction

(SHORT)

LEDs are important nanotechnology products, which is why making a LED was the lab task in TFE4575. While doing this lab the students used many nanotechnology techniques to produce a LED from a metal stack. Lithography, etching, deposition, characterization, and more were used to produce a LED. These techniques should be familiar for the nanotechnology students specializing in nanoelectronics at NTNU, and is why they were chosen for this lab. As stated in the introduction lecture, doing photolithography requires training with failing to be able to do it correctly. In almost every single lab session, the students managed to fuck up a big or a small step, resulting in a lot of learning and redoing. However, the students managed to produce a working LED in the end, and the lab was a great success. The LED will be sold to the highest bidder, or be used as the star in Thords Christmas tree. Merry Christmas, we hope you enjoy the read!

2. Theory

2.1. LED theory

LEDs are made of a PN junction, which is a semiconductor junction between a p-type and an n-type semiconductor. The p-type semiconductor is doped with a lot of holes, and the n-type semiconductor is doped with a lot of electrons. The junction is made by doping the semiconductor with impurities, which are atoms that are not part of the semiconductor crystal. The impurities are added to the semiconductor to change the electrical properties of the semiconductor. Light is emitted when an electron jumps from the n-type semiconductor to the p-type semiconductor. More on semiconductor physics can be found in [1].

2.2. Photolithography

Photolithography is used to make micro- and nanoscale structures on a substrate. The process is done in a cleanroom, where the air is filtered to remove dust and other particles. Small contamination can ruin the process by disturbing the resist. The photoresist is a polymer that is sensitive to light, which will either harden or dissolve depending on the type of photoresist. This is the steps of the process, and the reason for each step:

1. **Cleaning**: Remove any contamination from the substrate.
2. **Spin coating**: Spin coat the photoresist on the substrate.
3. **Soft bake**: Bake the photoresist to remove any solvent.
4. **Exposure**: Expose certain areas of the photoresist to light. Eventually with mask alignment.
5. **Develop**: Develop the photoresist to remove the softened parts.

6. **Post exposure bake**: Bake the photoresist to enhance adhesion. ??
7. **Hard bake**: Bake the photoresist to remove any solvent. Not often needed.
8. **Inspect**: Optical inspect the photoresist to see if it is good.

Negative photoresist are often used for lift-off, because negative photoresist can achieve an undercut which can improve the metallization edges. Photoresists needs different developing time and exposure doses, and they do change over time when the photoresist is exposed to light, heat, humidity, and time.

2.3. Etching?

2.4. Characterization equipment

The characterization equipment used in this lab was optical microscope, SEM, profilometer and IES-stuff to measure the LED efficiency. The theory behind these instuments and how they work are assumed to be known.

3. Methods

The LED sample with its metal layers shown in Figure 1 was grown by the staff of the course and given to the student group. To form a working LED from the metal layer sample, the following steps were done at NTNU NanoLab:

1. Front contact formation
2. GaAs contact layer etch
3. Backside contact formation
4. Mesa etch, PECVD passivation deposition, and contact annealing
5. Planarization and passivation layer etch
6. Pad metallization

Each step was first done with a GaAs dummy sample to check that the process was working as intended. After the last step, the LED was ready for testing at a lab at IES, the Department of Electronic Systems at NTNU.

3.1. LED design

Different finger spacings and finger widths were tested. An overview schematic of the LED design is shown in Figure 2. One LED was 1 mm x 1 mm. The bus bar for contact pad was 1 mm x 300 µm. The bus bar connecting the fingers was 1 mm x 100 µm. The fingers were 450 µm long, with widths ranging from 50 µm to 100 µm and spacings ranging from 50 µm to 100 µm. **FIX THESE NUMBERS FIGURE WITH DIFFERENT FINGER WIDTHS AND SPACINGS? CleWin stuff**

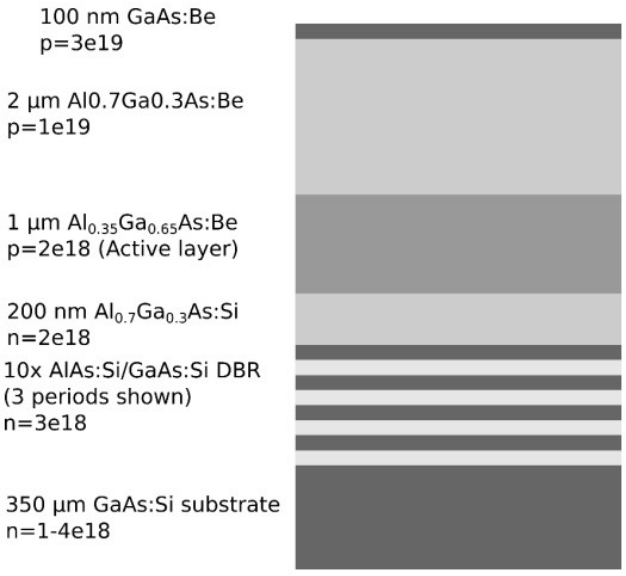

Figure 1: The metal layers the students got from the course staff to make the LED. The layers were grown in the MBE, molecular beam epitaxy, machine at NTNU NanoLab. Figure borrowed from the lab manual.

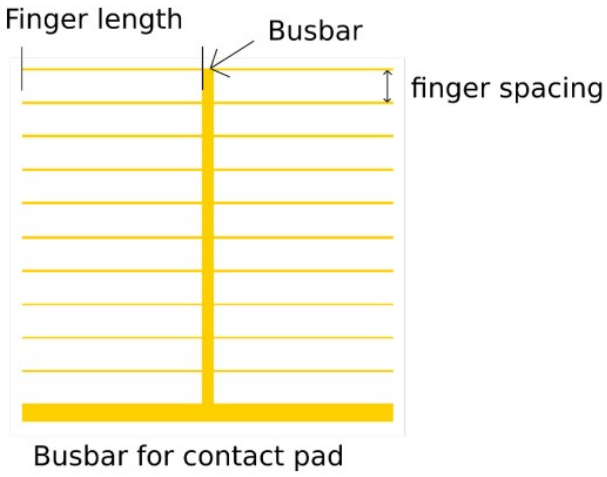

Figure 2: Schematic of the LED design. Figure borrowed from the lab manual.

3.2. Front contact formation

The bus bar and its fingers were formed with lithography and lift-off. A dose test was done to find the optimal dose and developing time for the resist, ensuring an undercut. An image of the achieved undercut in the dose test is shown in a SEM image in section 4 in Figure 3. The optimal dose was 1300 mJ/cm^2 and the optimal developing time was 5 min. All temperatures are probably some degrees off, since the hot plates at NanoLab havt not been calibrated for many years. **FIX THESE NUMBERS** Negative photoresist was used, and the steps were done in the following order:

1. Cleaned the sample with acetone and IPA.

2. Dehydration baked at 110 °C for 4 min. ???
3. Spin coated MAN 440 resist at 4000 rpm for 30 s with 1000 rpm/s acceleration.
4. Cleaned the backside.
5. Soft baked at 95 °C for 5 min.
6. Exposed the pattern at 1300 mJ/cm^2 in the MLA.
7. Developed in maD-332S developer for 5 min.
8. Optical inspected the pattern.
9. Teaching assistants metallized the pattern with Au. **Au or Pd/Ti/Pt/Au?**
10. Lift-off with acetone.

Unfortunately, the students mixed up the developer with another group the first time, and had to start over. The optical inspection before round number two showed some bubbles on the wafer, which was probably caused by the wrong developer. The wafer was cleaned thuroghly with acetone and IPA before the second round, but some residue might have been left behind.

Another problem was that the dose test were done with a resist that got emtied, and the students had to use a new resist for the actual process. The new resist needed some more time in developer, which gave an undercut but damaged the alignment marks and the thinnest fingers. **Was this the new resist with a weird dev time?**

3.3. GaAs contact layer etch

The heavy p-doped GaAs layer at the top of the metal stack was etched away to allow light to pass through the LED. The deposited Au fingers were measured to be 250 nm high in the profilometer. Measuring the Au height was important for the later measurement of the etch debth of the 100 nm GaAs layer. The Au fingers were protected with a positive photoresist before the wet etch. Optimal dose for the positive photoresist was found to be 130 mJ/cm^2. **True?** The preperation was done with the following steps:

1. Cleaned the sample with IPA.
2. Dehydration baked at 110 °C for 4 min. ??
3. Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.
4. Soft baked at 95 °C for 1 min.
5. Aligned the pattern in the MLA. The alignment marks were badly damaged, so the alignment was not perfect. See **??**.
6. Exposed the pattern at 130 mJ/cm^2 in the MLA.
7. Post exposure baked at 115 °C for 1 min.
8. Developed in maD-332S developer for 30 sec.
9. Optical inspected the pattern to see if it covered the Au fingers.

The students tried to use the Verniers to calculate the misalignment, but the Verniers were too badly damaged to get a number. The wet etch was done at the chemial clanroom at NTNU NanoLab, with NH4OH:H2O2:H20 in 3:1:300 ratio. The etch debth was tested on the GaAs dummy sample, and measured with the profilometer to figure out a etch time which would remove 100 nm of GaAs. The GaAs dummy was etched 50 nm at the first run, thus the time was doubled for the LED etch to achieve 100 nm. The etch steps were as follows:

1. All equipment and chemicals were placed in the avtrekksskap. ??????
2. 3 mL NH_3 was added to the etch tank with 300 ml H_2O.
3. 1 mL H_2O_2 was added to the etch tank.
4. The sample was placed in the etch tank for 60 sec. **True time?**
5. The sample was rinsed with H_2O and cleaned on the backside.
6. The protective photoresist was removed with acetone and IPA before profilometer measurement.
7. The etch debth was measured with the profilometer.

3.4. Backside contact formation (step 3 or 4?)

The backside of the LED wafer sample was metallized with Au to form the backside contact. The metallization was done by the teaching assistants, but the students had to protect the frontside with a photoresist. The student selected the positive photoresist SPR 700, since that one gave better results than MAN 440. **This is true? SPR 700 for protection?** The frontside protection was done with the following steps:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 110 °C for 4 min. ??
3. Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.
4. Soft baked at 95 °C for 1 min.
5. No exposure was done, since the whole frontside needed to be protected.
6. Post exposure baked at 115 °C for 1 min.
7. Developed in maD-332S developer for 30 sec.
8. Optically inspected the pattern to see if it covered the whole frontside.

3.5. Mesa etch, PECVD passivation deposition, and contact annealing

In one session the students did the mesa etch, passivation deposition and contact annealing. The mesa etch was done with a wet etch with H3PO4:H2O2:H2O 5:5:15, with the goal of seperating the 16 LEDs. The mesa etch had to get through the two p-doped $Al_0.7Ga_0.3As$ layers, i.e. had to be deeper than 3 µm. The preperation for the mesa etch was to add a positive photoresist mesa mask, which was done in the following steps:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 110 °C for 4 min. ??
3. Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.

4. Soft baked at 95 °C for 1 min.
5. Aligned the pattern in the MLA.
6. Exposed the pattern at 130 mJ/cm^2 in the MLA.
7. Post exposure baked at 115 °C for 1 min.
8. Developed in maD-332S developer for 30 sec.
9. Optically inspected the pattern to see if it covered the LEDs.

The mesa etch and passivation deposition was done in parallell at NTNU NanoLab. The wet etch was first done on the GaAs dummy to test the etch time, and the students figured out that 1 min 45 sec would be sufficient to etch through the two p-doped layers. The optimal thickness for the passivation layer was 253 nm to minimize reflection. The following steps were done:

1. Deposited Si_3N_4 passivation layer on Si to find an optimal layer thickness. The recipe used was "(OPT) Si3N4" for 10 min.
2. Wet etch of the dummy to find a suitable etch time. This etch time was 1 min 30 sec, which was increased by 15 sec for the LED etch.
3. The wet etch was done with H3PO4:H2O2:H2O 5:5:15 mL.
4. The resist was stripped of the dummy, and the etch debth was measured with the profilometer.
5. The inferometer was used to measure the passivation layer deposition thickness.
6. The LED was mesa wet etched as the dummy was, but with 1 min 45 sec etch time.
7. The etch debth was controlled to be deeper than 3 µm in the profilometer.
8. PECVD passivation layer deposition was done on the LED and the dummy with the same recipe as the Si test, because the recipe was found to be good enough. **True?**
9. The last step was the contact annealing, which was done at 400 °C for 30 sec in the RTP.

3.6. Planarization and passivation layer etch

The planarization was done by the students, which the passivation layer etch was done by the teaching assistants. The planarization and preperation for the passivation layer etch was to add a thick positive photoresist with a mask opening on the bottom bus bar, and was done in the following steps:

1. Cleaned the sample with acetone and IPA.
2. Dehydration baked at 110 °C for 4 min. ??
3. Spin coated AZ5214E positive resist at 1000 rpm for 34 sec with 250 rpm/s acceleration.
4. Soft baked at 95 °C for 1 min.
5. Exposed the pattern at 80 mJ/cm^2 in the MLA.
6. Developed in 70:30 ma-D 332S:H2O developer for 1 min 30 sec.
7. Hard baked at 175 °C for 15 min.
8. Optical inspection of the pattern.
9. Teaching assistants preformed HF etch to expose the Au in the bottom bus bar.

3.7. Pad metallization

The students did the preperation for the pad metallization, while the teaching assistants did the pad metallization. The lab manual said to use negative photoresist, but the students used positive photoresist, since that gave better results and does actually work for lift-off. The preperation was to make a positive photoresist mask for the pad metallization, and was done in the following steps:

1. Cleaned the sample with IPA.
2. Dehydration baked at 110 °C for 4 min. ??
3. Spin coated SPR 700 resist at 4000 rpm for 34 s with 1000 rpm/s acceleration.
4. Soft baked at 95 °C for 1 min.
5. Exposed the pattern at 80 mJ/cm^2 in the MLA.
6. Post exposure baked at 115 °C for 1 min.
7. Developed in maD-332S developer for 30 sec.
8. Optical inspected the pattern to see if it covered the bottom bus bar and an area below.
9. Handed in the sample to the teaching assistants, who did the pad metallization with Au.
10. The students did the lift-off of the resist with acetone.

3.8. LED testing/characterization

After all these steps the LED was ready for testing. Testing was done at IES, with ...

4. Results

We still need the following:

- images of alingment marks
- IES test of LED. I-V curve

Results we will list:

1. undercut in SEM image (done)
2. alignment accuracy
3. etch debth for GaAs etch
4. etch debth for AlGaAs etch
5. PECVD Si3N4 thickness vs. deposition time, reflection curve vs. wavelength (or at least the reflection minima for the final thickness and the reflectivity at 675 nm).
6. Optical images of the sample after finishing steps in the PECVD independent work.
7. Optical image of final LED

5. Discussion

As stated in section 1, the world needs LEDs to ...

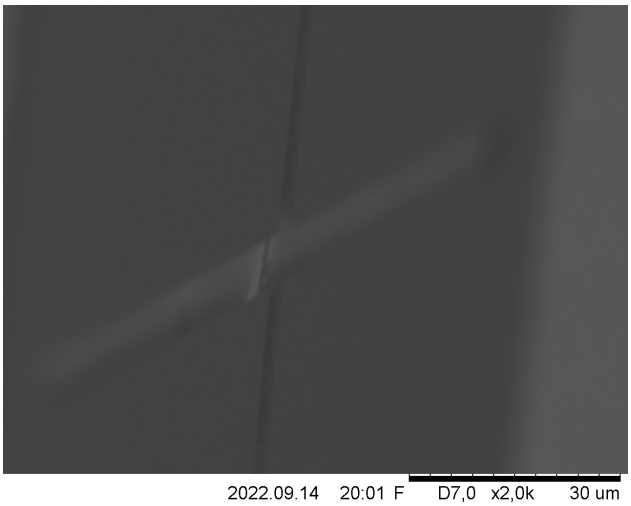

Figure 3: SE SEM image of the undercut in the dose test. The optimal dose was 1300 mJ/cm^2 and the optimal developing time was 5 min. The students were not able to measure the excact undercut, but from the image it seems to be around 1 µm. It is hard to determine the exact undercut from the image, because of the focus, the tilt and the debth in the image. However, it is clear that the given dose and developer time is sufficient to achieve an undercut. Acceleration voltage in the SE image was 5 kV. SEM image taken at the Hitachi TM3000 table top SEM at NTNU NanoLab.

5.1. smt

6. Conclusion

very nice [2]

References

[1] B.G. Streetman and S. Banerjee. *Solid State Electronic Devices*. Pearson, 2015.

[2] morra til thord. test av referanse. iamawesome.com, 2022. Accessed: 2420-06-09.