Digital Design and Computer Architecture: Lab Report		
Lab 1: Drawing Basic Circuits		
Date	08.03	Grade
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	Camil Schmid	Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and all other files you used for the report, i.e., the entire Verilog project folder and/or all schematics you drew. If any files are missing, it may negatively impact your grade. No shortcuts/links will be accepted.

Only one of the members of each group should submit. All members of the group will get the same grade.

The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

The deadline for the report is a hard deadline and it will not be extended.

Exercise 1 (1.5 Pts)

(a) Assume that we were only using 2-input AND gates and 2-input XNOR gates to create our comparator in Part 1 in this week's lab manual. How many of each gate would you use for a comparator of width 8, 16, 32 and 64 bits? What is the logic depth in each case?

*Note: The **logic depth** of a combinational circuit is defined as the number of **basic logic gates** (e.g., AND, OR, NOT, XOR, etc.) in the longest signal path (path from input to output). The **width** of the comparator indicates the number of bits of each input signal to compare.*

Comparator Width	2-input XNOR gates	2-input AND gates	Logic depth
8 bits	8	7	4
16 bits	16	15	5
32 bits	32	31	6
64 bits	64	63	7

(b) Given the comparator width is N, derive general expressions for calculating the following:

(i) The number of 2-input XNOR gates

N

(ii) The number of 2-input AND gates

N-1

(iii) The logic depth

$Log_2(N)+1$

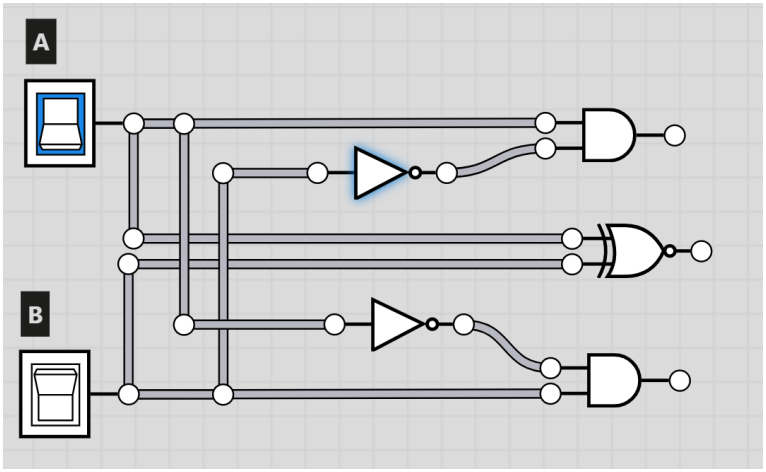
Exercise 2 (1 Pts)

Use two instances of the 1-bit comparator we designed in Part 2 in this week's lab to implement a 2-bit comparator. Draw the schematic of your design.

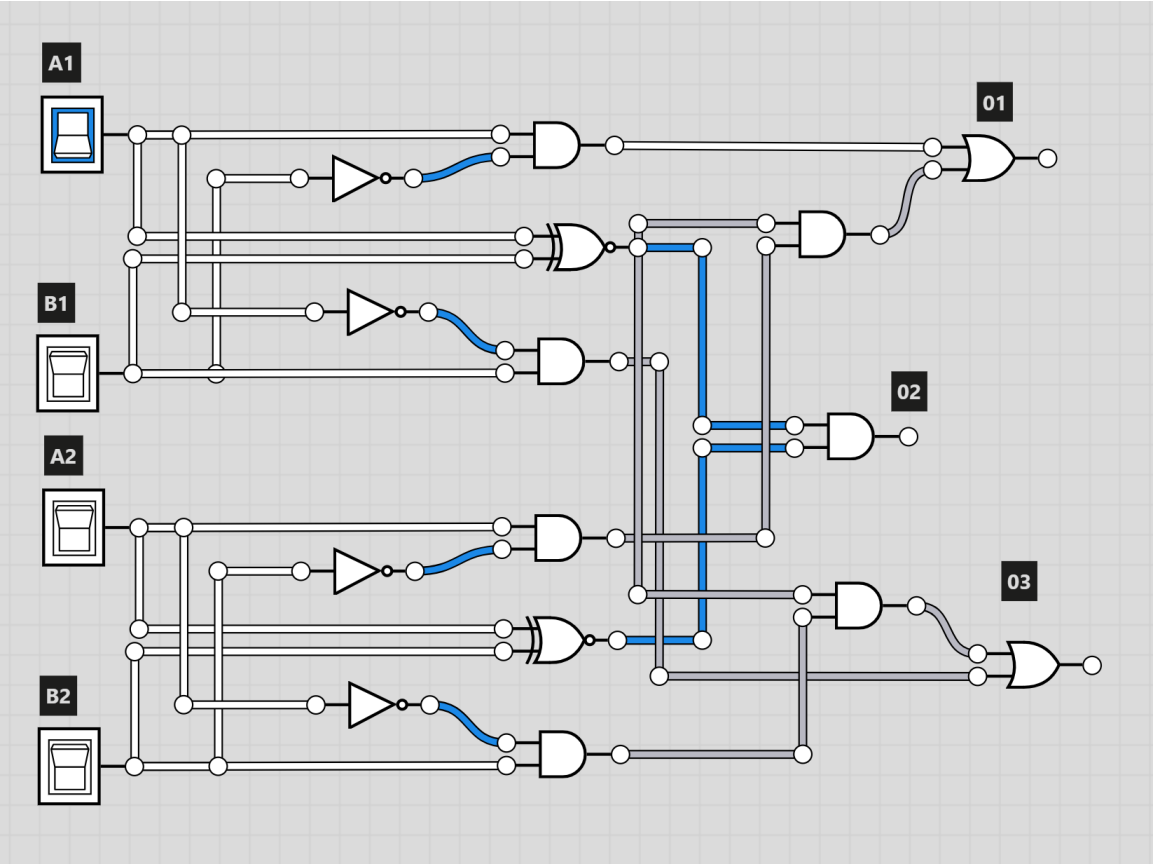
Make sure to include the schematic of your 1-bit comparator so we can verify your solution.

Note: You can either draw on a paper like in the lab session or use a tool such as circuitlab.com to draw a schematic on your computer.

This is the schematic of our 1-bit comparator. By using this twice and comparing the results we created this 2-bit comparator.



A1|B1 are the most important bits of the 2 inputs and A2|B2 are the less important 2 bits.



A is bigger if: A1 > B1 OR (A1 = B1 AND A2 > B2)
A and B are equal if: A1 = B1 AND A2 = B2
B is bigger if: B1 > A1 OR (B1 = A1 AND B2 > A2)

Exercise 3 (0.5 Pts)

What is the logic depth of each of the output ports in the circuit of Exercise 2?

Note: You need to calculate the logic depth of an output port based on the path that contains the highest number of basic logic gates from the inputs to the output port.

Max depth:

Output 01: 4

Output 02: 2

Output 03: 4