Short Introduction to Electrical Engineering

Digital Design and Computer Architecture
Mohammad Sadrosadati
Frank K. Gürkaynak

http://safari.ethz.ch/ddca

In This Lecture

- **Short Introduction to the Electrical Engineering**
  - Current, Voltage, Capacitance
  - Transistors, CMOS
  - Shameless promotion of the D-ITET
- **How to build logic gates**
- **Moore's Law**
- **Power consumption**

Abstraction

	Abstraction Levels	Examples
	Application Software	Programs
	Operating Systems	Device drivers
This Course	**Architecture**	Instructions, Registers
This Course	**Micro architecture**	Datapath, Controllers
This Course	**Logic**	Adders, Memories
This Course	**Digital Circuits**	AND gates, NOT gates
	Analog Circuits	Amplifiers
	Devices	Transistors, Diodes
	Physics	Electrons

Abstraction

	Abstraction Levels	Examples
	Application Software	Programs
	Operating Systems	Device drivers
	Architecture	Instructions, Registers
	Micro architecture	Datapath, Controllers
	Logic	Adders, Memories
Today	**Digital Circuits**	AND gates, NOT gates
	Analog Circuits	Amplifiers
	Devices	Transistors, Diodes
	Physics	Electrons

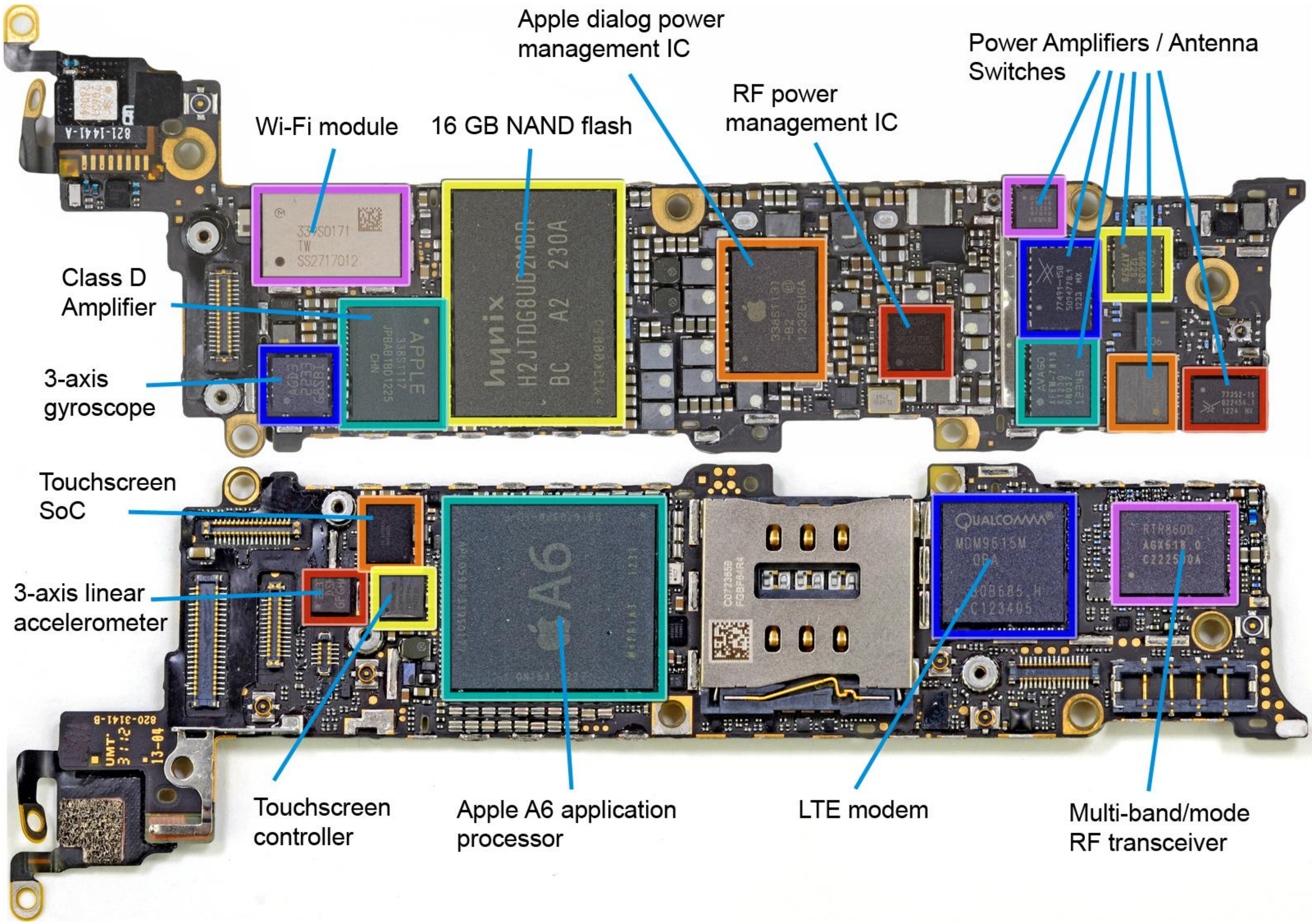
The Electrical Engineering Perspective

- **What areas are there in Electrical Engineering? What are they good for ?**

- **This course covers the basics, we will not go to much detail.**

- **Those who are more interested are welcome to visit classes from the D-ITET in later semesters.**
  - VLSI **1**,**2**,3,4 (5^{th} – 8^{th}) semester

Many Microchips in a System



Picture of iPhone5s from http://www.ifixit.com/Teardown/iPhone-5-Teardown/10525

Subsystems In iPhone (Example)

- Battery / power subsystem
- Processor / Memory
- Antenna / Radio frequency communication
- Telecommunication en/decoding
- Audio subsystem
- Camera and Display driver
- External Interfaces (touch screen, cards, data transfer)

What Specializations Are At D-ITET?

- **Transmitting and Receiving Electromagnetic Waves**
  - Design antennas to receive and transmit electromagnetic waves
  - Specialized circuits that can send and receive signals over long distances

- **Communication Theory**
  - Find out efficient ways of encoding data to improve data transmission over communication channels

What Specializations Are At D-ITET?

- **Audio / Video signal processing**
  - Enable talking even in noisy environments
  - Reduce the amount of data that needs to be transmitted for video sequences

- **Analog Electronics**
  - Convert analog signals to digital domain for further processing
  - Reproduce the analog signal from a sequence of digital values

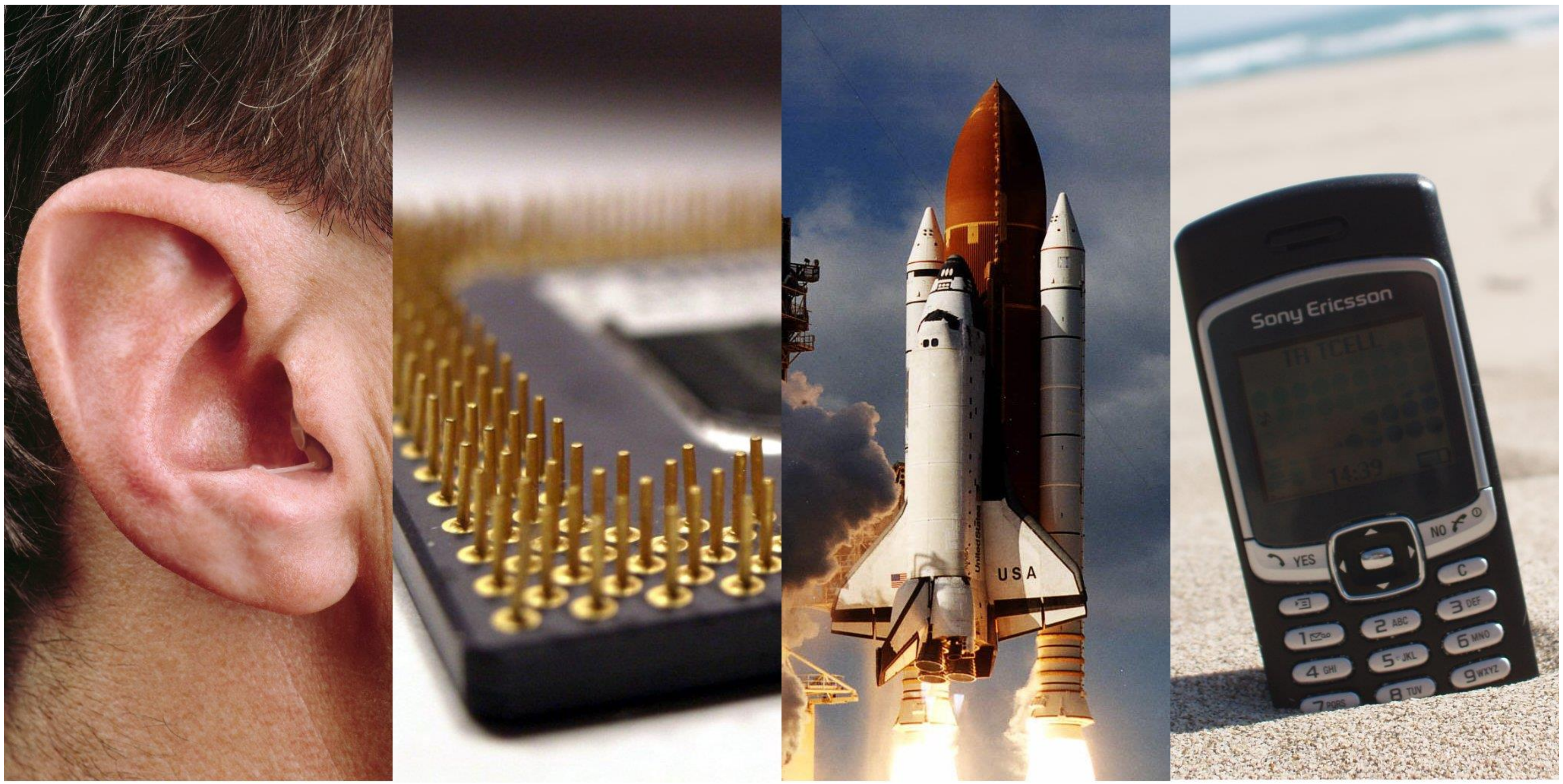
- **Digital Electronics**

The topic of this lecture

The Goal Of Circuit Design Is To Optimize:

- **Area**
  - Net circuit area is proportional to the cost of the device
- **Speed / Throughput**
  - We want circuits that work faster, or do more
- **Power / Energy**
  - Mobile devices need to work with a limited power supply
  - High performance devices dissipate more than $100W/cm^2$
- **Design Time**
  - Designers are expensive
  - The competition will not wait for you

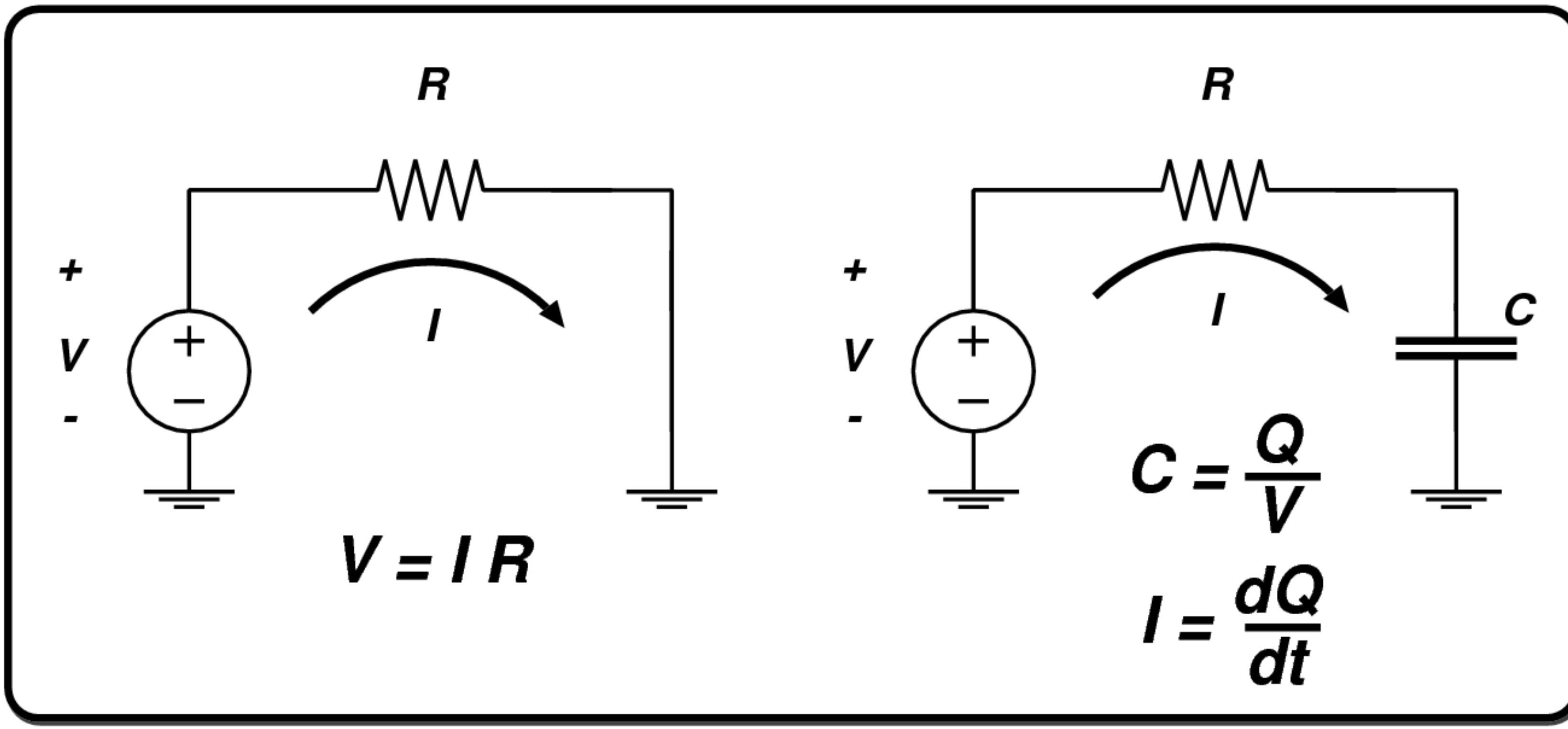
Requirements Depend On Application



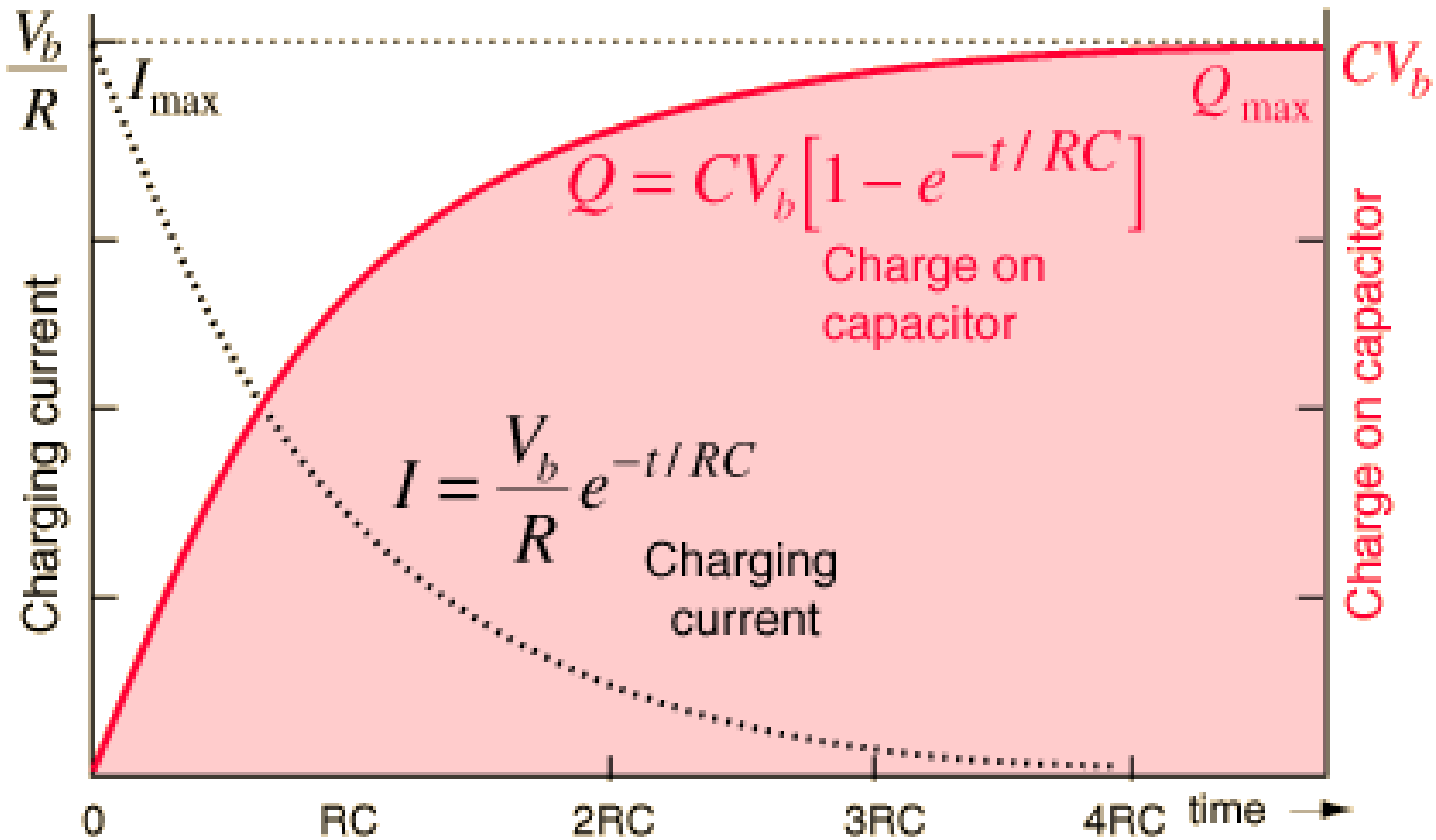
(My) Principles For Engineering

- **Good engineers are lazy**
  - They do not want to work unnecessarily, be creative
- **They know how to ask the question "WHY?"**
  - Take nothing for granted
- **Engineering is not religion**
  - Use what works best for you
- **Keep it simple and stupid**
  - Engineers' job is to manage complexity

Basic Electric Relations



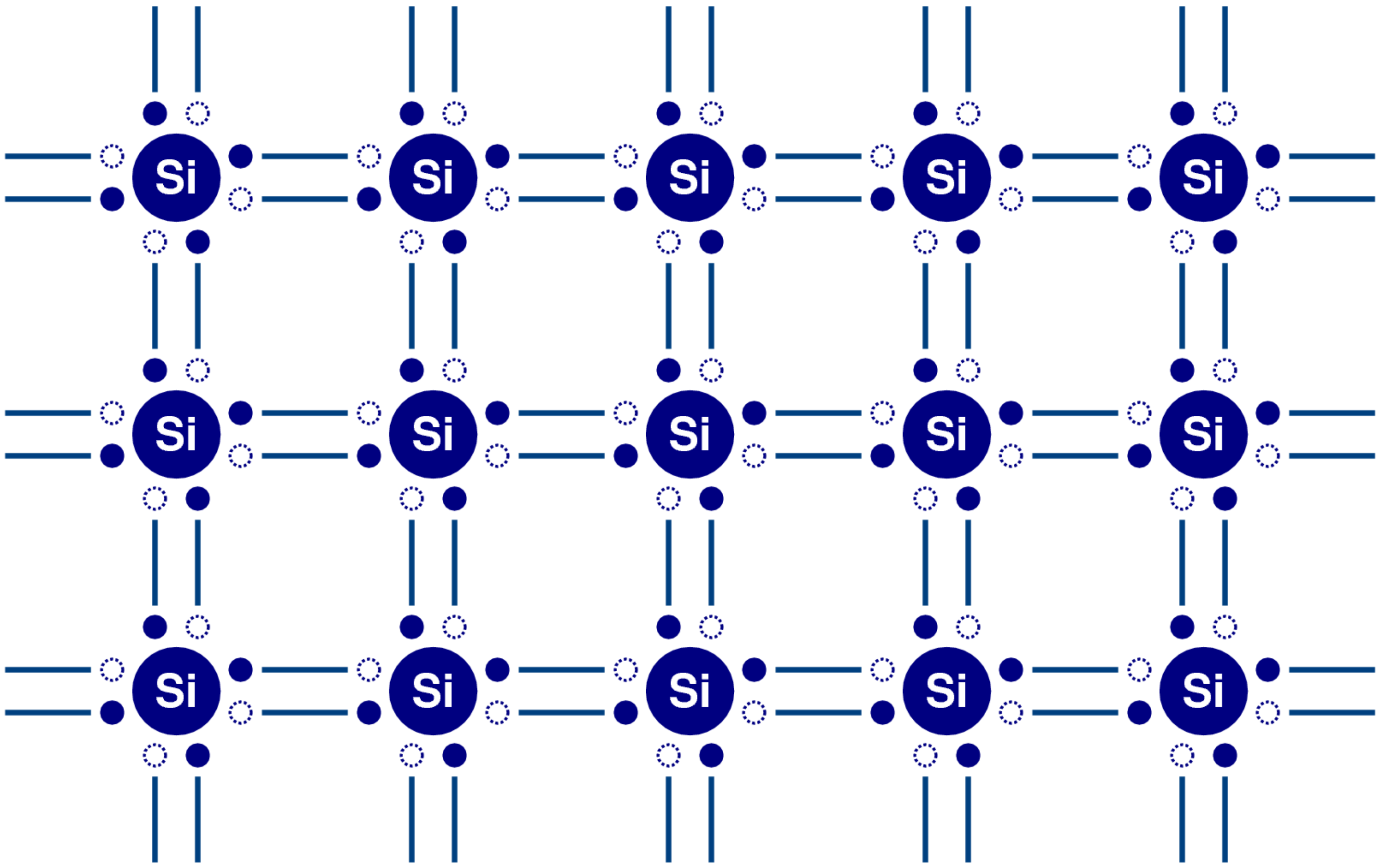
Charging a Capacitor Takes Time



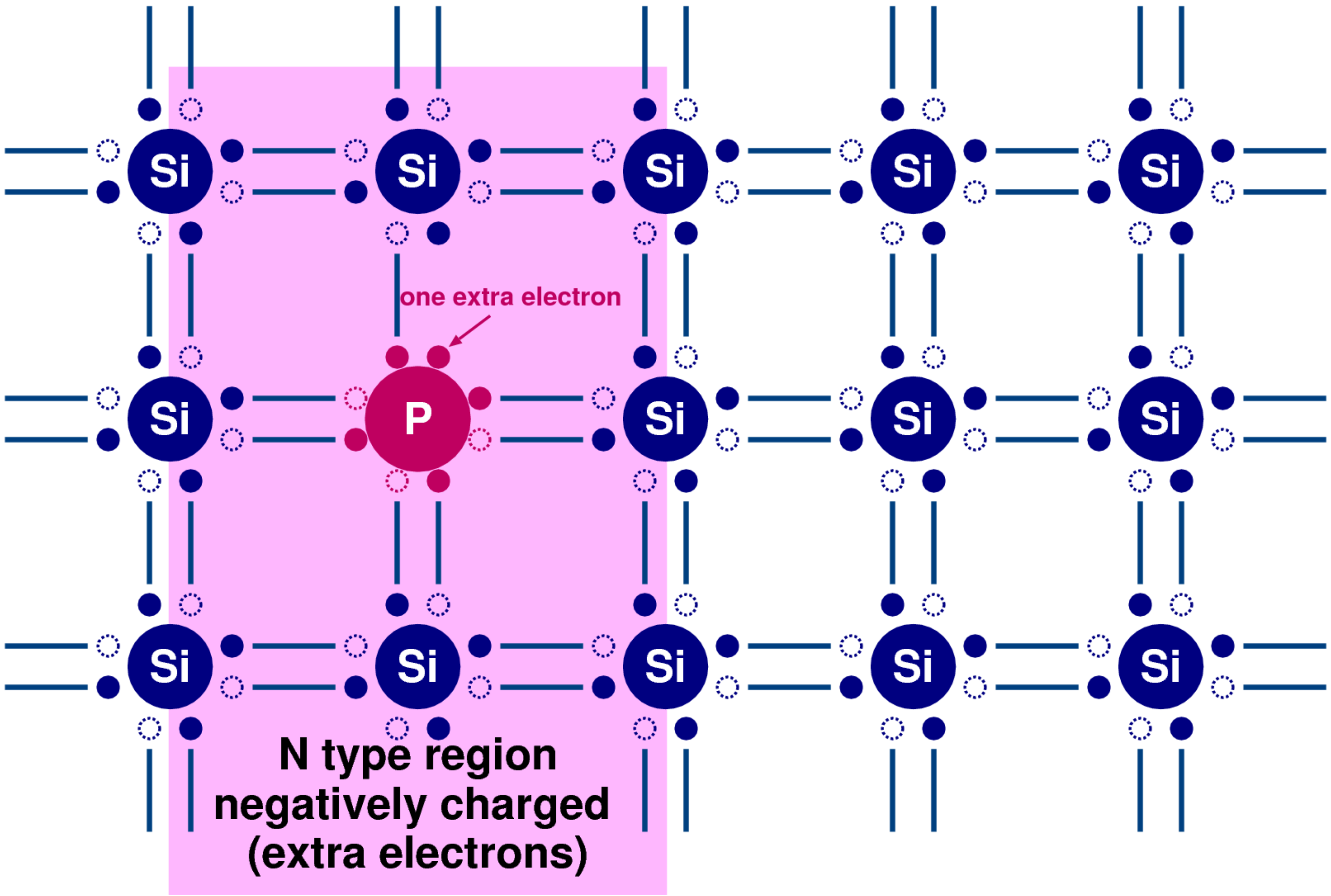
Building Blocks For Microchips

- **Conductors**
  - Metals: Aluminum, Copper
- **Insulators**
  - Glass (SiO_2), Air
- **Semiconductors**
  - Silicon (Si), Germanium (Ge)

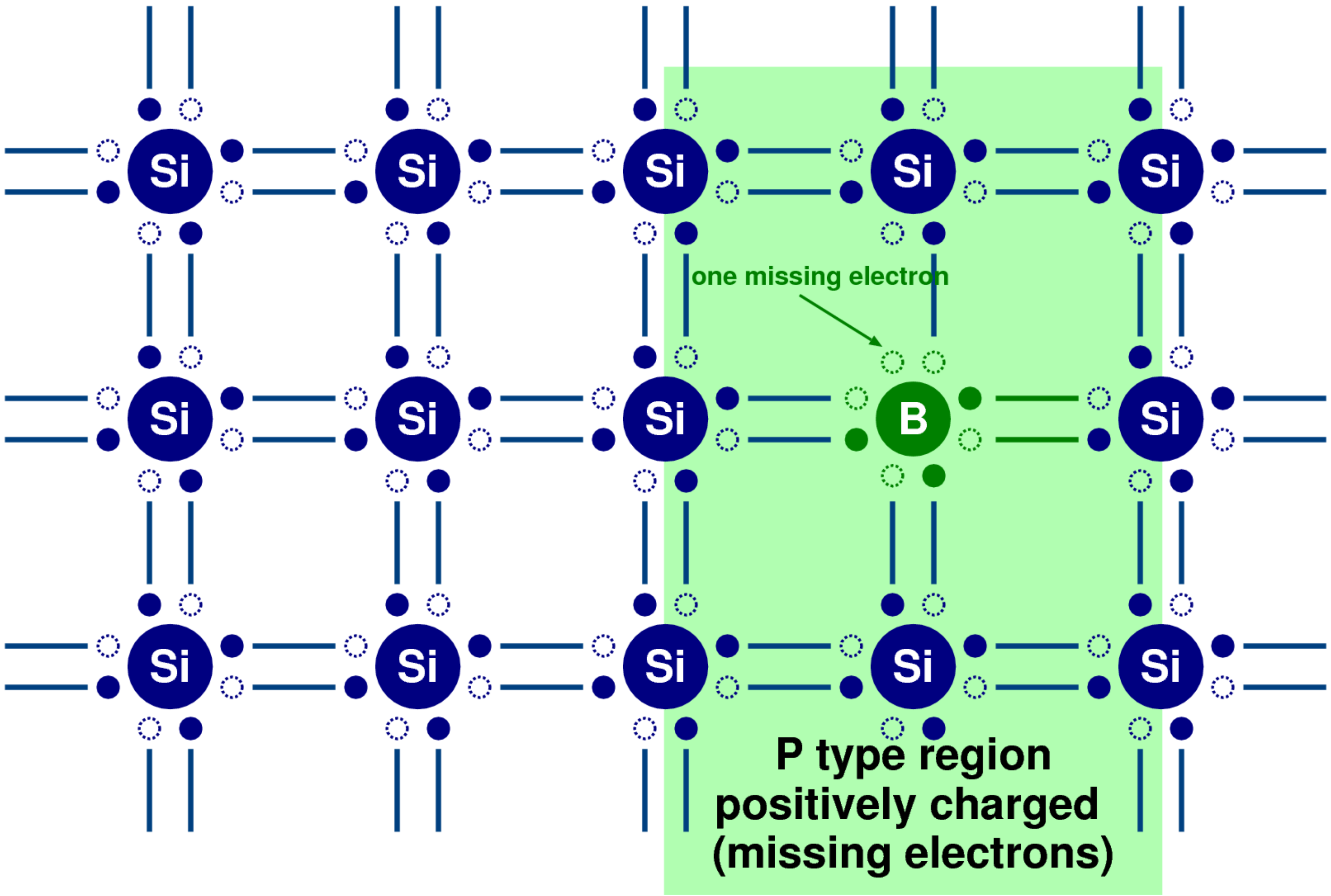
Semiconductor



N-type Doping



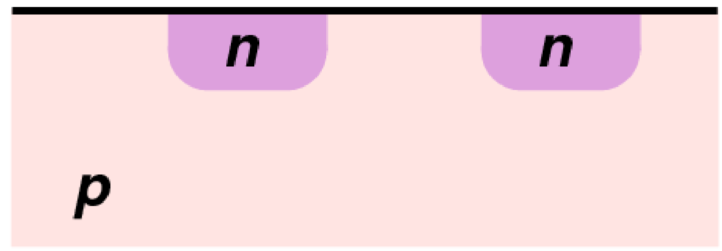
P-type Doping



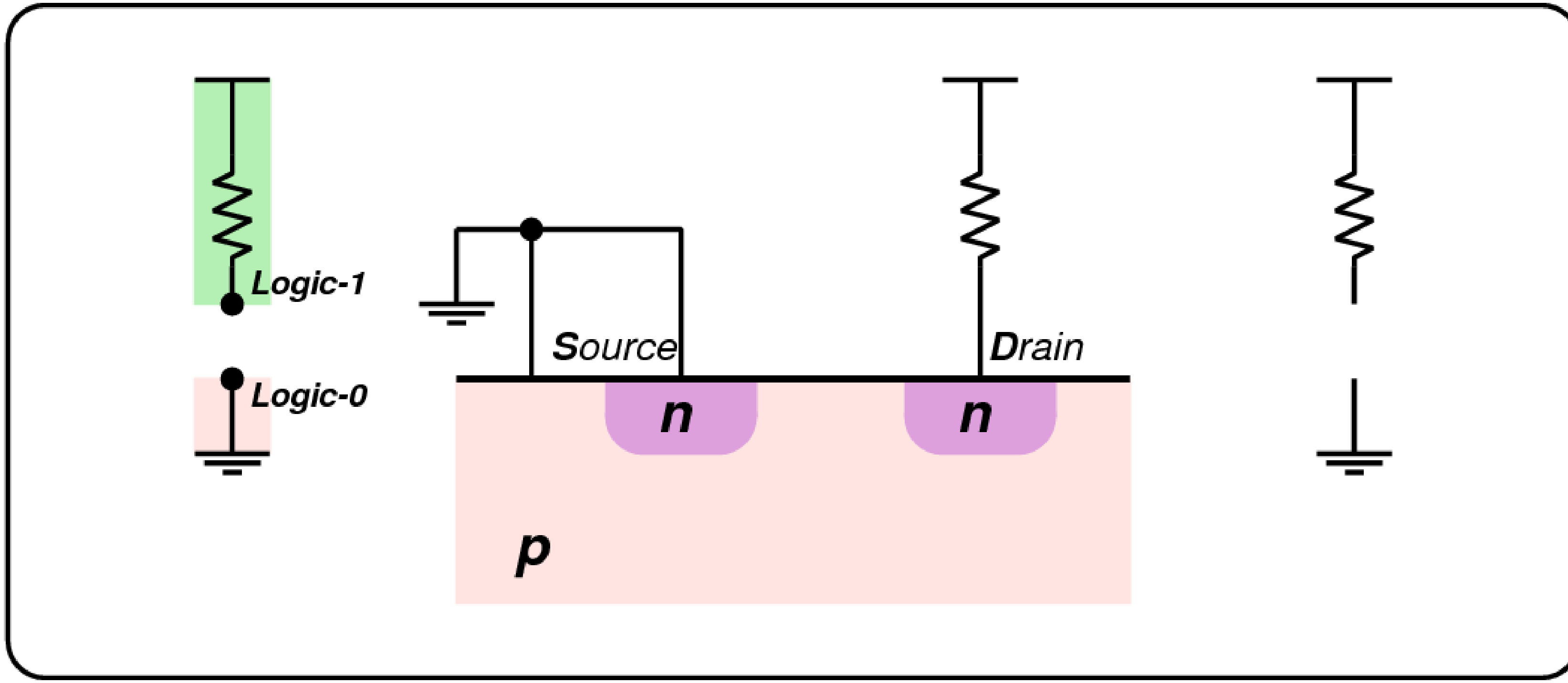
What Is So Great About Semiconductors?

- **You can "engineer" its properties**
  - Make it **P type** by injecting type-III elements (B, Ga, In)
  - Make it **N type** by injecting elements from type-V (P,As)
- **Starting with a pure semiconductor, you can combine P and N regions next to each other**
- **Allows you to make interesting electrical devices**
  - Diodes
  - Transistors
  - Thrystors

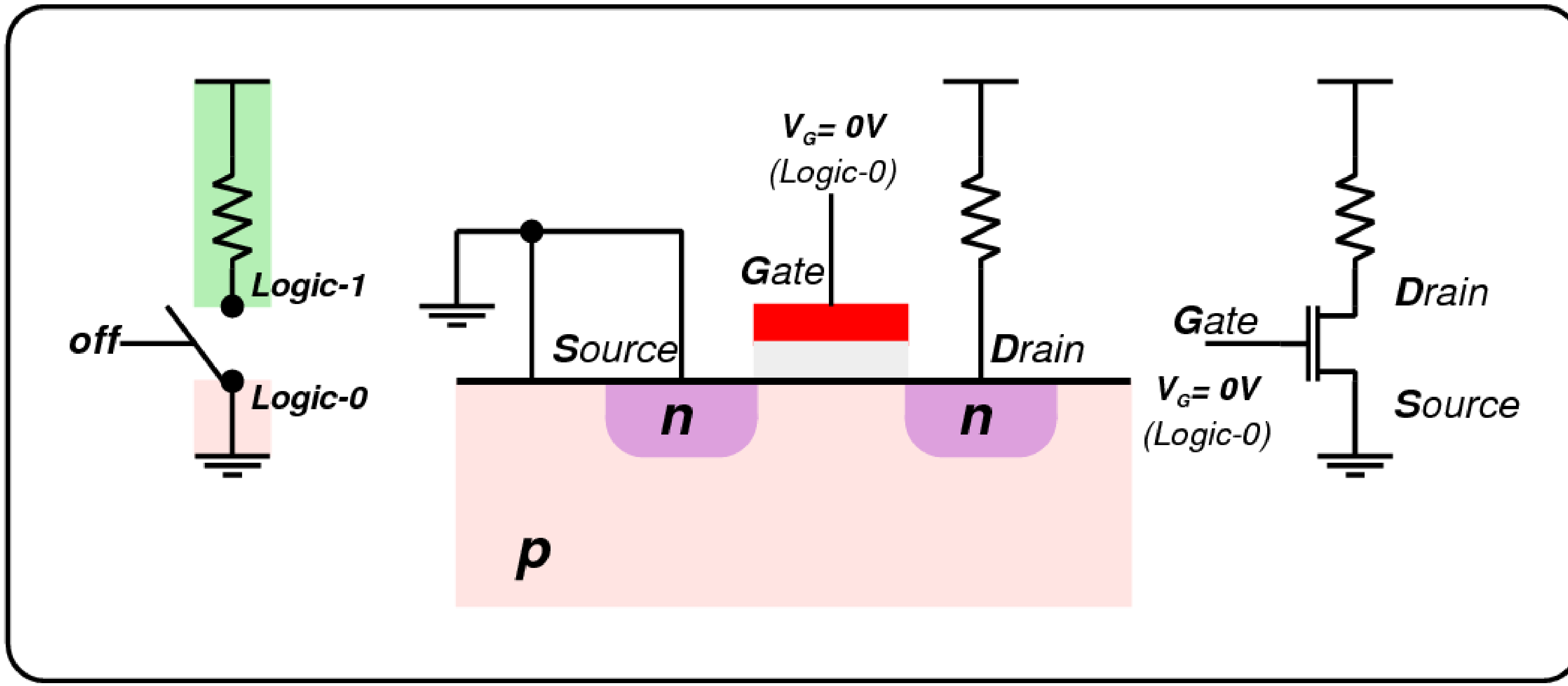
The Story About Transistors



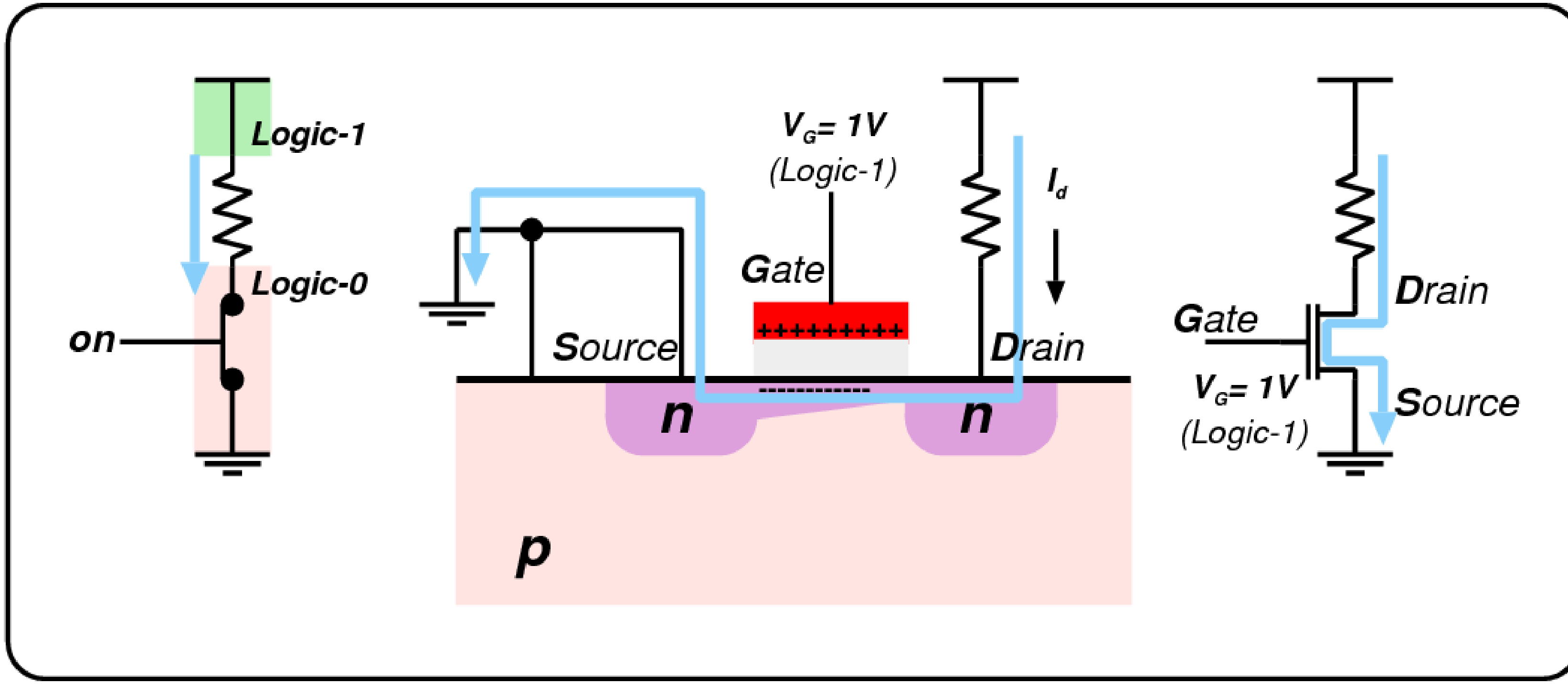
The Story About Transistors



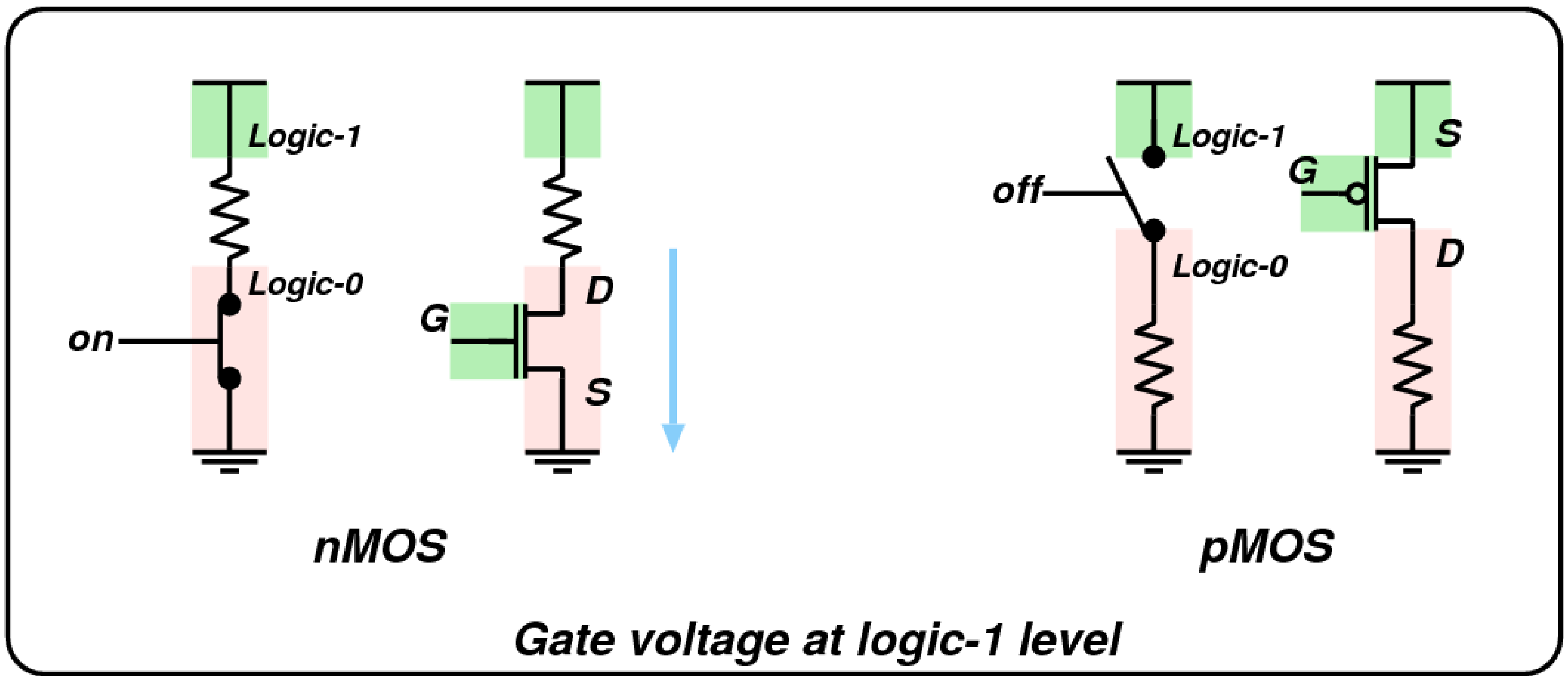
The Story About Transistors - Switch OPEN



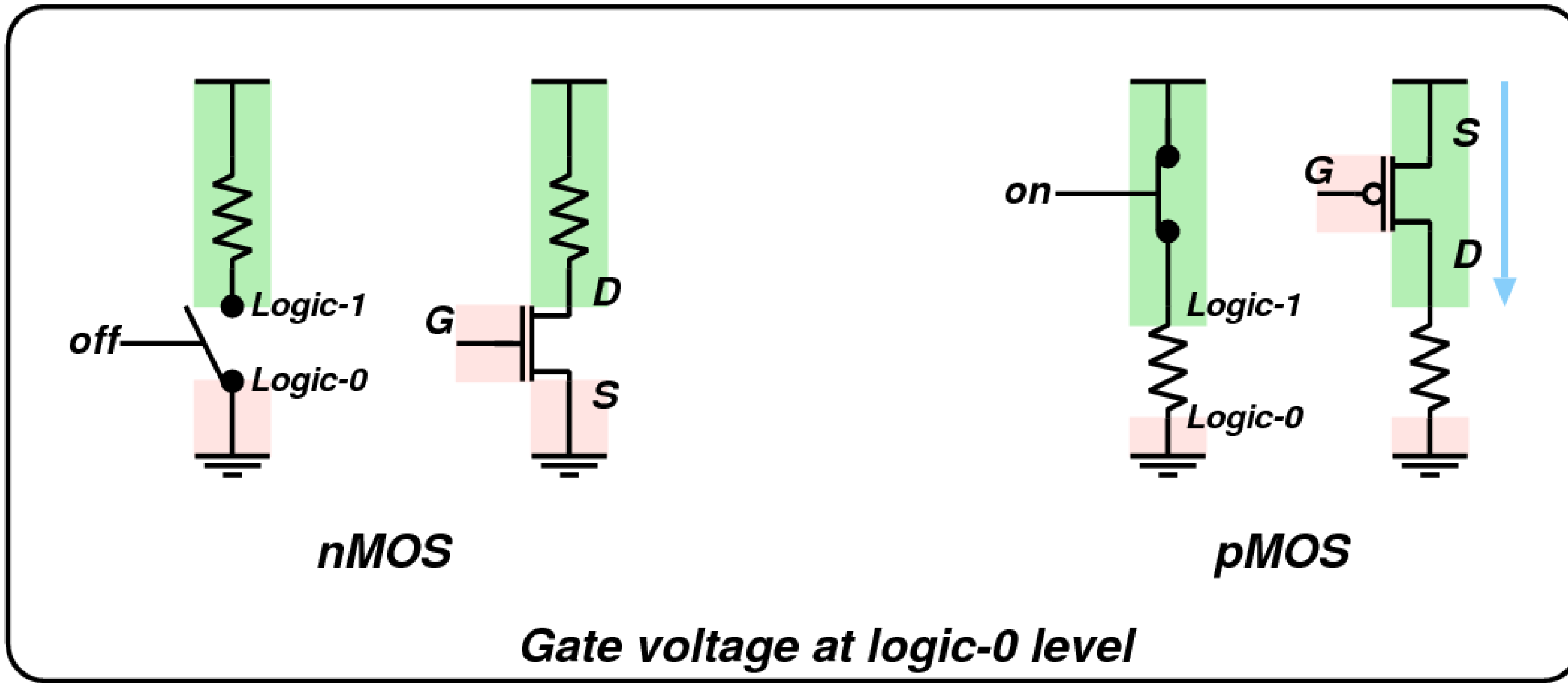
The Story About Transistors - Switch CLOSED



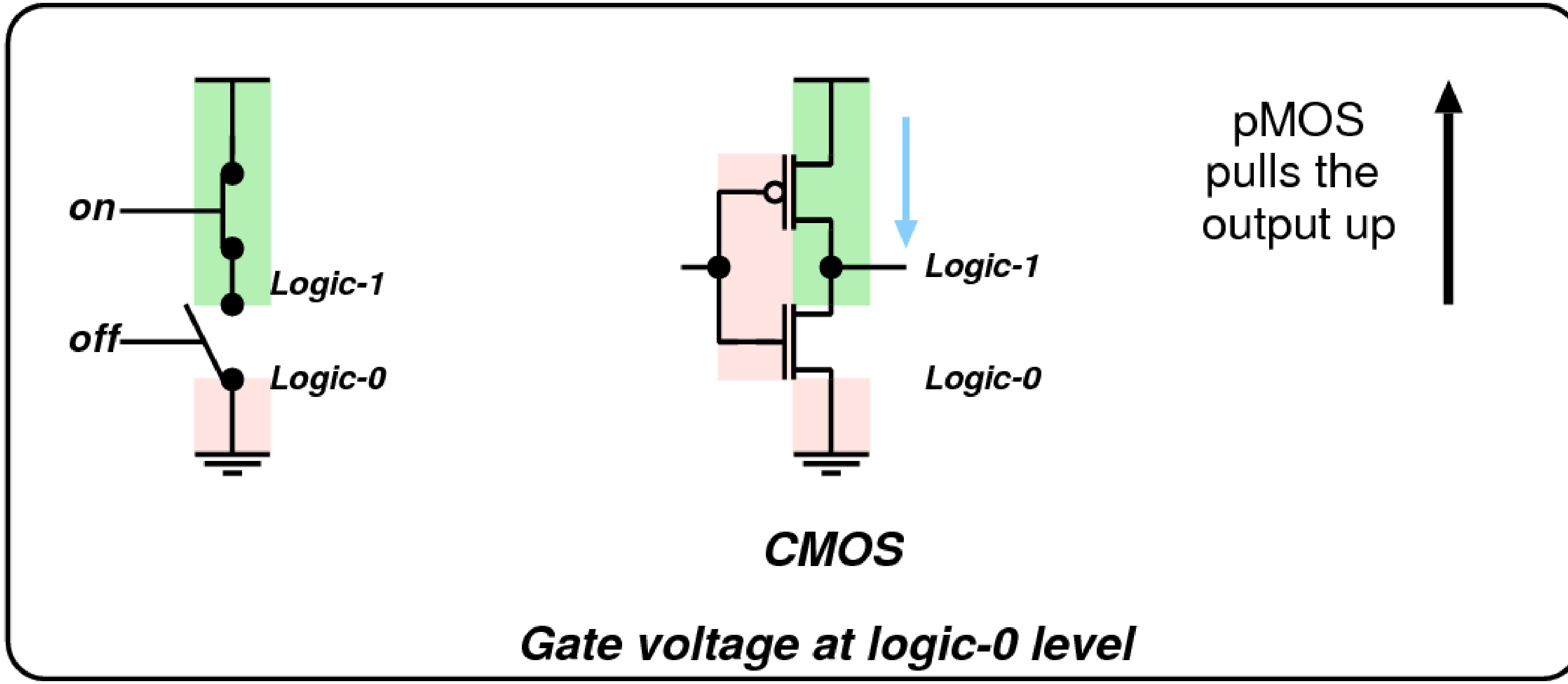
pMOS Is Just The Dual Of The nMOS



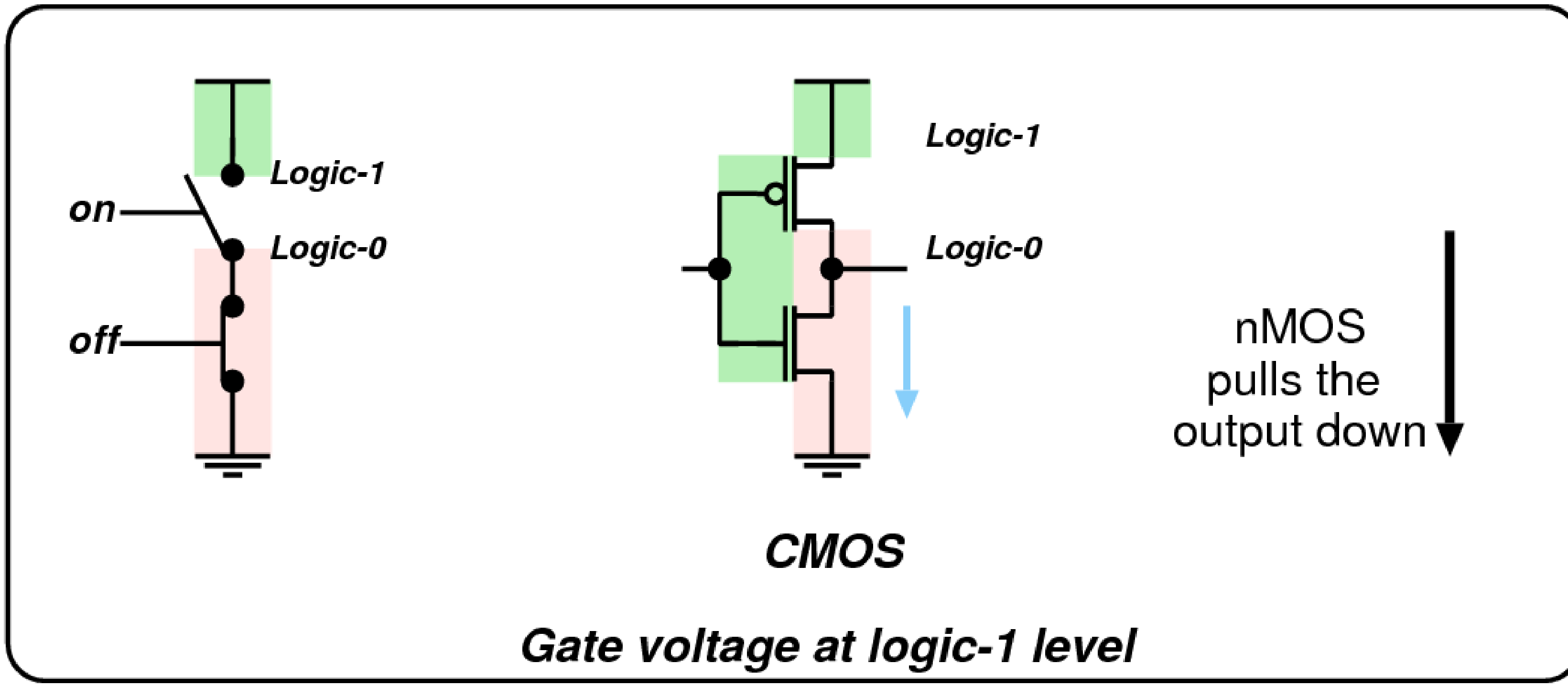
pMOS Is Just The Dual Of The nMOS



nMOS + pMOS = CMOS



nMOS + pMOS = CMOS



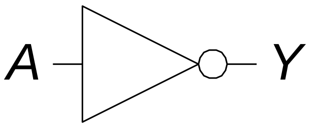
When One Type MOS works, the other is the load

What Is So Good About CMOS?

- **No input current**
  - Capacitive input, no resistive path from the input.
- **No current when output is at logic levels**
  - Little static power, current is needed only when switching
- **Electrical properties determined directly by geometry**
  - A transistor that is 2 times larger drives twice the current
- **Very simple to manufacture**
  - pMOS and nMOS can be manufactured on the same substrate

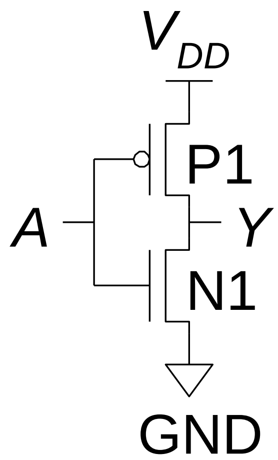
CMOS Gates: NOT Gate

NOT



$Y = \overline{A}$

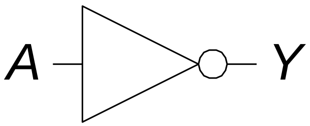
A	Y
0	1
1	0



A	P1	N1	Y
0			
1			

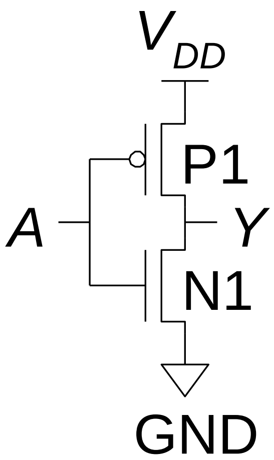
CMOS Gates: NOT Gate

NOT



$Y = \overline{A}$

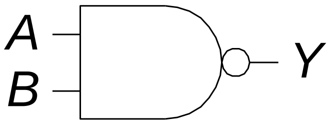
A	Y
0	1
1	0



A	P1	N1	Y
0	ON	OFF	1
1	OFF	ON	0

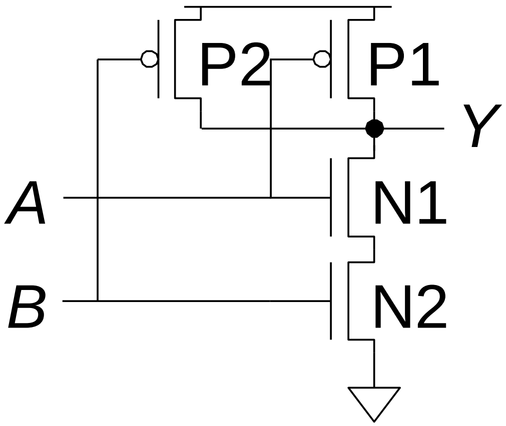
CMOS Gates: NAND Gate

NAND



$Y = \overline{AB}$

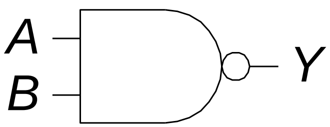
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



A	B	P1	P2	N1	N2	Y
0	0					
0	1					
1	0					
1	1					

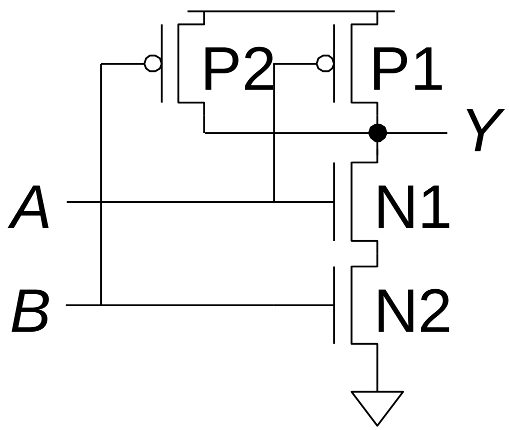
CMOS Gates: NAND Gate

NAND



$Y = \overline{AB}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



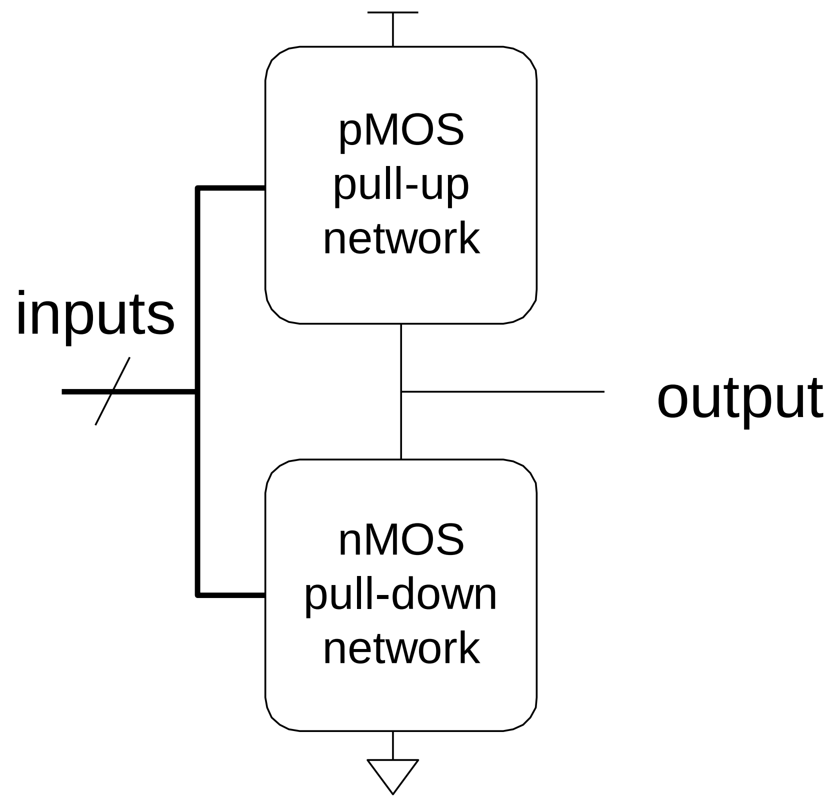
N1 and N2 are connected in series; both must be ON to pull the output to GND.

P1 and P2 are in parallel; only one must be ON to pull the output up to VDD.

A	B	P1	P2	N1	N2	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

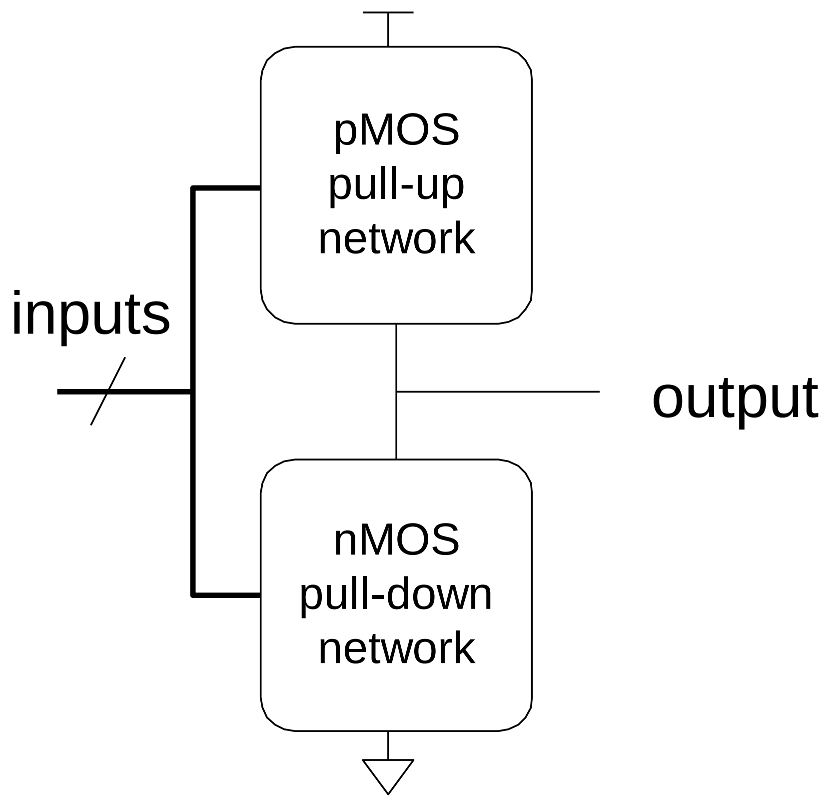
CMOS Gate Structure

- **The general form used to construct any inverting logic gate, such as: NOT, NAND, or NOR.**
  - The networks may consist of transistors in series or in parallel.
  - When transistors are in parallel, the network is **ON** if either transistor is **ON**.
  - When transistors are in series, the network is **ON** only if all transistors are **ON**.



CMOS Gate Structure

- **In a proper logic gate:**
  - One of the networks should be ON and the other OFF at any given time.
- **Use the rule of conduction complements:**
  - When nMOS transistors are in series, the pMOS transistors must be in parallel.
  - When nMOS transistors are in parallel, the pMOS transistors must be in series.

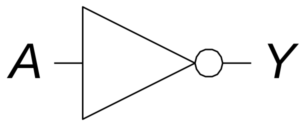


Logic Gates

- **Perform logic functions:**
  - inversion (NOT), AND, OR, NAND, NOR, etc.
- **Single-input:**
  - NOT gate, buffer
- **Two-input:**
  - AND, OR, XOR, NAND, NOR, XNOR
- **Multiple-input gates:**

Single-Input Logic Gates

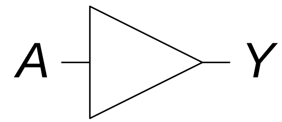
NOT



$$Y = \overline{A}$$

A	Y
0	
1	

BUF

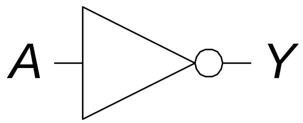


$$Y = A$$

A	Y
0	
1	

Single-Input Logic Gates

NOT

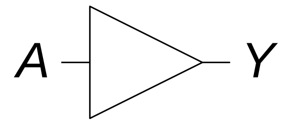


$$Y = \overline{A}$$

A	Y
0	1
1	0

NOT is also called an “inverter”

BUF



$$Y = A$$

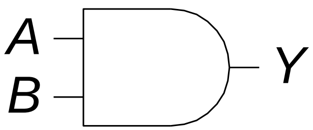
A	Y
0	0
1	1

Might seem useless “what does it do?”

Triangle represents a “buffer”, a “o” represents inversion

Two-Input Logic Gates

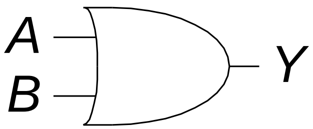
AND



$$Y = AB$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

OR

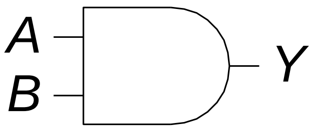


$$Y = A + B$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

Two-Input Logic Gates

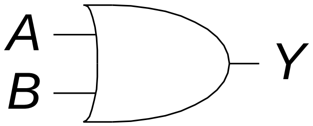
AND



$$Y = AB$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR



$$Y = A + B$$

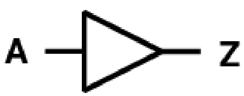
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Y=AB, Y=A AND B
Y=A∩B (intersection),
(therefore the representation)

Y=A+B Y=A OR B
Y=A∪B (Union)
(therefore the representation)

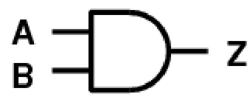
Common Logic Gates

Buffer



A	Z
0	0
1	1

AND



A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

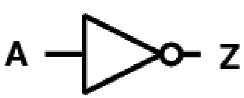
OR

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

XOR

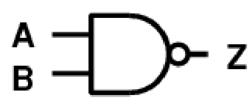
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

Inverter



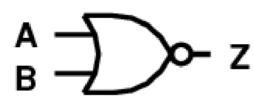
A	Z
0	1
1	0

NAND



A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

NOR



A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

XNOR

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

Multiple-Input Logic Gates

- **3, 4 (or even more) input AND, OR, XOR gates**

- **Compound gates**
  - AND-OR
  - OR-AND
  - AND-OR-INVERT
  - OR-AND-INVERT

- **Other cells**
  - Multiplexers (we will see them soon)
  - Adders (also coming soon)

Logic Levels

- **Define discrete voltages to represent 1 and 0**
- **For example, we could define:**
  - 0 to be *ground* or 0 volts
  - 1 to be V_{DD} or 5 volts
- **What about 4.99 volts? Is that a 0 or a 1?**
- **What about 3.2 volts?**
- As chips have progressed to smaller transistors, *VDD has* dropped to 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, or even lower to save power and avoid overloading the transistors.

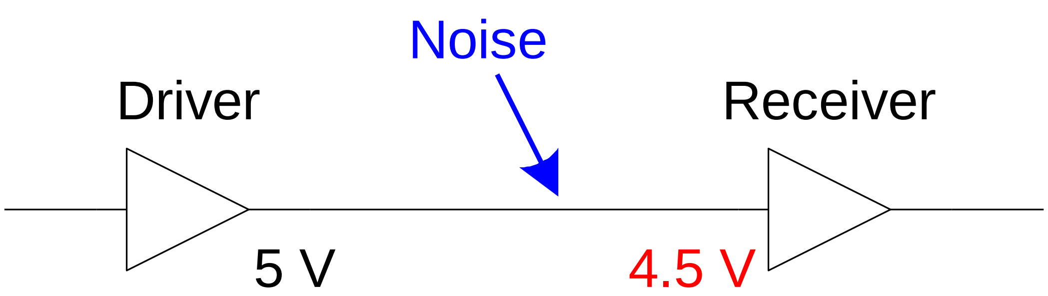
Logic Levels

- **Define a *range* of voltages to represent 1 and 0**
- **Define different ranges for outputs and inputs to allow for *noise* in the system**
- **What is noise?**

What is Noise?

- **Anything that degrades the signal**
  - E.g., resistance, power supply noise, coupling to neighboring wires, etc.

- **Example: a gate (driver) could output a 5 volt signal but, because of resistance in a long wire, the signal could arrive at the receiver with a degraded value, for example, 4.5 volts**

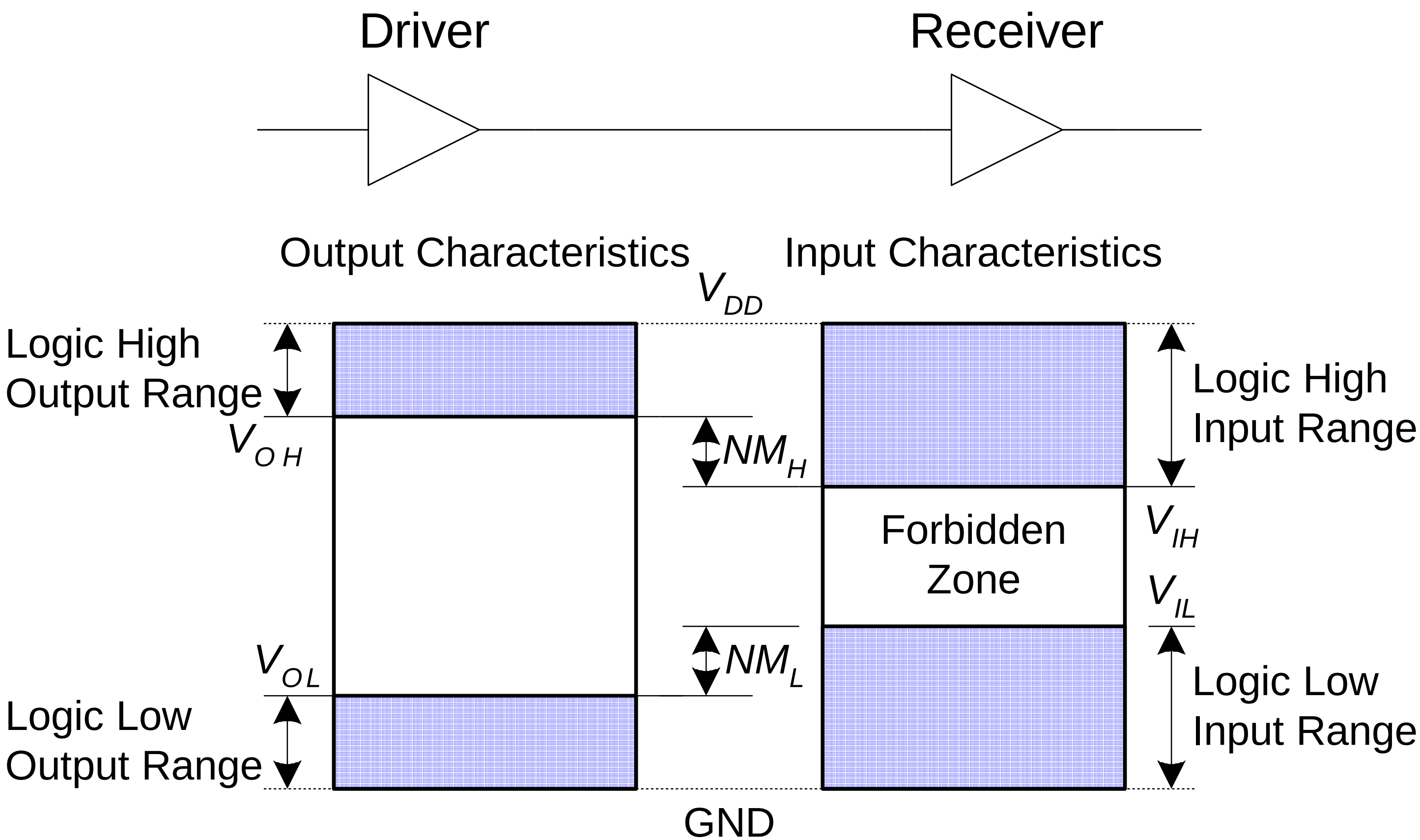


The Static Discipline

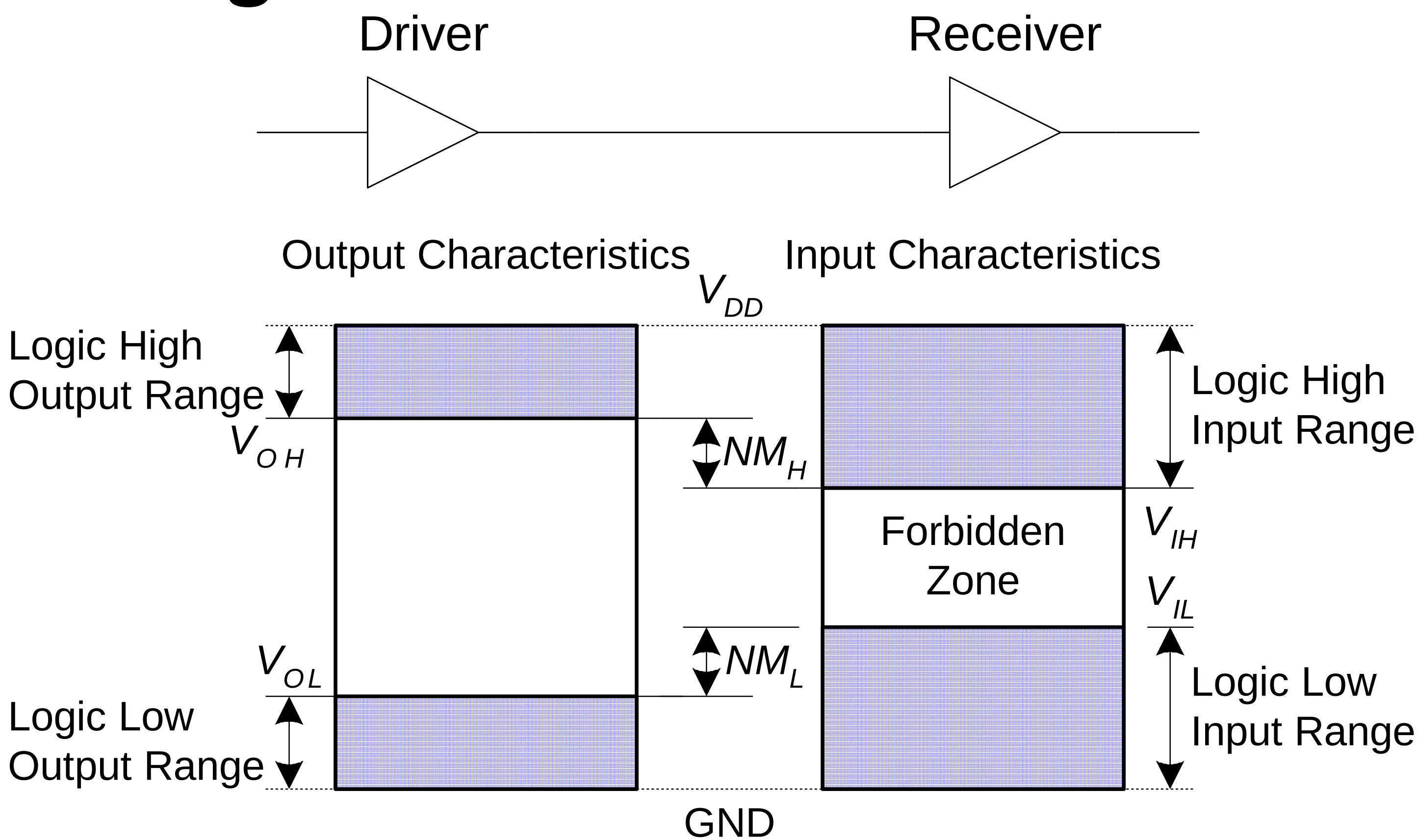
- **Given logically valid inputs, every circuit element must produce logically valid outputs**

- **Discipline ourselves to use limited ranges of voltages to represent discrete values**

Logic Levels



Noise Margins



$$NM_H = V_{OH} - V_{IH}$$

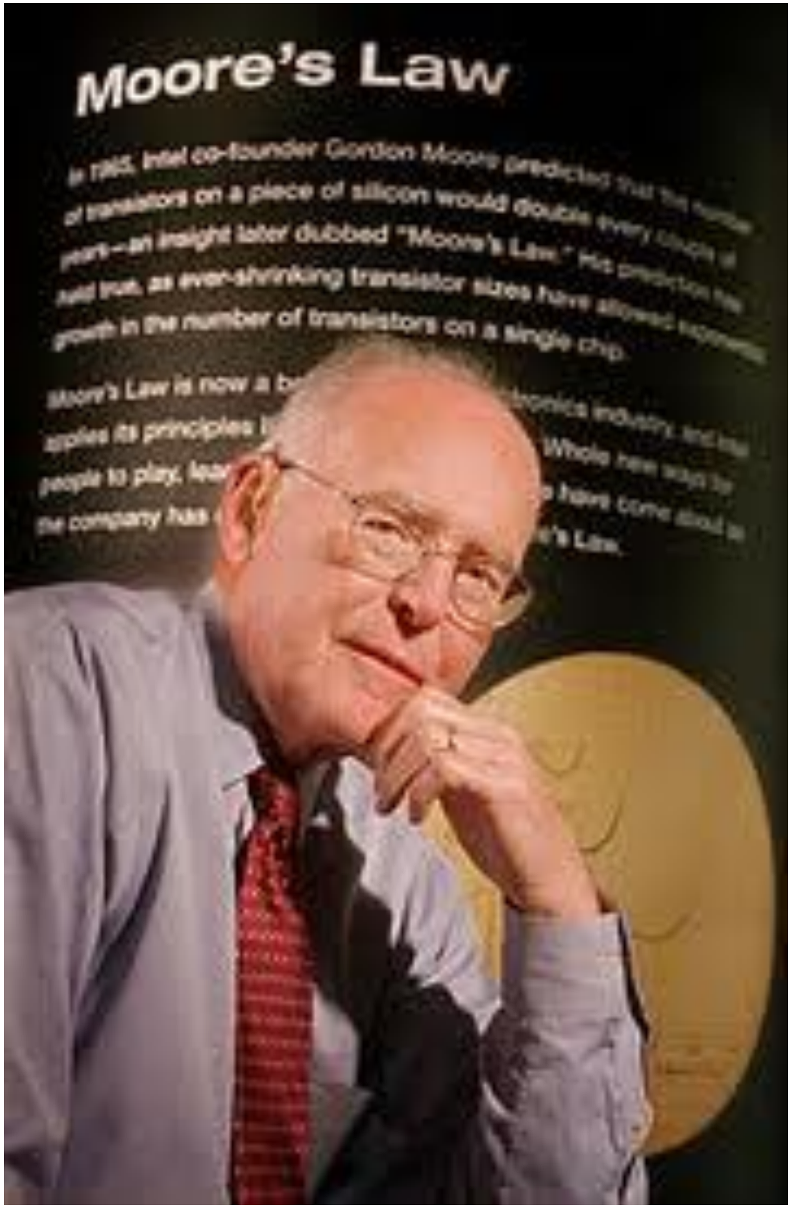
$$NM_L = V_{IL} - V_{OL}$$

Moore’s Law

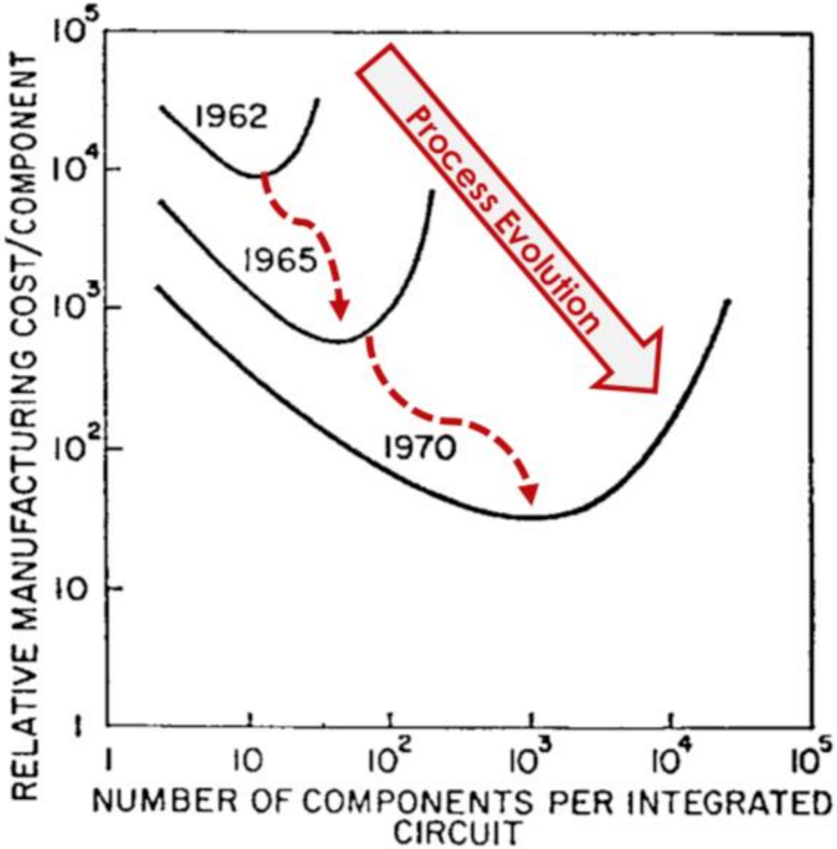
- **Coined by Gordon Moore:**
  - In 1965
  - Co-founder of Intel

Number of transistors that can be manufactured doubles roughly every 18 months.

- **In other words: it increases 100 fold over 10 years.**



Let's talk about Moore's Law



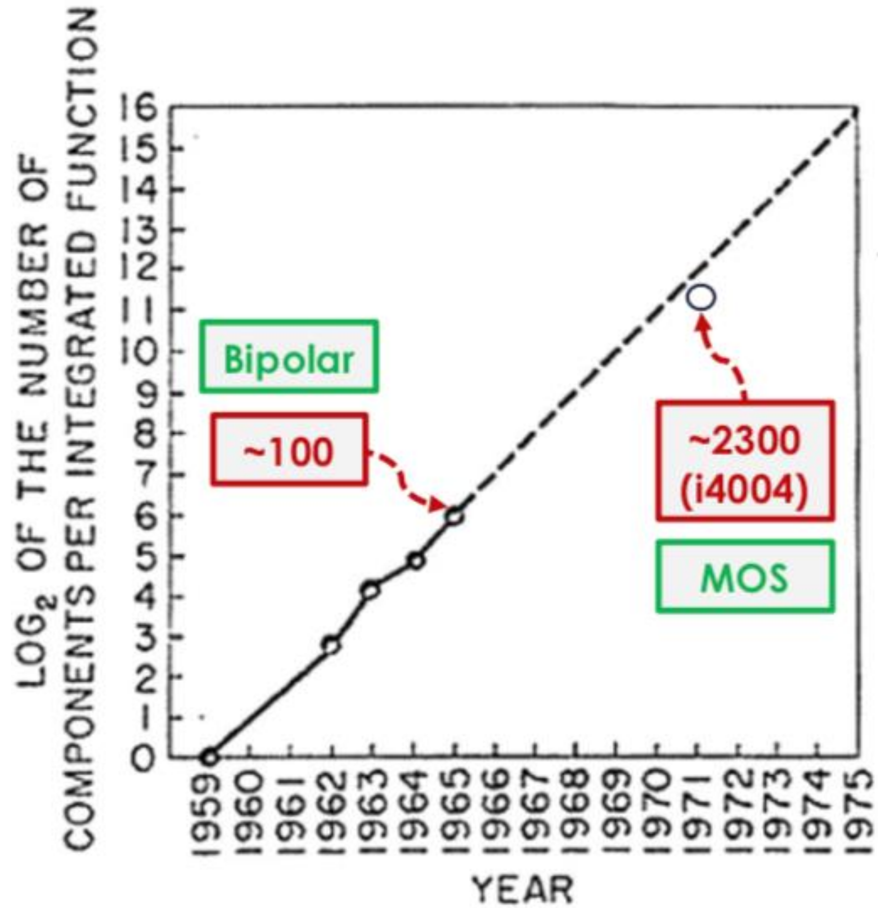


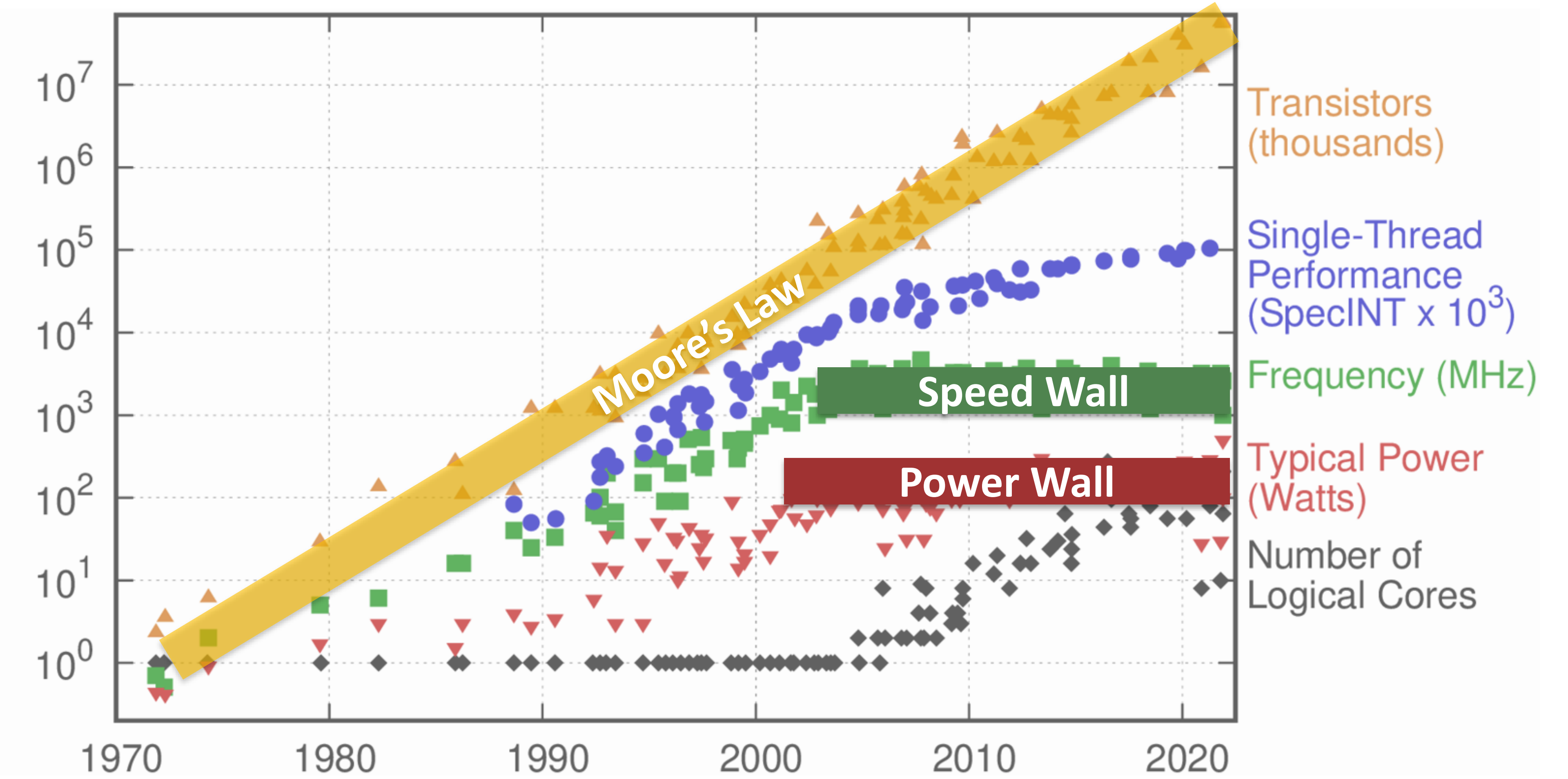
Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

Gordon Moore, Electronics Letters 1965, IEDM 1975

Moore's Law or Self-fulfilling prophecy

- **It started as an observation**
  - Has been predicated to stop many times (even by Gordon Moore)
- **It is catchy**
  - Every 2 years (or 18 months or..) the number of transistors (functions) double
  - Not terribly accurate
- **Good direction to follow**
  - In two years 2x transistors
- **Easy to sort of cheat**
  - Is the circuit area the same, is it the date it was prototyped or released

50 years of processor trend data (Karl Rupp)



https://github.com/karlrupp/microprocessor-trend-data

How Do We Keep Moore's Law

- **Manufacturing smaller structures**
  - Some structures are already a few atoms in size
- **Developing materials with better properties**
  - Copper instead of Aluminum (better conductor)
  - Hafnium Oxide, air for Insulators
  - Making sure all materials are compatible is the challenge
- **Optimizing the manufacturing steps**
  - How to use 193nm ultraviolet light to pattern 20nm structures
- **New technologies**
  - FinFET, Gate All Around transistor, Single Electron Transistor…

Power Consumption

- **Power = Energy consumed per unit time**

- **Two types of power consumption:**
  - Dynamic power consumption
  - Static power consumption

Dynamic Power Consumption

- **Power to charge transistor gate capacitances**

- **The energy required to charge a capacitance, *C*, to V_{DD} is CV_{DD}^2**

- **If the circuit is running at frequency *f*, and all transistors switch (from 1 to 0 or vice versa) at that frequency, the capacitor is charged *f*/2 times per second (discharging from 1 to 0 is free).**

- **Thus, the total dynamic power consumption is:**

$$P_{dynamic} = \frac{1}{2} C V_{DD}^2 f$$

Static Power Consumption

- **Power consumed when no gates are switching**
- **It is caused by the quiescent supply current, I_{DD}, also called the *leakage current***
- **Thus, the total static power consumption is:**

$$P_{static} = I_{DD}V_{DD}$$

Power Consumption Example

- **Estimate the power consumption of a wireless handheld computer**
  - V_{DD} = 1.2 V
  - C = 20 nF
  - f = 1 GHz
  - I_{DD} = 20 mA

Power Consumption Example

- **Estimate the power consumption of a wireless handheld computer**
  - V_{DD} = 1.2 V
  - C = 20 nF
  - f = 1 GHz
  - I_{DD} = 20 mA

$$
\begin{aligned}
P_{total} &= P_{dynamic} && + P_{static} \\
&= \tfrac{1}{2} C V_{DD}^2 f && + I_{DD} V_{DD} \\
&= \tfrac{1}{2}(20\text{ nF})(1.2\text{ V})^2(1\text{ GHz}) && + (20\text{ mA})\,(1.2\text{ V}) \\
&= \mathbf{14.4\text{ W}}
\end{aligned}
$$

What Did We Learn?

- **What is a transistor?**
  - It is a switch that can be controlled electrically
- **How are logic gates built?**
- **What is Moore's Law, why is it interesting**
- **What does the power consumption depend on?**
  - Activity (what does the circuit do)
  - Clock Frequency
  - Voltage
  - Total switched capacitance