Digital Design and Computer Architecture: Lab Report		
Lab 8: Full System Integration (Session II)		
Date		Grade
Names		
		Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and all other files you used for the report, i.e., the entire Verilog project folder and/or all schematics you drew. If any files are missing, it may negatively impact your grade. No shortcuts/links will be accepted.

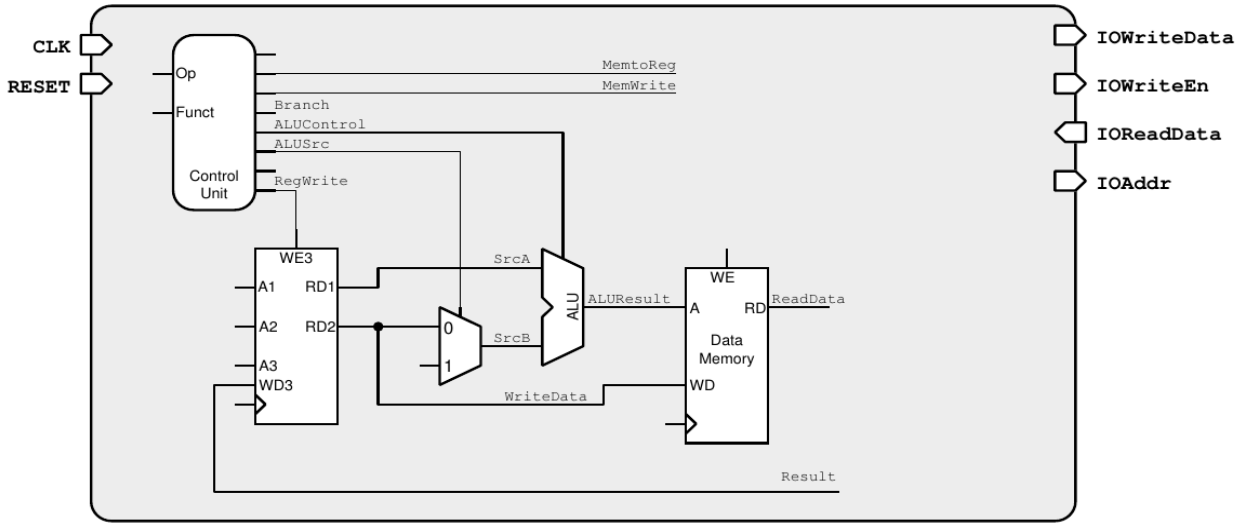
Only one member from each group should submit the report. All members of the group will get the same grade.

The submitted file's name should be *Lab8-2_LastName1_LastName2.zip* (or *.tar*), where *LastName1, LastName2* are the last names of the members of the group.

The deadline for the report is a hard deadline and it will not be extended.

Exercise 1 (2 Points)

Below is a part of the MIPS block diagram. Draw the necessary modifications for the memory-mapped I/O on this block diagram. (We are only interested in the SW and LW instructions; the rest of the block diagram has been purposefully left out. *Hint: If your circuit works, you already implemented this in the* MIPS.v *module.*



Exercise 2 (1 Point)

Using Figure 1 as a reference, what additional hardware/architectural changes are needed in the top module (*top.v* file) to implement Challenge 2 described in the Manual of Lab 8, Session 2? You can either draw the additional circuitry required or write in your own words here.