Digital Design and Computer Architecture: Lab Report		
Lab 9: The Performance of MIPS		
Date		Grade
Names		
		Lab session / lab room

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and all other files you used for the report, i.e., the entire Verilog project folder and/or all schematics you drew. If any files are missing, it may negatively impact your grade. No shortcuts/links will be accepted.

Only one of the members of each group should submit. All members of the group will get the same grade.

The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

The deadline for the report is a hard deadline and it will not be extended.

Exercise 1 (0.5 pts)

For the following values of A and B, how many clock cycles are needed to execute your first program from Lab 7 on your baseline MIPS processor, before adding optimizations of Lab 9? Assuming that we run the MIPS processor at 20 MHz, how much time (in seconds) would that take? (You can assume that the loading of the numbers requires only one instruction)

Value of A	Value of B	Number of cycles	Time in seconds
0	8		
6	8		
0	90’000		
89’996	90’002		

Exercise 2 (1.5 pts)

Fill in the new values for the Table in Exercise 1 when using the modified MIPS architecture running the optimized code, as discussed in the manual for Lab 9. (You can assume that the loading of the numbers requires only one instruction)

Value of A	Value of B	Number of cycles	Time in seconds
0	8		
6	8		
0	90’000		
89’996	90’002		

Exercise 3 (1 pts)

Compare the size/device utilization of the two implementations (before and after the modifications in Lab manual 9). What differences do you see? Briefly comment on them. *Hint: Look into the synthesis report.*