Modified CSA-CIA for Reducing Propagation Delay

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Abstract—**An adder is a fundamental component of various Very Large-Scale Integration (VLSI) circuits like Central Processing Unit (CPU), Arithmetic Logic Unit (ALU), Memory Access Unit (MAU) etc. A various number of operations can be achieved by adders such as addition, subtraction, multiplication, division, exponentiation etc. The basic circuit of the adder is designed using logic gates. The demand for high-performance VLSI systems are increasing rapidly for use in small and portable devices. The speed related to operation depends upon the delay of the adder as it happens to be one of the most fundamental components of all the computing units and it is a very important parameter for high performance. There have been so many research works on reducing the delay associated with the adder. In this paper, we have done a comparative study of Carry Save Adder (CSA) and Carry Increment Adder (CIA) and proposed a hybrid adder circuit to decrease the delay associated with the adder to an optimum level. As CIA has favorable performance regarding propagation delay and CSA also happens to have good performance in higher bit operations. A simulation study has been carried out for comparative study, the coding has been done using Verilog hardware description language (HDL) and the simulation has been realized with the help of Xilinx ISE 14.7 environment. The result shows the effectiveness of the hybrid circuit proposed for propagation delay improvement.**

Keywords-Carry Save Adder (CSA); Carry Increment Adder (CIA); Hybrid Adder; Propagation Delay; Verilog

I. INTRODUCTION

Adders are the main components in digital designs, not only in performing additions but also in filter designing, multiplexing, and computing division. The circuit performance depends on the design of the base adder. In mobile communication, the demand for low power VLSI [2] system has also increased considerably. As the power available for the device is limited and for the reasons of portability the designers have to make a device which consumes less power, utilizes smaller silicon area and maintain high speed of operation. In computation, Arithmetic Logic Unit (ALU) [3] and Floating-Point Unit (FPU) play the key role. ALU accomplishes the logical computations such as addition, subtraction, multiplication, division and logical operations such as OR, AND, INV and comparison commands, in achieving all these the basic component of an ALU happens to be the adder. So, improving the adder, with respect to computational speed, silicon area or power consumption will result in an improved and more reliable computational unit and will lead to a better circuit performance.

Full Adders operate on two inputs (A, B) and a carry in (Cin) and produces a Sum (S) and Carry-out (Cout). But it operates only on single bit operands. We need a circuit to operate on the multi-bit operands. Simply we can cascade the full adder to achieve that, there are many parallel adders that have been introduced for achieving n-bit addition operation. Some of them are Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Increment Adder (CIA), Carry Skip Adder (CSKA), Carry Save Adder (CSA), Carry Select Adder (CSLA) etc.

Amid the above-mentioned adders, RCA is the simplest adder with respect to circuit complexity and consumes the least area on a chip. Carry Look Ahead (CLA) adder calculates one or more carry bits before the sum, hence reduces the wait time in case of large value bits. The area consumed and the propagation delay associated with the design of CLA is less than that of RCA, because it has less number of gates. Against all the advantages it suffers because of an irregular layout. In Carry Save Adder three bit is added in parallel and carry is propagated through the stages. In Carry Select Adder it does the pre-computation of all the possible carry, so the delay is less. But among all the adders CIA is best regarding the delay and power dissipation. Carry Increment Adder is set of two RAC blocks of 4 bits. It has an Increment block with Half Adder (HA).

The subsequent sections of the paper have been organized as follows: Section II provides a comprehensive review of the work related to binary adders. Section III describes and illustrates the basic concept of CSA and CIA adder. While the section IV details the operation of the proposed hybrid adder Section V showcases and discusses the effectiveness of the proposed adder with experimental results. The conclusion has been presented in section VI.

II. LITERATURE REVIEW

Various types of adders have been invented so far [7] [9] [10], in order to speed up the operation. Comparison with respect to area, delay, power consumption is described in [8] [13] [10]. The basic and simplest adder is Ripple Carry Adder (RCA) [12] [7]. It has lowest circuit complexity with O(n) delay and O(n) area. Carry Look Ahead Adder [4] is designed after looking the lower bits and added if higher orders carry generated. The area and the delay are less because it has less number of gates than that of RCA. But it suffers from an irregular layout. The propagation delay is O (log n) and area O(n log n) for CLA [4].

There are some other kinds of adders that are efficient in higher bit operations. Carry Skip Adder (CSkA), Carry Increment Adder (CIA), Carry Select Adder (CSLA) [5], Carry Save Adder (CSA) have better performance regarding the area and delay and also has a regular layout. Carry Skip Adder is designed with simple RCA block with the addition of Skip Block

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[11]. This skip logic passes or skips the carry if needed, so the total propagation delay becomes lesser. Carry Save Adder has O(n) area and O(log n) delay. It can operate on three operands at a same time. If we need to operate on multi operands then we have to use tree structure which is also very effective for delay calculation.

It is proved that CIA [1] has the best performance regarding area and delay as it uses increment adder for carry propagation.

III. BASICS OF CSA AND CIA

A. *Carry Save Adder (CSA)*

Carry Save Adder works on the principle of delaying carry resolution until the end in other words, saving carries. When calculating the sum of three numbers - A, B, C, for example. Carry Save Adder splits it into two parts: A+B+C = S+C. CSA has 'n' number of full adders which perform the single summation and generates the carry individually. It does its first operation of summation in the first stage - simultaneously. As it saves the carry and propagates to the next stage that's why it is called Carry Save Adder. To add three number, each of n-bit operand we need 2nT delay in RCA. As delay in each full adder is 'T'. The same operation in CSA will take (n+1)T because the first stage of Full Adder will operate at same time and save the carry to the next level. So only one full adder from the first stage and the total full adders in the second stage is responsible for total delay. Entire sum can be calculated after we shift the carry sequence by one place to the left side. The main application of carry save algorithm is, well known for computer microarchitecture. The diagram of 4-Bit Carry Save Adder is shown in Figure 1.

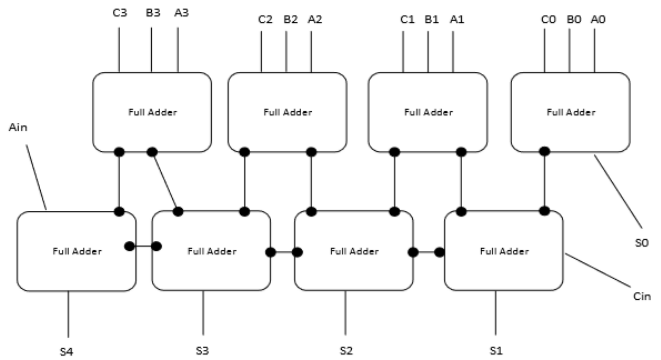

Figure 1 – 4 Bit Carry Save Adder

Advantages of CSA:

- The carry is not propagated through the stages. Instead, carry is stored in present stage, and updated as an addend value in the next stage.
- In the second stage, where the final operation is done by a simple n-bit RCA – which makes the circuit less complex.
- The delay is O (log N) for the tree CSA.

Disadvantages of CSA:

- It is only efficient for multibit operations, for less number of bits the operation causes high propagation delay with respect to RCA, less power consumption and as the number of transistors used are more it takes up higher chip area.
- At each stage of the CSA, we cannot comment on whether the result is produced to be greater or lesser than the input numbers.

B. *Carry Increment Adder (CIA)*

Carry Increment Adder is combination of two RCA circuit along with a carry increment circuit. For 8-bit CIA two number of - 4-bit RCA circuit is required. There is an increment block in CIA circuit. 4 bits RCA circuit processes the sum and generates carry partially and the carry outs from each block are propagated to the incremental circuit. First 4 sum from the RCA is directly taken from the block, but rest is calculated from the carry-out of the first block and rest input through conditional incremental circuit. Second block will continue the operation by summing and creating carry-out. Incremental circuit contains Half Adders (HA). The increment operation will take place based on the carry-out of the 1st block. As the incremental circuit contains Half Adder so it takes less time than simple RCA, to generate the carry, hence the delay is less than RCA circuit. The diagram is shown in Figure 2

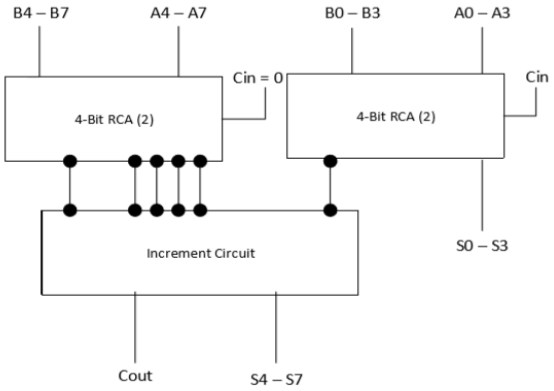

Figure 2 – Carry Save Adder

An increment circuit is combination of some half adders. As carry propagation delay is less in half adder than in full adder so, the total propagation delay through the increment adder is less. 2 blocks of 4-bit RCA does the operation in parallel and the carry out of the first block gets transferred to the increment circuit. Increment adder is shown in Figure 3.

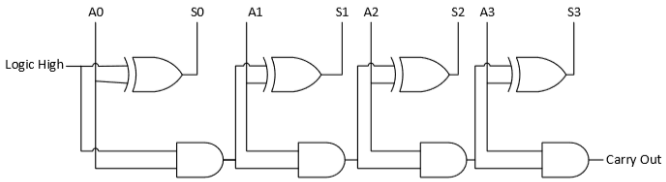

Figure 3 – 4 Bit Increment Adder

Advantages of CIA:

- It uses HA blocks for carry propagation. As we know that carry propagation in HA is much faster than that of FA. That's why the total propagation delay in CLA is much less that other adder circuits.
- Circuit complexity is less.
- It has a simple and regular layout in comparison with Carry Look Ahead Adder.
- Effective in higher (more numbers of) bit operation.

Disadvantages of CIA:

- It needs additional carry increment circuit and it also leads to higher power consumption than RCA.
- Chip area is high than that of a similar n-bit RCA circuit.
- Not much competent with respect to other adder circuits such as RCA for lower bit operation.

IV. PROPOSED CSA-CIA HYBRID ADDER

An 8-bit proposed hybrid adder is shown in Figure 4. The idea has been proposed to utilize the advantages of both the adders discussed in this paper, namely – Carry Save Adder and Carry Increment Adder.

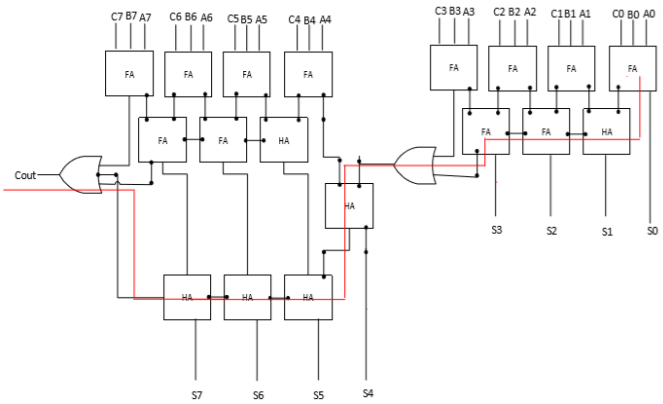

Figure 4 – 8 Bit Proposed Hybrid Adder

A. Working Principle of the Hybrid Adder

The main advantage of CSA is that it can operate on three inputs at the same time. Carry Increment Adder has the best performance on propagation delay as it has increment block.

So, in proposed adder we have three inputs with an increment adder circuit. In the first stage (where the adders take inputs), all the full adders operate in parallel and produce sum and carry which then gets passed to the next stage (the layer of HA and FA – middle block of Figure. 4) with left shifting. The proposed adder split the operands in 4-bit block. So, every 4-bit block produces the sum and carry at the same time but when we get the carry out from the first stage it gets transferred to the increment circuit. In Fig.4 the red line demonstrates the path of carry propagation.

In a simple carry save adder the carry is propagated through the second stage between FA block and need more time causing more propagation delay whereas in proposed adder circuit the carry is transferred through the HA blocks (Increment Circuit) which causes much lesser propagation delay.

B. Advantages of Proposed Hybrid Adder

- It operates on three operands just like a simple CSA.
- Carry propagates through the increment circuit like a simple CIA that's why the propagation delay is less than CSA.
- The circuit complexity is less.
- The design needs less number of FA blocks with respect to the CSA circuit.

C. Delay and Gate Calculation

Assuming the following,

- A XOR gate comprises of 2-unit of date delays.
- AND, OR considered to comprise of 1-unit gate delay each.

For Full Adder Operands A, B to Sum – needed gates and accordingly the calculated delay:

- Two number of XOR gates ≡ 4 Gate delays.

From Cin to Sum it would need:

- 1 XOR gate ≡ 2 gate delays.

From A, B to carry out it would need:

- 1 XOR, 1 AND, 1 OR gates ≡ 4 gate delays.

From Cin to Carry Out ≡ 2 gate delays.

For a half adder circuit from A, B to Sum we have –

- 1 XOR gate ≡ 2 gate delays.
- From A, B to Carry Out ≡ 1 gate delay.

So, for a simple 8-bit CSA we have 22 gate delays (from simple calculation). But in the proposed hybrid adder presented in the Figure 4 we get the total gate delay to be '13'

We can make a full adder circuit by using 9 NAND gates and a half adder by 5 NAND gates. So, for a simple 8-bit CSA we need 16 number of full adders. So total number of required gates is 144. On the other hand, in the proposed adder we get that it needs only 12 number of full adder and 6 half adders and 2 OR gates. So, the total gates required comes out to be 140.

V. RESULTS AND COMPARISON

Calculations has been carried out for 8-bit to 128-bit adder to get the propagation delay based on the 'gate number' or 'gate count' and the total number of gates required to design the circuit. Comparison between CSA and Hybrid Proposed adder is shown in Table I which presents the circuit complexity on the basis of gate count and the propagation delay on the basis of gate count has been presented in Table II.

TABLE I. CIRCUIT COMPLEXITY ON THE BASIS ON GATE COUNT

Bits	Number of basic gates required for implementation	
	CSA	***Hybrid***
8-Bit	144	140
16-Bit	288	300
32-Bit	576	620
64-Bit	1152	1260
128-Bit	2304	2540

TABLE II. PROPAGATION DELAY ON THE BASIS OF GATE COUNT

Bits	Number of basic gates required for implementation	
	CSA	***Hybrid***
8-Bit	22	15
16-Bit	38	25
32-Bit	70	45
64-Bit	134	85
128-Bit	262	165

The simulation study of the proposed CSA-CIA hybrid circuit is presented in this section. The RTL code is written using Verilog HDL and simulation is carried out using Xilinx ISE 14.7 environment. The comparison is done with CSA and our CSA-CIA hybrid adder. Figure 5. shows the simulation result of a 16-bit normal CSA and Figure 6 presents the addition by using the Hybrid Adder. Here A, B, C are the inputs and 'S' and 'C' are defined as the Sum and Carry out respectively. For a 16-bit operation

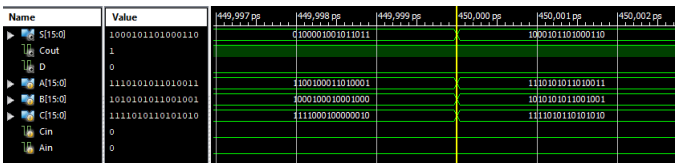

Figure 5 – Simulation result of 16-bit addition using CSA.

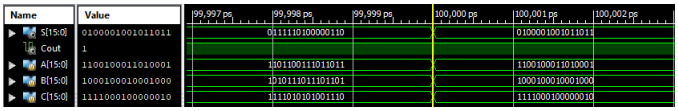

Figure 6 – Simulation result of 16-bit addition using Hybrid Adder.

The RTL Schematic view of the 16-bit Hybrid adder is shown in Figure 7. The schematic is generated after the HDL code is synthesized, and it presents the pre-optimized design in terms of generic symbols that are independent of targeted Xilinx Device. The device under which the schematics HDL is written belongs to the family of – Artix 7 and the device – XC7A100T.

The Device utilization summary of both CSA and Hybrid Adder is presented in Table III.

TABLE III. PROPAGATION DELAY ON THE BASIS OF SIMULATION RESULTS

Bits	Adder	Delay (ns)	Slice LUT (Area)
8 - Bit	CSA	4.799	16
	Hybrid	3.125	17
16- Bit	CSA	8.401	32
	Hybrid	4.743	39

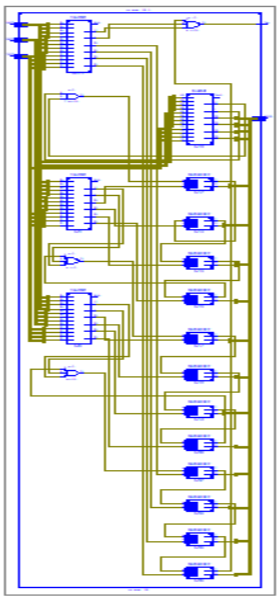

Figure 7 - RTL Schematic view of 16-bit Hybrid adder

The technology schematic view of 16-bit Hybrid Adder is shown in Figure.8. This represents the design in terms of the logic elements such as LUTs, I/O buffers and some alternative technology specific components.

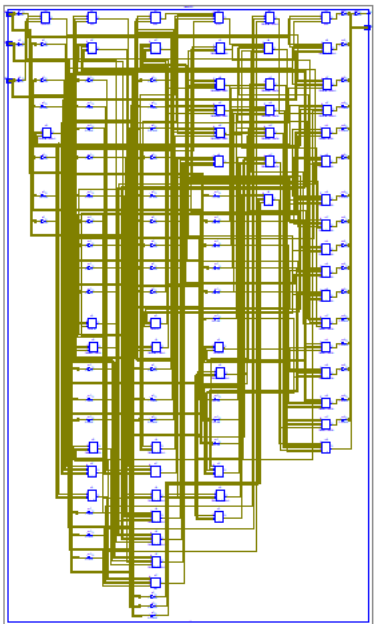

Figure 8 – Technology Schematic view of 16 Bit Hybrid Adder

The ratio of propagation delay between CSA and Hybrid adder by simulation and theoretical findings are approximately the same. The comparison of gate delay is shown in Figure 10.

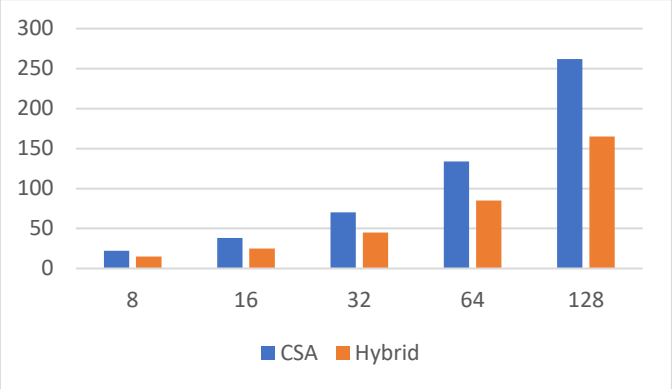

Figure 10 – Gate delay representation of CSA vs Hybrid

VI. CONCLUSION

In this paper we have described the CSA and CIA adder and presented the hybrid adder by merging the advantages of both the adders. We have calculated the gate numbers and gate delays and demonstrated a comparison for the same. The design has been tested and verified using Verilog HDL and the simulation is carried out in Xilinx ISE 14.7 environment. As the theoretical and experimentally verified values of the ratio comes out to be - approximately same. Therefore, we conclude that the hybrid adder is better in terms of propagation delay than CSA. The work has been carried out for 8-bit and 16- bit operation. Although the choice of adder is completely dependent on intended use of application. The experimentation could be achieved for higher bits using similar logic.

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