

1. Description

1.1. Project

Project Name	MI_Project_F407
Board Name	custom
Generated with:	STM32CubeMX 6.8.1
Date	05/30/2023

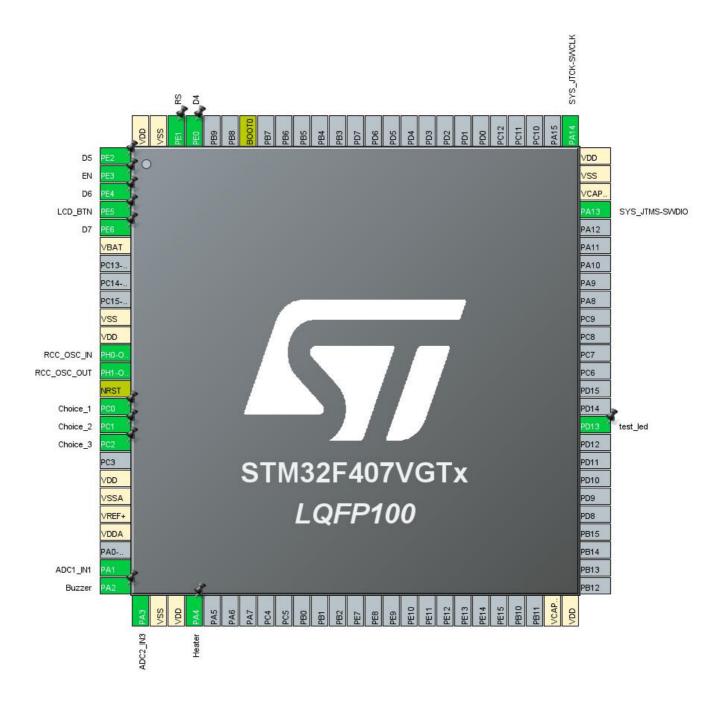
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



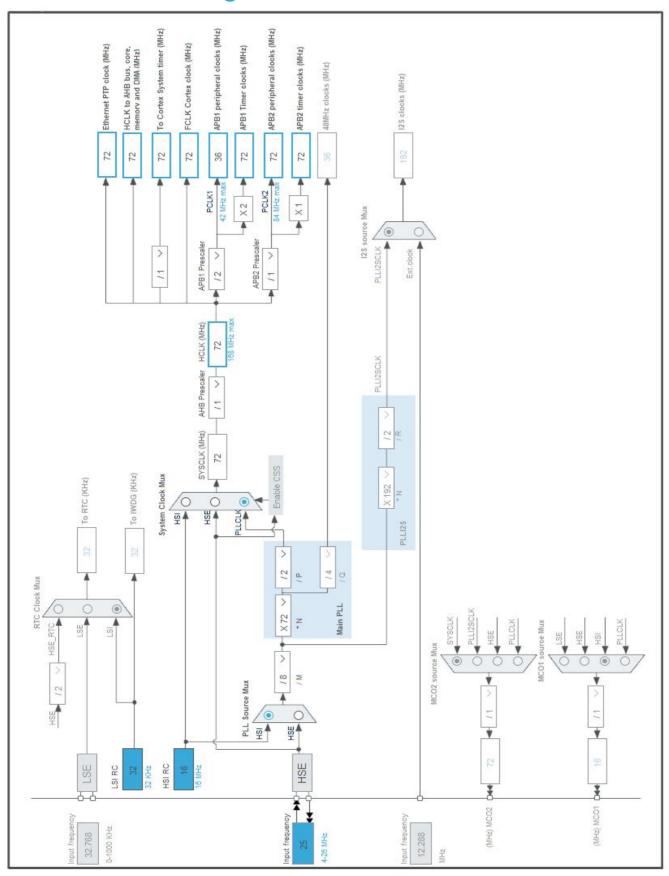
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP100	(function after		Function(s)	
LQ11 100			r driotion(o)	
,	reset)	1/0	ODIO Outroit	DE
1	PE2 *	1/0	GPIO_Output	D5
2	PE3 *	1/0	GPIO_Output	EN
3	PE4 *	1/0	GPIO_Output	D6
4	PE5	I/O	GPIO_EXTI5	LCD_BTN
5	PE6 *	I/O	GPIO_Output	D7
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	GPIO_EXTI0	Choice_1
16	PC1	I/O	GPIO_EXTI1	Choice_2
17	PC2	I/O	GPIO_EXTI2	Choice_3
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
24	PA1	I/O	ADC1_IN1	
25	PA2 *	I/O	GPIO_Output	Buzzer
26	PA3	I/O	ADC2_IN3	
27	VSS	Power		
28	VDD	Power		
29	PA4 *	I/O	GPIO_Output	Heater
49	VCAP_1	Power		
50	VDD	Power		
60	PD13 *	I/O	GPIO_Output	test_led
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
94	воото	Boot		
97	PE0 *	I/O	GPIO_Output	D4
98	PE1 *	1/0	GPIO_Output	RS
99	VSS	Power	00_0uiput	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
100	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MI_Project_F407
Project Folder	C:\Users\Dell\STM32CubeIDE\workspace_1.12.1\MI_Project_F407
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.27.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM1_Init	TIM1
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
мси	STM32F407VGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

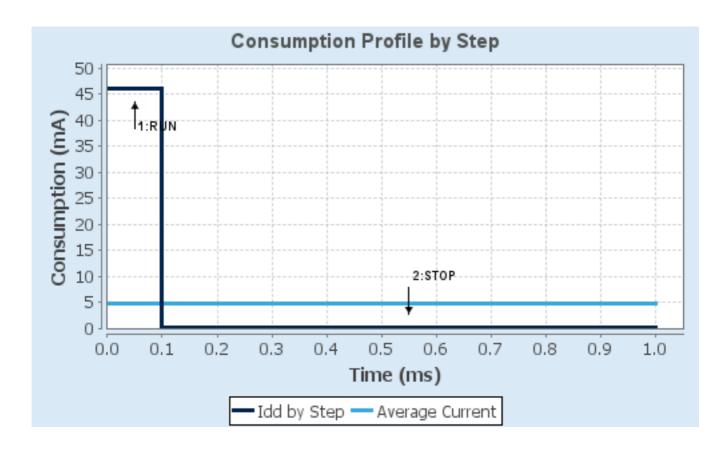
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN1

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel 1
Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. ADC2

mode: IN3

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel Channel 3
Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 72-1 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 0xffff-1 *
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA3	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D5
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D6
	PE5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	Pull-down *	n/a	LCD_BTN
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D7
	PC0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	Choice_1
	PC1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	Choice_2
	PC2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	Choice_3
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Buzzer
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Heater
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	test_led
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D4
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RS

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI line0 interrupt	true	0	0
EXTI line1 interrupt	true	0	0
EXTI line2 interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

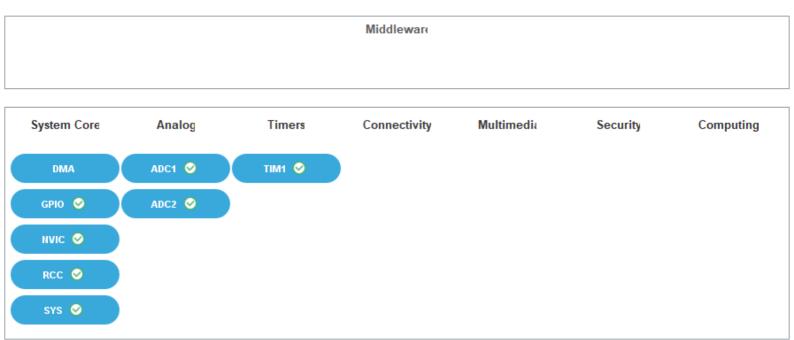
Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
<u> </u>	false	true	true

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
EXTI line0 interrupt	false	true	true
EXTI line1 interrupt	false	true	true
EXTI line2 interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true

^{*} User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-

417 bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f405-415_407-

417_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4_svd.zip

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