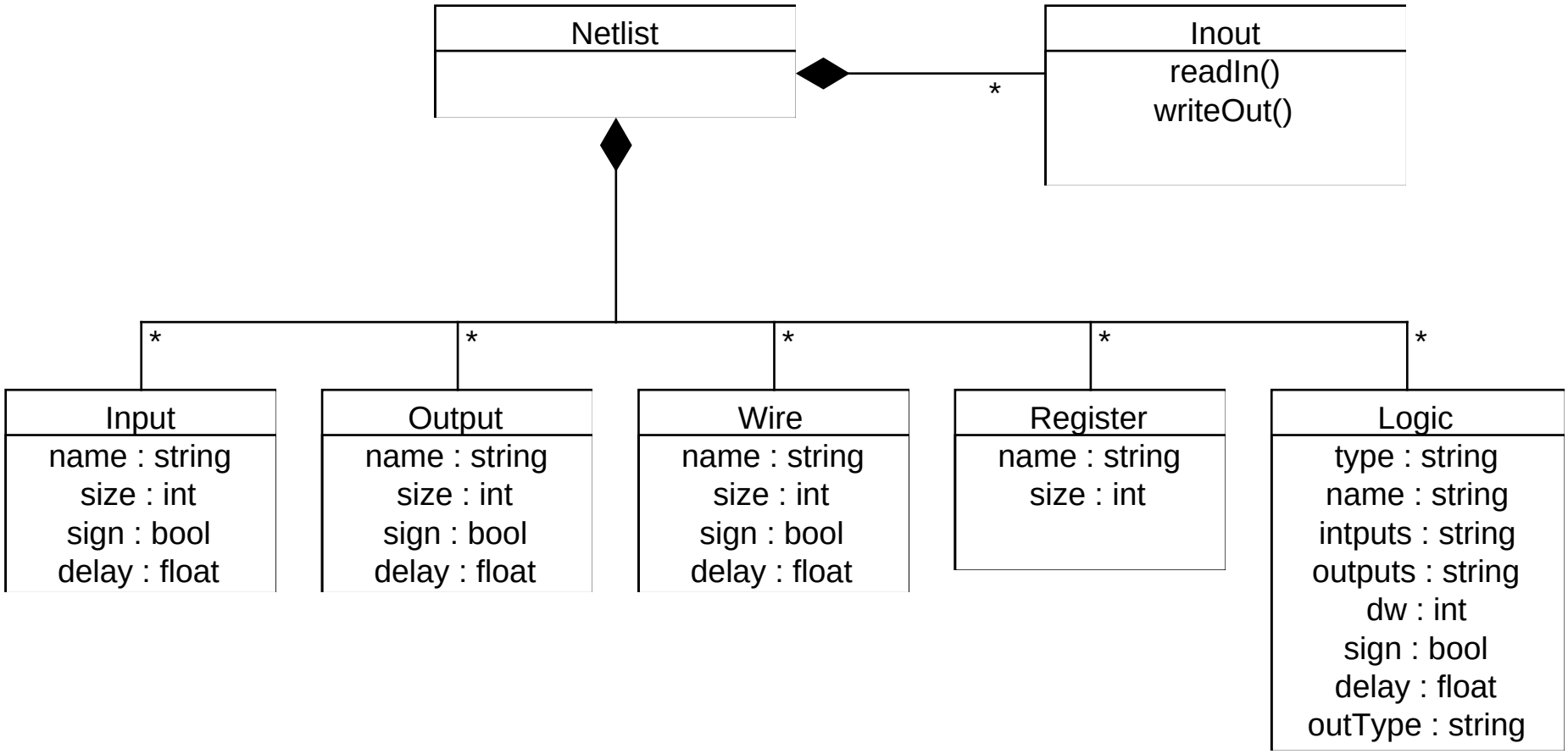

Do these have a sign component?
REG
MUX2x1
SHR
SHL

Do we throw an error if in/out/wire/reg declared somewhere in the middle of the file?

For critical path, do you want the longest path of the whole circuit or the longest input-to-reg / reg-to-reg path?

Parse flow:
1. create inputs, outputs, wires, and regsisters
2. create logic list
- check validity
- for registers, check output signals
- for internal registers, add wire
- calculate delays