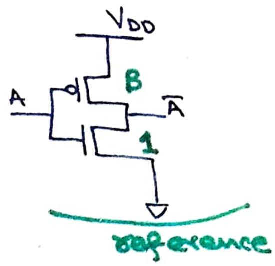
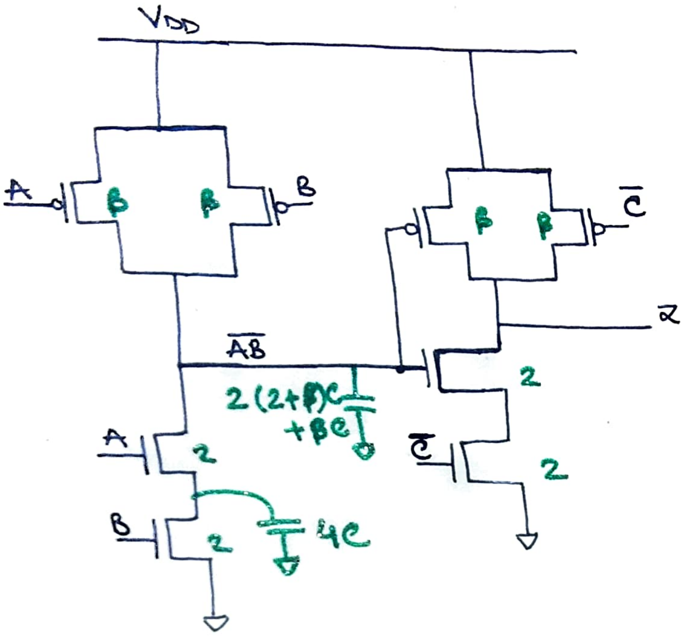
OR

(a), (b), (c)





* worst $t_{pLH} = 0.69 \left\{ \frac{R}{\beta} \times [2(2+\beta)C + \beta C] \right\} \rightarrow A=1, B=0$ or $A=0, B=1$

* worst $t_{pHL} = 0.69 \left\{ \frac{R}{2} \times 4C + R \times [[2(2+\beta)C] + \beta C] \right\} \rightarrow A=1, B=1$

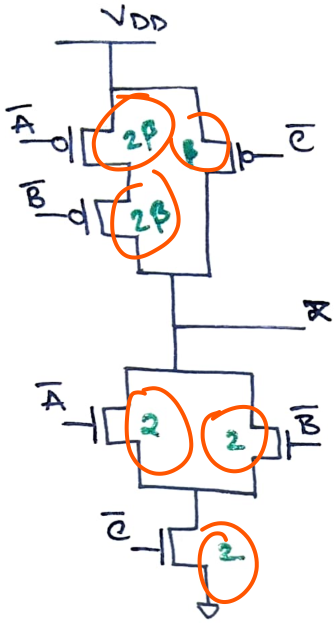
* $t_p = \max \{ t_{pLH}, t_{pHL} \}$

or

* $t_p = \left\{ \frac{t_{pLH} + t_{pHL}}{2} \right\}$

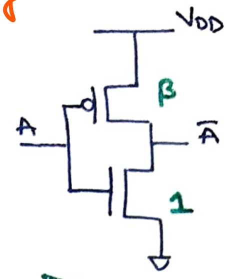
Q6.

(a),(b)



$Z = \overline{(\bar{A}+\bar{B})\cdot\bar{C}} = \underline{\underline{AB+C}}$

give marks even if they directly took β = 2.



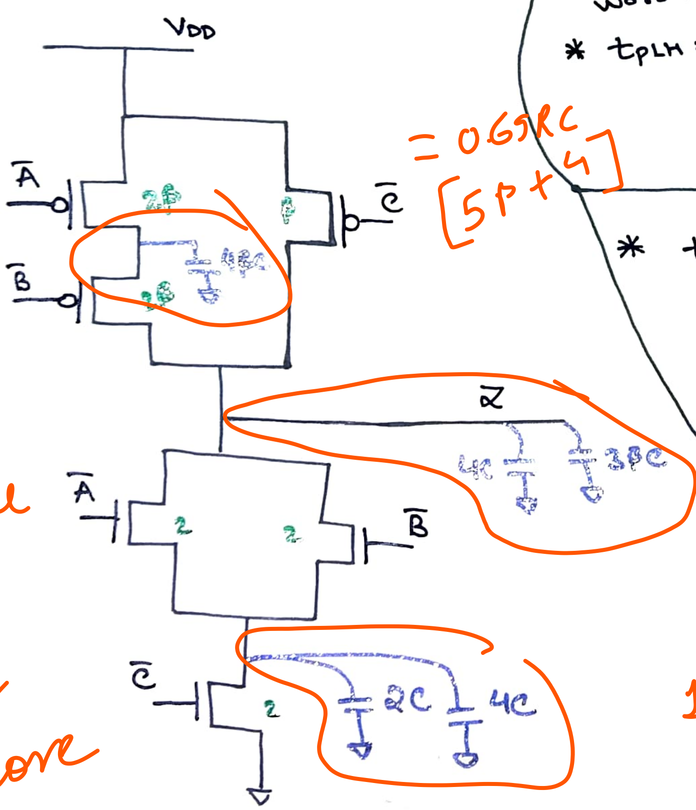
reference

PDN size – 1 mark

PUN size – 1 mark

implementation : 4 marks. if proceeds along correct direction, give appropriate marks

(c)



worst case {A=1, B=1}

$* \; t_{pLH} = 0.69\left[\frac{R}{2\beta}\times 4\beta C + \frac{R}{\beta}\times(4+3\beta)C\right]$

$\cancel{= 0.69\left[2 + \frac{4+3\beta}{\beta}\right]RC}$

$= 0.65RC\,[5\beta+4]$

$* \; t_{pHL} = 0.69\left[\frac{R}{2}\times 6C + R\times(4+3\beta)C\right]$

$= 0.69\,[3+4+3\beta]\,RC$

$= 0.69\,[7+3\beta]\,RC$

worst case ⇒ {A=0 & C=0} or {B=0 & C=0}

1 mark for correct value of cap.

1 mark for using el more delay.

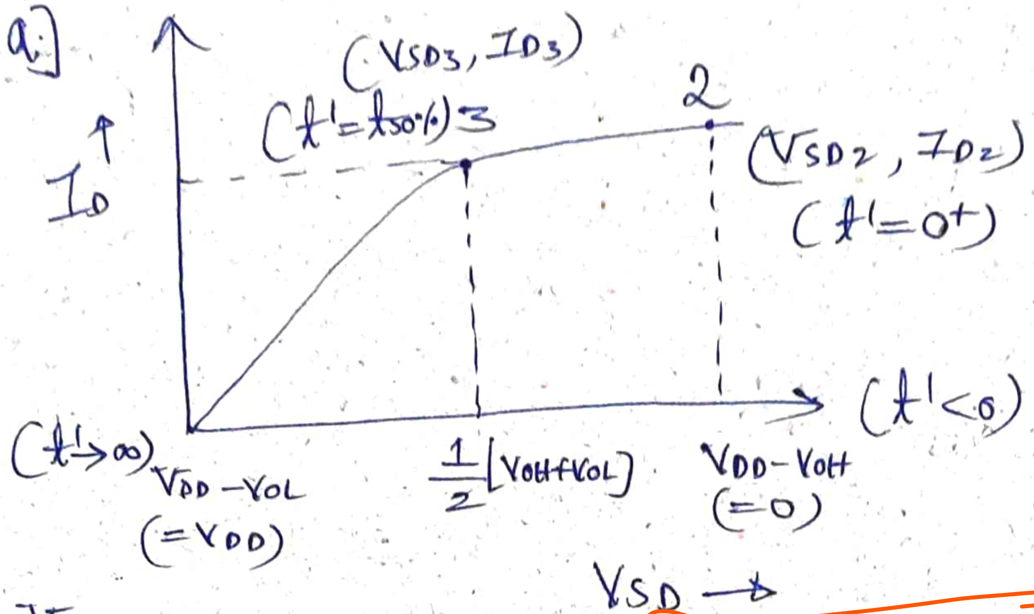
1 mark for final answer.

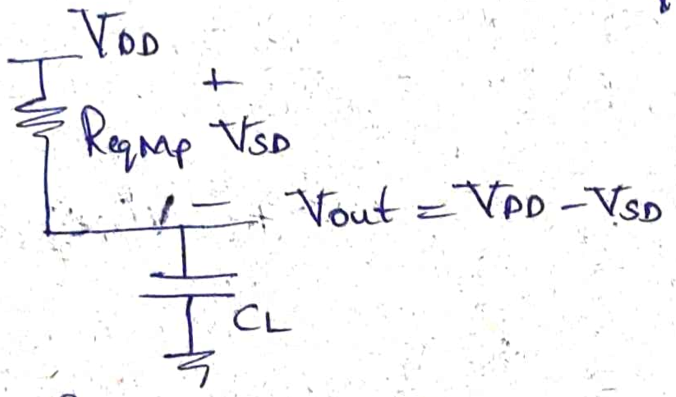
$\Rightarrow t_p = \max\{t_{pLH}, t_{pHL}\}$ → worst one

or

$\Rightarrow t_p = \left\{\frac{t_{pLH}+t_{pHL}}{2}\right\}$

Q.7] a.]





* Minimum sized inverter $\Rightarrow$ $\boxed{W_P = 2W_n}$

$\Rightarrow$ At $t = 0^+$, $R_{eqMp}(0^+) = \dfrac{V_{SD2}}{I_{D2}}$

1/2

* $V_o \simeq 0V$ [just after $t = 0$] and PMOS is in saturation [$\because V_{SD} > V_{SG} - |V_{tp}| \Rightarrow V_D < V_G + |V_{tp}|$
$\Rightarrow \sim 0 < 0 + 0.4$, Hence Prooved]

$$V_{SD2} = V_{DD} - 0 = 1.8V$$

$$I_{SD2} = \frac{K_p'}{2} \times 2 \times \left[V_{SG} - |V_{tp}|^2\right]\left[1 + \lambda V_{SD}\right]$$

$[\because \frac{2W}{L}]$

$$= \frac{150 \times 10^{-6}}{\cancel{2}} \times \cancel{2}\left[1.8 - 0 - 0.4\right]^2\left[1 + (0.01 \times 1.8)\right]$$

$$= 0.299 \text{ mA}$$

$$\Rightarrow R_{eqMp}(0^+) = \frac{1.8}{0.299 \times 10^{-3}} = 6.02\text{k}\Omega$$

1/2

$\Rightarrow$ $t = 50\%$, $R_{eqMP}(t_{50\%}) = V_{SD3}/I_{D3}$ and

MP is in linear region. 1/2

$$V_{SD3} = \frac{1}{2}[V_{OH} + V_{OL}] = \frac{1}{2}[1.8] = 0.9V$$

$$I_{D3} = K_p' \cdot \frac{W}{L} \cdot \left[(V_{SG} - |V_{tp}|) V_{SD} - \frac{V_{SD}^2}{2} \right] \times \{1 + \lambda V_{SD}\}$$

$$= 150 \times 10^{-6} \times 2 \times \left[(1.8 - 0 - 0.4) 0.9 - \frac{0.9^2}{2} \right] \times \{1 + (0.01 \times 0.9)\}$$

$$= 258.8085 \, \mu A$$ 1/2

$$\therefore R_{eq}[t_{50\%}] = \frac{0.9 \times 10^3}{258.8085} k\Omega = 3.477 k\Omega$$

$\Rightarrow$ Total $R_{eq MP} = \frac{1}{2}[6.02k + 3.477k]$

$$= 4.7485 k\Omega$$ 1/2

$\Rightarrow$ $t_{PLH} = 0.69 \, C_L \, R_{eq MP}$ 1/2

$$= 0.69 \times 100 \times 10^{-15} \times 4.7485 \times 10^3$$

$$= 0.69 \times 4.7485 \times 10^{-10}$$

$$= 3.276465 \times 10^{-10} \text{ seconds}$$

b] I_{scmax} occurs when $\boxed{V_{in} = V_m}$ 1

$\rightarrow$ $V_m = \frac{V_{DD}}{2} = \frac{1.8\,V}{2} = 0.9\,V$ $\frac{1}{2}$

both the MOSFETs are in saturation region.

$\rightarrow$ $I_{Dnsat} = \frac{K_n}{2}\left[V_{GS} - V_{tn}\right]^2 \times \left[1 + \lambda V_{DS}\right]$

$= \frac{300 \times 10^{-6}}{2}\left[0.9 - 0.4\right]^2 \times \left[1 + 0.01 \times 0.9\right]$

$= 0.037\ mA$ $\frac{1}{2}$

$\therefore I_{scmax} = 0.037\ mA$

b] [OR] We get $(I_{sc})_{max}$ when both the Txs are in saturation.

$\boxed{I_{DSn} = -I_{DSP}}$ | $V_{in} = V_m$ → 1

You can also go with $I_{DSn} = I_{SPP}$

$$I_{DSn} = \frac{1}{2} K_n' \frac{W_n}{L} [V_m - V_{tn}]^2$$
$$I_{DSP} = \frac{1}{2} K_p' \frac{W_P}{L} [V_m - V_{DD} - V_{TP}]^2$$
→ 2

from 1 and 2, → -ve number

$$\Rightarrow V_m - V_{tn} = \pm x [V_m - V_{DD} - V_{tp}]$$

-ve is correct for $(V_m - V_{tn})$ to be +ve

$$\Rightarrow V_m (1+x) = V_{Tn} + x [V_{DD} + V_{tp}]$$

$$\therefore V_m = \frac{V_{tn} + x[V_{DD} + V_{tP}]}{1+x}$$

$\boxed{\therefore x = \sqrt{\frac{+K_p' W_P}{K_n' W_n}}}$

$$V_m = \frac{0.4 + 1[1.8 - 0.4]}{1 + (1)}$$

$V_M = \cancel{0.814}$ 0.9 V ~~$(I_{sc})_{max} = 0.028mA$~~

$$\therefore (I_{sc})_{max} = 0.037 \text{ mA}$$

c) We get steep slope for a V_{in} range of "V_{tn}" to "$V_{DD} - |V_{tp}|$".

1/2

⇒ At V_{tn} : NMOS in Sat and PMOS in Linear.

∀ NMOS

$V_{DS} > V_{GS} - V_{tn}$

$\therefore \boxed{V_o > 0V} \rightarrow (1)$

∀ PMOS

$V_{SD} < V_{SG} - |V_{tp}|$

$V_D > V_G + |V_{tp}|$

$V_o > 0.4 + 0.4$

$\therefore \boxed{V_o > 0.8V} \rightarrow (2)$

⇒ At $V_{DD} - |V_{tp}|$: NMOS in Linear and PMOS in Saturation.

∀ NMOS

$V_o < 1.8 - 0.4 - 0.4$

$(\because V_{DS} < V_{GS} - V_{tn})$

$\therefore \boxed{V_o < 1V} \rightarrow (3)$

∀ PMOS

$V_{SD} > V_{SG} - |V_{tp}|$

$V_D < V_G + |V_{tp}|$

$V_o < V_{DD} - |V_{tp}| + |V_{tp}|$

$\therefore \boxed{V_o < 1.8V} \rightarrow (4)$

Hence, from (1), (2), (3) and (4) we get output range as

$$\boxed{0.8V < V_o < 1V}$$

1/2

Midsem Q8

23 September 2022 02:50 PM

$$(\mu_p)_{SiGe} = 2.4(\mu_p)_{Si}$$
$$= 2.4\left(\frac{\mu_n}{2}\right)_{Si}$$
$$= 1.2\, \mu_{n\,Si}$$

1/2

$\Rightarrow$ to have a symmetric CMOS inverter

$$\left(\frac{W}{L}\right)_n = 1.2\left(\frac{W}{L}\right)_p$$

1/2

one approach would be to choose

- $L_n = L_p = L_{min}$
- $W_p = W_{min} = L_{min}$
- $W_n = 1.2\, W_{min} = 1.2\, L_{min}$

1

$\Rightarrow$ area under gate of PMOS $= W_p \times L_p = L_{min}^2$

area under gate of NMOS $= W_n \times L_n = 1.2\, L_{min}^2$

$\Rightarrow$ total area under gates for 1 MOSFET $= 2.2\, L_{min}^2$

———— 100 ———— $= 220\, L_{min}^2$ — ①

- chip area available for making gates

$$= 90\% \times 5\, mm^2$$
$$= 4.5\, mm^2 \quad \text{— ②}$$

equating ① and ②,

$$220\, L_{min}^2 = 4.5\, mm^2$$
$$\Rightarrow L_{min} = \sqrt{\frac{4.5}{220}}\, mm$$
$$= 143\, \mu m$$

1

$= 143\ \text{Nm}$

$\Rightarrow$ Sizing :

PMOS	NMOS
L = 143 Nm	L = 143 Nm
W = 143 Nm	W = 143 X 1.2 = 171.6 Nm

1

1