

Name:

Roll No.:

**Department of Electrical Engineering**  
**Indian Institute of Technology Kanpur**

**EE370A**

**End-semester Examination**

**16/11/2022**

**Total Marks: 60**

**Time: 3 hours**

**Instructions**

- Read the questions carefully.
- Answer the questions to the point.
- The question paper carries 60 marks which will be rescaled to 35 marks for final grading.

1) Realize a **3-input XOR gate** using two stages of:

- (a) Static CMOS gates. *S* (2 marks)
- (b) Pass transistor logic. *C* (3 marks)

[Assume that both inputs and their complementary forms are readily available]

- (c) Find the (W/L) ratios of the n-MOSFETs and p-MOSFETs for the different circuits designed in parts (a) and (b). *C* (3 marks)

(d) Compare circuits designed in (a) and (b) in terms of:

- (i) Number of transistors and their respective areas. *C* (2 marks)
- (ii) Propagation delays. Use Elmore's method to estimate the delay. Assume that a minimum sized MOSFET offers an equivalent resistance  $R$  and a capacitance  $C$ . *S* (6 marks)
- (iii) Static power dissipation. *C* (2 marks)
- (iv) Dynamic power dissipation of the first stage. *S* (4 marks)

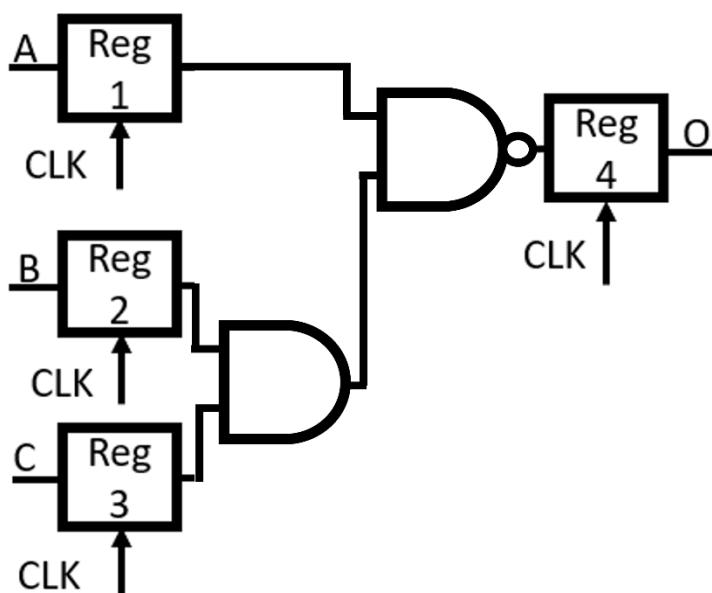
(e) Also, find the delay for the circuit designed in (a) using Logical Effort method. *S* (4 marks)

(f) Compare the total delay obtained using Logical Effort method with the Elmore delay method for design (a) and fill in the blanks:

The Elmore delay method .....the delay as compared to Logical Effort method. *S* (2 mark)

YSC 2) Implement the expression  $F = \overline{(A + B)}C$  using **DCVSL** logic. Size the pull-down network. (3 marks)

3)



(a) Realize the combinational logic block of the given circuit with **Static CMOS** logic and size the transistors appropriately. (2 marks)

(b) Determine the maximum and minimum delay in the combinational logic block. (3 marks)

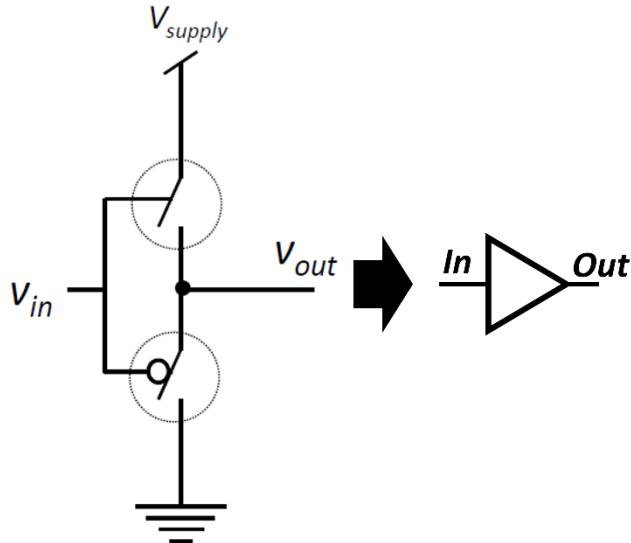
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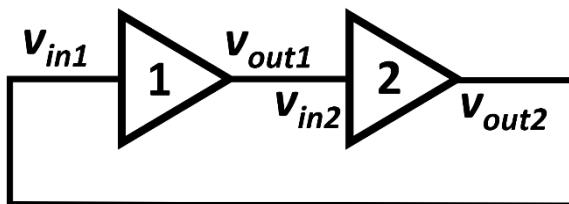
(c) Registers used here are implemented using **C<sup>2</sup>MOS** logic. Find setup time ( $t_{su}$ ), hold time ( $t_h$ ), clock-to-Q delay ( $t_{c-q}$ ), and contamination delay ( $t_{cd}$ ). **(5 marks)**

(d) Determine minimum clock period of this circuit. **(2 marks)**

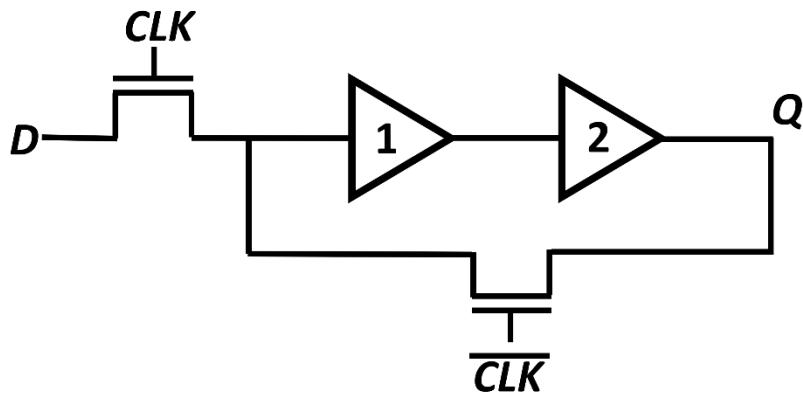
- A 4) (a) Realize the non-inverting buffer using n-MOSFET and p-MOSFET as switches and draw the voltage transfer characteristics (VTC) qualitatively (only the nature). **(3 marks)**



(b) Does the element shown in the circuit below act like a bistable element? If yes, how? If no, why? **(3 marks)**



(c) Does the circuit shown below act like a Latch? If yes, how and what kind of latch? If no, why? **(2 marks)**



- A 5) A circuit consists of three logic blocks with delays of  $5 \pm 1$  ns,  $4 \pm 3$  ns,  $3 \pm 1$  ns, and  $2 \pm 0.5$  ns. Registers available for pipelining have delays ( $t_{su} + t_{c-q}$ ) of  $3 \pm 1$  ns. The circuit is pipelined with registers between each of the logic blocks.

What is the minimum clock period required for operating this pipelined circuit? **(2 marks)**

- VS 6) The number of bits in a typical word for a digital system is 32. The number of pages in a memory of  $2^{24}$  bits (16 Mb) built using the standard square architecture is: ..... **(1 mark)**

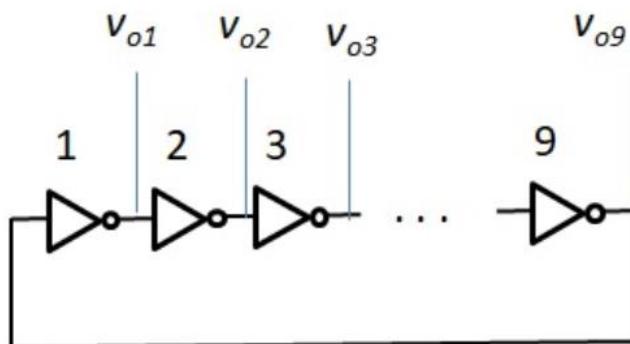
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- YSL 7) For a DRAM technology, the bit line capacitance  $C_{BL}$  is  $10 \text{ pF}$  ( $10^{-11} \text{ F}$ ). The cell capacitance  $C_s$  is  $50 \text{ fF}$  ( $50 \times 10^{-15} \text{ F}$ ). The leakage current of the access transistor is  $0.1 \text{ nA}$  and its threshold voltage is  $0.2 \text{ V}$  while the supply voltage is  $0.7 \text{ V}$ . What should be the refresh rate for this DRAM? **(2 marks)**

- YSL 8) The number of students originally registered for this course is 216. The minimum number of address lines required to uniquely address 216 locations storing the student's marks are ..... **(1 mark)**

- YSL 9) A 9-stage ring oscillator is designed with inverters and the signals are tapped at the output of the third inverter ( $v_{o3}$ ) and the eighth inverter ( $v_{o8}$ ). The phase difference between these two signals is ..... degrees. **(1 mark)**

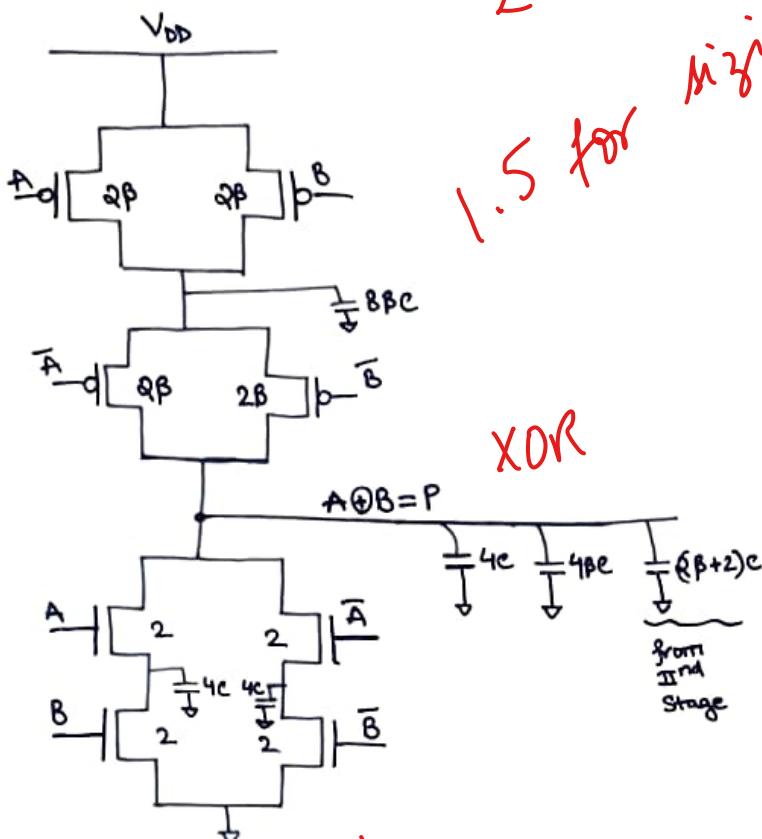


- YSL 10) State true or false: Dynamic circuits typically exhibit a lower area but suffer from low noise margin and charge leakage issue..... **(1 mark)**

- 11) Submitted a handwritten cheat sheet? ..... **(1 mark)**

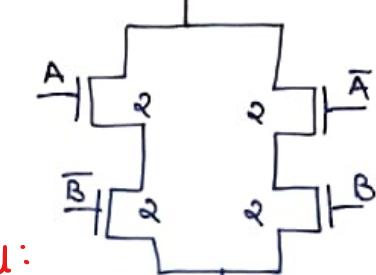
Q1.

(a), (c) Stage I



first stage

XNOR

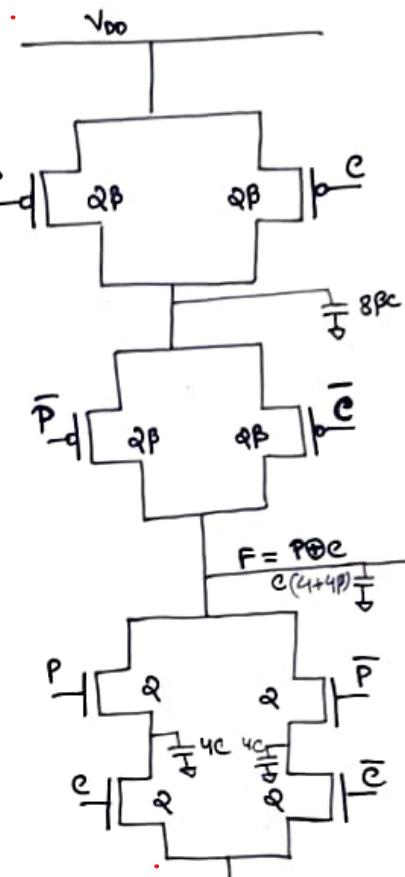


Partial:

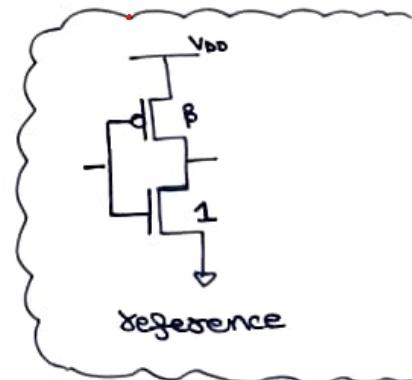
Consider those solutions such as  $XOR \rightarrow \text{inv} \rightarrow XOR$  as well

2 for realizing

Stage II



2nd stage



Consider alternative

solutions such as:

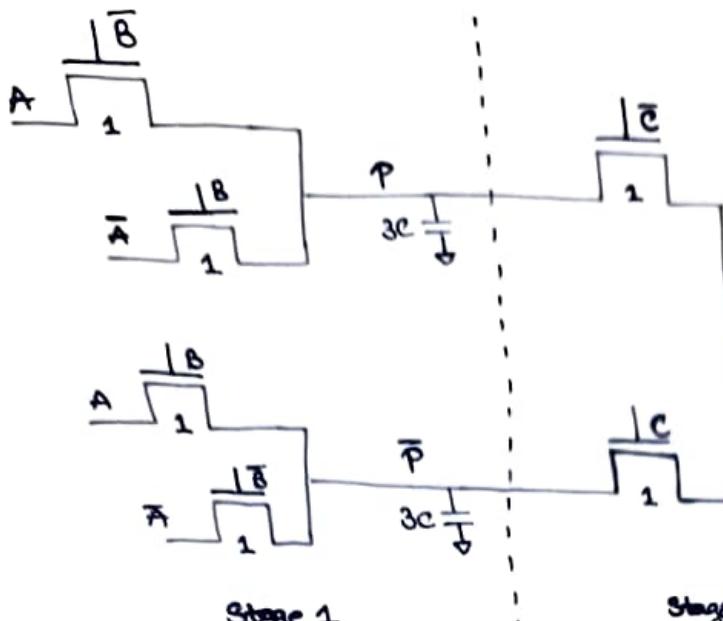
3 input XNOR followed by inverter

where they used 3 stages

(b), (c)

but give them ① for implementation  
& ④ for sizing.

min sized  
All are NMOS



③ for implementation  
④ for sizing

Here also plan consider alternate solutions &  
Partial give ④ to those realizing it in 3 stages  
(d) give ④ if they size correctly

(i) No. of transistors

①  $\rightarrow$  static CMOS  $>$  PTL

$A_{min} \rightarrow$  Area of min sized NMOS  
\* static CMOS  $\rightarrow 24(\beta+1)A_{min}$   
\* PTL  $\rightarrow 6A_{min}$

①

Give marks even if they just write correct inequality sign or if they provide area & no. of transistors

\* Static CMOS

Stage 1 Delay

$$t_{PLH} = \left( \frac{R}{2} \times 8\beta e + R \times [(4+4\beta)e + (2\beta+2)e] \right)^{0.63}$$

①

$$t_{PHL} = \left( \frac{R}{2} \times 4e + R \times [(4+4\beta)e + (2\beta+2)e] \right)^{0.63}$$

$$t_P = (R \times 3e + R \times Qc)^{0.63}$$

$$t_P = (7RC)^{0.63}$$

③

Partial:  
Give ② marks

Stage II Delay

$$t_{PLH} = \left( R \times 8\beta e + R \times [(4+4\beta)e] \right)^{0.63}$$

$$t_{PHL} = \left( \frac{R}{2} \times 4e + R \times [4+4\beta]e \right)^{0.63}$$

Partial:  
if they have identified correct value of capacitances

Overall delay = mark  $(t_{PLH_1} + t_{PHL_2}) + t_{PLH_2}$

Partial:  
here also, give ② if they have identified correct cap value

Static CMOS  $>$  PTL

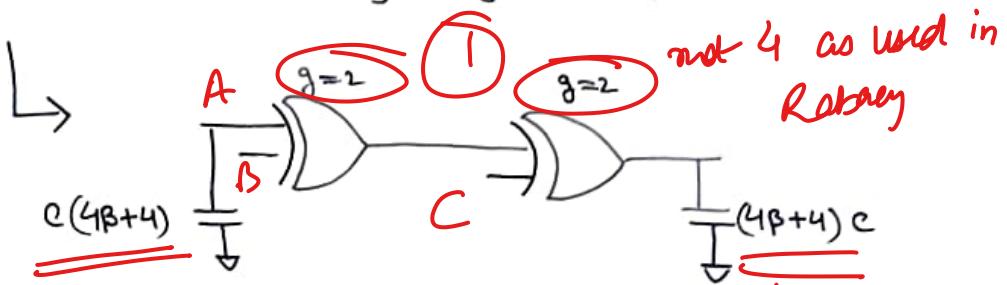
(111) Static Power Dissipation

Less  $I_{DD}$   $\Rightarrow$  Less no. of transistors.

2

Partial: give 1 marks if they only write the answer.

(e) Delay calculation by Logical Effort method



from CMOS

(will change if realized using a different technique)

$$G_i = \prod g_i = 2 \times 2 = 4$$

$$P = 2 + 2 = 4$$

Consider alternative gate-level designs as well like:

$$B = 1$$

$$D = N \frac{t_p}{h} + P = N h t_p$$

$$D = 2 \times (4)^{1/2} + 4$$

$$D = 8(t_p)$$

\* By Elmore delay, as calc. before

$$\therefore \beta \geq 1$$

Delay calc.  $> 8t_p$

depends on design

use logical effort;

if that's correct, give them

2.5 marks

(f) Therefore, Elmore delay overestimates the delay as compared to Logical Effort method.

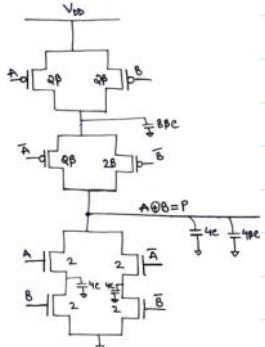
or similar words  $\rightarrow$

give marks even if they write only answer

Q1(d)

16 November 2022 10:51 PM

CMOS



		P = A ⊕ B	Probability
A	B		
0	0	0	$P_{\bar{A}} \times P_{\bar{B}}$
0	1	1	$P_{\bar{A}} \times P_B$
1	0	1	$P_A \times P_{\bar{B}}$
1	1	0	$P_A \times P_B$

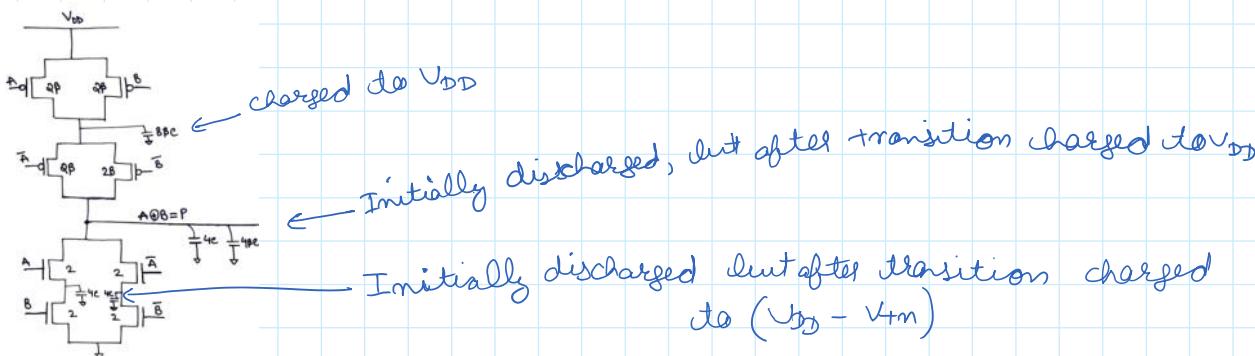
0.5

Conditions for 0 → 1 transitions :

	Probability	Prob. Assuming $P_A = P_B = P_{\bar{A}} = P_{\bar{B}} = 0.5$
1) $A=0, B=0 \rightarrow 1$	$(P_{\bar{A}} P_{\bar{B}})(P_A P_B)$	1/16
2) $A=0 \rightarrow 1, B=0$	$(P_{\bar{A}} P_{\bar{B}})(P_A P_{\bar{B}})$	1/16
3) $A=1, B=1 \rightarrow 0$	$(P_A P_B)(P_A P_{\bar{B}})$	1/16
4) $A=1 \rightarrow 0, B=1$	$(P_A P_B)(P_{\bar{A}} P_B)$	1/16

Case 1 :

when  $A = 0, B = 0 \rightarrow 1$



case 2, 3, 4 can be analysed similarly

$$\Rightarrow P_{dynamic} = f \times \frac{1}{16} \begin{cases} (4C + 4\beta C)V_{DD}^2 + 4C(V_{DD})(V_{DD} - V_{TN}) & // case 1 \\ + (4C + 4\beta C)V_{DD}^2 + 4C(V_{DD})(V_{DD} - V_{TN}) & // case 2 \\ + (8\beta C)V_{DD}^2 + (4C + 4\beta C)V_{DD}^2 + 4C(V_{DD})(V_{DD} - V_{TN}) & // case 3 \\ + (8\beta C)V_{DD}^2 + (4C + 4\beta C)V_{DD}^2 + 4C(V_{DD})(V_{DD} - V_{TN}) & // case 4 \end{cases}$$

1.5

PTL

Case 1

$A=0, B=0 \rightarrow 1$



case 2, 3, 4 can be analysed similarly

$$P_{dynamic} = f \times \frac{1}{16} \times \left[ \begin{array}{ll} 3C \times V_{DD}(V_{DD} - V_{tm}) & // \text{case 1} \\ + 3C \times V_{DD}(V_{DD} - V_{tm}) & // \text{case 2} \\ + 3C \times V_{DD}(V_{DD} - V_{tm}) & // \text{case 3} \\ + 3C \times V_{DD}(V_{DD} - V_{tm}) & // \text{case 4} \end{array} \right]$$

$$= f \left( \frac{1}{4} \right) (3C) V_{DD} (V_{DD} - V_{tm})$$

(1)

Comparing PTL and CMOS XOR gate,

dynamic power is greater for CMOS implementation

(1)

Partial:

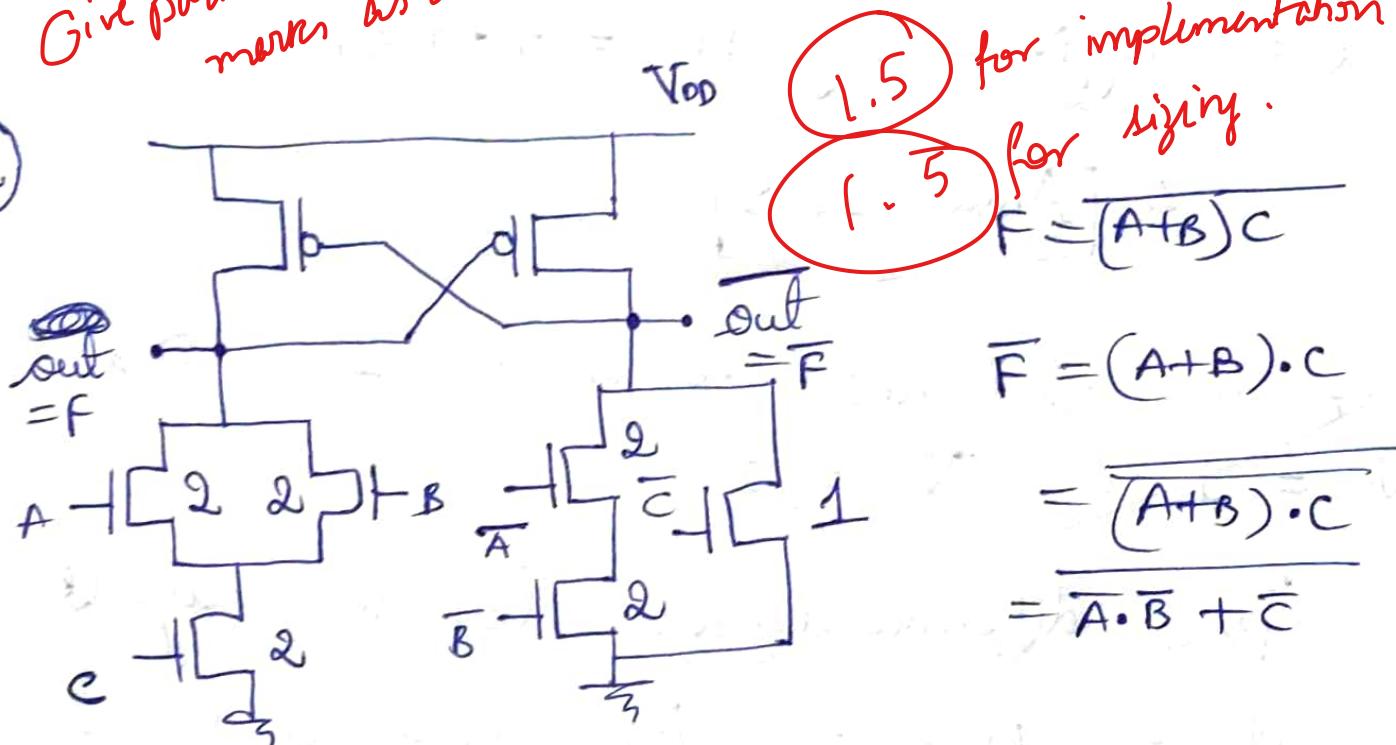
even if they tried using truth table, PT, 1's  
& first principles for finding which caps  
are ON during which transitions, give  
them (2) straight away.

them

(2)

Give partial marks as well

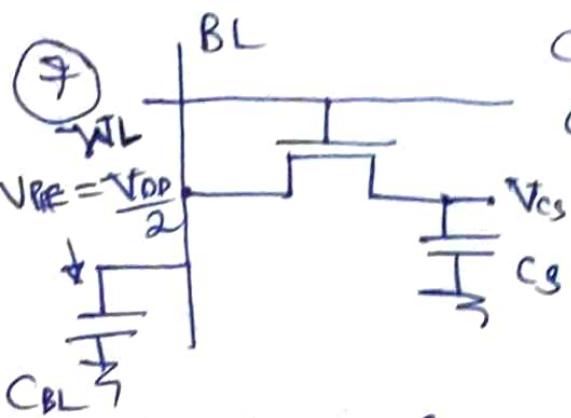
②



⑥ Number of bits = word length = 32

1

Give marks even if  
they only write  
final answer



$$C_s = 50 \times 10^{-15} F$$

$$C_{BL} = 10^{-11} F$$

If bit 1 was written already into  $C_s$  then until it discharges from  $V_{DD}$  to  $\frac{V_{DD}}{2}$  we can consider it as Bit 1 [but degrading] So we need to refresh back by  $\Delta V = \frac{V_{DD}}{2}$

$$\Delta Q = I_{leak} \times t_{refresh}$$

$$C_s \Delta V = I_{leak} \times t_{refresh}$$

$$t_{refresh} = \frac{50 \times 10^{-15} \times 0.35}{0.1 \times 10^{-9}} = 17.5 \times 10^{-5} \text{ seconds}$$

0.5

8 216 locations  $\Rightarrow$  minimum no. of address lines =  $\log_2 N = \log_2 216 = 7.754$

∴  $\boxed{\text{Answer } \approx 8}$

give full even if they write final solution

$$⑨ \quad 2\phi_p \times 9 = T$$

$$\phi_p = \frac{T}{18}$$

$$T \rightarrow 2\pi$$

$$\phi_p \rightarrow \frac{\pi}{9} [\phi_p]$$

Let us assume that input of 1st inv changes at  $t=0$  seconds /  $\phi = 0$  radians

when o/p of 1st inverter changes :

$$1 \rightarrow \phi_p + \pi [ \phi_{vo1} \text{ temporal to } \phi=0 ]$$

$$2 \rightarrow 2\phi_p + 2\pi [ \phi_{vo2} " ]$$

$$3 \rightarrow 3\phi_p + 3\pi$$

$$8 \rightarrow 8\phi_p + 8\pi$$

$$\therefore \phi_{vo8} - \phi_{vo3} = 8\phi_p + 8\pi - 3\phi_p - 3\pi \\ = 5\phi_p + 5\pi$$

$$= \boxed{\frac{5\pi}{9} + 5\pi \rightsquigarrow \pi + \frac{5\pi}{9} \text{ (E-period)}}$$

*In deg = 180 + 100*

TRUE

1

Give marks if they wrote either 0 or these.

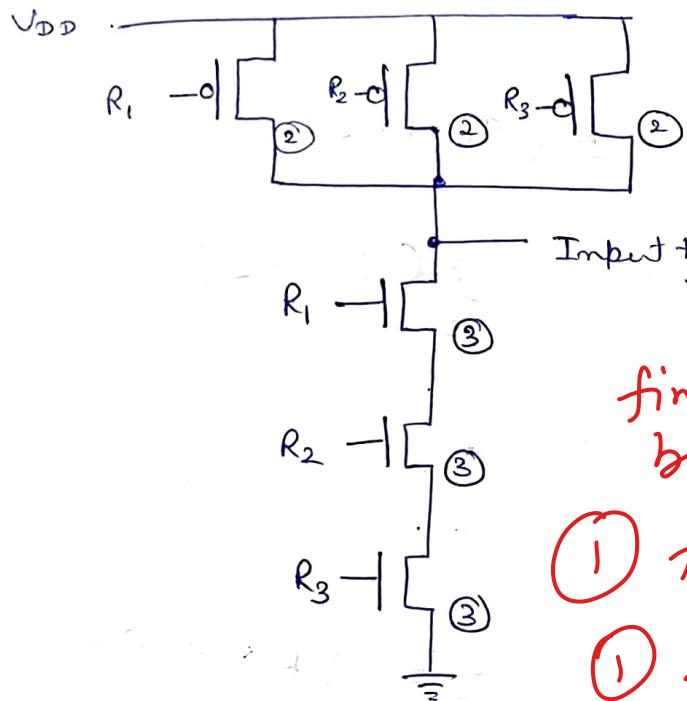
1

3(a)

$$\text{Input to Reg 4} = \overline{(R_2 \cdot R_3) \cdot R_1}$$

$$= \overline{R_1 \cdot R_2 \cdot R_3}$$

Essentially, it's a 3 i/p NAND



Give them full marks  
if they realize it

using any no. of  
stage &  
any no. of gates

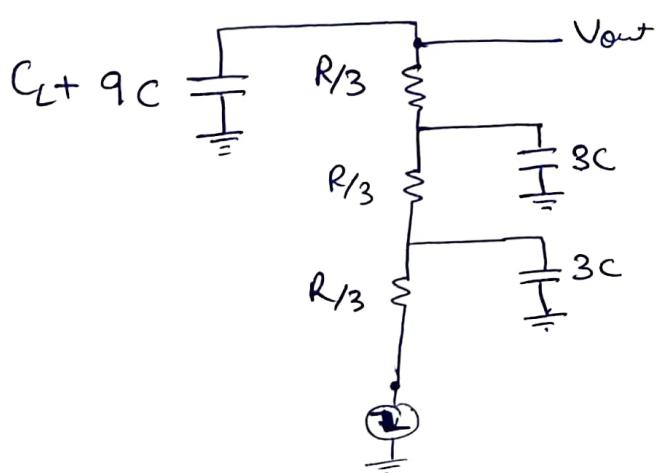
final implementation should  
be  $\overline{ABC}$

① for realization

① for adequate sizing

if they use the above implementation,

$$t_{phl(max)} : R_1 = 1, R_2 = 1, R_3 = 0 \rightarrow 1$$



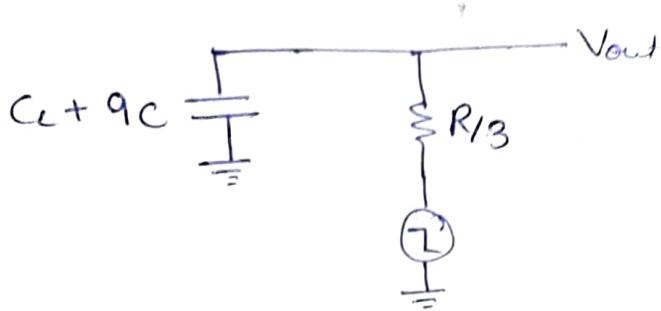
$$\tau = \frac{R}{3} \times 3C + \frac{2R}{3} \times 3C + \cancel{\frac{3R}{3} \times 9(C + CL)}$$

$$\tau = \cancel{RRC} R (12C + CL)$$

$$\Rightarrow t_{phl(max)} = \frac{0.69 R}{0.69 R (12C + CL)}$$

①

•  $t_{\text{PHE(min)}}$  :  $R_1: 0 \rightarrow 1$ ,  $R_2 = 1$ ,  $R_3 = 1$



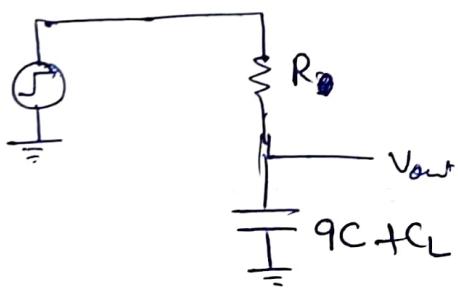
$$\tau = \frac{R}{3} \times (9C + C_L) = \cancel{0.69} \frac{R}{3} (9C + C_L)$$

$$\Rightarrow t_{\text{PHE(min)}} = \cancel{0.69} \frac{R}{3} (9C + C_L)$$

•  $t_{\text{PLH(max)}} = t_{\text{PEN(min)}}$

(assuming only 1 input can change at a time)

$$R_1: 1 \rightarrow 0, R_2 = 1, R_3 = 1$$



$$\tau = 9RC + C_RC$$

$$\Rightarrow t_{\text{PLH}} = \cancel{0.69} RC \\ 0.69 R (9C + C_L)$$

1

More  
(Worst case delay):  $t_{\text{PLH}} + t_{\text{PHL, max}}$

1

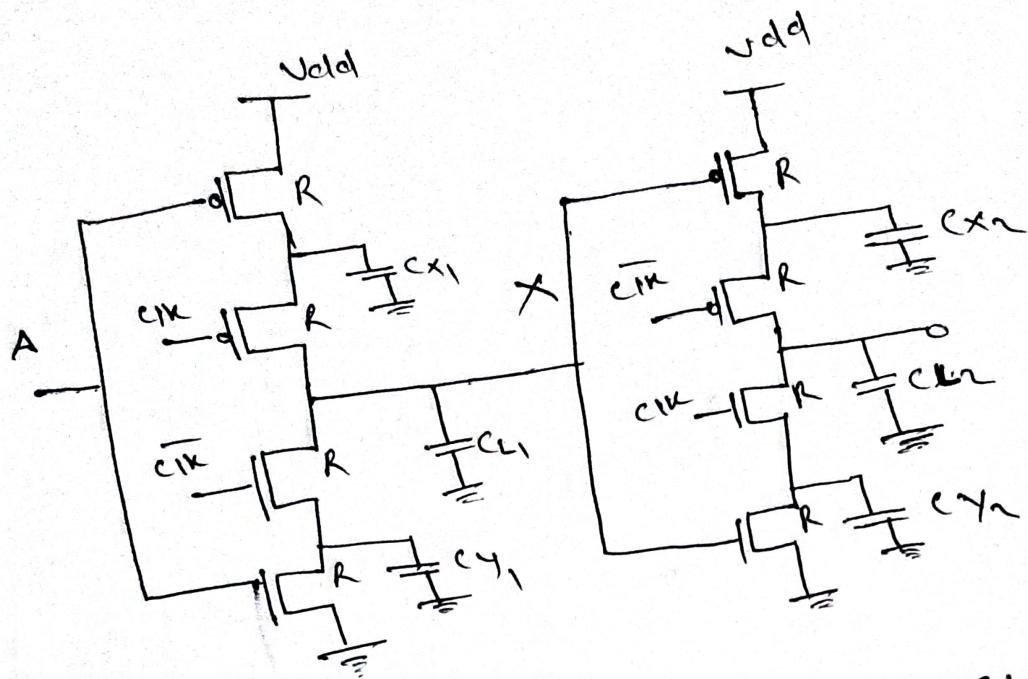
Min  
(best case delay):  $t_{\text{PLH}} + t_{\text{PHL, min}}$

In case they realized ABC using some other implementation, see if they found worst-case & best-case  $t_{\text{PLH}}$  &  $t_{\text{PHL}}$  or not. If they did it,

give them 2 even if they just found the  
Parasitic capacitances, give them 1.5 overall.

+1

③ For C<sup>2</sup>MOS



then ①

- ① t<sub>su</sub>  $\Rightarrow$  if data reach to CL1 then data can be sampled.

$$t_{su} = 0.69 \left[ (R+R) CL_1 + R CX_1 + 2R CY_1 \right]$$

CK=0, CK=1  $\Rightarrow$  CY1 also charges

- ② thold  $\Rightarrow$  C<sup>2</sup>MOS register with clocking is insensitive to overlap.  
so,  $\boxed{\text{Thold}=0}$

①

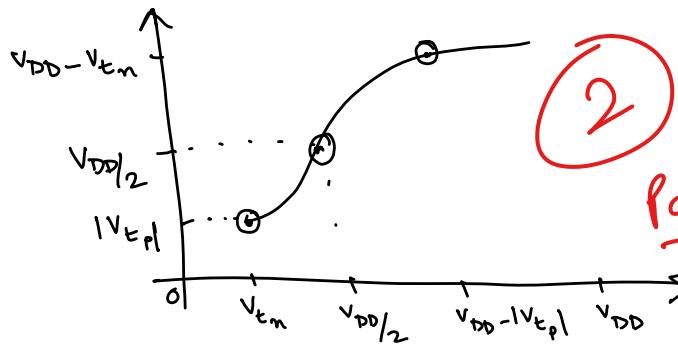
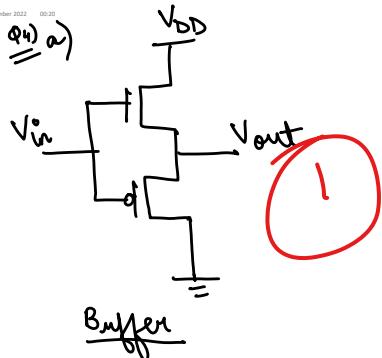
$$t_{cav,d} = 0.69 \left( (R+R) CL_2 + R CX_2 + 3R CY_2 \right)$$

- ④ t<sub>cav,c</sub>  $\Rightarrow$  min. [ ~~t<sub>cav,d</sub>~~ + t<sub>cav,d</sub> ]  
 $\Rightarrow$  if ~~x1~~ is stable below clock  
and charge CX2 before clock edge.

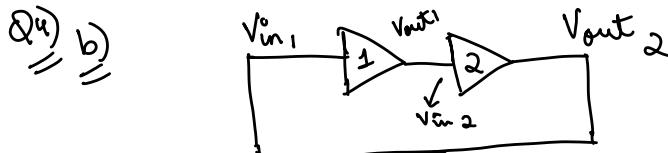
then  $t_{cav,c} = 0.69 \left[ 2R CL_2 + 2R CY_2 \right]$

CK=0  
CY2 over

④  $T_{\min} = t_{cav,d} + t_{su} + t_p(\max) \text{ (in part a)}$   
for this formula + ① for answer.

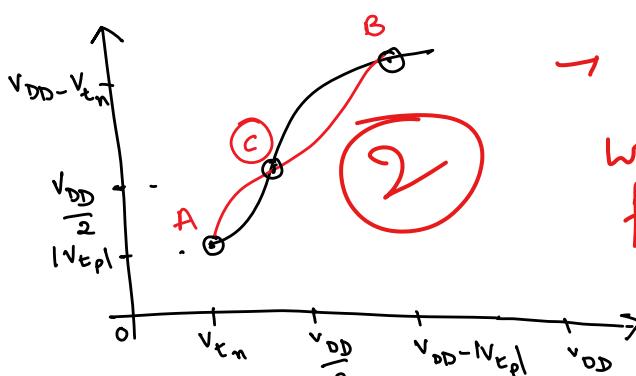


Partial:  
Give them  
1.5 if



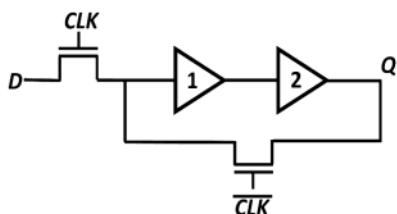
they make it from 0 to VDD  
instead of  $V_{tn}$  to  $V_{DD} - |V_{tp}|$

- Two stable states  
 $A \rightarrow$  stable state  
 $B \rightarrow$  stable state  
 $C \rightarrow$  unstable state



→ even if they explain  
with help of perturbation  
from pt. C, give them  
full marks

(1) Hence, acting as an bistable element



Give them 1 mark if they just  
write the latch.

→ When  $\text{clk} = 1$ , D is transmitted

↳ when I/P is  $V_{DD}$   $\rightarrow Q = V_{DD} - V_{tn}$

when I/P is Gnd  $\rightarrow Q = |V_{tp}|$

1

When  $\text{clk} = 0$

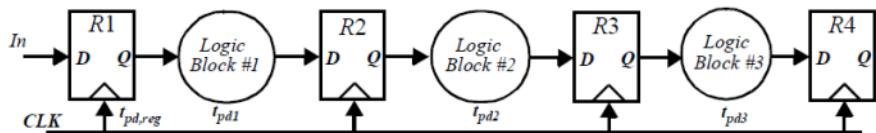
↳ the value of Q is held in the Latch

The circuit act like the Latch, transparent during  
clock is high and opaque when clock is low.

Note → If there  $V_t$  mismatch of pass transistor & Buffer is  
Consider then latch is not formed. } Could have been next  
part of question

- $\text{Q5) }$   
 5) A circuit consists of three logic blocks with delays of  $5 \pm 1$  ns,  $4 \pm 3$  ns,  $3 \pm 1$  ns, and  $2 \pm 0.5$  ns. Registers available for pipelining have delays ( $t_{su} + t_{c-q}$ ) of  $3 \pm 1$  ns. The circuit is pipelined with registers between each of the logic blocks.

What is the minimum clock period required for operating this pipelined circuit? (2 marks)



$$T > \max(t_{pd,reg}, t_{pd1}, t_{pd2}, t_{pd3}) + t_{cq,reg} + t_{su,reg}$$

1

$$T > 7 + 4$$

$$T > 11 \text{ nsec}$$

$$f_{\max} < \frac{1}{11} \text{ of}$$

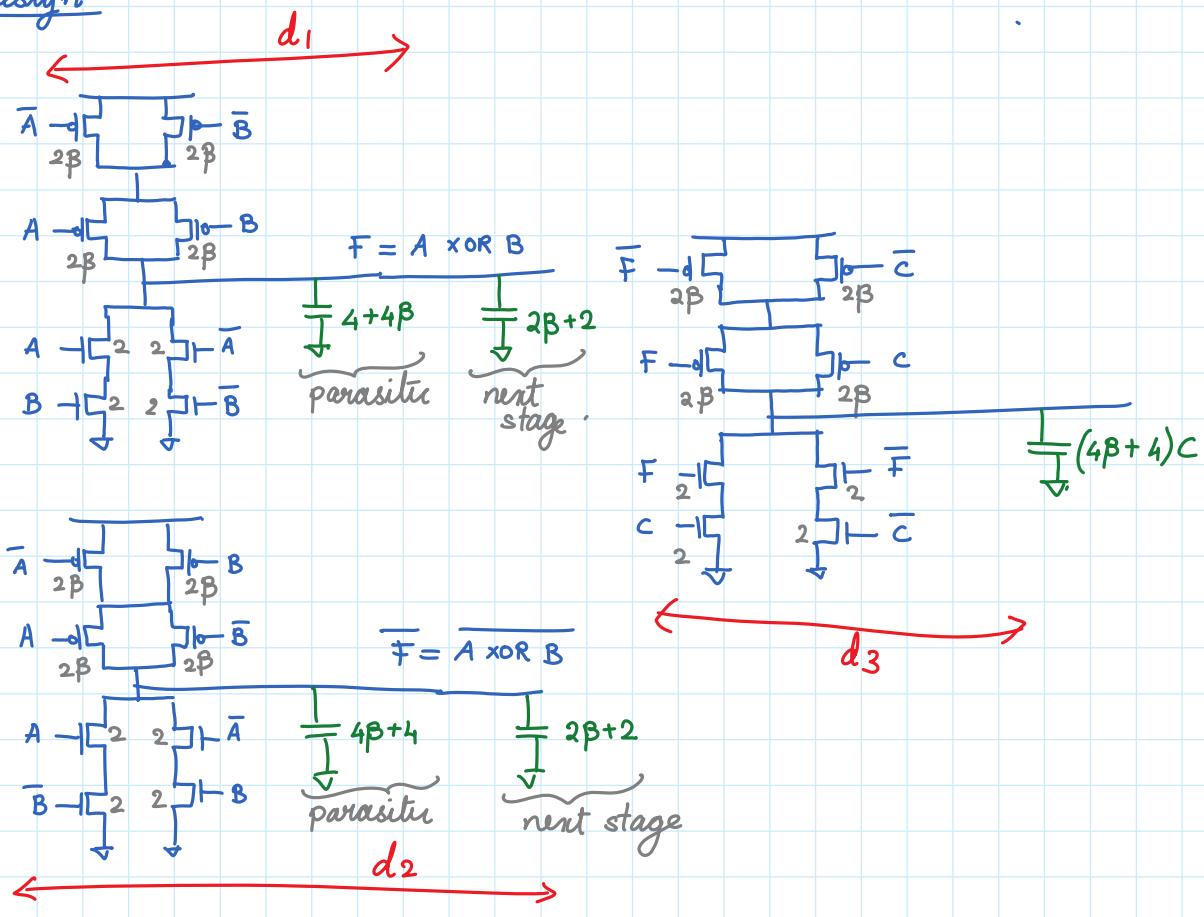
$$\boxed{f_{\max} < 90.90 \text{ MHz}}$$

Give them 2 marks  
even if they wrote correct  
answer regarding  
 $f_{\max}$  or  $T_{\min}$ .

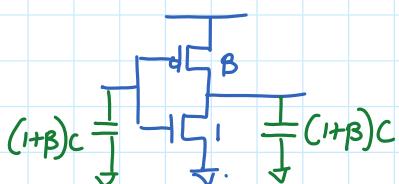
# Delay calculation based on logical effort

Saturday November 19, 2022 10:17 AM

## Design



## reference inverter



## Calculation of $d_1, d_2$

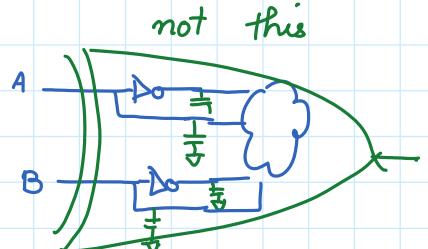
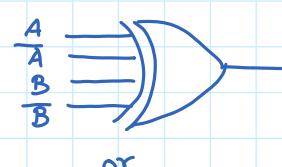
$$\text{parasitic effort}, \quad P_1 = \frac{(4+4\beta)C}{(1+\beta)C} = 4.$$

$$\text{logical effort}, \quad g_{IA} = \frac{(2+2\beta)C}{(1+\beta)C} = 2 = g_{I\bar{A}} = g_{IB} = g_{I\bar{B}}$$

$$\text{electrical effort}, \quad f = \frac{2+2\beta}{2+2\beta} = 1 \quad (\text{for all 4 inputs})$$

$$\therefore d_1 = 4 + 2 = 6.$$

model used for calculation



$$\therefore d_1 = 4 + 2 = 6$$

$$d_2 = 6 \quad (\text{same as } d_1)$$

Calculation of  $d_3$

parasitic effort,  $p_3 = 4$

logical effort,  $g_3 = 2 \quad (\text{for all } 4 \text{ i/p})$

electrical effort,  $f_3 = \frac{0}{(1+18)C} \quad (\text{no load, only parasitic cap})$   
 $= 0$

$$\therefore d_3 = \underline{\underline{4}}$$

$$D = (d_1 \text{ or } d_2) + d_3 = 6 + 4 = \underline{\underline{10}}$$

from A  
to out