



MINI QUIZ 1

Mini Quiz 1

Q1 Which of the following statements are correct about input high voltage V_{IH} and input low voltage V_{IL} :

Max. score: 1; Neg. score: 0; Your score: 0

- $V_{IH} - V_{IL}$ is the range of acceptable logic voltages.
- V_{IH} and V_{IL} demarcate the regions showing attenuation (gain < 1) and amplification (gain > 1).
- The regions of acceptable high and low voltages are bounded by V_{IH} and V_{IL} , respectively.
- We define V_{IH} and V_{IL} at a slope of |1| because it separates the undefined region from the acceptable logic voltage range.

Q2 Which of the statements are correct about nominal voltages V_{OH} and V_{OL} ?

Max. score: 1; Neg. score: 0; Your score: 0

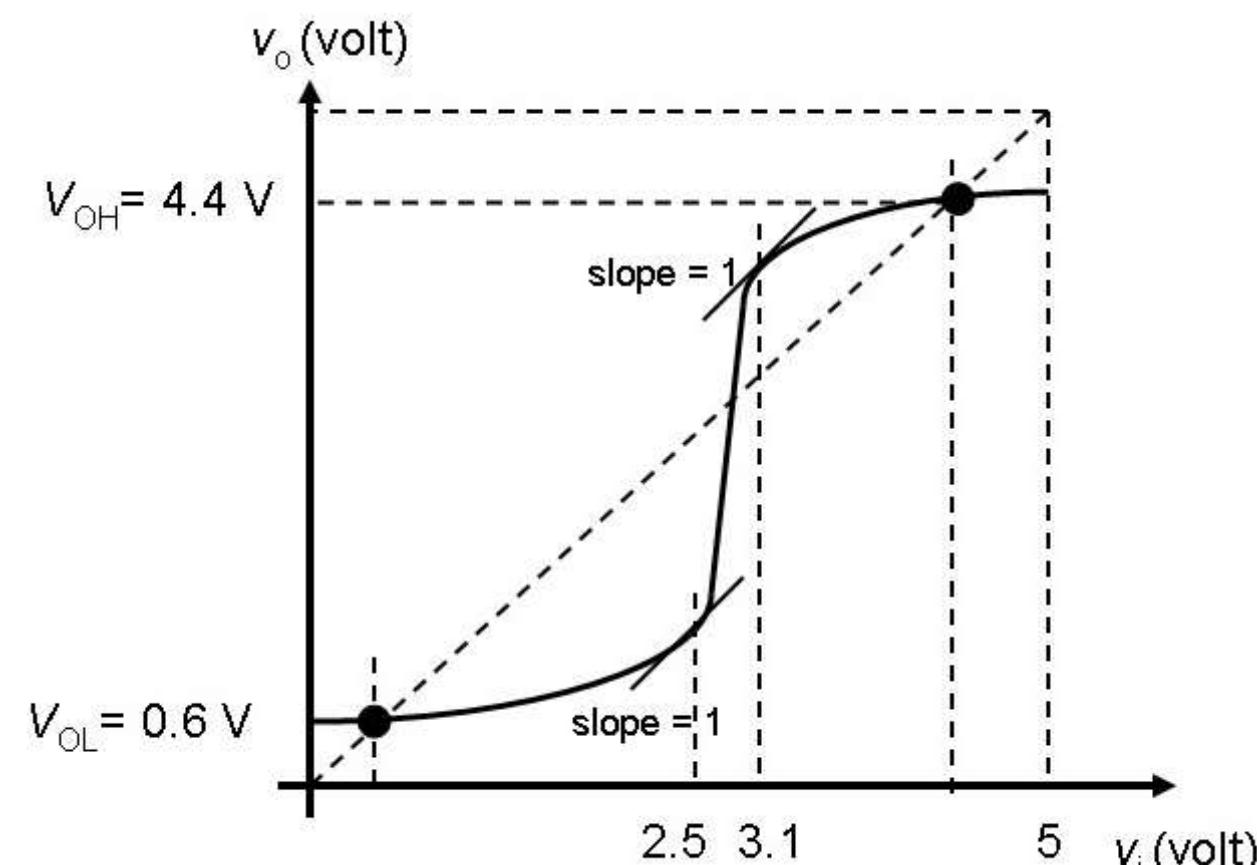
- For non-inverting voltage transfer characteristics (VTC), application of V_{OH} as input yields V_{OL} at the output and vice versa.
- For non-inverting voltage transfer characteristics (VTC), application of V_{OH} as input yields V_{OH} at the output and vice versa.
- For inverting voltage transfer characteristics (VTC), application of V_{OH} as input yields V_{OL} at the output and vice versa.
- For inverting voltage transfer characteristics (VTC), application of V_{OH} as input yields V_{OH} at the output and vice versa.

Q3 Noise margin high for a non-inverting buffer circuit

===== Question =====

For the VTC of buffer given below, what is noise margin high, NM_H ?

Write the numerical value of the answer in volt units to one decimal place accuracy.



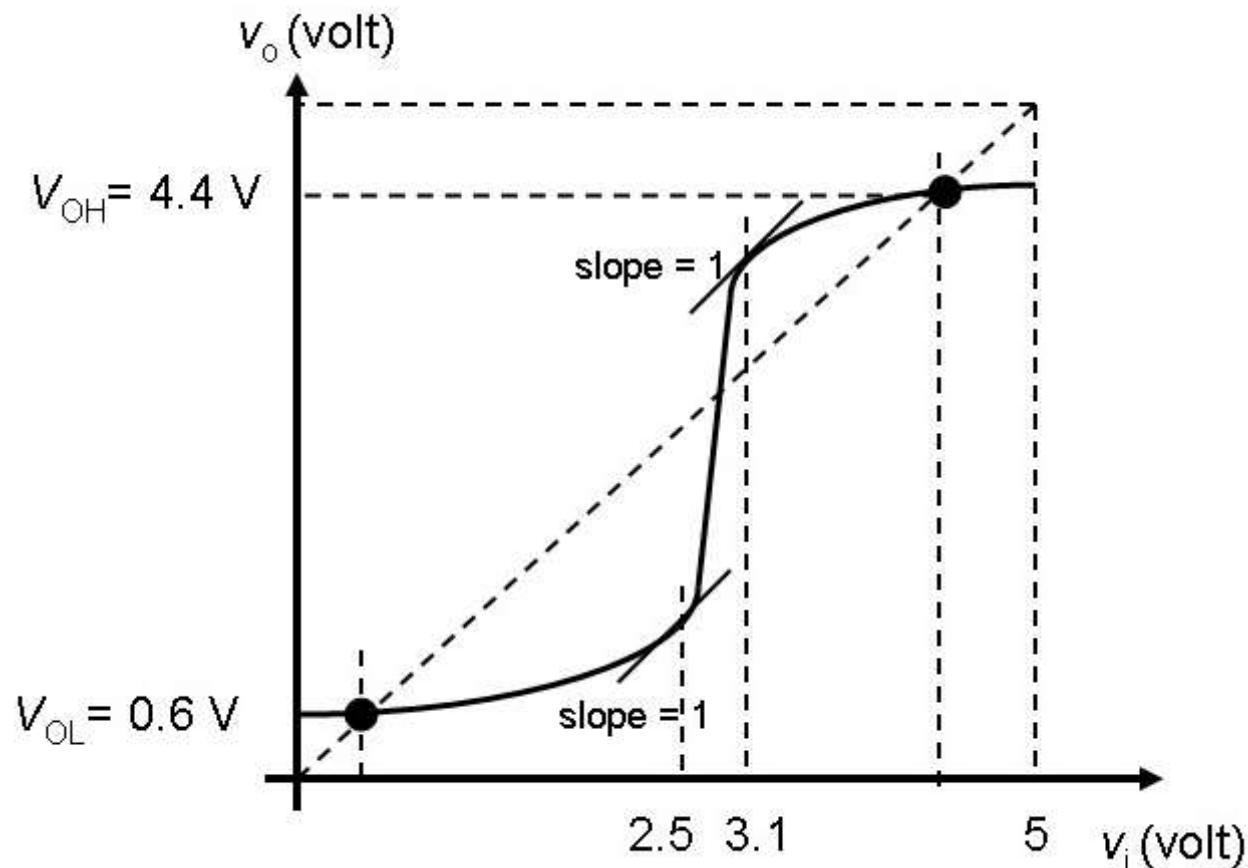


1.3

Correct answer:

1.3

Q4 The VTC of a non-inverting buffer is shown here. This is not a regenerative circuit.



Max. score: 1; Neg. score: 0; Your score: 1

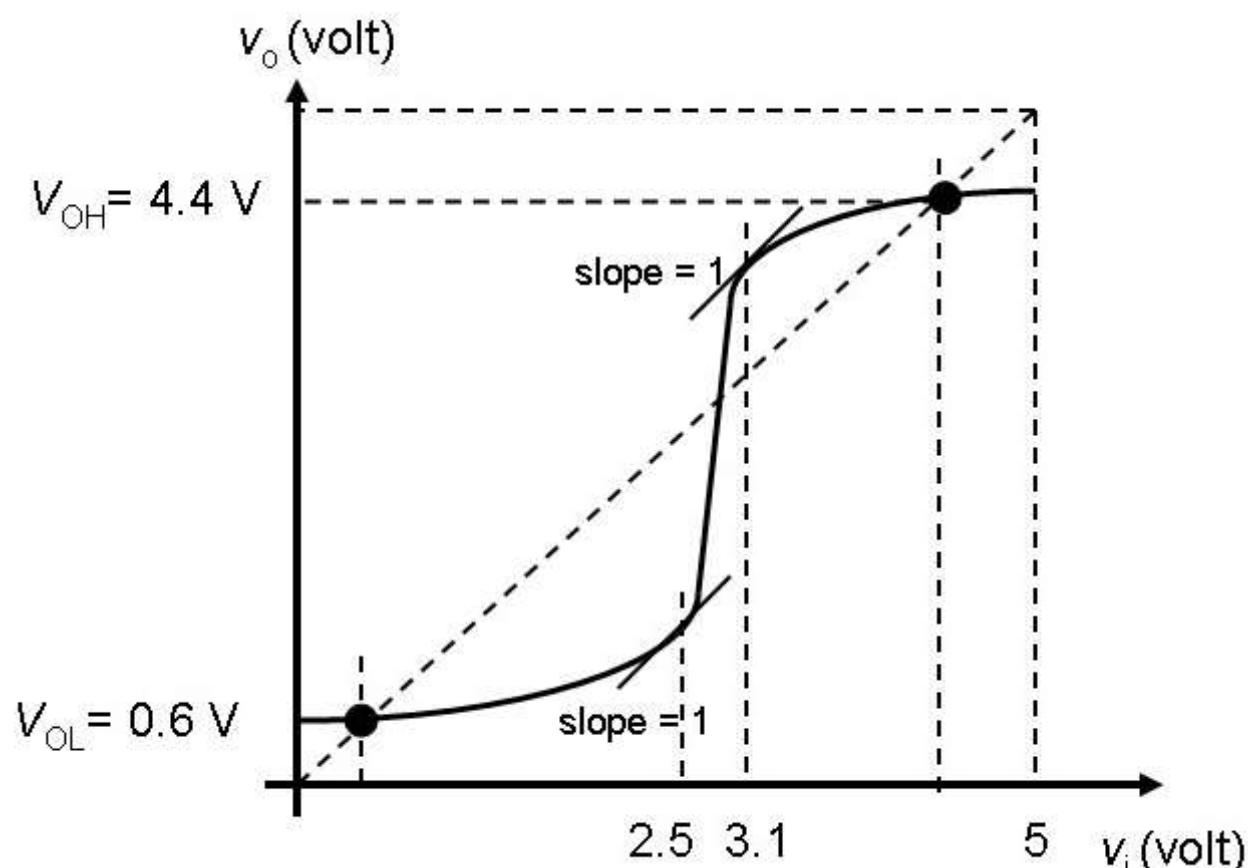
- ✓ false
- true

Q5 Transition region range for a non-inverting buffer circuit

===== Question =====

What is the range of the transition region where you avoid biasing the input of the buffer circuit?

Write the numerical value of the answer in volt units to one decimal place accuracy.





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Users Online : 19

Your answer:

0.6

Correct answer:

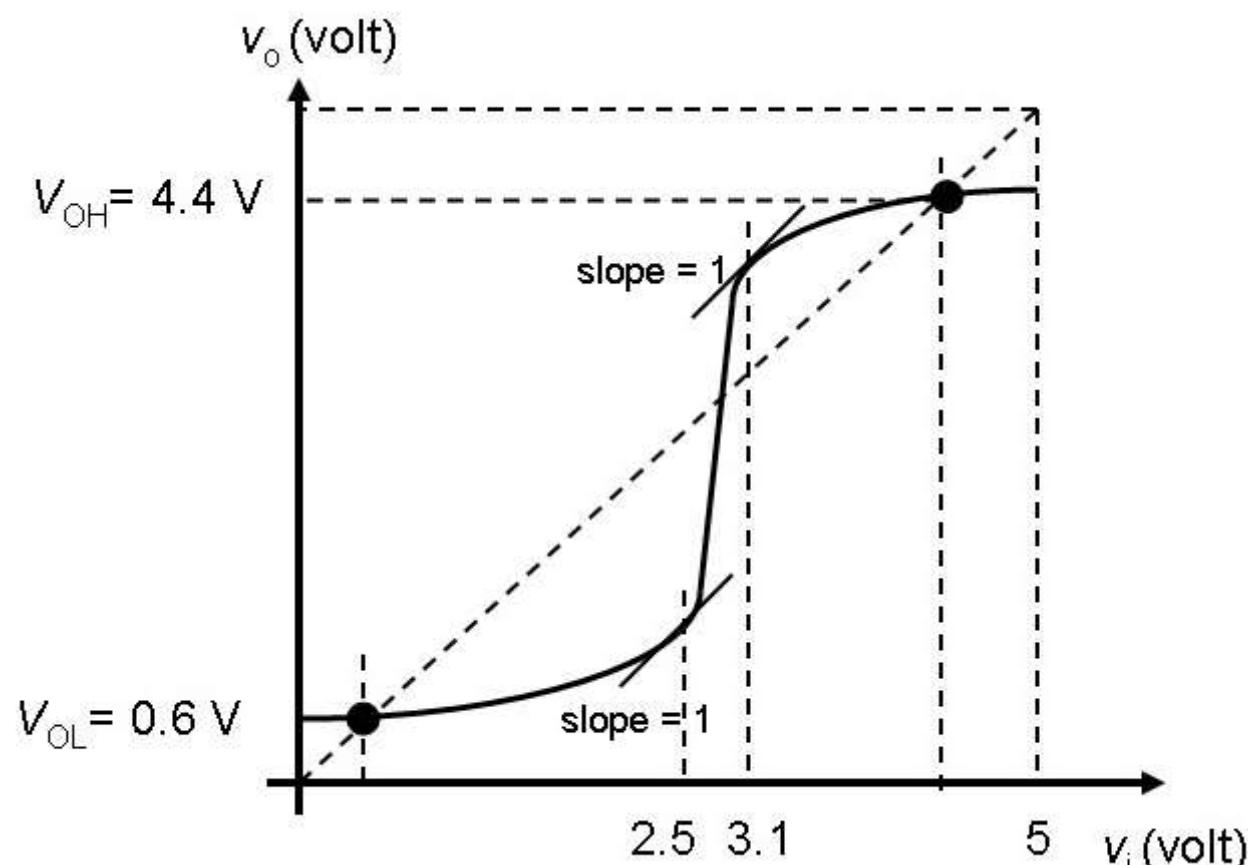
0.6

Q.6 The maximum acceptable low voltage for a non-inverting buffer circuit

===== Question =====

For the VTC of buffer given below, what is V_{IL} , the maximum acceptable “low” voltage?

Write the numerical value of the answer in volt units to one decimal place accuracy.



Max. score: 1; Neg. score: 0; Your score: 1

Your answer:

2.5

Correct answer:

2.5

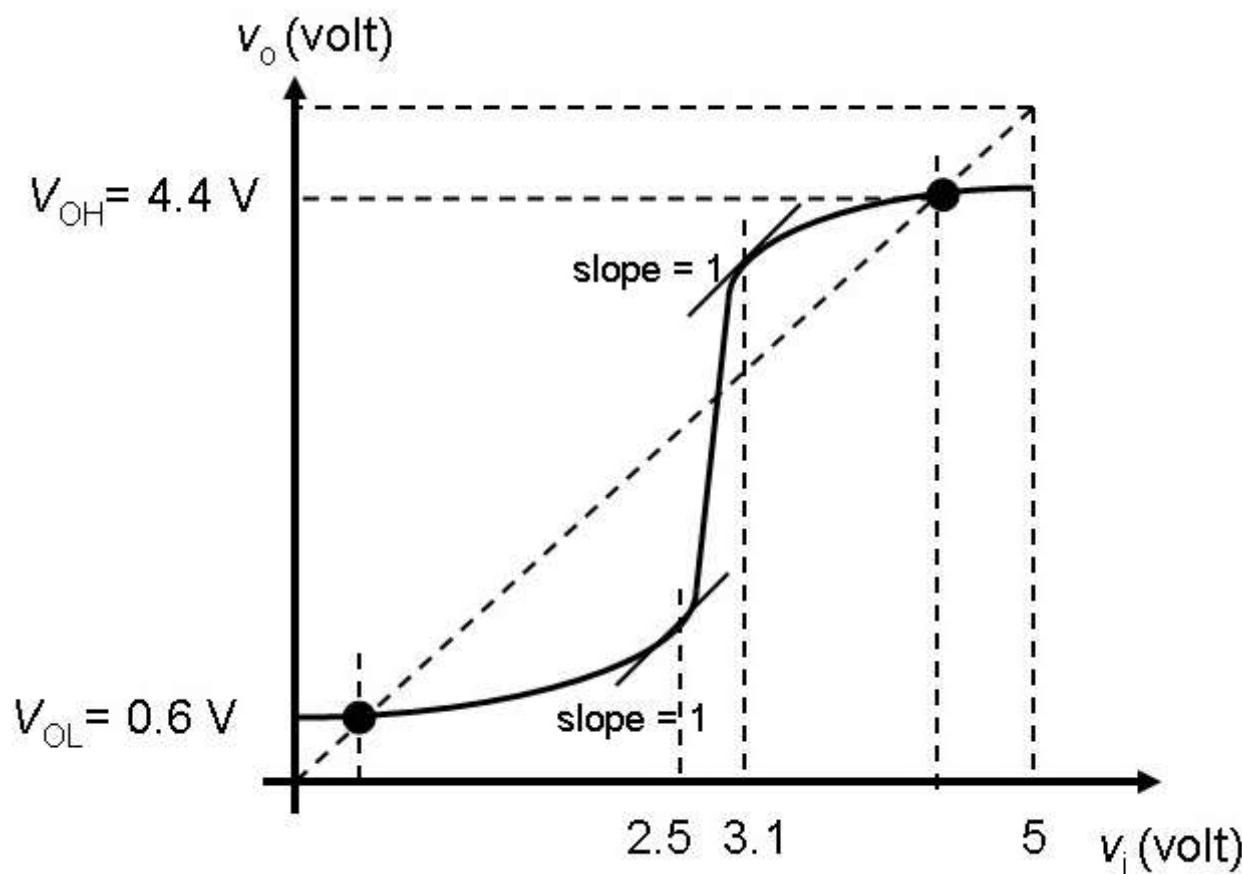
Q.7 The idea of implementing Boolean logic with circuits was first proposed by:

Max. score: 1; Neg. score: 0; Your score: 0

- William Shockley
- Claude Shannon
- Jack Kilby and Robert Noyce
- George Bool
- Charles Babbage
- Gordon Moore

Q.8 The minimum acceptable high voltage for a non-inverting buffer circuit

===== Question =====



Max. score: 1; Neg. score: 0; Your score: 1

Your answer:

3.1

Correct answer:

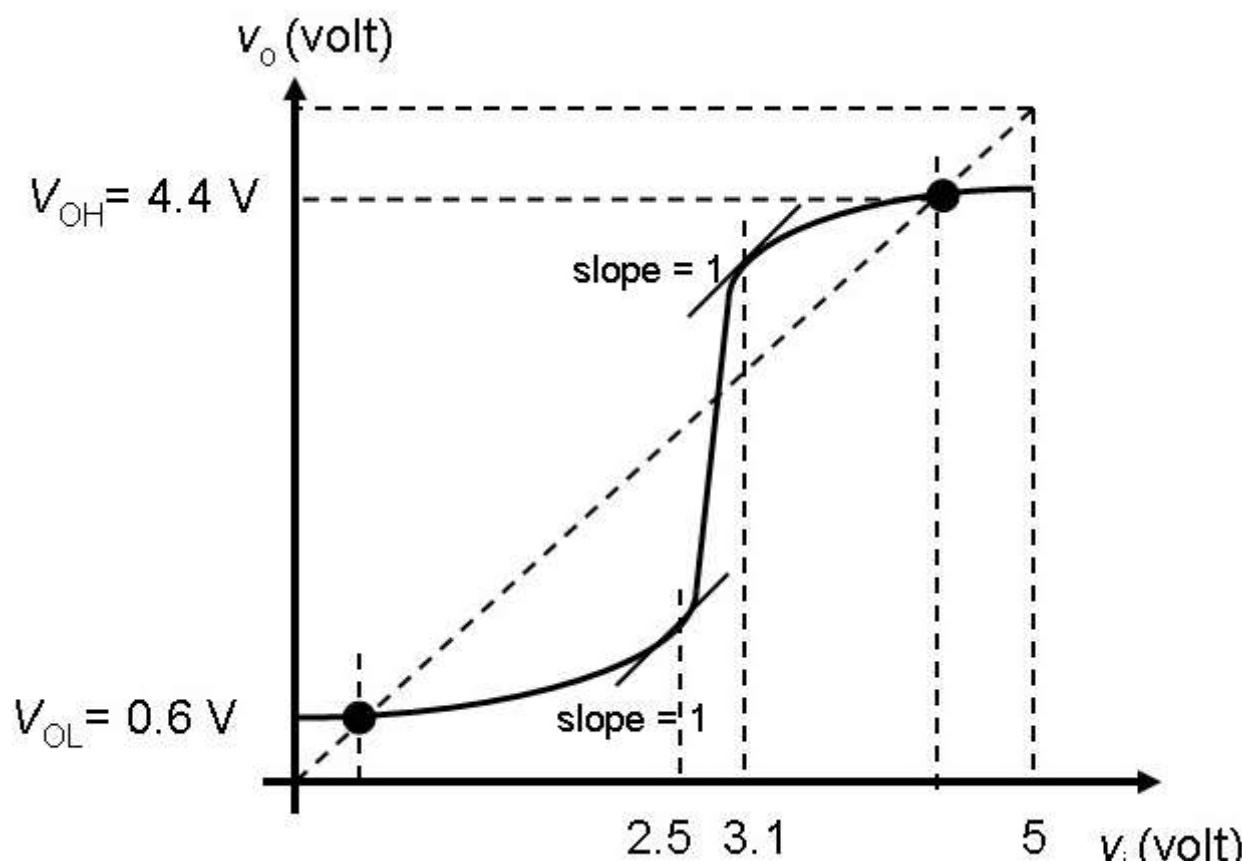
3.1

Q.9 Noise margin low for a non-inverting buffer circuit

===== Question =====

For the VTC of buffer given below, what is noise margin low, NM_L ?

Write the numerical value of the answer in volt units to one decimal place accuracy.



Max. score: 1; Neg. score: 0; Your score: 1



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Users Online : 19

Correct answer:

1.9

Q.10 Suppose the supply voltage rail (V_{DD}) is 20% more noisy than the ground.

We designed a logic circuit which has an abrupt transition between the logic levels (i.e. amplification/transition region width = 0 V) and a full output swing ($V_{OH} = V_{DD}$ and $V_{OL} = 0$ V)

What should be the value for noise margin high (NM_H) and noise margin low (NM_L) for this circuit to work correctly with this noise constraint?

Max. score: 1; Neg. score: 0; Your score: 0

- $NM_L = 0.5 V_{DD}; NM_H = 0.5 V_{DD}$
- $NM_L = 0.4 V_{DD}; NM_H = 0.6 V_{DD}$
- $NM_L = 0.55 V_{DD}; NM_H = 0.45 V_{DD}$
- $NM_L = 0.45 V_{DD}; NM_H = 0.55 V_{DD}$

Score: 6

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Mini-Quiz II

23/08/2022

Time: 25 minutes

Total Marks: 10

Instructions

- Read the questions carefully.
- Answer the questions to the point. Do not write more than 2-3 lines of explanation.

Binod wants to design a two-input NAND gate, a two-input NOR gate and a two-input XOR gate. Due to the resource constraints in Phulera, he only has access to positive switches and resistors. The positive switches exhibit a resistance R_{Low} when turned ON and R_{High} when turned OFF while the load resistor value is R_L . Binod seeks your help while designing the logic gates and analyzing their performance. Please help him by answering the following questions:

- a) Draw the schematic for logic gate realizations using positive switches and resistors. (1 Mark)
- b) Analyze the t_{PLH} and t_{PHL} for realized logic gates. Assume the load capacitance to be C_L . Find the propagation delay (t_p) and the maximum frequency for toggling of inputs. (5 Marks)
- c) Determine the static power dissipation and the dynamic power dissipation for these logic gates. Assume that the duty cycle for inputs is 50%. (3 Marks)
- d) Which configuration out of NAND/NOR would you recommend to Binod and why? (1 Mark)

(Hint: try to recall the classroom discussion on handling performance metrics for multi-input gates.)

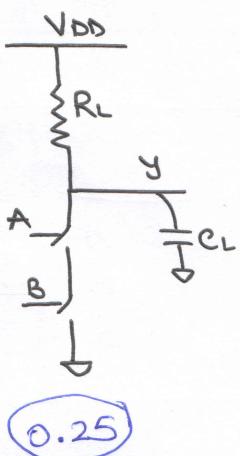
1

MinP Quiz II

(a)

NAND gate $A, B \rightarrow \text{inputs}$
 $y \rightarrow \text{output}$

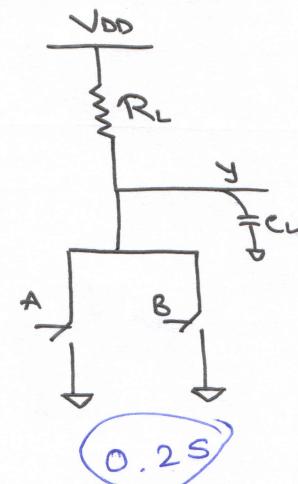
$$Y = \overline{A \cdot B}$$



0.25

NOR gate $A, B \rightarrow \text{inputs}$
 $y \rightarrow \text{output}$

$$Y = \overline{A + B}$$

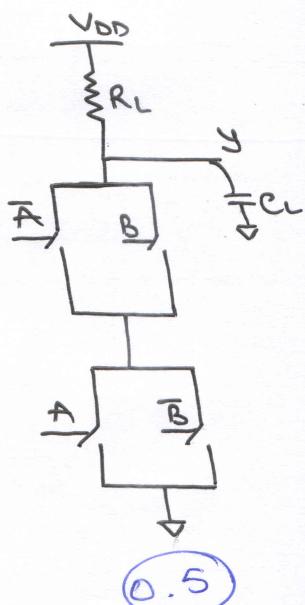


0.25

XOR gate $A, B \rightarrow \text{inputs}$
 $y \rightarrow \text{output}$

$$Y = A \oplus B$$

$$Y = AB + \overline{A}B$$



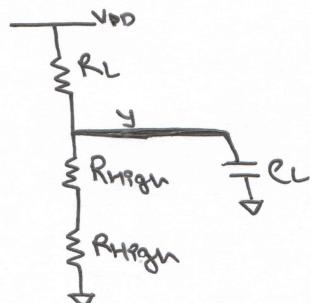
0.5

(b)

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

* For input $A, B = 0, 0$, replace both switches by R_{High} .

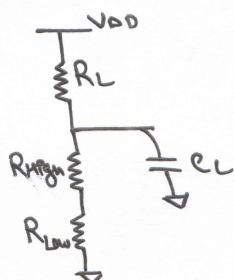


$$t_{PLH} = 0.69 (2R_{High} \parallel R_L) C_L$$

(1) We'll take the worst case

①

* For input $A, B = 0, 1$ or $1, 0$, we have



$$t_{PLH} = 0.69 \{ (R_{High} + R_{Low}) \parallel R_L \} C_L$$

$$= 0.69 \{ R_{High} \parallel R_L \} C_L$$

* Assumptions

↳ $R_{High} \gg R_{Low}$

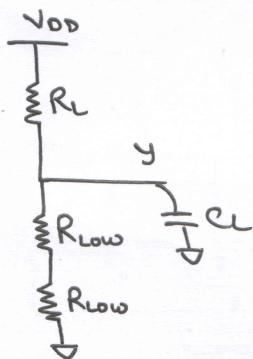
$$\therefore R_{High} + R_{Low} \approx R_{High}$$

$$\rightarrow (R_{High} \parallel R_{Low}) \approx R_{Low}$$

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

* For inputs A B , we have
 1 1

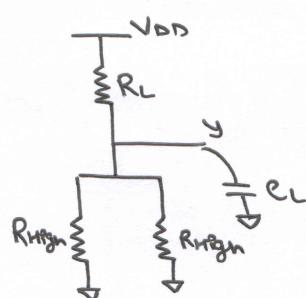


$$C_{PHL} = 0.69 \{ 2R_{low} \| R_L \} C_L$$

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

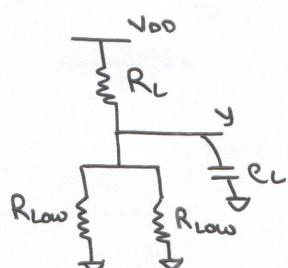
* For inputs A B , we have
 0 0



$$A \quad B \\ 0 \quad 0, \text{ we have}$$

$$C_{PLH} = 0.69 \left\{ \frac{R_{high}}{2} \| R_L \right\} C_L$$

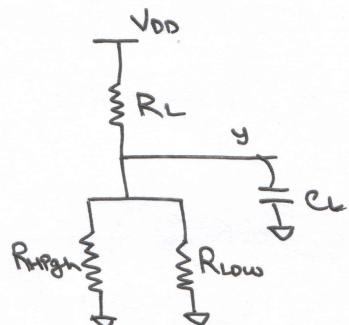
* For inputs A B , we have
 1 1



$$C_{PHL} = 0.69 \left\{ \frac{R_{low}}{2} \| R_L \right\} C_L$$

(1)

* For inputs A B or A B , we have
 0 1 1 0



$$C_{PHL} = 0.69 \{ R_{high} \| R_{low} \| R_L \} C_L \\ \approx 0.69 \{ R_{low} \| R_L \} C_L$$

We'll take the worst case

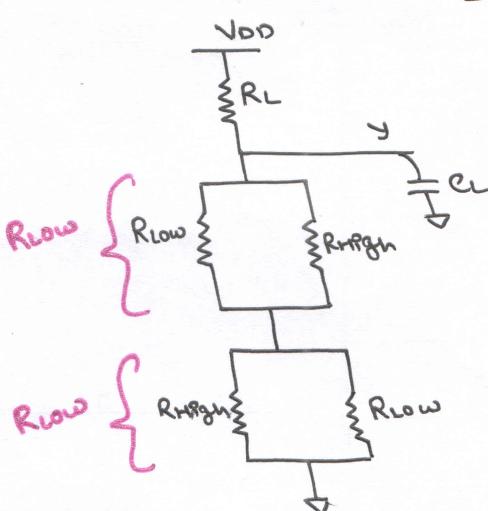
XOR

* For inputs

A B
0 0
1 1

, we have

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



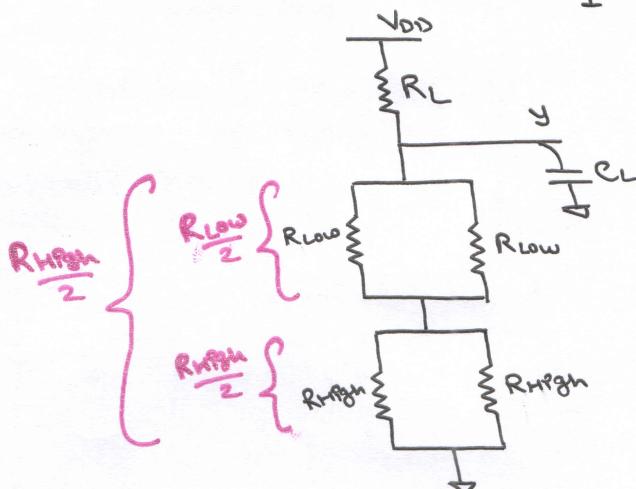
$$t_{PHL} = 0.69 \{ 2R_{low} \| R_L \} C_L$$

①

* For inputs

A B
0 1
1 0

$$t_{PLH} = 0.69 \left\{ \frac{R_{high}}{2} \| R_L \right\} C_L$$



*

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

y worst case t_{PHL} & t_{PLH}

$$t_p(\text{NAND}) \rightarrow \frac{1}{2} \left\{ 0.69 C_L \right\} \left\{ (2R_{high} \| R_L) + \{ 2R_{low} \| R_L \} \right\}$$

$$t_p(\text{NOR}) \rightarrow \frac{1}{2} \left\{ 0.69 C_L \right\} \left\{ \left(\frac{R_{high}}{2} \| R_L \right) + (R_{low} \| R_L) \right\}$$

①

$$t_p(\text{XOR}) \rightarrow \frac{1}{2} \left\{ 0.69 C_L \right\} \left\{ (2R_{low} \| R_L) + \left(\frac{R_{high}}{2} \| R_L \right) \right\}$$

Two alternatives

$$(i) T > 2 \max \{ t_{PL} \}$$

Relatively
Better
choice

(ii) NAND

$$T > 2 \times \frac{1}{2} 0.69 C_L \left[\frac{(2R_{High} || R_L)}{(2R_{Low} || R_L)} \right]$$

$$\Rightarrow T > 0.69 C_L \left[(2R_{High} || R_L) + (2R_{Low} || R_L) \right]$$

$$\Rightarrow f' < \frac{1}{0.69 C_L \left[(2R_{High} || R_L) + (2R_{Low} || R_L) \right]}$$

↓
max. freq.

* One can calculate f_{max} for the other gates by following the method above.

0	1	1	$\sqrt{V_{DD}} / (R_{High} + R_{Low} + R_L)$
1	0	1	$\sqrt{V_{DD}} / (R_{High} + R_{Low} + R_L)$
1	1	0	$\sqrt{V_{DD}} / (2R_{Low} + R_L)$



(i)

$$\hookrightarrow P_{Dynamic} = f_{pin} C_L V_{DD}^2$$

Neglect switching factor for the time being.
Accurate soln should have $\propto 0 \rightarrow$ for each gate.

$$\hookrightarrow \text{Total } P_{Static, avg.} = \frac{\sum P_{Static}}{4}$$

(i) $P_{Static, rating} = \text{Worst Case Scenario}$

(i)

$$(iii) T > 2 \max \{ t_{PHL}, t_{PLH} \}$$

As a designer, we prefer this to be on the safer side

(iv) NAND (Margins)

$$T' > 2 \times \frac{1}{2} \times 0.69 C_L \left[2R_{High} || R_L \right]$$

$$f' < \frac{1}{0.69 C_L [2R_{High} || R_L]}$$

max. freq.

(ii) NOR

$$f < \frac{1}{0.69 C_L \left\{ \left(\frac{R_{High}}{2} \parallel R_L \right) + \left(R_{Low} \parallel R_L \right) \right\}}$$

$$f' < \frac{1}{0.69 C_L \left[\frac{R_{High}}{2} \parallel R_L \right]}$$

(iii) XOR

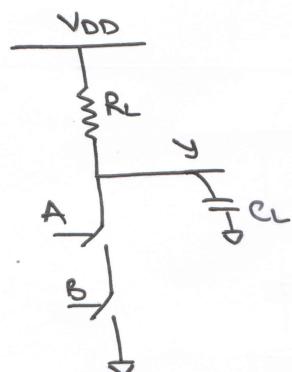
$$f < \frac{1}{0.69 C_L \left\{ \left(\frac{R_{High}}{2} \parallel R_L \right) + \left(2R_{Low} \parallel R_L \right) \right\}}$$

$$f' < \frac{1}{0.69 C_L \left\{ \frac{R_{High}}{2} \parallel R_L \right\}}$$

(c)

NAND

A	B	y	P _{static}
0	0	1	$V_{DD}^2 / (2R_{High} + R_L)$
0	1	1	$V_{DD}^2 / (R_{High} + R_{Low} + R_L)$
1	0	1	$V_{DD}^2 / (R_{High} + R_{Low} + R_L)$
1	1	0	$V_{DD}^2 / (2R_{Low} + R_L)$



①

$$\hookrightarrow P_{Dynamic} = f_{in} C_L V_{DD}^2$$

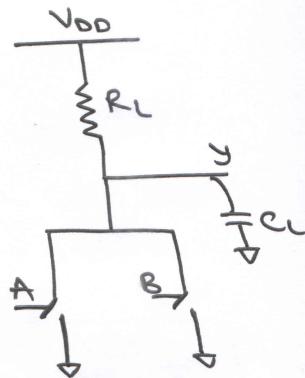
Neglect switching factor for the time being.
Accurate soln should have $\propto 0 \rightarrow$ for each gate.

$$\hookrightarrow \text{Total } P_{Static}^{\text{avg.}} = \frac{\sum P_{Static}}{4}$$

① P_{static} rating = Worst case scenario.

NOR

A	B	Y	P _{static}
0	0	1	$\frac{V_{DD}^2}{2} / (R_{High} + R_L)$
0	1	0	$\frac{V_{DD}^2}{2} / (R_{Low} \parallel R_{High} + R_L)$
1	0	0	$\frac{V_{DD}^2}{2} / (R_{Low} \parallel R_{High} + R_L)$
1	1	0	$\frac{V_{DD}^2}{2} / (R_{Low} + R_L)$

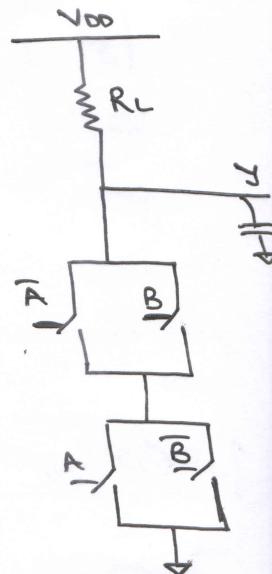


$$P_{dynamic} = f_{pin} C_L V_{DD}^2$$

$$\text{Total } P_{static} = \frac{1}{4} \sum P_{static}$$

XOR

A	B	Y	P _{static}
0	0	0	$\frac{V_{DD}^2}{2} / (2[R_{High} \parallel R_{Low}] + R_L)$
0	1	1	$\frac{V_{DD}^2}{2} / (\frac{R_{Low}}{2} + \frac{R_{High}}{2} + R_L)$
1	0	1	$\frac{V_{DD}^2}{2} / (\frac{R_{Low}}{2} + \frac{R_{High}}{2} + R_L)$
1	1	0	$\frac{V_{DD}^2}{2} / (2[R_{High} \parallel R_{Low}] + R_L)$

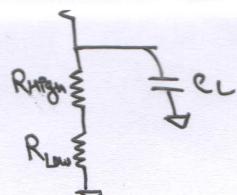


$$P_{dynamic} = f_{pin} C_L V_{DD}^2$$

$$\text{Total } P_{static} = \frac{1}{4} \sum P_{static} \quad (1)$$

(d) Performance wise \rightarrow NOR is better than NAND

$$\begin{aligned} t_{PLH} &= 0.03 \{ (R_{High} + R_{Low}) \parallel R_L \} C_L \\ &= 0.69 \{ R_{High} \parallel R_L \} C_L \end{aligned}$$



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Mini-Quiz III

23/08/2022

Total Marks: 10

Time: 30 minutes

Instructions

- **Read the questions carefully.**
- **Answer the questions to the point. Do not write more than 2-3 lines of explanation.**

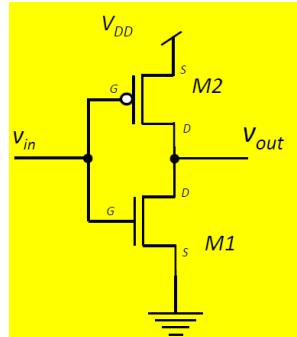
The MOSFETs somehow go berserk and take a resolution that they would not saturate and follow the equation for linear mode of operation for any range of V_{DS} given by:

$$I_{DS,n} = \begin{cases} \frac{k'_n C_{OX} W}{L} \left[(V_{GS} - V_{th,n}) V_{DS} - \frac{V_{DS}^2}{2} \right]; I_{DS} > 0 \\ 0; I_{DS} \leq 0 \end{cases}$$

and

$$I_{SD,p} = \begin{cases} \frac{k'_p C_{OX} W}{L} \left[(V_{SG} - |V_{th,p}|) V_{SD} - \frac{V_{SD}^2}{2} \right]; I_{SD} > 0 \\ 0; I_{SD} \leq 0 \end{cases}$$

- 1) Under these unusual circumstances, do you think that the circuit given below works like an inverter? (2 marks)



- 2) If so, find out the load-line characteristics and VTC of this inverter using the following parameters for MOSFETs:

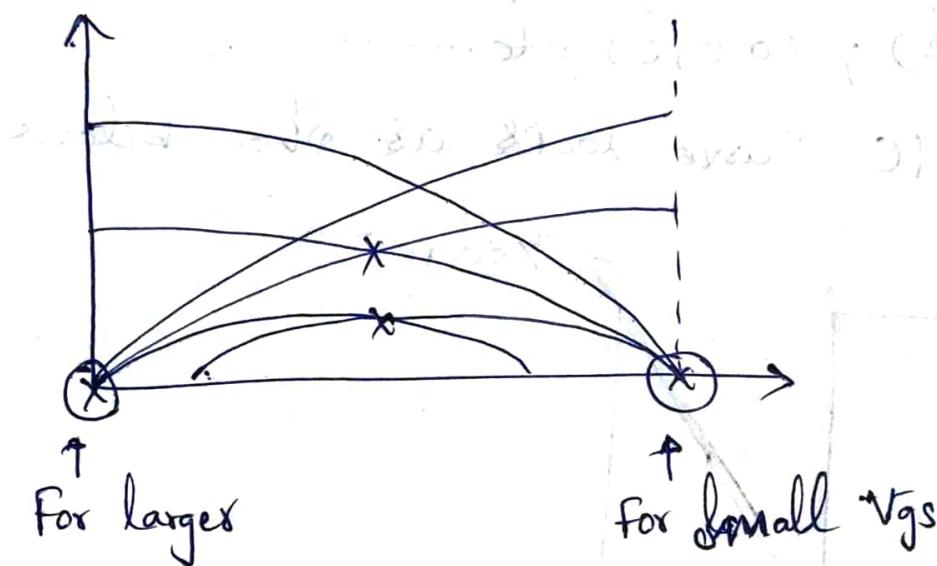
$$\frac{k'_n C_{OX} W}{L} = \frac{k'_p C_{OX} W}{L} = 10^{-4}; V_{th,n} = |V_{th,p}| = 0.05 \text{ V}; V_{DD} = 0.3 \text{ V}$$

You may take help of MATLAB/Python/R, etc. for your analysis. You may even go for first-hand calculations using calculator (even a qualitative plot of load line and VTC would work fine in that case). (5 marks)

- 3) What is the V_{IH} and V_{IL} of this inverter (if it works like an inverter)? Is the inverter regenerative? (3 marks)

Mini-Quiz III

- ① Yes, even if the given MOSFETs don't saturate, $I_{SOP} = I_{DSN}$ must be satisfied so the load line characteristics will approximately look as shown below,



- For small $V_{GS}(V_{in}) \rightarrow$ larger $V_{DS}(V_{out})$
 → For larger $V_{GS}(V_{in}) \rightarrow$ small $V_{DS}(V_{out})$
- Inverter's Nature

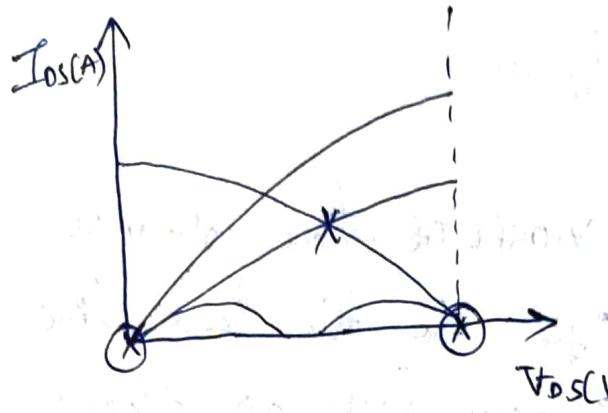
∴ Answer is "YES".

$$\frac{K_n' C_{ox} W}{L} = \frac{K_p' C_{ox} W}{L} = K = 10^{-4} \text{ A/V}^2$$

$$V_{th,n} = |V_{th,p}| = 0.05$$

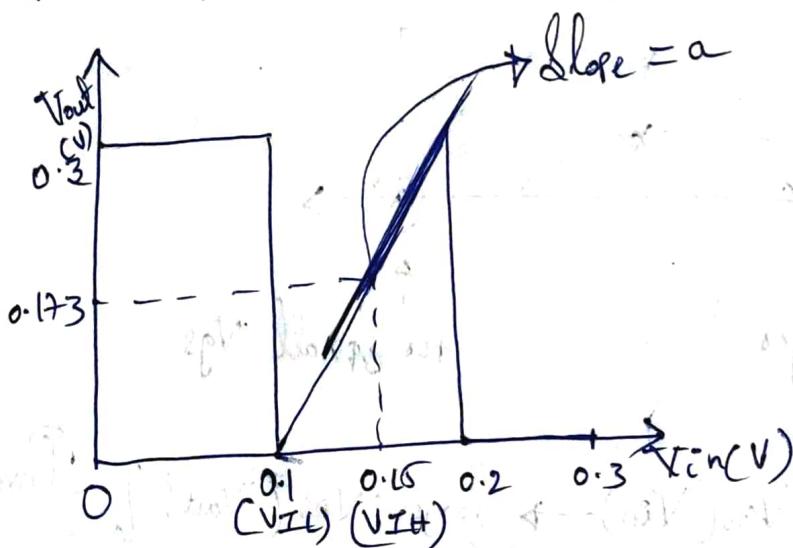
$$V_{DD} = 0.3$$

- Using MATLAB, our loadlines will come in this way,



⇒ By using "disp" function in MATLAB, (V_{ds}, V_{os}) Points that we get are $(0.1, 0)$; ~~$(0.15, 0.173)$~~ ; $(0.13, 0.115)$; $(0.15, 0.173)$; $(0.2, 0)$ etc.....

∴ The VTC curve looks as show below



$$(3) V_{IL} = 0.1V$$

$$V_{IH} = 0.2V$$

Yes, the inverter is regenerative because slope "a" is very large. If any noise occurs in that range region (in that input range $(0.1-0.2)$) then output goes to either "1" or "0" depending on the noise magnitude.

```

%Code with different inputs

clc;
close all;
%Vfb=-1;
%phi_F=0.4503;
%gamma=0.707;
%phi_o=1.004;
Vt=0.05;
Vgs1=0.05;
Vgs2=0.1;
Vgs3=0.15;
Vgs4=0.2;
Vgs5=0.25;
k=1e-4;
Vds=0:0.000001:0.3;
%vdd=0.3;

Idsn1=k*((Vgs1-Vt)*(Vds)-0.5*(Vds.^2));
Idsp1=k*0.5*((0.3-Vgs1-Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

Idsn2=k*((Vgs2-Vt)*(Vds)-0.5*(Vds.^2));
Idsp2=k*0.5*((0.3-Vgs2-Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

Idsn3=k*((Vgs3-Vt)*(Vds)-0.5*(Vds.^2));
Idsp3=k*0.5*((0.3-Vgs3-Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

Idsn4=k*((Vgs4-Vt)*(Vds)-0.5*(Vds.^2));
Idsp4=k*0.5*((0.3-Vgs4-Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

Idsn5=k*((Vgs5-Vt)*(Vds)-0.5*(Vds.^2));
Idsp5=k*0.5*((0.3-Vgs5-Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

%Idsn2=k*((Vgs2-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp2=k*0.8*((Vgs2-0.3+Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

%Idsp2=k*((Vgs3-Vt)*(Vds)-0.5*(Vds.^2));
%Idsn3=k*((Vgs3-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp3=k*0.8*((Vgs3-0.3+Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

%Idsn4=k*((Vgs4-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp4=k*0.8*((Vgs4-0.3+Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

%Idsn5=k*((Vgs5-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp5=k*0.4*((Vgs5-Vt)*(Vds-Vgs5)-0.5*((Vds-Vgs5).^2));
%Ids2=k*((Vgs2-Vt)*(Vds)-0.5*(Vds.^2));

%[Ids1_max,Ids1_max_ind]=max(Ids1);
%[Ids2_max,Ids2_max_ind]=max(Ids2);

%Vds_ids1 = Vds(Ids1_max_ind);
%Vds_ids2 = Vds(Ids2_max_ind);

```

```

%vds_ids1_x = Vds_ids1:0.01:Vds(length(Vds));
%ids1_pk = ones(1,length(vdb_ids1_x))*Ids1_max;
%vdb_ids2_x = Vdb_ids2:0.01:Vdb(length(Vdb));
%ids2_pk = ones(1,length(vdb_ids2_x))*Ids2_max;

%def
%red_int = polyxpoly(Vds, Idsn1, Vds, Idsp1);
%blue_int = polyxpoly(Vds, Idsn2, Vds, Idsp2);
%c_int = polyxpoly(Vds, Idsn3, Vds, Idsp3);
%green_int = polyxpoly(Vds, Idsn4, Vds, Idsp4);
%display(red_int, blue_int, c_int, green_int)
disp([Vgs1, Vds(find(round(Idsp1, 10) == round(Idsn1, 9))))]);
disp([Vgs2, Vds(find(round(Idsp2, 10) == round(Idsn2, 10))))]);
disp([Vgs3, Vds(find(round(Idsp3, 9) == round(Idsn3, 9))))]);
disp([Vgs4, Vds(find(round(Idsp4, 10) == round(Idsn4, 10))))]);
disp([Vgs5, Vds(find(round(Idsp5, 10) == round(Idsn5, 10))))]);

figure
plot(Vds,Idsn1,'r');
hold on
plot(Vds,Idsn2,'b');
hold on
plot(Vds,Idsn3,'c');
hold on
plot(Vds,Idsn4,'y');
hold on
plot(Vds,Idsn5,'g');
hold on
plot(Vds,Idsp1,'r');
hold on
plot(Vds,Idsp2,'b');
hold on
plot(Vds,Idsp3,'c');
hold on
plot(Vds,Idsp4,'y');
hold on
plot(Vds,Idsp5,'g');

%plot(Vds,Idsn3,'c');
%plot(Vds,Idsn4,'y');
%plot(Vds,Idsn5,'g');
hold off;
%ylim([0,3*10^(-5)]);
xlabel("drain body voltage(V)");
ylabel("drain to source current(A)");

%Code with single input (Change the input values for which you want to see output to
get the VTC)
clc;
close all;
%Vfb=-1;
%phi_F=0.4503;
%gamma=0.707;

```

```

%phi_o=1.004;
Vt=0.05;
Vgs1=0.15;
k=0.1e-4;
vdd=0.3;
Vds=0:0.000001:vdd;

Idsn1=k*((Vgs1-Vt)*(Vds)-0.5*(Vds.^2));
Idsp1=k*0.5*((vdd-Vgs1-Vt)*(-Vds+vdd)-0.5*((-Vds+vdd).^2));

%Idsn2=k*((Vgs2-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp2=k*0.8*((Vgs2-0.3+Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

%Idsp2=k*((Vgs3-Vt)*(Vds)-0.5*(Vds.^2));
%Idsn3=k*((Vgs3-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp3=k*0.8*((Vgs3-0.3+Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

%Idsn4=k*((Vgs4-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp4=k*0.8*((Vgs4-0.3+Vt)*(-Vds+0.3)-0.5*((-Vds+0.3).^2));

%Idsn5=k*((Vgs5-Vt)*(Vds)-0.5*(Vds.^2));
%Idsp5=k*0.4*((Vgs5-Vt)*(Vds-Vgs5)-0.5*((Vds-Vgs5).^2));
%Ids2=k*((Vgs2-Vt)*(Vds)-0.5*(Vds.^2));

%[Ids1_max,Ids1_max_ind]=max(Ids1);
%[Ids2_max,Ids2_max_ind]=max(Ids2);

%Vds_ids1 = Vds(Ids1_max_ind);
%Vds_ids2 = Vds(Ids2_max_ind);

%vds_ids1_x = Vds_ids1:0.01:Vds(length(Vds));
%ids1_pk = ones(1,length(vdb_ids1_x))*Ids1_max;
%vdb_ids2_x = Vdb_ids2:0.01:Vdb(length(Vdb));
%ids2_pk = ones(1,length(vdb_ids2_x))*Ids2_max;

%def
%red_int = polyxpoly(Vds, Idsn1, Vds, Idsp1);
%blue_int = polyxpoly(Vds, Idsn2, Vds, Idsp2);
%c_int = polyxpoly(Vds, Idsn3, Vds, Idsp3);
%green_int = polyxpoly(Vds, Idsn4, Vds, Idsp4);
%display(red_int, blue_int, c_int, green_int)
disp([Vgs1, Vds(find(round(Idsp1, 10) == round(Idsn1, 10)))]);
%disp([Vgs2, Vds(find(round(Idsp2, 10) == round(Idsn2, 10)))]);
%disp([Vgs3, Vds(find(round(Idsp3, 9) == round(Idsn3, 9)))]);
%disp([Vgs4, Vds(find(round(Idsp4, 10) == round(Idsn4, 10)))]);
%disp(Vgs4, Vds(find(round(Idsp4, 10) == round(Idsn4, 10))));
figure

```

```

plot(Vds,ldsn1,'r');
%plot(Vds,ldsp2,'b');
%plot(Vds,ldsn3,'c');
%plot(Vds,ldsn4,'y');
%plot(Vds,ldsn5,'g');
hold on;
%plot(vds_ids1_x,ids1_pk, 'r')
%plot(Vds,lds2,'b');
%plot(vds_ids2_x,ids2_pk, 'b')
%plot(Vds,ldsn2,'b');
plot(Vds,ldsp1,'g');
%plot(Vds,ldsp2,'b');
%plot(Vds,ldsp3,'c');
%plot(Vds,ldsp4,'y');
%plot(Vds,ldsp5,'g');

%plot(Vds,ldsn3,'c');
%plot(Vds,ldsn4,'y');
%plot(Vds,ldsn5,'g');
hold off;
ylim([0,7*10^(-5)]);
xlabel("drain body voltage(V)");
ylabel("drain to source current(A)");

```

MINI QUIZ 5

Q.1 A student of EE370A had a doubt regarding the sizing of MOSFETs for symmetric operation in CMOS inverters. His hypothesis was: one can make the VTC symmetric even by using a minimum sized p-MOSFET and an n-MOSFET with length = $2L_{min}$ and width = L_{min} . Is his hypothesis correct? If yes, why don't the designers use this approach?

Max. score: 2; Neg. score: 0; Your score: 0

Q.2 "Decreasing the length of the source and drain regions can reduce the gate capacitance."
Is the statement correct? If yes, what limits the scaling of the source/drain regions?

Max. score: 2; Neg. score: 0; Your score: 0

Q.3 Can a CMOS inverter charge the voltage source (V_{DD} node) during transient operation?
if yes, how? if no, why?

Max. score: 2; Neg. score: 0; Your score: 0.5

Q.4 "The foundries typically provide two flavors of MOSFETs for circuit design: HVT or High performance MOSFETs and LVT or Low power MOSFETs". Is this statement correct? if its false, please rectify the statement and give appropriate reason.

Max. score: 2; Neg. score: 0; Your score: 0

Q.5 In power gating technique, which variant of transistors do we use for the sleep transistors: HVT or LVT and why?

Q.6 A student measured the short circuit current of a CMOS inverter experimentally and plotted it as a function of the transition time of the input. Contrary to what one would expect, the short circuit current exhibited a monotonous trend throughout the transition period. Is it even possible? If yes, what could be the potential reason behind this observation?

Max. score: 2; Neg. score: 0; Your score: 0

Q.7 As a digital designer, how would you size the n-MOSFETs and p-MOSFETs in a CMOS inverter when:

- a) the consumer wants a symmetric VTC and t_{pLH} and t_{pHL} and the load capacitor is dominated by extrinsic capacitance.
- b) the consumer demands a symmetric VTC and load capacitance is dominated by intrinsic capacitance.
- c) the consumer demands a fast speed of operation.
- d) the consumer wants the least static power dissipation.
- e) the consumer wants a symmetric operation but a reduced area.
- f) the consumer wants the least dynamic power dissipation.

Note: Don't try to find out the exact values of sizing factors or length/width. Just mention a qualitative estimate..

Max. score: 3; Neg. score: 0; Your score: 0

1) Yes, we will obtain symmetric VTC in that case 1

why is it not used by designers :

- * Taking on-state resistance of min. sized NMOS as reference ($= R_{ref}$)
- * Taking input gate capacitance of min. sized MOSFET as reference ($L_{min} W_{min} C_{ox} = C_{ref}$)
- * Taking $N_m = 2 N_p$

Case A

$$\text{NMOS: } W = W_{min}, L = L_{min}$$

$$\text{PMOS: } W = 2W_{min}, L = L_{min}$$

$$\text{on-state res. of NMOS} = R_{ref}$$

$$\text{" " PMOS} = R_{ref}$$

$$\text{I/P gate capacitance (NMOS)} = C_{ref}$$

$$\text{" " (PMOS)} = 2C_{ref}$$

$$\Rightarrow \text{Total I/P capacitance} = 3C_{ref}$$

Case B

$$\text{NMOS: } W = W_{min}, L = 2L_{min}$$

$$\text{PMOS: } W = W_{min}, L = L_{min}$$

$$\text{on-state res. of NMOS} = 2R_{ref}$$

$$\text{" " PMOS} = 2R_{ref}$$

$$\text{I/P gate capacitance (NMOS)} = 2C_{ref}$$

$$\text{" " (PMOS)} = C_{ref}$$

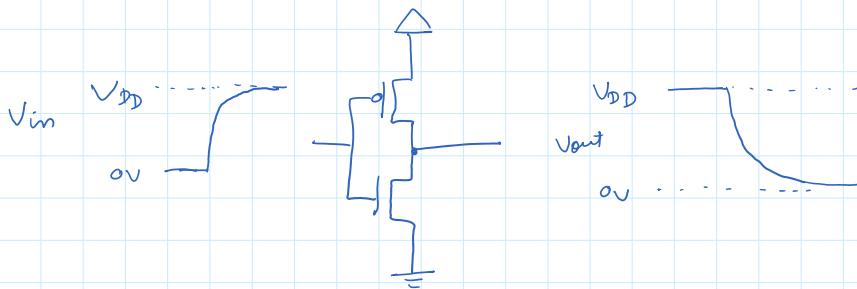
$$\Rightarrow \text{Total I/P capacitance} = 3C_{ref}$$

\therefore we do not prefer case B as it will make the transient response slower (larger RC time constant) 1

2) 1 False ; scaling of source and drain regions is limited by the area required for making ohmic contact 1

3) 1 Yes, during high to low transition 1

- In the absence of any parasitic capacitance between I/P and O/P :



- However, due to parasitic capacitance, a fraction of input voltage may get coupled to output
⇒ Output transient response will be modified to



- for duration t_1 , $V_{out} > V_{DD}$ and CMOS inverter will charge the voltage source

4) Foundries provide 2 flavours of transistors -

Statement is false

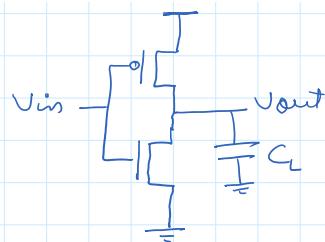
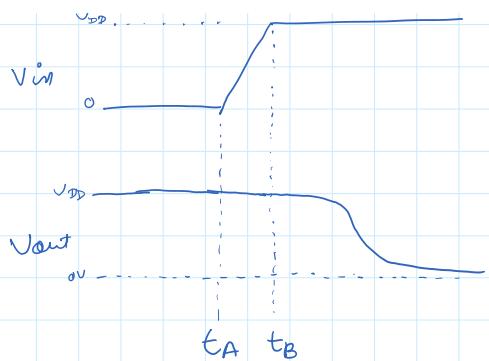
- HUT (High V_t) = Low power transistor as it has low static power consumption during off state (low subthreshold leakage)
- LVT (Low V_t) = High performance transistor as it would have a larger overdrive voltage and hence, better driving strength for any value of gate voltage

5) HUT → because it will exhibit lower leakage current and therefore lesser static power dissipation in off-state

6) Consider the case for a very large value of C_L and for input transitioning from 0 to 1



yes, it is possible



- Before input transition begins at $t = t_A$, $V_{out} = V_{DD}$ & $V_{in} = 0V$, at this point, C_L is charged to V_{DD}
- during the transition period t_A to t_B , NMOS turns on and begins to discharge C_L
Since C_L is very large, it stays close to V_{DD} for this entire duration
 $\Rightarrow V_{SD,PMOS} = V_{DD} - V_{out} \approx 0$ for this duration & $I_{SD,PMOS} = 0$
 \therefore there is no short circuit current

1

on
n-mos
 $L = 2L_{min}$
OP 1st question

7) a) NMOS \rightarrow min size
PMOS $\rightarrow L = L_{min}$
 $w = \beta w_{min}$

$$\left(\beta = \frac{N_m}{N_p} \right)$$

0.5

b) NMOS \rightarrow min size
PMOS $\rightarrow L = L_{min}$
 $w = \beta w_{min}$

0.5

c) NMOS \rightarrow min sized
PMOS $\rightarrow L = L_{min}$
 $w = \sqrt{\beta} w_{min}$

0.5

d) Increase L for both NMOS, PMOS to reduce subthreshold leakage, thereby reducing static power dissipation

$L > w$
0.5

e) NMOS \rightarrow min size

$$\text{NMOS} \rightarrow L = 2L_{min}$$

$$w = w_{min}$$

- Below
 n-well area has to
 increase P-MOS
 realising P-MOS
 with 2L_{min}
 width
- e) NMOS \rightarrow min size
 PMOS \rightarrow $L = L_{\min}$
 $w = 2w_{\min}$
- NMOS \rightarrow $L = 2L_{\min}$
 $w = w_{\min}$
 PMOS \rightarrow min sized
- from layout perspective
- 0.5
- NMOS, PMOS both min sized
- $P_{dyn} \propto C_L$
 \Rightarrow we should aim to minimize capacitance
 at output mode
- 0.5
- Also, short circuit
 current is lower if
 both are min sized!

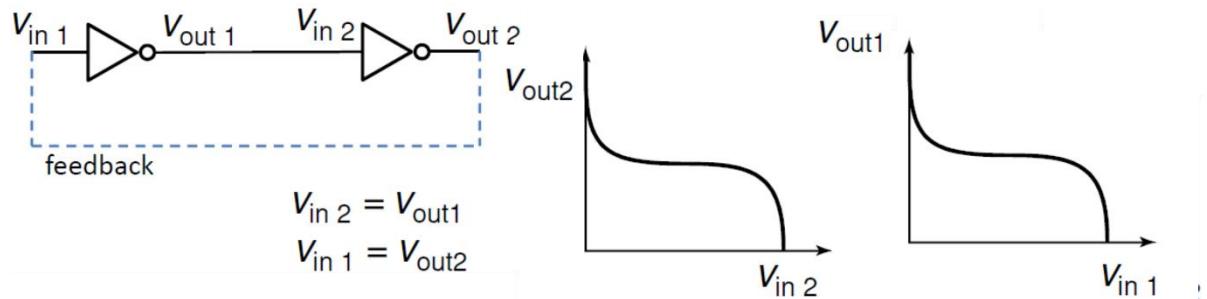
**Department of Electrical Engineering,
Indian Institute of Technology, Kanpur**

EE370A
Total Marks: 10

Mini-Quiz VII

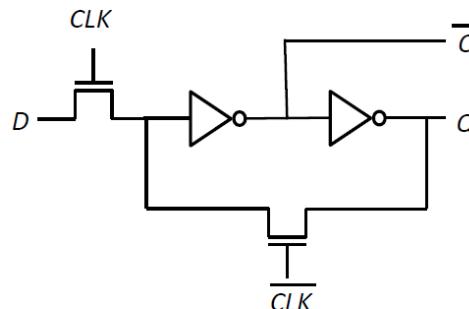
01/11/2022
Time: 20 minutes

- 1) Two inverters having VTCs as shown below have been connected so that output of inverter 2 provides feedback to the input of inverter 1. Kindly comment on the following:
 - (a) What kind of feedback does inverter 2 output provide to the input of inverter 1? **(1 mark)**
 - (b) Does this inverter circuit act like a bistable element? If yes, how? if not, why? **(2 marks)**
 - (c) Considering that $t_{p,inv1} = t_{p,inv2} = 1 \text{ ps}$, what is the minimum time duration for which an external pulse must be applied to change the state of any bistable element. **(1 mark)**



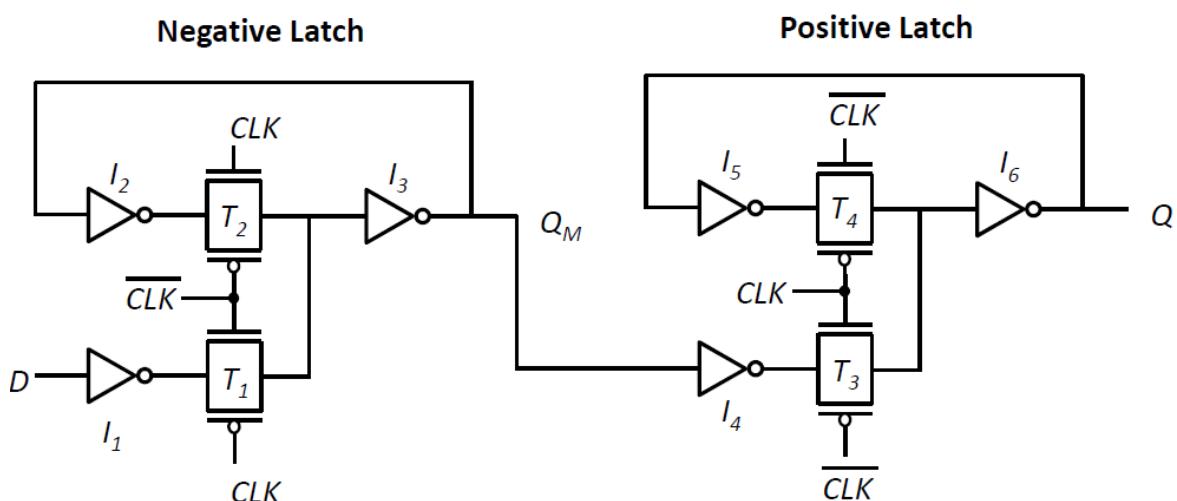
- 2) I connect the following latch with a similar latch in a master-slave configuration.

(a) What kind of latch is shown in the figure. **(1 mark)**
 (b) Does the master-slave configuration act like an edge-triggered register? **(1 mark)**
 (c) Does your answer to part (b) change if you consider clock skew (0-0 and 1-1 overlap between clk and !clk). **(2 marks)**



- Negative Latch**

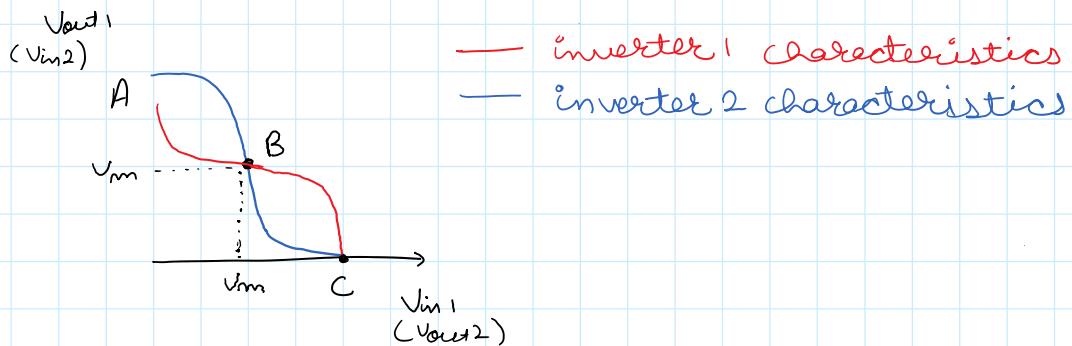
(a) What kind of latch is shown in the figure. **(1 mark)**
 (b) Does the master-slave configuration act like an edge-triggered register? **(1 mark)**
 (c) Does your answer to part (b) change if you consider clock skew (0-0 and 1-1 overlap between clk and !clk). **(2 marks)**



- 3) Find out the constraints on the 0-0 overlap and 1-1 overlap for the edge triggered register shown above. **(2 marks)**

- 1(a) The plot for V_{out} v/s V_{in} is monotonically decreasing for both inverters.

We can overlap the characteristics of in1 and in2



The characteristics have 3 points of intersection, out of which A and C are unstable, while point B is stable

- near operating point A \rightarrow +ve feedback
- near operating point C \rightarrow +ve feedback
- near operating point B \rightarrow -ve feedback

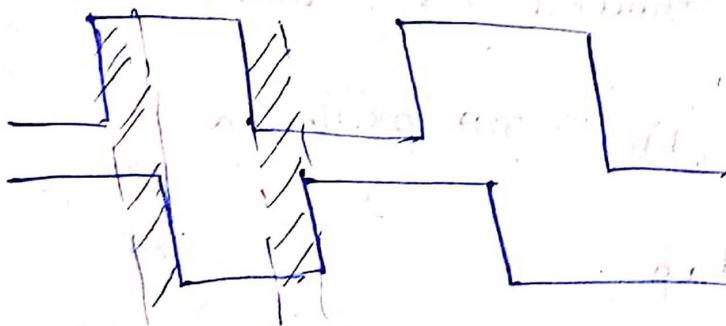
- (b) No, it does not behave like a bistable element

at operating point A, for any small increment in V_{in1} , the feedback causes it to increase further and at point C, for any small decrement in V_{in1} , the feedback causes it to reduce further

eventually, the circuit will either settle at point B or it will continue to oscillate

- (c) 2ps

- Q2
- a) +ve Latch
 - b) No, as two +ve Latch connected together does not form an edge triggered register.
 - c) No, if the duration of (0,0 and 1,1 overlap is small)



→ During (0,0) overlap both the Latch are conducting (F/F) opaque and hence holding.

→ During (1,1) overlap both the Latch are transparent and hence $Q_2 = D$
So if it is not working as edge triggered F/F.

However, during the non overlapping period of the clock, it does act like a register.

Q3) The given circuit is a true edge Triggered Flop.

→ for $(1, 1)$ overlap

Both clk & $\bar{\text{clk}}$ are conducting

so data would travel but we want after $(1, 1)$ overlap, $L_2 \rightarrow \text{Transparent}$ &

$L_1 \rightarrow \text{Opaque}$

means data should not travel to Q_m

Overlap $(1, 1)$ = no problem

for $(0, 0)$ overlap

~~But~~ But after $(0, 0)$ overlap $L_1 \rightarrow T$, $L_2 \rightarrow 0$

at overlap $(0, 0) < t_{I_1} + t_{T_{Q_1}} + t_{I_3} + t_{I_4} + t_{T_{Q_3}}$

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**Department of Electrical Engineering,
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EE370A

Mini-Quiz VIII

10/11/2022

Total Marks: 10

Time: 8 minutes

1. Which of the following statements are true?
 - (a) Cache memory is content addressable memory (CAM) array followed by SRAM array.
 - (b) L1 cache is faster than L2 cache.
 - (c) Storage block is fast, memory block is slow.
 - (d) Storage blocks are denser, memory blocks have limited capacity. **(2 marks)**
2. Which of the statements are false?
 - (a) DRAM is a memory block while SRAM is storage block.
 - (b) Hard disk is a storage block while DRAM is a memory block.
 - (c) L3 cache is composed of embedded DRAM cells.
 - (d) Storage class memory aims to fill the gap between low speed memory and high speed storage. **(2 marks)**
3. Which of the following statements are false?
 - (a) Aspect ratio of memory array does not play any role in performance of the memory block.
 - (b) Peripherals must be designed to pitch-match the memory array.
 - (c) Row decoders are required to reduce the number of address lines and interconnect lengths.
 - (d) Division of large memories into smaller blocks leads to additional peripheral circuit requirement and hence, is not a good solution to increase the speed. **(2 marks)**
4. Which of the following statements are true for SRAM?
 - (a) BL and BL_bar capacitances are due to the parasitic interconnect capacitance as well as the parasitic capacitance of the access transistors and the peripheral circuitry.
 - (b) Driving strength of nMOSFETs in inverter pairs > Driving strength of Access transistors > Driving strength of pMOSFETs in inverter pairs.
 - (c) A pull ratio of 1 is sufficient to ensure correct writing of data into SRAM cell.

(2 marks)
5. Which of the following statements are true:
 - (a) Read is non-destructive for DRAMs.
 - (b) Read is destructive for SRAMs.
 - (c) Bootstrapping allows application of exact V_{DD} at the WLs.
 - (d) DRAM is the most promising memory for control circuitry of quantum computers. **(2 marks)**

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EE370A

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10/11/2022

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