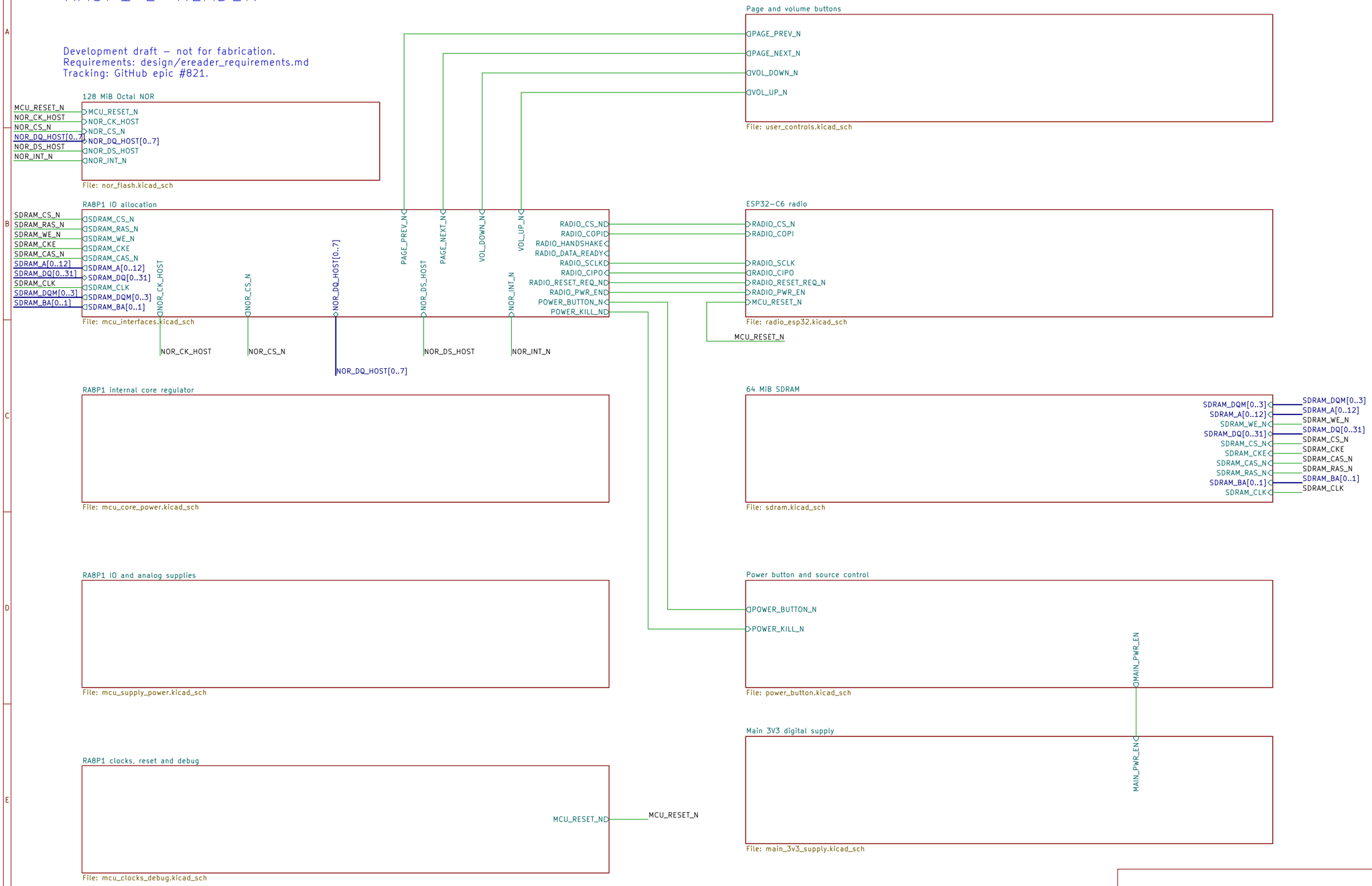
RA8P1 E-READER

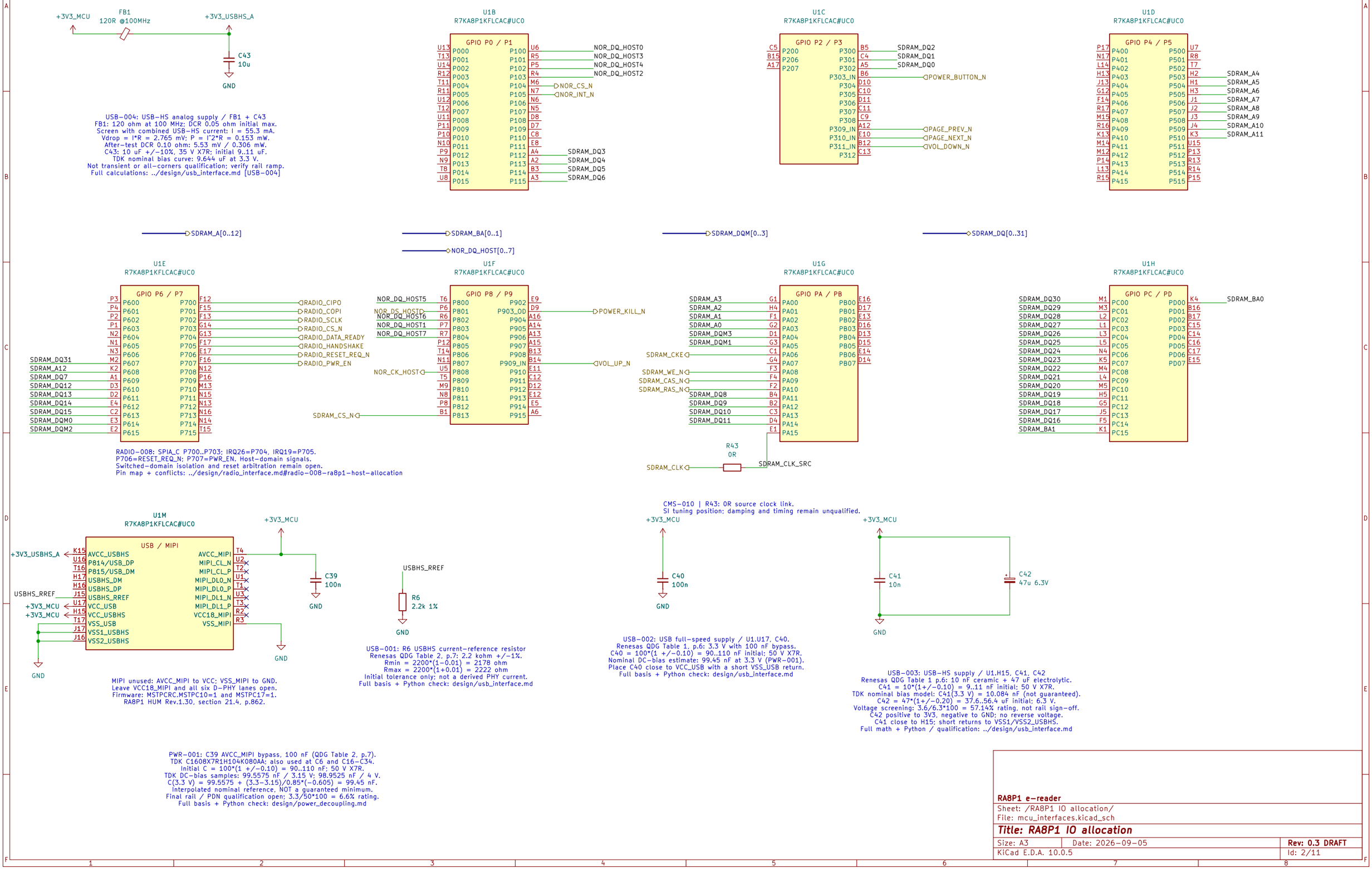
Development draft - not for fabrication.
Requirements: design/ereader_requirements.md
Tracking: GitHub epic #821.



Global supplies: +3V3_MCU and GND.
MCU_VCORE remains local to the processor core-power sheet.
Circuit notes link to the supporting engineering calculations.
Footprint and PCB qualification are deferred by scope.

Sheet: /		
File: ereader_rev1.kicad_sch		
Title: RA8P1 e-reader - schematic index		
Size: A3	Date: 2026-09-05	**Rev: 0.3 DRAFT**
KiCad E.D.A. 10.0.5		Id: 1/11

DRAFT: Existing processor units retained. Signal allocation and clocks/debug wiring are not yet complete.



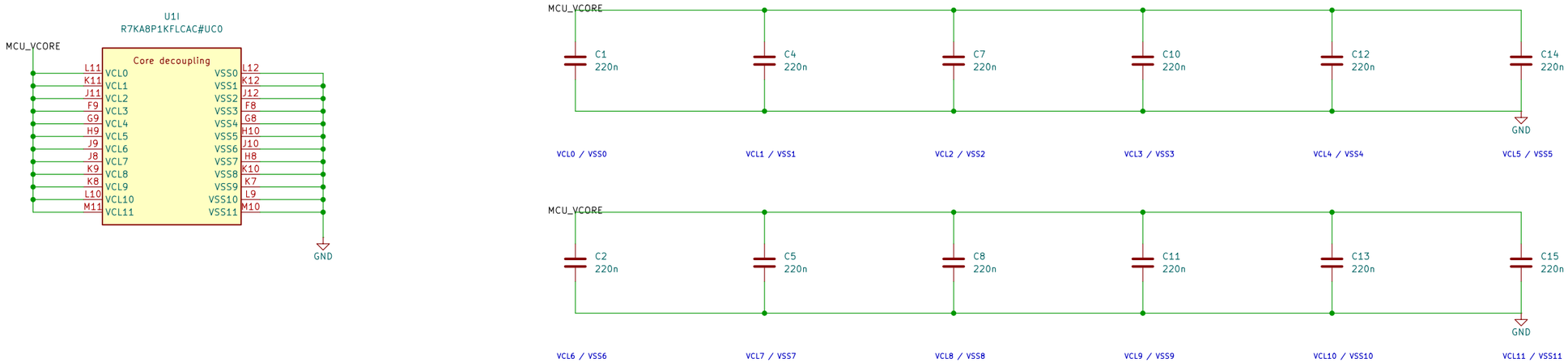
RA8P1 e-reader

Sheet: /RA8P1 IO allocation/
File: mcu_interfaces.kicad_sch

Title: RA8P1 IO allocation

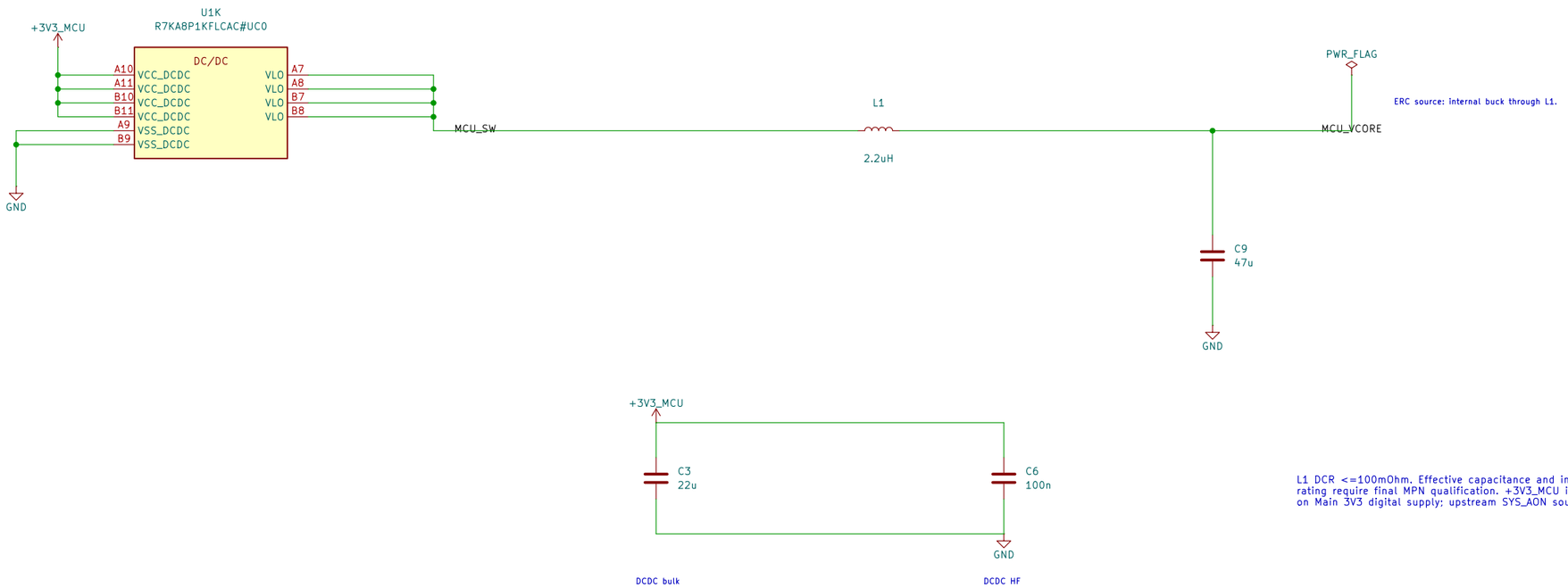
Size: A3	Date: 2026-09-05	**Rev: 0.3 DRAFT**
KiCad E.D.A. 10.0.5		Id: 2/11

CORE DECOUPLING — 220 nF AT EACH VCL / VSS PAIR



OFS2.DCDCEN = 1. All VLO balls share MCU_SW.
L1 feeds every VCL ball; never tie MCU_VCORE to 3.3 V.
C9 returns to VSS_DCDC. VCC_DCDC is tied to VCC.
HUM Rev.1.30, Table 69.2 / Fig.69.1, pp.4042–4044.

INTERNAL BUCK REGULATOR



L1 DCR <=100mOhm. Effective capacitance and inductor current rating require final MPN qualification. +3V3_MCU is supplied by U13 on Main 3V3 digital supply; upstream SYS_AON source remains open.

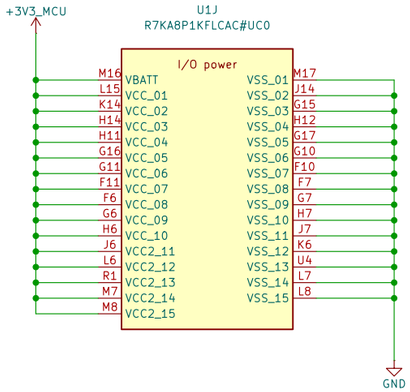
RA8P1 e-reader

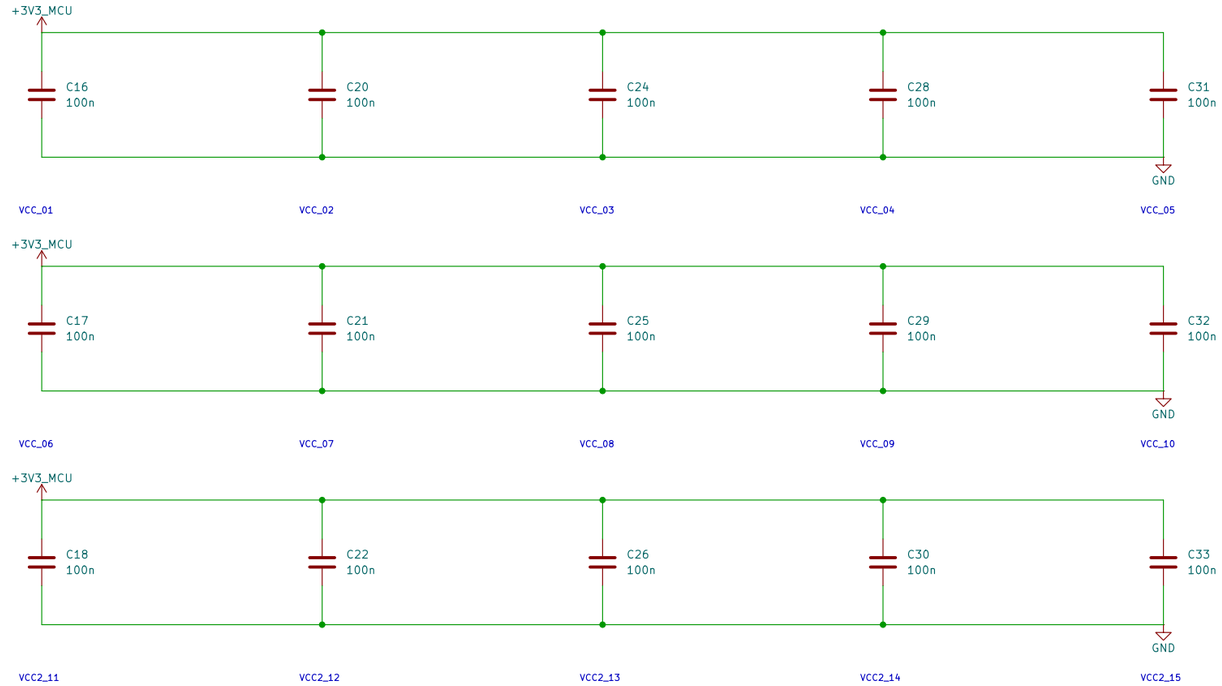
Sheet: /RA8P1 internal core regulator/
File: mcu_core_power.kicad_sch

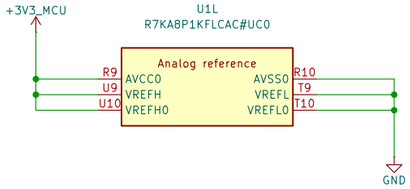
Title: RA8P1 internal core regulator

Size: A3	Date: 2026-09-05	**Rev: 0.3 DRAFT**
KiCad E.D.A. 10.0.5		Id: 3/11

I/O DECOUPLING — 100 nF AT EACH NUMBERED VCC / VSS PAIR







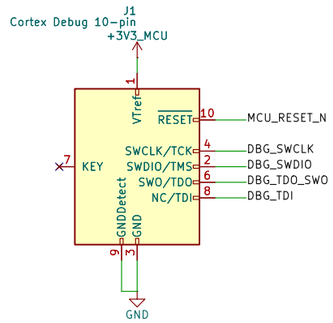
VCC and VCC2 use 3.3 V. All returns use one board ground plane.
VBATT follows the main rail; no separate backup-cell supply.
Analog references use AVCC0 / AVSS0. Place bypasses at named ball pairs.
USB/MIPI supplies remain on the interface sheet and are not yet wired.
HUM Rev.1.30: Table 69.2 p.4042; unused references: section 21.4 pp.861–862.
This is an electrical draft; capacitor MPN qualification remains open.

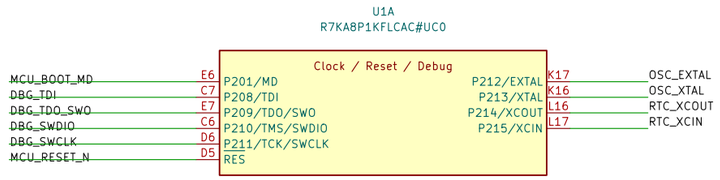
RA8P1 e-reader

Sheet: /RA8P1 IO and analog supplies/
File: mcu_supply_power.kicad_sch

Title: RA8P1 I/O and analog supplies

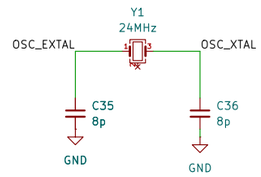
Size: A3	Date: 2026-09-05	**Rev: 0.3 DRAFT**
KiCad E.D.A. 10.0.5		Id: 4/11

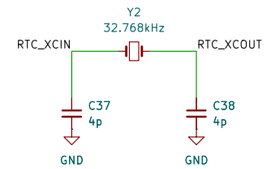


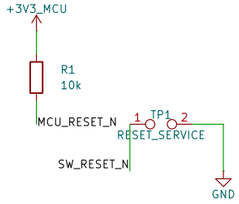


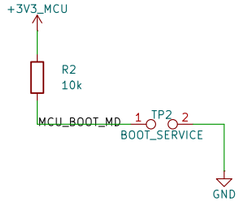
CLK-001: Y1 24 MHz / Murata XRCGB24M000F3M19R0
Crystal CL = 6 pF: effective Cstray = 2 pF ASSUMED.
CL = C35*C36/(C35+C36) + Cstray
C35 = C36 = 2*(6-2) = 8 pF (NP0, +/-0.5 pF).
Check: 8*8/(8+8) + 2 = 6 pF. At fixed stray: 5.75..6.25 pF.
Different crystal or changed parasitics: recalculate and rematch.
Initial matching only: verify frequency, startup and drive <= 300 uW.
Full derivation + Python check: ../design/clock_calculations.md

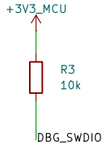
CLK-002: Y2 ABS07-LR-32.768KHZ-6-1-T
Crystal CL=6 pF; Cstray=4 pF ASSUMED.
CL=C37*C38/(C37+C38)+Cstray
C37=C38=2*(6-4)=4 pF, +/-0.25 pF NP0.
Check: 4*4/(4+4)+4=6 pF.
Fixed-stray tolerance: 5.875..6.125 pF.
Initial mode: SODRV=10b; SOSEL=0.
Qualify startup, frequency, drive <=0.5 uW.
Full math/Python: ../design/clock_calculations.md

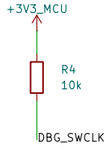


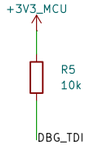


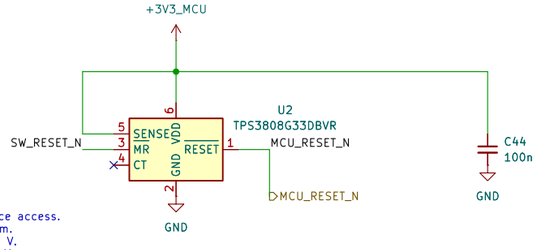












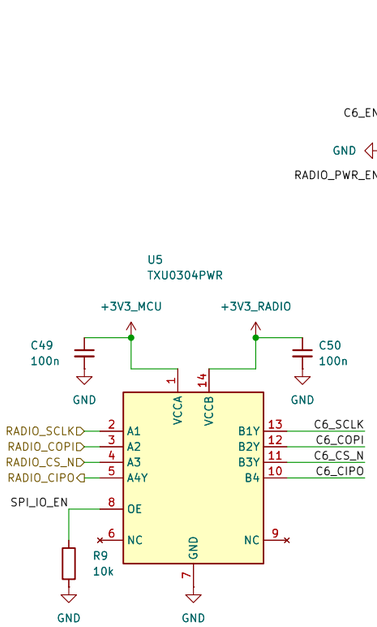
RST-001: U2 supervises +3V3_MCU; TP1 is internal MR service access.
CT open: release delay 12..28 ms; 12/2.4 = 5x MCU minimum.
Falling threshold = 3.07*(1 +/- 0.015) = 3.02395..3.11605 V.
Conservative release screen = 3.11605*1.025 = 3.19395125 V.
ASSUMED rail +/-2%: 3.3*0.98 - 3.19395125 = 40.05 mV margin.
R1 worst pull-up current = 3.6/9900 = 0.364 mA < 1 mA.
RES low margin = 0.2*3.02395 - 0.4 = 0.20479 V.
No RES capacitor; open-drain reset drivers only.
External RES startup path; do not assume internal POR flag.
Full math, limits and Python: design/boot_and_debug.md RST-001.

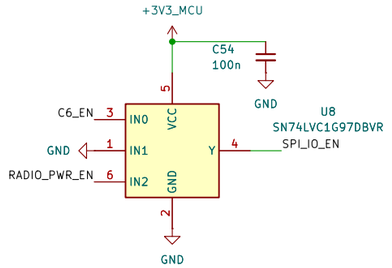
References: RA8P1 HUM Rev.1.30 sections 2.5, 4.3-4.4, 21.4.
Quick Design Guide R01AN7883EU0110 sections 2 and 6.
Reset timing: RA8P1 Datasheet Rev.1.30 Table 2.52 p.118.
Exact purchasing selections and status are maintained in the BOM.

Sheet: /RA8P1 clocks, reset and debug/
File: mcu_clocks_debug.kicad_sch

Title: RA8P1 clocks, reset and debug

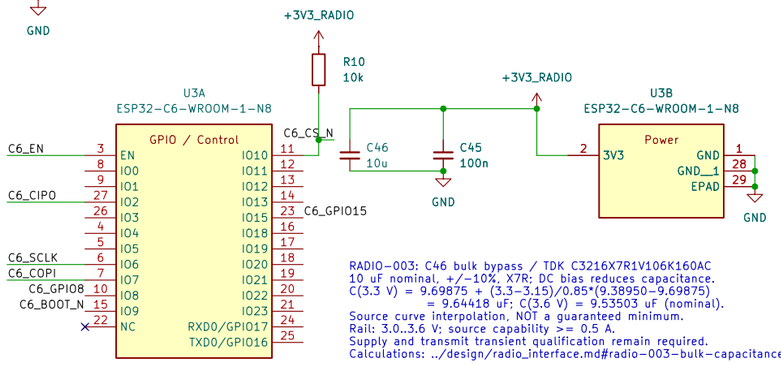
Size: A3	Date: 2026-09-05	**Rev: 0.3 DRAFT**
KiCad E.D.A. 10.0.5		Id: 5/11



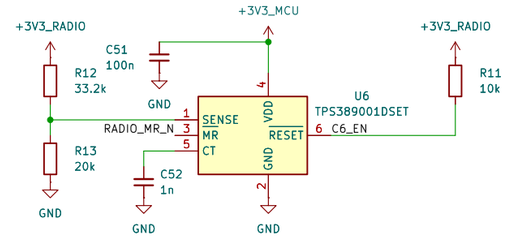


RADIO-016: SPI_IO_EN = C6_EN AND RADIO_PWR_EN
R9 bounds: 9.801k..10.201k (1%, 100ppm/K, 100K).
Ihigh <= 3.6/9801 + 12uA = 0.379309mA.
3V test-point margins: 2.4-1.92=0.48V high;
0.89-0.45=0.44V low. Full-rail sequencing OPEN.
12uA/node allocation includes U8; other loads unqualified.
Calculations: ../design/radio_interface.md#radio-016-spi-output-enable-arbitration

RADIO-012: C52 / U6 reset-release delay
C52 = 1nF +/-5% NPO, CT to GND (not VIN).
At 100 C excursion, +/-30 ppm/C: 947.15..1053.15 pF.
tnom = 1nF*1.23V/1.15uA + 25us = 1.094565 ms.
Allocate +/-10nA external CT leakage; start discharged.
tcharge_min = 947.15pF*1.17V/1.36uA = 814.828 us.
tcharge_max = 1053.15pF*1.29V/0.89uA = 1526.476 us.
Charge-only screen, NOT total reset min/max limits.
C6 requires 50us stable supply and 50us reset low.
Complete reset sequencing remains open.
Math: ../design/radio_interface.md#radio-012-supervisor-reset-release-delay

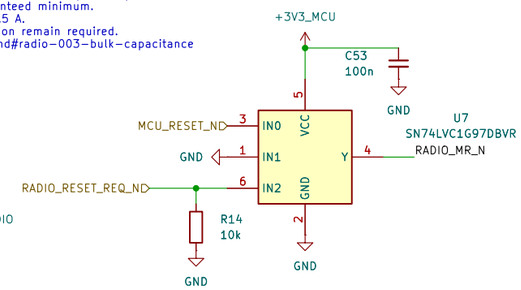


RADIO-003: C46 bulk bypass / TDK C3216X7R1V106K160AC
10 uF nominal, +/-10%, X7R; DC bias reduces capacitance.
C(3.3 V) = 9.69875 + (3.3-3.15)/0.85*(9.38950-9.69875)
= 9.64418 uF; C(3.6 V) = 9.53503 uF (nominal).
Source curve interpolation, NOT a guaranteed minimum.
Rail: 3.0..3.6 V; source capability >= 0.5 A.
Supply and transmit transient qualification remain required.
Calculations: ../design/radio_interface.md#radio-003-bulk-capacitance

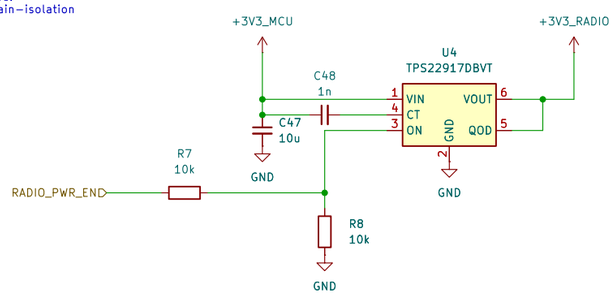


RADIO-014: R12/R13 switched-radio sense divider
33.2k / 20k; Susumu RG, 0.1%, 25ppm/C.
Allocate deltaT=100 C, 0.15% drift, +/-150nA total.
fmin/max=(1 +/-0.001)*(1 +/-0.0025)*(1 +/-0.0015)
= 0.99500774625 / 1.00500775375.
Vtrip = Vsense*(1+Rt/Rb) + Is*Rt.
Vfall >=1.15*0.99*(1+Rtmin/Rbmax)-150nA*Rtmax
= 3.004600 V; margin above 3V only 4.600mV.
Vrise <=1.15*1.01*1.00825*(1+Rtmax/Rbmin)
+150nA*Rtmax = 3.139622 V.
PWR-002 release headroom: 14.923mV, static only.
Idiv_nom=3.3/53.2k=62.030uA; each P <0.652mW.
MR arbitration and brownout dynamics remain open.
Math: ../design/radio_interface.md (RADIO-014)

RADIO-009: U5 isolates host and switched-radio signal domains.
C49/C50: 100 nF local bypass; TI TXU0304 section 12.1.
C50 adds 0.1 uF: fitted external radio capacitance = 10.2 uF nominal.
5 MHz budget: 100 - 11 - 11 = 78 ns remaining (5 pF test load).
SPI/OE and reset qualification remain open; timing is not closed.
Math: ../design/radio_interface.md#radio-009-spi-power-domain-isolation

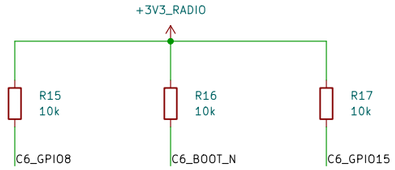


RADIO-010: R9/R10 idle-state bias, 10k 1%
Rmin/max = 10k*(1 +/-1%)*(1 +/-1%) = 9801/10201 ohm.
12 uA adverse leakage is an ALLOCATION, not measured.
R9: Vlow = 12u*10201 = 0.122412 V.
TI VT- min = 0.17 V at the 1.1 V equal-rail test point.
R10 @3.3 V: VCS >=3.177588 V > VIH 2.475 V (25 C).
R9 enabled current = 3.3/10k = 0.330 mA.
R10 draws similar current only while CS is low.
OE arbitration, all-state leakage and timing remain open.
Math: ../design/radio_interface.md#radio-010-idle-state-bias

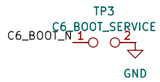


RADIO-004: U4 TPS22917DBVT / radio power gating
QOD tied to VOUT: Rdis = 150 ohm TYPICAL.
C45+C46+C50 = 0.1+10+0.1 = 10.2 uF nominal external load.
t90..10 = ln(9)*150*10.2u = 3.362 ms (ideal RC).
Not a guaranteed off-time: module C/load and VIN decay matter.
C48 connects CT to VIN, not GND; 50 V rating >=7 V required.
Reset/isolation and upstream regulator remain incomplete.
Load update: RADIO-009; device limits: RADIO-004.
Math: ../design/radio_interface.md#radio-009-spi-power-domain-isolation

PWR-002: upstream regulator / reset voltage budget
U13 TPS63802DLAR: MODE=VIN for fixed PWM.
R41/R42=56k/10k, 0.1%, 25ppm/C; deltaT=100C.
Vout=Vfb*(1+Rt/Rb)+Ib*Rt; allocate +/-100nA.
PWM static screen: 3.242044..3.358485V.
Radio: 3.242044-0.5A*0.175ohm=3.154544V.
Above U6 RADIO-014 rising screen: 14.923mV remains.
MCU reset release headroom: 48.093mV.
U13 circuit: Main 3V3 digital supply; transient qualification OPEN.
Math: ../design/power_decoupling.md PWR-002/PWR-003.



RADIO-005: C47 / U4 VIN local bypass
10 uF nominal, +/-10%, 35 V X7R; same exact TDK part as C46.
C(3.3 V) = 9.69875 + (3.3-3.15)/0.85*(9.38950-9.69875)
= 9.64418 uF nominal; NOT a guaranteed minimum.
Droop = integral(Iload-Isource)dt / Ceff + ESR/ESL effects.
TI section 11: 1 uF usually sufficient; slow sources may need more.
C47 is upstream: exclude it from C45+C46 output-discharge math.
Regulator/transient qualification required; no source flag added.
Calculations: ../design/radio_interface.md#radio-005-input-bypass



RADIO-006: R7/R8 / active-high enable, default OFF
R7 series = R8 pulldown = 10k 1%; +/-2% screening envelope.
TPS22917 ON: low <=0.35 V; high >=1.0 V.
Assume node leakage <=10 uA and host VOL<=0.5 V, VOH>=2.5 V.
Rparallel <=5.1k; divider fraction = 0.49..0.51.
Vlow <=0.5*0.51+10u*5.1k = 0.306 V <0.35 V.
Vhigh >=2.5*0.49-10u*5.1k = 1.174 V >1.0 V.
Hi-Z screen: 10u*10.2k = 0.102 V; disable host pull-up.
Host pin, all power states, leakage and timing need qualification.
Full math: ../design/radio_interface.md#radio-006-enable-divider

RADIO-013: R11 / C6_EN reset pull-up
10k 1%, 100ppm/C; deltaT=100 C allocation.
Rmin/max=10k*(1 +/-1%)*(1 +/-1%)=9801/10201 ohm.
Allocate +/-12uA total adverse node leakage.
Isink <=3.6/9801+12uA=0.379310mA <0.4mA.
U6 VOL<=0.25V at 0.4mA, VDD>=1.5V.
At C6 table point 3.3V, 25 C:
VEN>=3.3-12uA*10201=3.177588V >2.475V VIH.
VIL=0.825V; low margin=0.825-0.25=0.575V.
Pmax=3.6^2/9801=1.322314mW.
MR arbitration, power states and timing remain open.
Math: ../design/radio_interface.md (RADIO-013)

RADIO-015: U7 Schmitt-input reset arbitration
IN1=GND: Y = MCU_RESET_N AND RADIO_RESET_REQ_N.
Either low asserts U6 MR; C53 = 100nF MCU-rail bypass.
R14: Rmin/max=10k*(1 +/-1%)*(1 +/-1%)=9801/10201 ohm.
12uA adverse-current ALLOCATION: Vlow <= 0.122412 V.
At U7 3V test point: VT-_min-Vlow = 0.717588 V.
At 3.6V: I_R14 <= 0.367309 mA; P <= 1.322314 mW.
If |I_U7out|<=100uA: MR low/high margins >=0.65/0.8V
on shared 3.0-3.6V rail. MR load bound NOT yet verified.
Reset hierarchy connected; full-rail thresholds/sequencing open.
Math: ../design/radio_interface.md#radio-015-reset-request-arbitration

RADIO-007: C48 / CT slew-rate control, TDK C1608NP01H102J080AA
1nF +/-5%, 50 V NPO; CT-to-VIN, NOT CT-to-GND.
TI 3.6 V / 25 C TYPICAL table point, not guaranteed at 3.3 V:
Slew = 1900/1000 = 1.9 mV/us; tON = 3.8*1000 = 3.8 ms.
tR(10..90%) = 1.6*1000 = 1.6 ms (TI test load).
C45+C46+C50 = 10.2 uF: Icap = C*dV/dt = 19.38 mA.
Open-CT comparison: 10.2u*44mV/us = 448.8 mA (typical).
Total inrush also includes module C/load and future rail parts.
Not a current limiter or reset delay; startup qualification required.
Timing model: RADIO-007; updated load: RADIO-009.
Full math: ../design/radio_interface.md#radio-009-spi-power-domain-isolation

RADIO-017: R15/R16/R17 boot/debug strap pull-ups to switched radio rail.
Flash boot: GPIO9=1. Download: GPIO8=1, GPIO9=0; service pads TP3 (RADIO-018).
GPIO15=1 selects USB JTAG with applicable eFuses; retain straps >=3ms after EN rises.
Rmin/max=10k*(1+/-1%)*(1+/-100ppm/K*100K)=9801/10201 ohm.
At 3.3V: Vhigh>=3.3-12uA*10201=3.177588V; VIH=2.475V; margin=0.702588V.
External low-state current<=3.6/9801=0.367309mA each; P<=1.322314mW each.
12uA total/node is an allocation. Internal pull-up sink current and full-state timing OPEN.
Math: ../design/radio_interface.md#radio-017-boot-and-debug-strap-bias

RADIO-018: TP3 internal C6 BOOT service pads; no fitted switch.
Fixture shorts pad 1 (GPIO9) to pad 2 (GND); GPIO8 must be high.
Hold GPIO9 low before C6_EN rises and >=3ms after C6_EN rises.
R16 external current <=3.6/9801=0.367309mA; add internal pull-up.
Fixture ALLOCATION: total sink <=1mA and path <=1ohm => Vlow<=1mV.
At 3.3V: low margin=0.25*3.3-0.001=0.824V (screen only).
Host-independent radio power/reset arbitration remains to be connected.
Math: ../design/radio_interface.md#radio-018-internal-boot-service-pads

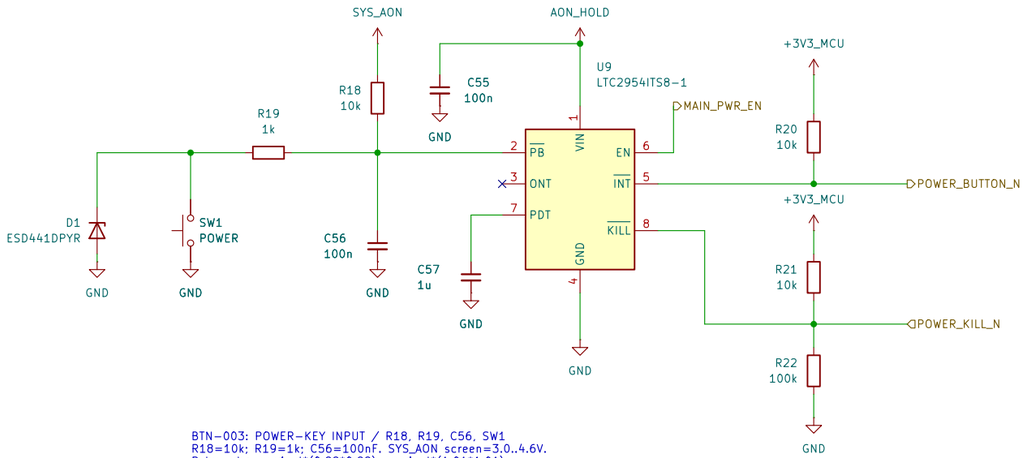
Incomplete electrical design - not for manufacture

Sheet: /ESP32-C6 radio/
File: radio_esp32.kicad_sch

Title: ESP32-C6 radio

Size: A3	Date: 2026-09-05	Rev: DRAFT
KiCad E.D.A. 10.0.5		Id: 6/11

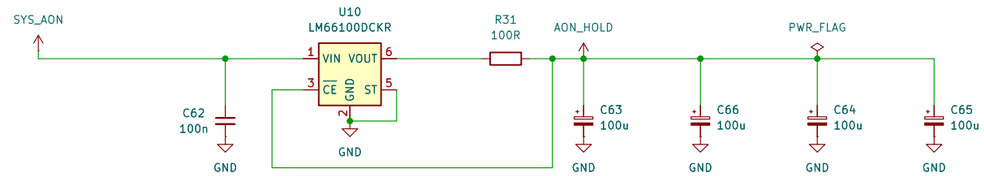
INCOMPLETE POWER CONTROL — NOT FOR FABRICATION
PB, INT, KILL, held supply and source supervisor are connected.
U12/Q1/Q2 provide fault KILL clamp and main-rail discharge.
MAIN_PWR_EN now controls U13 on Main 3V3 digital supply.
SYS_AON source and USB permission-latch clear remain to be built.
Power-control operation is not yet complete or qualified.
Engineering: ../design/system_power_design.md SYS-007;
converter math: ../design/power_decoupling.md PWR-002/PWR-003.



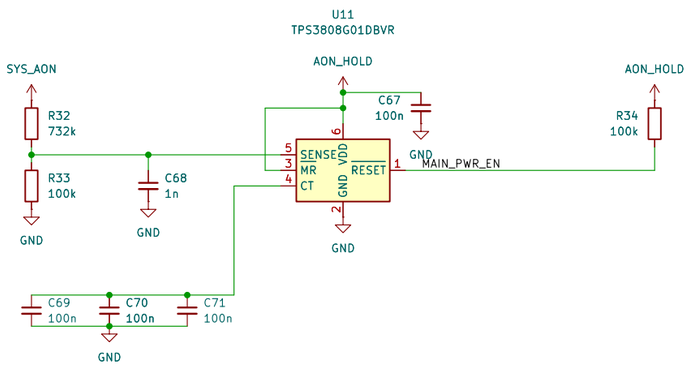
BTN-003: POWER-KEY INPUT / R18, R19, C56, SW1
R18=10k; R19=1k; C56=100nF. SYS_AON screen=3.0..4.6V.
R bounds: nominal*(0.99*0.99)..nominal*(1.01*1.01).
At PB=0.6V: Isource<=(4.6-0.6)/9801 + 15uA + 12uA
<435.13uA; Isink=0.6/(1020.1+0.5)>587.88uA.
Thus the closed switch pulls PB below its 0.6V falling threshold.
Min contact current=3/(10201+1020.1+0.5)-12uA>255.34uA.
Open contact>=2.87748V; SW1 minimum rating=10uA at 2V.
C56 discharge peak<=4.6/980.1<4.694mA < SW1 50mA rating.
12uA is a leakage ALLOCATION; ESD/transient validation required.
Full derivation + Python: ../design/single_button_power.md BTN-003/005/010.

BTN-004: HARDWARE FORCED-OFF TIMING / C57
C57=1uF; TDK C2012X7R1E105K125AB, 25V X7R +/-10%.
C[uF]=1.56e-4*(t_added[ms]-1).
t_force,nom=64ms + 1ms + 1/1.56e-4=6475.256ms (6.48s).
C tolerance/temp only: 1*0.90*0.85=0.765uF;
1*1.10*1.15=1.265uF -> 4.969..8.174s using NOMINAL IC equation.
Not guaranteed timing: excludes IC spread, DC bias, aging, leakage.
ONT intentionally open: internal turn-on debounce=26..41ms.
Release the initial ON press; after forced off, release then press again.
Full calculation + Python: ../design/single_button_power.md BTN-004/005.

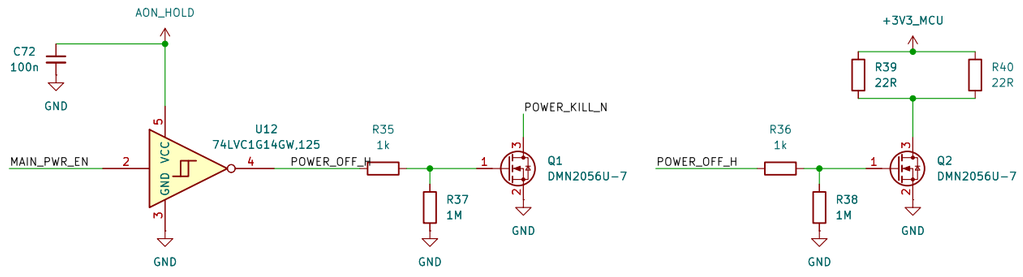
ERC supply path: U10 VOUT through R31.
PWR_FLAG declares that series-fed source only;
raw SYS_AON source remains unimplemented.



SYS-007 REVISED: HELD SUPPLY / U10, R31, C62-C66
C63-C66: 4 x 100uF/10V; Cmin=400uF*0.9^3=291.6uF.
VIN=raw SYS; VOUT->R31->reservoir; CE senses reservoir.
Icontrol<=1.125mA incl 500uA bank leakage allocation.
Pre-trip reverse: 80mV/98.01ohm<0.817mA. Itotal=1.942mA.
Vinitial=3.263705831-max(0.250,0.001125*102.24)
=3.013705831V (threshold OR resistive-drop limit).
t_hold=[291.6uF*(3.013705831-2.7)V-1uC]/1.942mA
=46.589ms >38.380ms shutdown allocation.
1uC covers initial undershoot + reverse/gate transitions.
Qualify VIN=0..4.6V, slow/floating-source collapse and load.
R31 short: 4.6^2/98.01<0.216W; 1W nominal rating.
Control only: no MCU/audio/display loads on AON_HOLD.
Full assumptions and Python: ../design/system_power_design.md SYS-007.



SYS-007: SOURCE SUPERVISION / U11, R32-R34, C67-C71
Vtrip=Vref*(1+R32/R33)+Isense*R32.
Nominal=0.405*(1+732k/100k)=3.369600V.
Vref +/-2%, Isense +/-25nA; each R +/-0.1%, 25ppm/C, 100C.
Corner trip=3.263705831..3.476597632V.
C68: tau=(732k||100k)*1n=87.980769us (nominal).
C69-C71: 3x100n C0G; initial/temp=284.145..316.827nF.
CT delay=300/175+0.0005=1.714786s nominal.
0.6*(284.145/175+0.0005)=0.974511s MODEL, not guarantee.
Require qualified reset hold >=0.90s >650ms KILL blank +10ms.
R34: ENhigh>=2.7-3uA*(100k*1.01*1.01)=2.393970V.
ENlow<=0.4V; TPS63802 thresholds 1.13V rise/0.97V fall.
U12/Q1/Q2 implement shutdown; USB latch-clear branch still needed.
Full math, Python and qualification: ../design/system_power_design.md SYS-007.

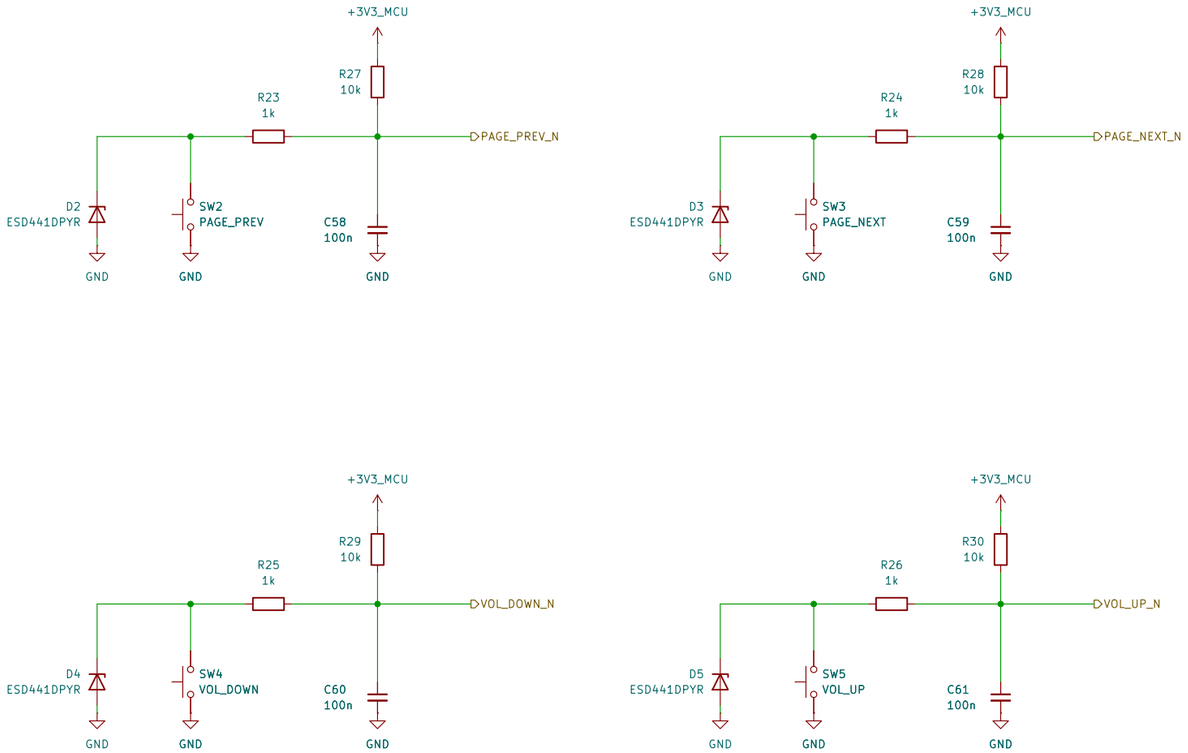


SYS-007: SHUTDOWN / U12, Q1-Q2, R35-R40, C72
POWER_OFF_H=NOT(MAIN_PWR_EN); held-domain VCC=2.7..4.6V.
R35/R36=1k; R37/R38=1M; 1% + 100ppm/C over 100C.
3-gate peak<=3*4.6/(1000*0.99^2)=14.080196mA <50mA.
Includes future USB-clear gate; static<=17.080196uA <100uA.
VGSmin=(2.6-1020.1*1uA)/(1+1020.1/980100)=2.596278V.
1uA per gate/board leakage is a qualification allocation.
R39||R40 + Q2: Rmax=22*1.01^2/2+0.2=11.4211ohm.
For Cmain<=1mF: t=R*C*ln(3.6/0.3)=28.380367ms.
Total<=10+28.380367=38.380367ms <46.589ms held supply.
Each 22R: P<=3.6^2/(22*0.99^2)=0.601052W; 1W at 70C.
Qualify 0.2ohm FET, 10ms TOTAL response, derating and backfeed.
Gate/transient charge shares the existing 1uC reserve.
Full assumptions, Python and tests: ../design/system_power_design.md SYS-007.

Sheet: /Power button and source control/
File: power_button.kicad_sch

Title: RA8P1 E-reader — power button and source control

Size: A3	Date: 2026-09-07	Rev: 0.3 DRAFT
KiCad E.D.A. 10.0.5		Id: 7/11



CMS-009 - FOUR INDEPENDENT PAGE / VOLUME KEYS
SW2..SW5: R23..R26=1k; R27..R30=10k; C58..C61=100n.
D2..D5: ESD441DPYR, IO1 / GND2, before series resistors.
VCC=+3V3_MCU: 3.0..3.6V screening envelope.
Resistors: +/-1%, plus +/-100ppm/C over 100C.
RPU=10k*(0.99^2..1.01^2)=9801..10201 ohm.
RS=1k*(0.99^2..1.01^2)=980.1..1020.1 ohm.
Contact <=0.5 ohm; adverse leakage allocation=2.2uA/key:
1uA MCU +0.1uA TVS +0.1uA capacitor +1uA board.
Capacitor and board leakage terms are design allowances.

VLOW=(VCC/RPU+Ileak)/(1/RPU+1/(RS+Rcontact)).
Worst screened VLOW<0.342V; correlated VIL margin>0.315V.
VHIGH>=3-2.2uA*10201=2.9776578V; VIH margin>0.57755V.
Icontact>=3/(10201+1020.6)-2.2uA >265.14uA.
Open contact>2.97745V; switch minimum load=10uA at 2V.
Peak capacitor discharge<3.6/980.1=3.674mA (<50mA).
Four keys held: 4*(3.6/(9801+980.1)+2.2uA)<1.345mA.

Full derivation, corner enumeration and verified Python:
../design/camera_storage_interfaces.md CMS-009.

CMS-009 - FILTER TIMING AND BUTTON BEHAVIOR
C58..C61: TDK C1608X7R1H104K080AA, 100nF, X7R, 50V.
Tolerance / temperature-only capacitance bounds:
Cmin=100n*0.90*0.85=76.5nF; Cmax=100n*1.10*1.15=126.5nF.
DC bias and aging excluded; qualify effective capacitance.

Nominal tau_assert=(10k||1k)*100n=0.090909ms.
t_assert=-tau_assert*ln[(0.2-1/11)/(1-1/11)]=0.193ms.
t_release=-10k*100n*ln[(1-0.8)/(1-1/11)]=1.514ms.
RC filters noise; it does NOT provide complete debounce.
Require 20ms continuously stable state; switch bounce<=10ms.
IRQ starts wake/debounce, not an immediate page/volume action.

Opposing page or volume keys cancel their associated action.
Ignore boot-held ordinary actions until release; no auto-repeat
from a stuck key. Disable MCU internal pulls.
In hard-off, these four keys cannot start power.
The separate POWER switch controls hardware start/forced-off.
ESD441 is not a 3.3V clamp; residual MCU voltage, series
resistor pulse stress and ESD current return need physical tests.

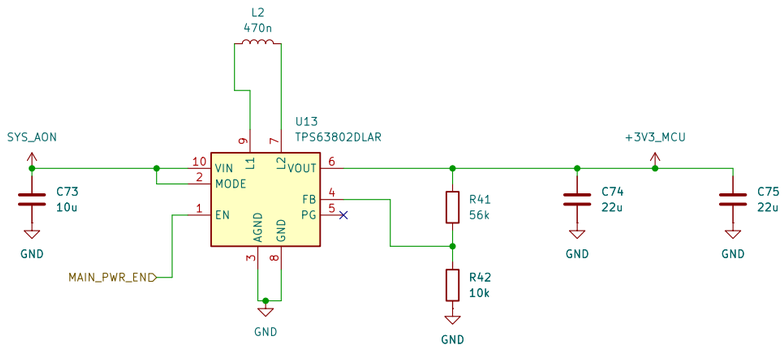
Full corner calculations, Python and wake-register contract:
../design/camera_storage_interfaces.md CMS-009.

Sheet: /Page and volume buttons/
File: user_controls.kicad_sch

Title: RA8P1 E-reader - page and volume buttons

Size: A3	Date: 2026-09-07	**Rev: 0.3 DRAFT**
KiCad E.D.A. 10.0.5		Id: 8/11

MAIN DIGITAL 3.3 V SUPPLY
TPS63802 buck-boost; hardware-controlled enable; fixed PWM.
Engineering draft: upstream source and corner qualification remain open.



PWR-002 / PWR-003: SETPOINT AND LOCAL COMPONENTS
U13 TPS63802DLAR; MODE=VIN, fixed PWM.
R41=56k; R42=10k; each +/-0.1%, 25ppm/C.
Vnom=0.500*(1+56k/10k)=3.300V.
Idivider=3.300/(56k+10k)=50uA.
For 100C resistor-temperature change:
fLo=0.999*0.9975=0.9965025; fHi=1.001*1.0025=1.0035025.
Vmin=0.495*(1+56k*fLo/(10k*fHi))-100nA*56k*fHi
=3.242044V.
Vmax=0.505*(1+56k*fHi/(10k*fLo))+100nA*56k*fHi
=3.358485V.
Static screen only; ripple, load steps and drift still require validation.

C73: CIN_model=10u*0.90*0.85*0.60=4.590uF >=4uF.
C74+C75: COUT_model=2*22u*0.90*0.85*0.60=20.196uF >=7uF.
0.90=tolerance; 0.85=X7R temperature; 0.60=residual ALLOCATION.
Qualify bias, aging, excitation and assembly; 60% is not guaranteed.
L2: 0.47uH +/-20% gives 0.376..0.564uH INITIAL only.
Required installed effective L=0.37..0.57uH; bias/reflow/hot tests OPEN.

TI SLVSEU9D Table 7-1, sections 9.4/10.2; exact parts in native BOM.
Full derivation, primary sources and executable Python:
../design/power_decoupling.md PWR-002/PWR-003.

PWR-003: LOAD, SOURCE AND STARTUP ACCEPTANCE LIMITS
Main continuous allocation: 0.750 MCU + 0.500 radio
+ 0.250 SDRAM + 0.250 NOR + 0.050 logic = 1.800A.
These are qualification allocations, not measured maximum currents.
SD, camera, audio, display/touch/frontlight need separate SYS supplies.

Pout=3.358485094*1.80=6.045273W.
VIN>=3.20V allocation; raw trip min=3.263705831V.
Allowed raw-to-VIN loss=3.263705831-3.20=63.705831mV.
At ASSUMED eta=85%: Iin=Pout/(eta*3.20)=2.222527A.
Ploss=Pout*(1/eta-1)=1.066813W.
Reference rise=Ploss*81C/W=86.411846C; NOT enclosure prediction.
Verify hot current capability and junction temperature <125C with margin.

Cold subtotal, RADIO OFF: 1.330 DCDC + 0.550 other = 1.880A.
Radio on would give 2.380A > nominal 2A; keep radio OFF through start/wake.
Largest wake-reference subtotal=1.270+0.550=1.820A.
DCDC figures are reference-only; non-DCDC start and extra charging excluded.
Additional charging: I=Cadditional*dV/dt; qualify the actual ramp.
Total directly connected main-rail C <=1mF for SYS-007 discharge budget.
No externally driven +3V3_MCU: forced PWM can sink reverse current.

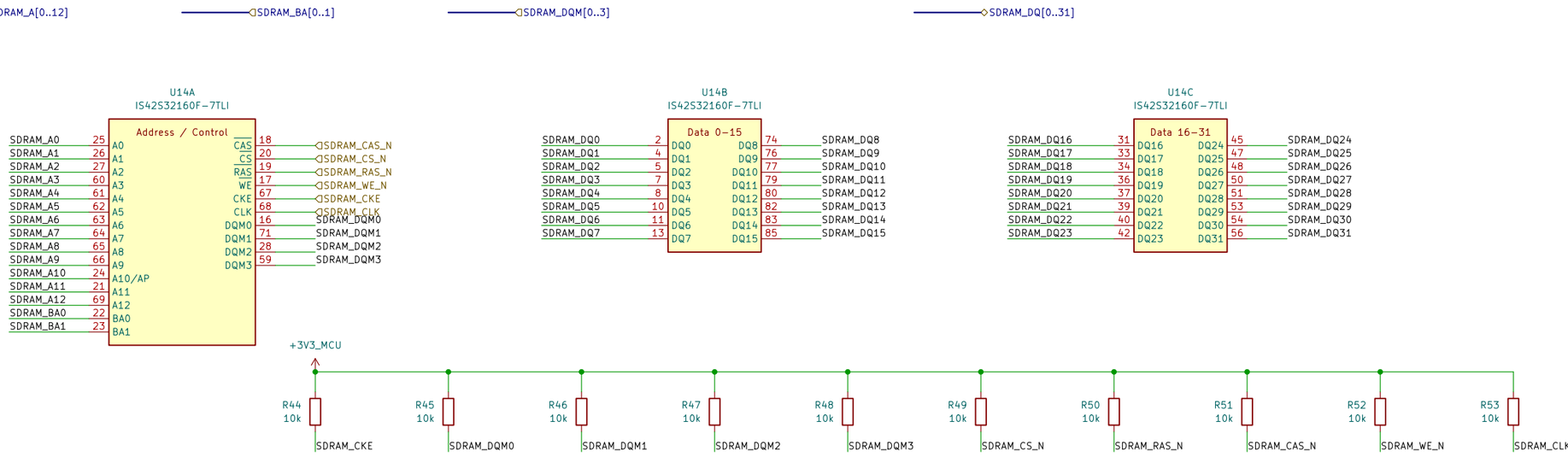
PWR-002 static release margin: radio 14.922537mV; MCU 48.092861mV.
Ripple, startup and transients must fit; no fabrication release.
Full sources, derivation and Python: ../design/power_decoupling.md PWR-003;
source-loss shutdown: ../design/system_power_design.md SYS-007.

Sheet: /Main 3V3 digital supply/
File: main_3v3_supply.kicad_sch

Title: RA8P1 E-reader - main digital 3.3 V supply

Size: A3	Date: 2026-09-08	Rev: 0.3 DRAFT
KiCad E.D.A. 10.0.5		Id: 9/11

64 MiB SDRAM | ISSI IS42S32160F-7TLI
Signal and reset-default circuits | CMS-010.
Startup, SI/timing and hardware qualification remain open.



CMS-010 | SDRAM power and bypass
VDD and VDDQ share +3V3_MCU (3.0 to 3.6 V).
C76–C79: 4 x 100 nF for the four VDD pins.
C80–C87: 8 x 100 nF for the eight VDDQ pins.
C88: 10 uF local bulk; Cnom = 12 x 0.1 + 10 = 11.2 uF.
Included in the PWR-003 1 mF whole-rail limit.
Effective C, placement and PDN impedance require qualification.

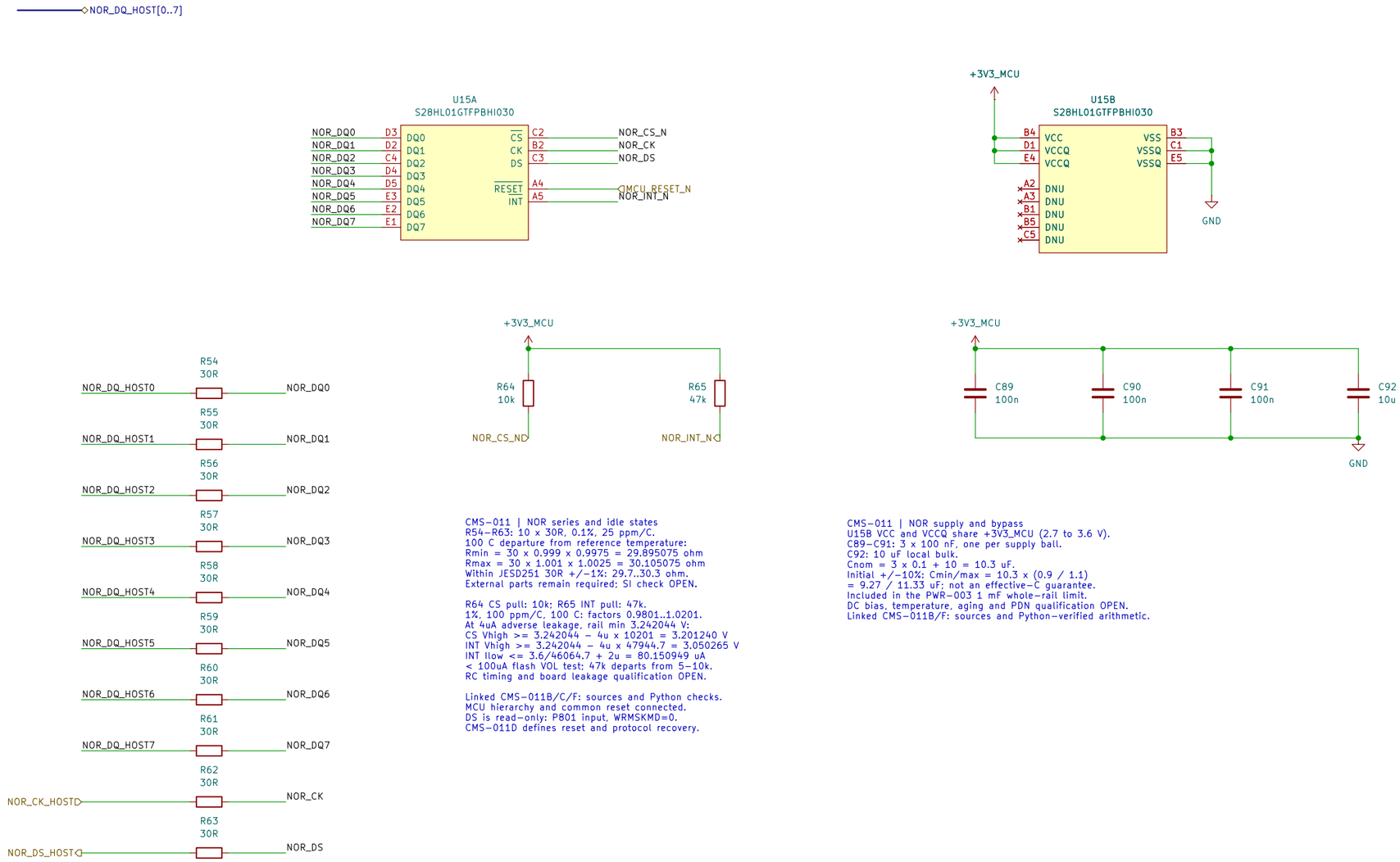
CMS-010 | R44–R53: 10k reset defaults
Rail 3.0..3.6V; +/-1%, 100ppm/C, |dT|<=100C.
Rmin=10k*0.99*0.99=9801 ohm.
Rmax=10k*1.01*1.01=10201 ohm.
Ioff=5uA SDRAM+1uA MCU+1uA board=7uA.
VHIGHmin=3.0-7uA*10201=2.928593V (>2.0V VIH).
Board leakage and temperature screen require qualification.

CMS-010 | Pull load and power states
Sink leakage: 5uA SDRAM+1uA board=6uA.
Isink=3.6/9801+6uA=0.373309mA (<0.374mA).
Pmax=3.6^2/9801=1.322314mW per pull.
All ten LOW: 10*3.6/9801=3.673095mA rail;
10*3.6^2/9801=13.223140mW resistor heat.
Reserve 4mA within the 250mA SDRAM allocation.
CKE/DQM and CS_N default HIGH; CLK HIGH is not a clock.
Switched-rail pulls; self-refresh actively holds CKE LOW.
Startup, dynamic I/O, SI and shutdown qualification OPEN.

Sheet: /64 MiB SDRAM/
File: sdram.kicad_sch

Title: RA8P1 E-reader – 64 MiB SDRAM

Size: A3	Date: 2026-09-08	Rev: 0.3 DRAFT
KiCad E.D.A. 10.0.5		Id: 10/11



CMS-011 | NOR series and idle states
R54-R63: 10 x 30R, 0.1%, 25 ppm/C.
100 C departure from reference temperature:
Rmin = 30 x 0.999 x 0.9975 = 29.895075 ohm
Rmax = 30 x 1.001 x 1.0025 = 30.105075 ohm
Within JESD251 30R +/-1%: 29.7..30.3 ohm.
External parts remain required; SI check OPEN.

R64 CS pull: 10k; R65 INT pull: 47k.
1%, 100 ppm/C, 100 C: factors 0.9801..1.0201.
At 4uA adverse leakage, rail min 3.242044 V:
CS Vhigh >= 3.242044 - 4u x 10201 = 3.201240 V
INT Vhigh >= 3.242044 - 4u x 47944.7 = 3.050265 V
INT Ilow <= 3.6/46064.7 + 2u = 80.150949 uA
< 100uA flash VOL test; 47k departs from 5-10k.
RC timing and board leakage qualification OPEN.

Linked CMS-011B/C/F: sources and Python checks.
MCU hierarchy and common reset connected.
DS is read-only: P801 input, WRMSKMD=0.
CMS-011D defines reset and protocol recovery.

CMS-011 | NOR supply and bypass
U15B VCC and VCCQ share +3V3_MCU (2.7 to 3.6 V).
C89-C91: 3 x 100 nF, one per supply ball.
C92: 10 uF local bulk.
Cnom = 3 x 0.1 + 10 = 10.3 uF.
Initial +/-10%: Cmin/max = 10.3 x (0.9 / 1.1)
= 9.27 / 11.33 uF; not an effective-C guarantee.
Included in the PWR-003 1 mF whole-rail limit.
DC bias, temperature, aging and PDN qualification OPEN.
Linked CMS-011B/F: sources and Python-verified arithmetic.

Sheet: /128 MiB Octal NOR/
File: nor_flash.kicad_sch

Title: RA8P1 E-reader - 128 MiB Octal NOR

Size: A3	Date: 2026-09-08	**Rev: 0.3 DRAFT**
KiCad E.D.A. 10.0.5		Id: 11/11