# Bharat Singhal

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## Research Interests

- My research interests lie primarily in the area of control theory, optimization, network science, and nonlinear dynamics. Specifically, I apply tools from control theory and optimization to understand complex networks of nonlinear units and effectively regulate their collective behavior.

## Education

### Ph.D. in Systems Science and Mathematics

*Exp. May'25*

Washington University in St. Louis, Missouri

- GPA 3.98/4.0, Advisor: Jr-Shin Li

### M.Tech. in Control System Engineering

*July'16-June'17*

Indian Institute of Technology Kharagpur, India **(IIT-Kharagpur)**

- GPA 8.85/10, Advisor: Siddhartha Mukhopadhyay

### B.Tech. (Honours) in Electrical Engineering

*July'12-June'16*

Indian Institute of Technology Kharagpur, India **(IIT-Kharagpur)**

- GPA 8.85/10

## Publications

**Accepted:**

- **Bharat Singhal**, Minh Vu, Shen Zeng, and Jr-Shin Li. "An Iterative Approach to Optimal Control Design for Oscillator Networks." In 2023 American Control Conference (ACC), pp. 3466-3471. IEEE, 2023.
- **Bharat Singhal**, Minh Vu, Shen Zeng, and Jr-Shin Li. "A Data-efficient Framework for Inference of Nonlinear Oscillator Networks." IFAC-PapersOnLine 56, no. 2 (2023): 10089-10094.
- **Bharat Singhal**, István Z. Kiss, and Jr-Shin Li. "Optimal phase-selective entrainment of heterogeneous oscillator ensembles." SIAM Journal on Applied Dynamical Systems 22, no. 3 (2023): 2180-2205.
- Walter Bomela, **Bharat Singhal**, and Jr-Shin Li. "Engineering Spatiotemporal Patterns: Information Encoding, Processing, and Controllability in Oscillator Ensembles." Biomedical Physics & Engineering Express, vol. 9, no. 4, p. 045033, 2023.
- Walter Bomela, Michael Sebek, Raphael Nagao **Bharat Singhal**, István Z. Kiss, and Jr-Shin Li. "Finding influential nodes in networks using pinning control: Centrality measures confirmed with electrochemical oscillators." Chaos: An Interdisciplinary Journal of Nonlinear Science 33, no. 9 (2023).
- Minh Vu, **Bharat Singhal**, Jr-Shin Li, and Shen Zeng. "Data-driven moment-based control of linear ensemble systems." (Accepted for ACC 2024)

**In-Submission:**

- Minh Vu*, **Bharat Singhal***, Shen Zeng, and Jr-Shin Li. "Data-Driven Control of Neuronal Networks with Population-Level Measurement" (Under review at Chaos; *: equal contribution)
- **Bharat Singhal**, ShiCheng Li, and Jr-Shin Li. "Decoding Network Interactions from Time Series Data: A Model-Free Iterative Approach." (Under review at chaos)
- **Bharat Singhal**, Jorge Luis Ocampo-Espindola, K. L. Nikhil, Erik D. Herzog, István Z. Kiss, and Jr-Shin Li. "Uncertainty Quantification of Network Inference with Data Sufficiency." (Under review at IEEE Transactions on Network Science & Engineering)

## Research Experience

### Graduate Research Assistant

*Sep. 2020 - Present*

Applied Mathematics Lab, Washington University in St. Louis

- Understanding how neuron connectivity influences the behavior of populations as a whole, as well as how to harness the connectivity structure for effective regulation, which is essential to neuroscience and circadian biology.
- Developing data-driven protocols to decode the connectivity structure of complex networks and predict the collective dynamics.
- Designing fast entrainment protocols for the heterogeneous nonlinear oscillators.

## Professional Experience

### Taiwan Semiconductor Manufacturing Company (TSMC)

*Oct. 2017-Sep. 2020*

Research Engineer (RC interconnect modeling for sub 10nm CMOS technology nodes) *Hsinchu, Taiwan*

- Worked on Integrating different SOC designs like ASIC on ASIC (AOA), system on integrated chip (SOIC), and wafer on wafer (WOW) to implement 3D-IC RC tech files for 7nm and 12nm nodes.
- Provided a comprehensive Gate resistance model to reduce silicon to simulation gap when multiple vias land on gate-poly by analyzing multiple resistance network combinations for 5nm finfet.
- Modeling of various RC features like Cfi tables to compensate for gate-to-drain and gate-to-source capacitance, damage-based dielectric constant, and marker layers by anatomizing silicon data for 5nm and 7nm nodes.

### Altisource Business Solutions

*May 2015-July 2015*

Intern, Business Analyst *Bangalore, India*

- Designed and implemented the front end for Vresolve, Altisource's web-based mortgage collection platform which resulted in increased efficiency of company's mortgage collection.

## Research Projects

### Modeling and Control of an Anti-lock Braking System in Hybrid Electric Vehicles

*July 2016 - May 2017*

Master's thesis, Department of Electrical Engineering, IIT Kharagpur

- Developed a complete four-wheel vehicle model for its longitudinal motion and implemented a sliding mode controller to prevent wheel lock-out and minimize stopping distance.
- Designed a controller to maximize the amount of regenerative energy, in case of braking, while maintaining stopping distance for hybrid vehicles.

### Speed Control of E-bikes Based on User-Customized Assistance Level

*July 2015 - April 2016*

Bachelor's project, Department of Electrical Engineering, IIT Kharagpur

- Built a Simulink model of a three-phase star-connected BLDC motor using state space and implemented a PI controller to regulate the speed oof motor as per assistance level
- Simulated dynamics of a bicycle from the force on pedals, through the transmission system, to wheels in Simulink.

### Online Monitoring System for Overhead Equipment Traction Parameter Measurement

*May 2014 - June 2014*

Summer Research Project, Department of Electrical Engineering, IIT Kharagpur

- Implemented image segmentation and blob detection algorithm using real-time image processing software (Sapera APF) for non-contact measurement of dynamic conditions of overhead equipment synchronized with position obtained via GPS.

## Teaching Experience

### Control and Instrumentation Laboratory

*Fall 2016*

Department of Electrical Engineering, IIT Kharagpur

- Guided 35, 3rd-year undergraduate, students through laboratory experiments and helped them to understand the theory behind the experiment.

### Embedded Systems Laboratory

*Spring 2016*

Department of Electrical Engineering, IIT Kharagpur

- Taught assembly language programming for AVR ATmega32 microcontroller and helped 40 students to implement keyboard, LCD, and ADC interface.

### Optimization

*Fall 2021 & 2022*

Department of Electrical & Systems Engineering, Washington University

- Taught optimization algorithms, such as Gradient Descent, Newton's method, and Conjugate Gradient method, to a class of 70 undergraduate students.

## Technical Skills

**Languages**, C, C++, R, Python, Matlab

**Libraries**, NumPy, pandas, Matplotlib, Tensorflow, Keras, scikit-learn,

**EDA Tools**, StarRC, Calibre, Hspice, Cadence Virtuoso