Seungmin Baek

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Profile

My research primarily centers on DRAM microarchitecture, including efforts to reverse-engineer internal structures and operations. I also work on reliability, such as analyzing DRAM error characteristics, and security, with a particular focus on RowHammer attacks. In addition, I am interested in improving memory system performance. More recently, my work has focused on optimizing memory systems for large language model (LLM) workloads.

Education

Ph.D | ***Intelligence & Information Convergence*** — Mar. 2023 – Present
Seoul National University — Seoul, South Korea

B.S. | ***Electrical & Electronic Engineering*** — Mar. 2017 – Feb. 2023
Korea University — Seoul, South Korea

Research Experience

Graduate research assistant — Mar. 2023 – Present
Scalable Computer Architecture Laboratory, Seoul National University — Seoul, South Korea

- Reverse-engineering DRAM internal structure and analyzing error characteristics using an FPGA.
- RowHammer attack via a DRAM structural anomaly through corrupting a page table.
- Reverse-engineering DRAM address mapping using a software-only tool.
- Analysis of performance overhead of Per-Row Activation Counting (PRAC) in a real server system.
- Memory system optimizations for Large Language Model (LLM) workloads.

Undergraduate research assistant — Jun. 2022 – Aug. 2022
Scalable Computer Architecture Laboratory, Seoul National University — Seoul, South Korea

- Designing RowHammer generator verilog module in DDR3 SoftMC (a FPGA-based DRAM testing infrastructure)
- RowHammer error characteristics analysis on HBM2

Undergraduate research assistant — Sep. 2021 – Jun. 2022
Compiler & Microarchitecture Laboratory, Korea University — Seoul, South Korea

- PointPillars model performance analysis on TI-SoC and CPU-GPU platforms

Publication

"SoK: Systematizing a Decade of Architectural RowHammer Defenses Through the Lens of Streaming Algorithms" — May. 2026
IEEE Symposium on Security and Privacy (S&P)
Michael Jaemin Kim, **Seungmin Baek**, Jumin Kim, Hwayong Nam, Nam Sung Kim, Jung Ho Ahn.

"The New LLM Bottleneck: A Systems Perspective on Latent Attention and Mixture-of-Experts" — Jul. 2025
arXiv
Sungmin Yun, Seonyong Park, Hwayong Nam, Younjoo Lee, Gunjun Lee, Kwanhee Kyung, Sangpyo Kim, Nam Sung Kim, Jongmin Kim, Hyungyo Kim, Juhwan Cho, **Seungmin Baek**, Jung Ho Ahn.

"Per-Row Activation Counting on Real Hardware: Demystifying Performance Overheads" Jul. 2025
IEEE Computer Architecture Letters (CAL)
Jumin Kim, **Seungmin Baek**, Minbok Wi, Hwayong Nam, Michael Jaemin Kim, Sukhan Lee, Kyomin Sohn, Jung Ho Ahn.

"Sudoku: Decomposing DRAM Address Mapping into Component Functions" Jun. 2025
DRAM Security (DRAMSec)
Minbok Wi, **Seungmin Baek**, Seonyong Park, Mattan Erez, Jung Ho Ahn.

"Marionette: RowHammer Attack via Row Coupling" Mar. 2025
ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
Seungmin Baek, Minbok Wi, Seonyong Park, Hwayong Nam, Michael Jaemin Kim, Nam Sung Kim, Jung Ho Ahn.

"DRAMScope: Uncovering DRAM Microarchitecture and Characteristics by Issuing Memory Commands" Jul. 2024
ACM/IEEE International Symposium on Computer Architecture (ISCA)
Hwayong Nam, **Seungmin Baek**, Minbok Wi, Michael Jaemin Kim, Jaehyun Park, Chihun Song, Nam Sung Kim, Jung Ho Ahn.

"X-ray: Discovering DRAM Internal Structure and Error Characteristics by Issuing Memory Commands" Jul. 2023
IEEE Computer Architecture Letters (CAL)
Hwayong Nam, **Seungmin Baek**, Minbok Wi, Michael Jaemin Kim, Jaehyun Park, Chihun Song, Nam Sung Kim, Jung Ho Ahn.

Honors and Awards

LG Electronics Paper Award Jun. 2022
Summer Anual Conference of IEIE

Excellent Research Talent Fellowship Sep. 2023 – Feb. 2024
BK21

Skills

Programming: Python, C/C++, Verilog
Tools: VTune (Intel), Vivado (Xilinx), Xcelium (Cadence), Design Compiler (Synopsys)