25VL682 RTL DESIGN AND FPGA SYNTHESIS LAB

M. Tech. VLSI Design

Batch: VLD - 11

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1.ABSTRACT

This project presents the design and implementation of a 1×3 router using Verilog HDL, based solely on a Finite State Machine (FSM) for control and data routing. The router receives data packets through a single input port and forwards them to one of three output ports according to the destination address specified in the packet header. Each packet includes a header, payload data, and a parity bit for basic error detection. The FSM governs all routing operations, including header decoding, data transfer, parity calculation, and packet validation. A comprehensive testbench is developed to verify router functionality under multiple scenarios, such as valid packets, incorrect destination addresses, and parity errors. Simulation results demonstrate successful packet routing, proper FSM-based control flow, and reliable parity-error identification. The simplified architecture offers an efficient, synthesizable solution suitable for compact digital communication and on-chip interconnect applications.

2.INTRODUCTION

In digital communication systems, data must be transferred efficiently and accurately between different modules or network components. Routers play an essential role in this process by directing incoming data packets to their appropriate destinations. Designing a reliable and hardware-efficient router is therefore crucial for achieving effective communication in embedded systems, System-on-Chip (SoC) architectures, and on-chip networks.

This project focuses on the design and implementation of a **1×3 router** using **Verilog HDL**, where a single input port is used to receive data packets and route them to one of three output ports. The routing decision is based on the destination address encoded within the packet header. Each packet also contains payload data and a parity bit used for basic error detection.

Unlike traditional router architectures that rely on multiple hardware modules such as FIFOs or synchronizers, this design uses a **Finite State Machine (FSM)** as the central control unit. The FSM manages all key operations, including header decoding, packet validation, data forwarding, and parity checking. This approach simplifies the overall architecture while maintaining reliable and predictable routing behavior.

A Verilog testbench is developed to verify the functionality of the router under various conditions. The tests include valid packet transmissions, packets with incorrect destination addresses, and packets with parity errors. Simulation results confirm correct routing, effective control flow through the FSM, and proper identification of error conditions.

The overall design demonstrates a compact and synthesizable routing solution suitable for applications requiring low hardware complexity and dependable data communication. The FSM-based approach ensures ease of implementation while providing accurate and efficient packet routing in digital systems.

3.OBJECTIVE

- Develop a simple, efficient, and synthesizable routing architecture without relying on additional hardware modules such as FIFO buffers or synchronizers.
- Enable correct routing of incoming data packets from a single input port to one of three output ports based on the destination address in the packet header.
- Implement basic error detection using a parity bit and ensure that the FSM accurately identifies and handles invalid or corrupted packets.

4.ARCHITECTURE

4.1 1×3 Router Architecture Description

The 1×3 router module accepts an 8-bit input stream and routes each incoming data byte to one of three output ports based on the destination field encoded in the packet header. The design operates synchronously with the input clock (clk) and includes an active-low reset (rstm). Packet reception is indicated through the pkt_valid signal, while the data_in bus carries header, payload, and parity information.

Internally, the router uses a four-state FSM—**IDLE**, **HEADER**, **DATA**, and **PARITY**—to control the flow of packet processing. In the HEADER state, the destination field (data_in[1:0]) is extracted and stored in the dest register. During the DATA state, incoming payload bytes are forwarded to one of the three output data ports (data_out_0, data_out_1, or data_out_2) based on this dest value. Correspondingly, the valid signals (vld_out_0, vld_out_1, vld_out_2) identify which output port contains a new byte.

The architecture also incorporates a built-in parity checking mechanism. As payload bytes are received, the router computes running parity using XOR operations. When the payload ends (pkt_valid goes low), the router transitions to the PARITY state, where it captures the received parity byte and compares it with the internally calculated parity. Any mismatch asserts the error output, indicating corruption in the packet.

Thus, the 1×3 router integrates packet decoding, data routing, and error detection in a compact FSM-driven architecture, ensuring reliable and deterministic byte-wise transmission to one of three independent output channels.

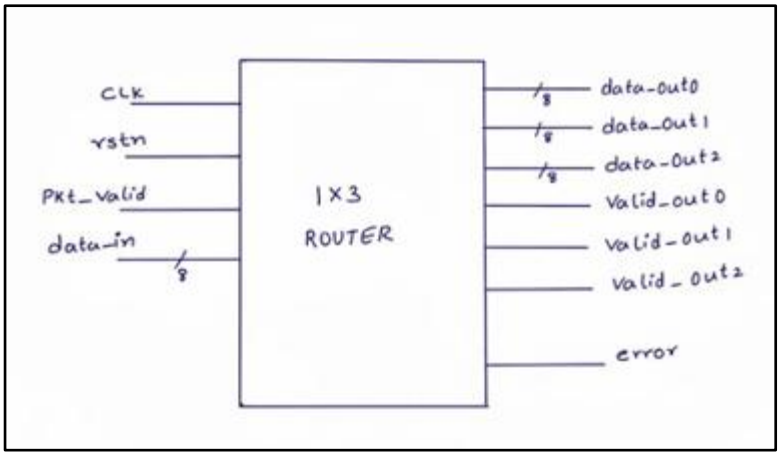

Fig 4.1 Architecture block

5.ASMC (Algorithmic State Machine Chart)

The ASM for the 1×3 router consists of four states: IDLE, HEADER, DATA, and PARITY. In the IDLE state, the router waits for pkt_valid while resetting all output registers, parity registers, and the error flag. When a new packet begins, the FSM moves to the HEADER state, where it extracts the destination field (dest = data_in[1:0]) and initializes parity_calc. The machine then enters the DATA state, routing each incoming byte to the appropriate output port based on the decoded destination while continuously updating the running parity using XOR operations. When pkt_valid goes low—indicating the end of payload—the FSM transitions to the PARITY state, where it captures the received parity byte (when parity_ready is low) and compares it with the calculated parity. If both values match, err remains zero; otherwise, it is asserted. After completing parity verification, the FSM returns to the IDLE state, ready to process the next packet.

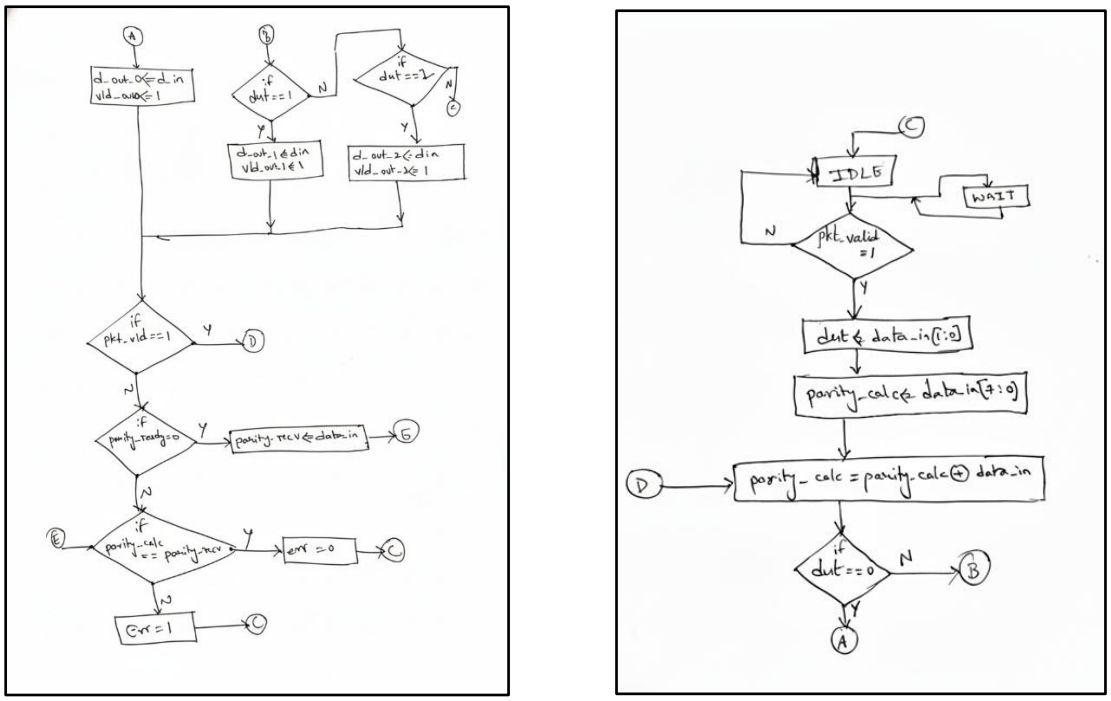

Fig 5.1 ASMC of 1x3 Router

6.TIMING

BEHAVIOURAL SIMULATION:

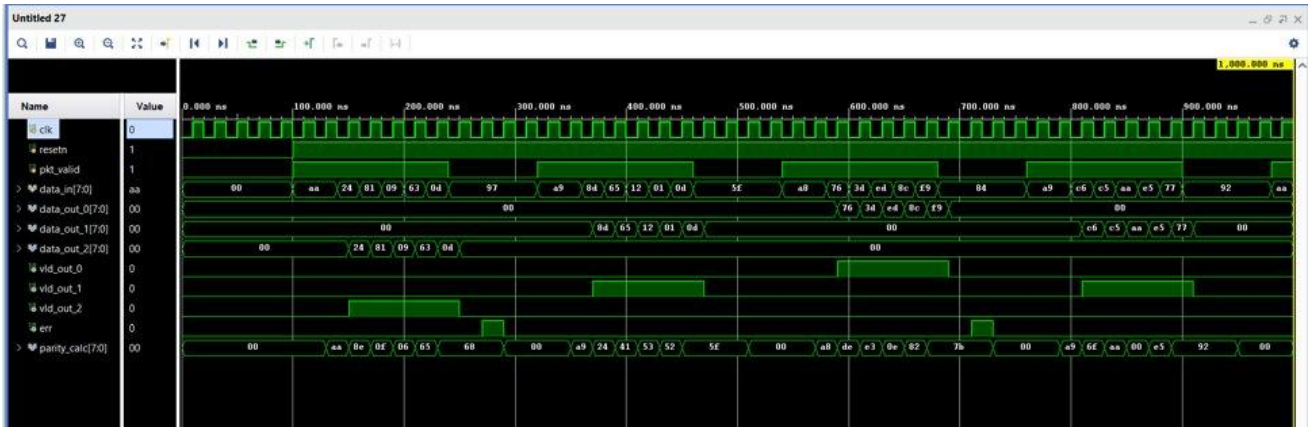

Fig 6.1 Timing diagram of behavioral simulation

POST-IMPLEMENTATION TIMING SIMULATION

Fig 6.2 Post-Implementation Timing simulation

7.SIMULATION AND IMPLEMENTATION RESULTS

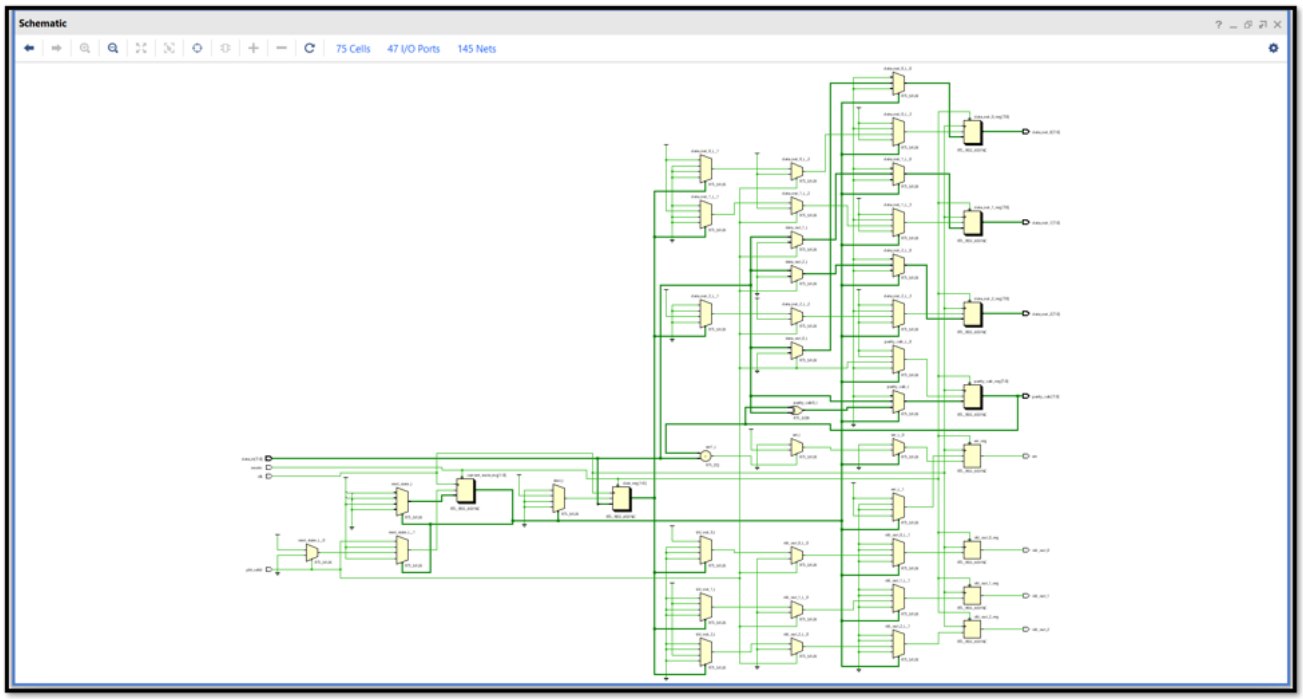

Fig 7.1 RTL Schematic

8.UTILIZATION REPORT

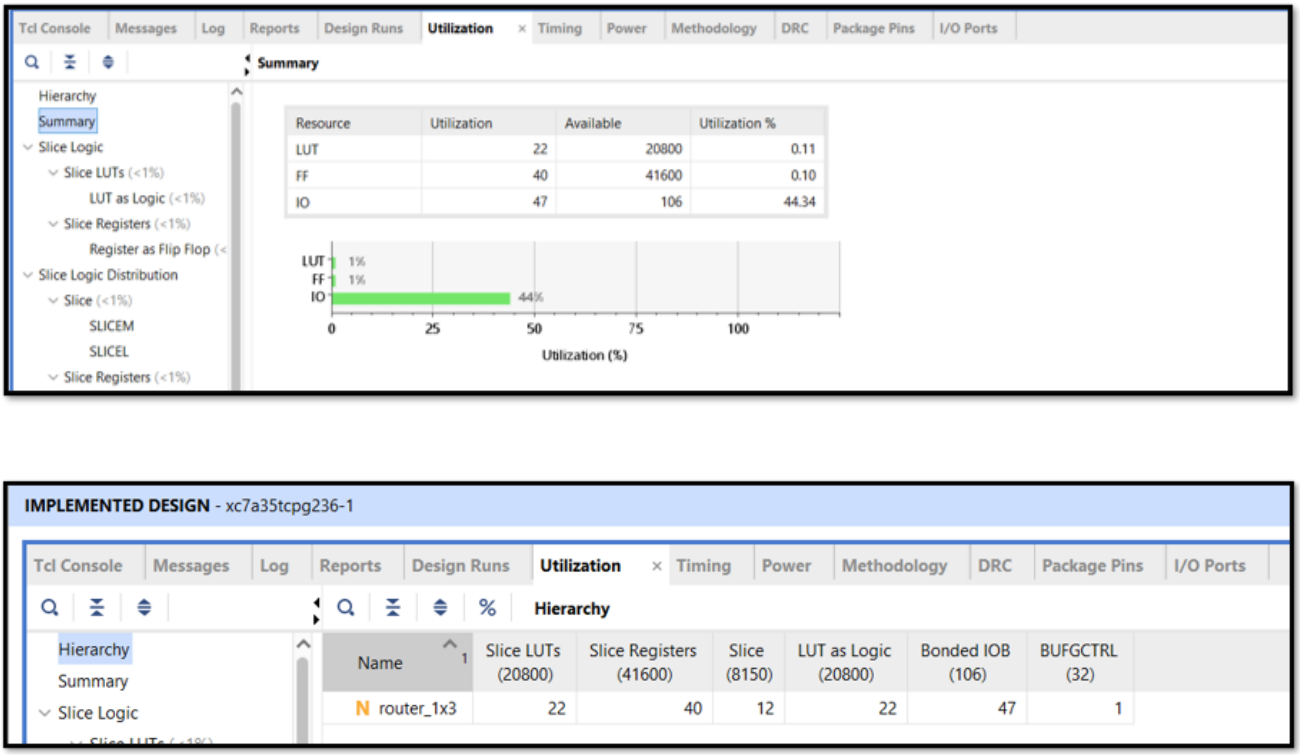

Fig 8.1 Utilization Report

The resource utilization report for the 1×3 router design shows that the implementation uses only **22 LUTs (0.11%)** and **40 Flip-Flops (0.10%)**, indicating that the design is extremely lightweight and occupies a negligible portion of the available FPGA logic resources. The design also consumes **47 I/O pins (44.34%)**, which forms the largest share of utilization. This is expected, as the router requires multiple external ports—three data outputs, three valid signals, packet control signals, and a clock/reset interface—resulting in a relatively high I/O count compared to internal logic usage. The minimal LUT and FF utilization confirms the efficiency of the RTL architecture and the simplicity of the state machine, while the higher I/O consumption reflects the inherently parallel nature of a multi-port router that must expose separate dedicated output channels to the top-level interface.

9.POWER REPORT & THROUGHPUT

Power Report:

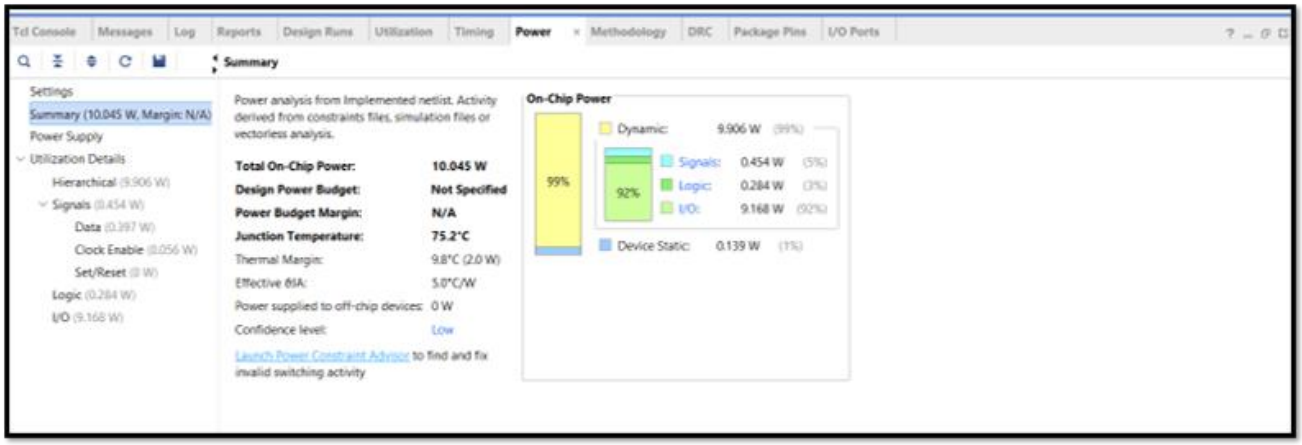

Fig 9.1 Power Report

The total on-chip power consumption of the 1×3 router design is **10.045 W**, indicating a moderately active implementation dominated by dynamic switching activity. Dynamic power accounts for **9.906 W (99%)**, which is expected due to continuous data movement through the router's output ports and frequent toggling of internal logic during packet reception and routing. Among the dynamic components, **I/O power is the largest contributor at 9.168 W (92%)**, reflecting the high activity level on the three data-out buses and their corresponding valid signals. Signal network power and logic power remain relatively small at **0.454 W (5%)** and **0.284 W (3%)**, demonstrating that the core FSM and datapath logic are lightweight in comparison to the I/O interface demands. Static power remains minimal at **0.139 W (1%)**, showing efficient leakage characteristics. The junction temperature stabilizes at **75.2°C**, remaining within acceptable operating limits, with a thermal margin of **9.8°C**, ensuring that the design functions safely without risk of thermal overstress.

THROUGHPUT:

- Considering 1st data packet transmission of 5bytes between 159.539 ns → 259.393 ns.
- Each byte of the packet being routed is of 8 bits in length.
- $T_{CLK} \approx 20$ ns
- $f_{CLK} = \frac{1}{20\text{ ns}} = 50$ MHz

So, for 1 Packet:

- Throughput $= \frac{\text{Number of bits transferred}}{\text{Transfer time}}$
- Throughput $= \frac{5x8}{99.854 \text{ ns}} = 400\text{Mbps}=50\text{MBps}$

10.FUTURE SCOPE

1. **Functional Design Expansion:** The router design can be extended to multi-input and multi-output systems for large-scale data communication networks**.**
2. **Hardware Implementation:** The design can be implemented on FPGA or ASIC platforms, making it suitable for real-time hardware applications.
3. **System Optimization**: Future improvements may include multi-depth FIFO, error correction, and dynamic routing for higher efficiency.
4. **Educational and Research Value**: Serves as a practical model to understand FSM-based control, data communication, and Verilog hardware design concepts.
5. **Industrial Relevance**: Provides a base for developing network routers, on-chip communication systems, and digital data transfer architectures used in modern VLSI designs.

11.CONCLUSION

The design and implementation of the 1×3 Packet Router were successfully completed using Verilog HDL. The router architecture was built using a finite state machine (FSM) with four states—IDLE, HEADER, DATA, and PARITY—allowing reliable packet processing from header reception to data transfer and parity verification. The module dynamically routes incoming data packets to one of the three output ports based on the destination address encoded in the header.

A parity-based error-detection mechanism was implemented to ensure data integrity. The router calculates parity in real time and compares it with the received parity byte, asserting the error signal accurately in the PARITY state. The routing logic for valid outputs, data forwarding, and parity computation was verified through simulation, confirming correct functionality under different input scenarios.

12.REFERENCES

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3. https://github.com/aniketb005/rtl-implementation-1x3-router.git