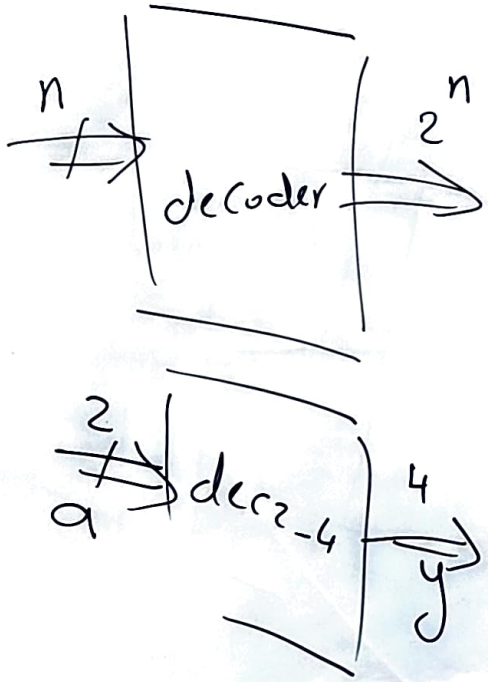
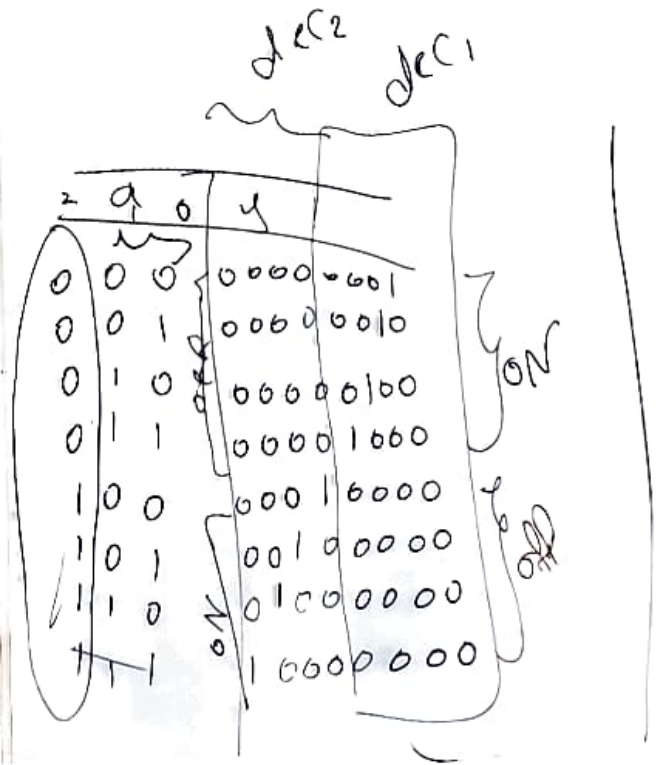
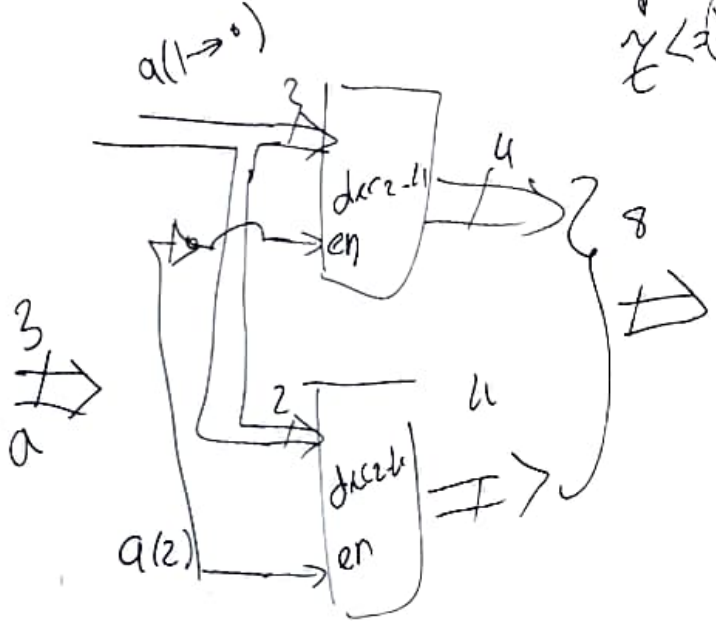
DeCoder



		3	2	1	0
a		y			
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0


add
clk
8
load0
load1
reg0
reg1
reg7
0001
0
0010
1
0100
2
1000
3
2
dec2-4
3
decoder 3-8
Mux 8-1
8


dec2
dec1
a
0
4
0000 0001
0000 0010
0000 0100
0000 1000
0001 0000
0010 0000
0100 0000
1000 0000
ON
OFF


a(1->0)
3
dec2-4
en
4
8
3
a
2
4
dec2to4
en
a(2)

```
if (A_temp > B_temp) then
  y <= "00";
elsif ( A_temp
  y <= "01";
```

```
entity comp is
Port ( A, B : in std_logic_vector (3 downto 0);
       y    : out std_logic_vector (1 downto 0));
end comp;
architecture rtl of comp is
Signal A_temp, B_temp : Signed (3 downto 0);
begin
Process( A_temp, B_temp)
begin
```