Traffic Light Controller

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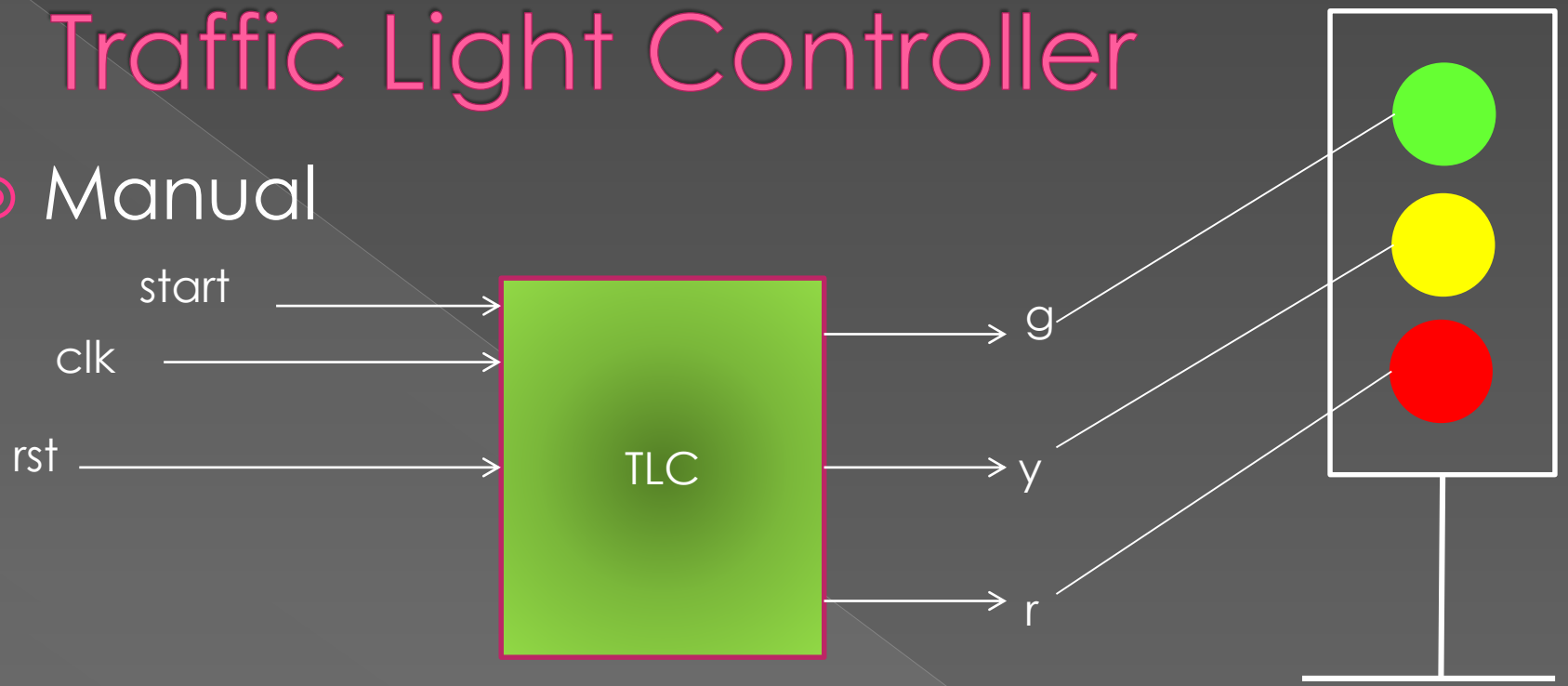
Traffic Light Controller

- Manual



- Assume a 1 kHz clock.
- The design will start operation by a trigger (start) signal from a user
- The default stat is green
- When the start signal occurs, the TLC will go to the yellow state.
- Remain four seconds in yellow state.
- Then change to the red state and remain for sixteen seconds.
- Finally return to the green state.

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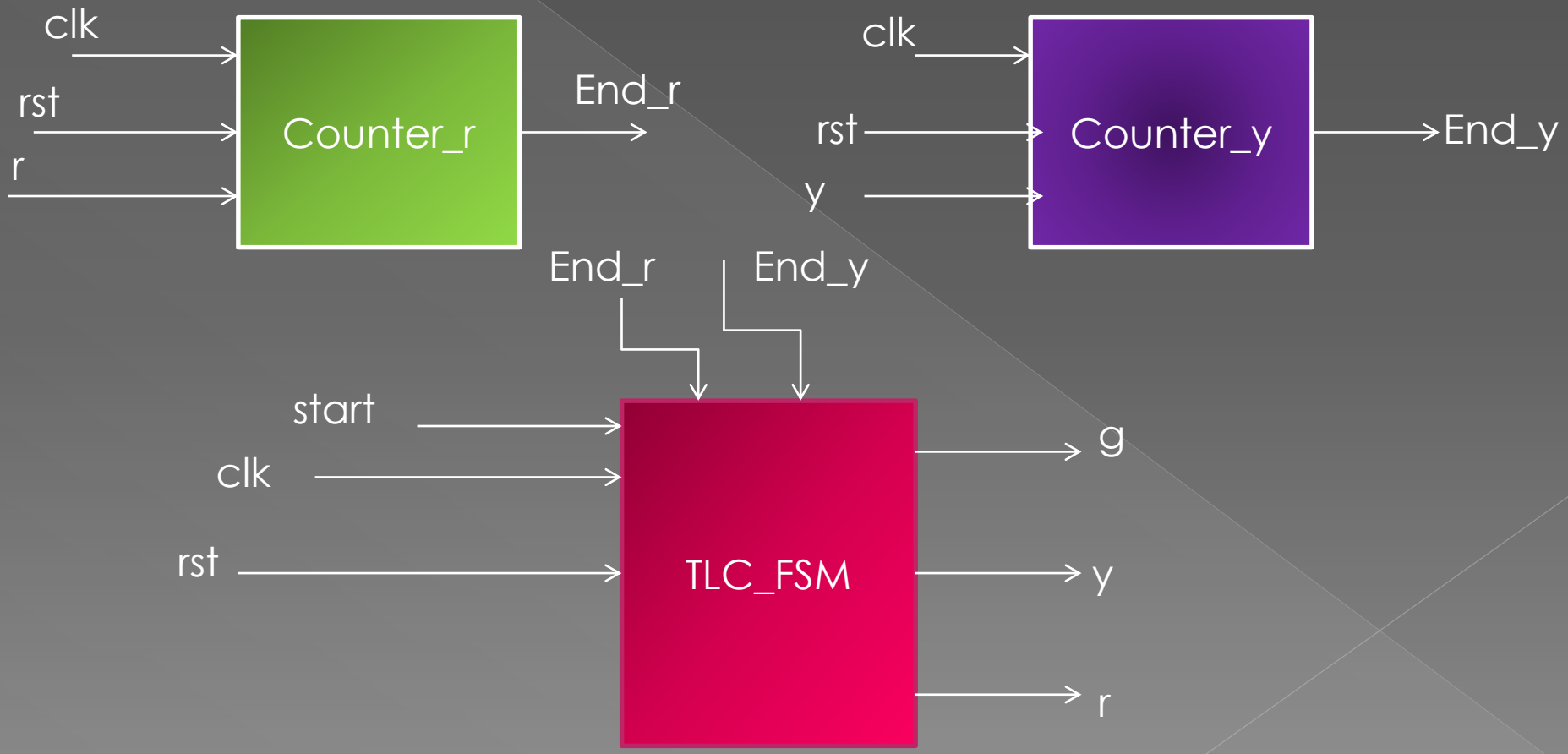

Traffic Light Controller

- Couter_r

```
ENTITY count_r IS
port(clk,en,rst: in std_logic;
q: out std_logic);
END count_r ;
ARCHITECTURE rtl OF count_r IS
signal count_sig: unsigned (3 downto 0);
BEGIN
process (rst,clk)
begin
if (rst='1') then
count_sig <=(others=> '0');
elsif (rising_edge (clk)) then
if (en='1') then
count_sig <= count_sig+1;
end if;
end if;
end process;
q <= count_sig(0) and count_sig(1)and
count_sig(2) and count_sig(3);
END rtl;
```

Traffic Light Controller

- Couter_y

```
ENTITY count_y IS
port(clk,en,rst: in std_logic;
q: out std_logic);
END count_y;
ARCHITECTURE rtl OF count_y IS
signal count_sig: unsigned (1 downto
0);
BEGIN
process (rst,clk)
begin
if (rst='1') then
count_sig <=(others=> '0');
elsif (rising_edge (clk)) then
if (en='1') then
count_sig <= count_sig+1;
end if;
end if;
end process;
q <= count_sig(0) and count_sig(1);
END rtl;
```

Traffic Light Controller

- TLC_FSM