I need to design a timer circuit

I need to design a circuit to count for example the number of people that entering such a place

Counter

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Timer

- Write a legal VHDL code for a 8 seconds stopwatch timer. The clock frequency is 2 Hz.

Number of counts needed=
total time/clock period

What is the number of counts needed?

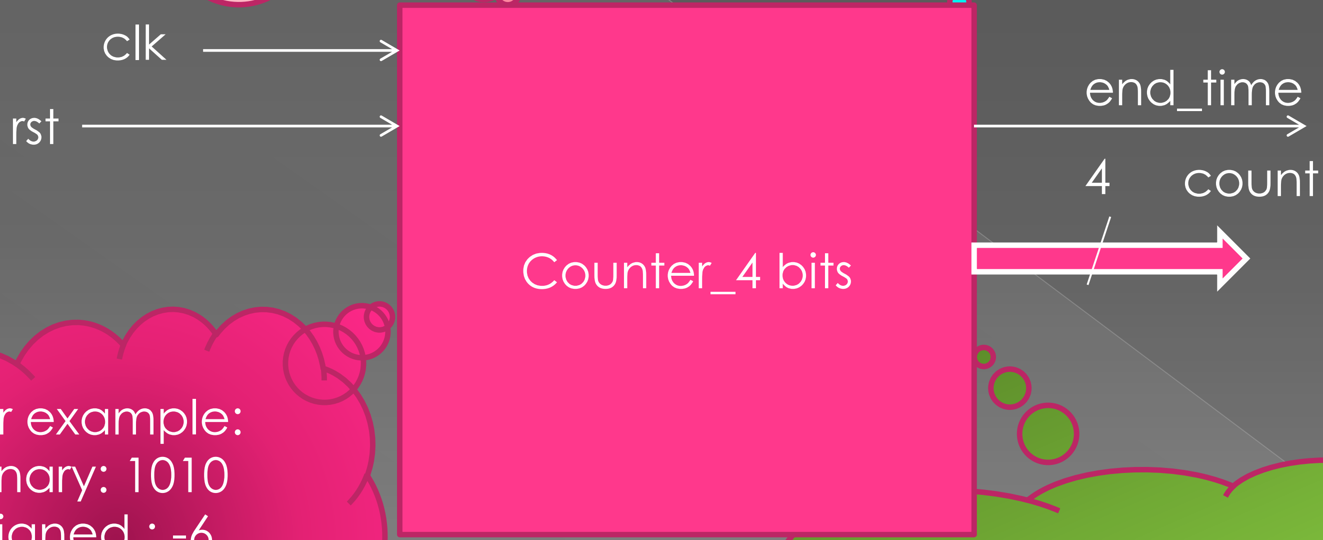
The number of counts =
8 sec/0.5 Sec=16 counts

Clock period =1/fclk=1/2Hz =0.5 Sec

Timer

Signed or unsigned numbers

~~Count <= count + 1~~



0000
0001
0010
:
:
1111

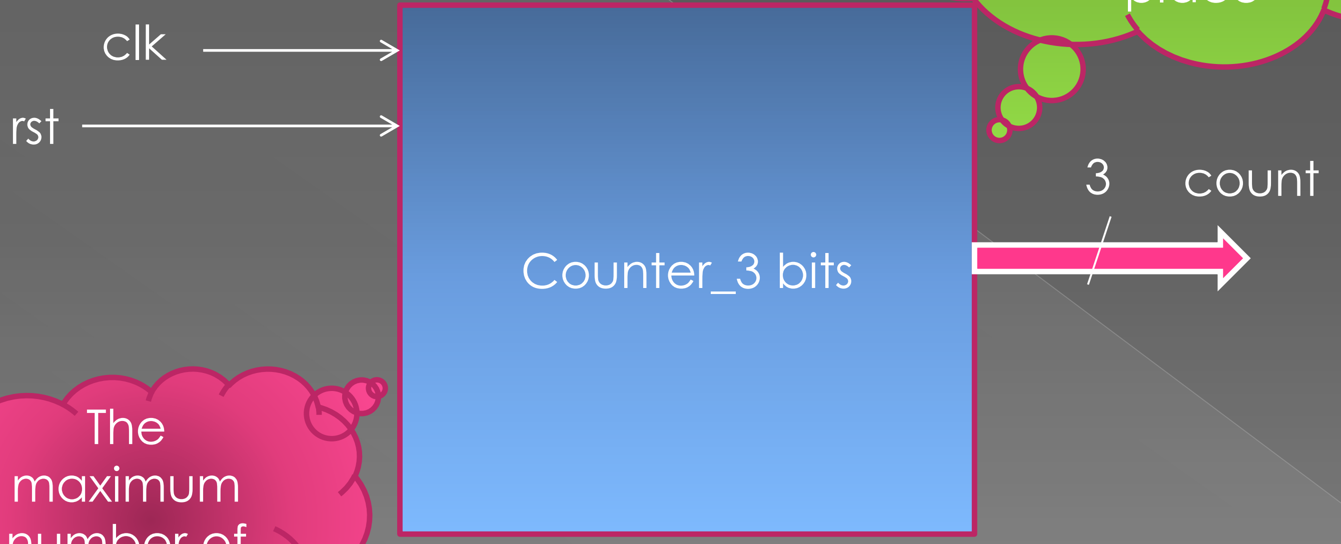
For example:
Binary: 1010
Signed : -6
Unsigned : 10

Count_temp<=count_temp +1

Timer

```
entity binary_count is
port (clk, rst: in std_logic;
        end_time :out std_logic;
Count : out std_logic_vector(3 downto 0));
end entity binary_count;
architecture rtl of binary_count is
signal count_temp: unsigned(3 downto 0);
begin
process (rst, clk)
begin
if (rst = ‘1’) then
count_temp <= (others => ‘0’);
elsif (rising_edge(clk)) then
count_temp <= count_temp + 1;
end if;
end process;
end_time<= ‘1’ when (count_temp= 15) else ‘0’;
count<= std_logic_vector(count_temp);
end architecture rtl;
```

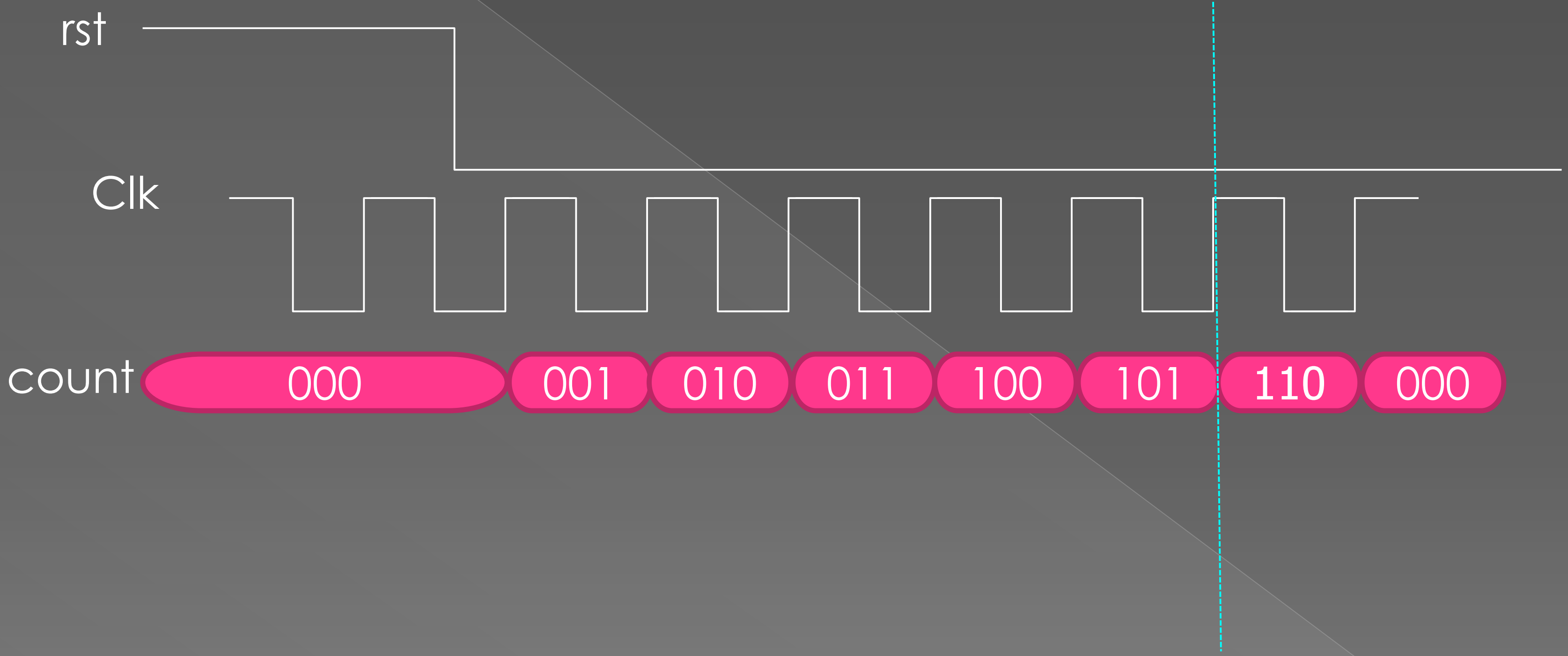
How to a counter that counts a certain number ?



If we want to count the people that entering such a place

The maximum number of people is 7

How to a counter that counts a certain number ?



How to a counter that counts a certain number ?

```
entity binary_count is
port (clk, rst: in std_logic;
Count : out std_logic_vector(2 downto 0));
end entity binary_count;
architecture rtl of binary_count is
signal count_temp: unsigned(2 downto 0);
begin
process (rst, clk)
begin
if (rst = ‘1’) then
count_temp <= (others => ‘0’);
elsif (rising_edge(clk)) then
count_temp <= count_temp + 1;
If (count_temp=6) then
Count_temp<=(others => ‘0’);
end if;
end if;
end process;
count<= std_logic_vector(count_temp);
end architecture rtl;
```