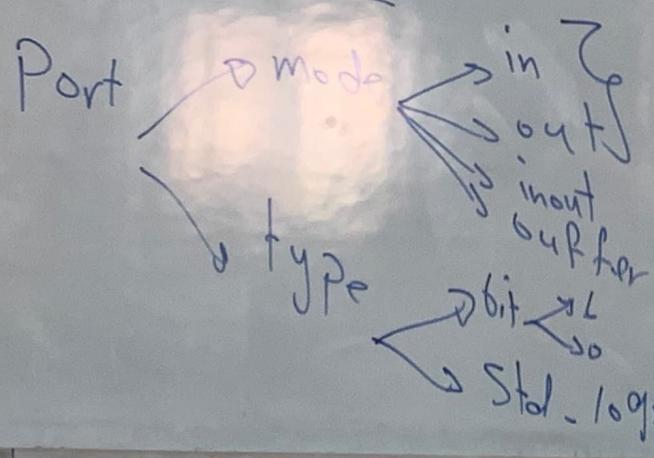
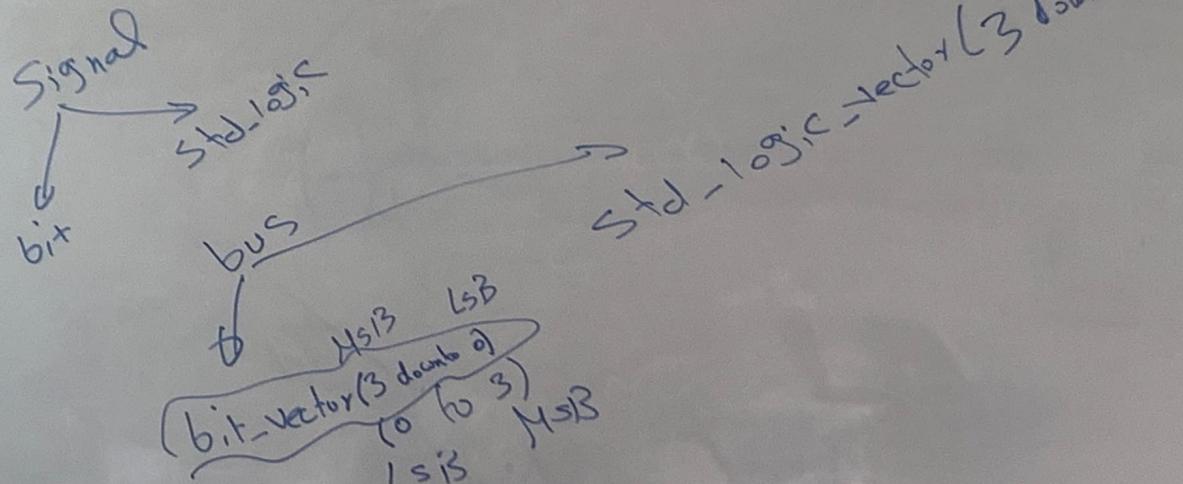
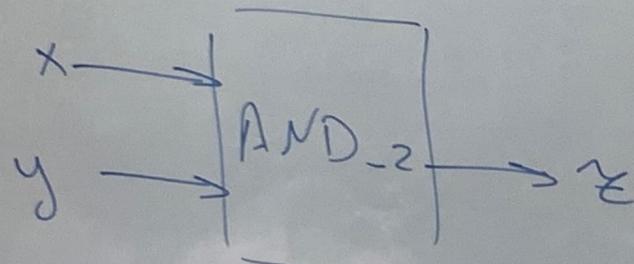


MSB
1010 LSB



entity AND_2 is

Port (x, y : in std-logic;
z : out std-logic);

2
4
t.

entity

AND-2

is

Port

(x, y
z

:in std-logic;
:out std-logic);

end

AND-2;

architecture

begin

rtl

OR

AND-2 is

$z = (x \text{ AND } y) \text{ XOR } (\text{NOT } z);$

entity

AND_2

is

Port (x, y : in std_logic;
z : out std_logic);

end AND_2;

architecture

rtl

of

AND_2

is

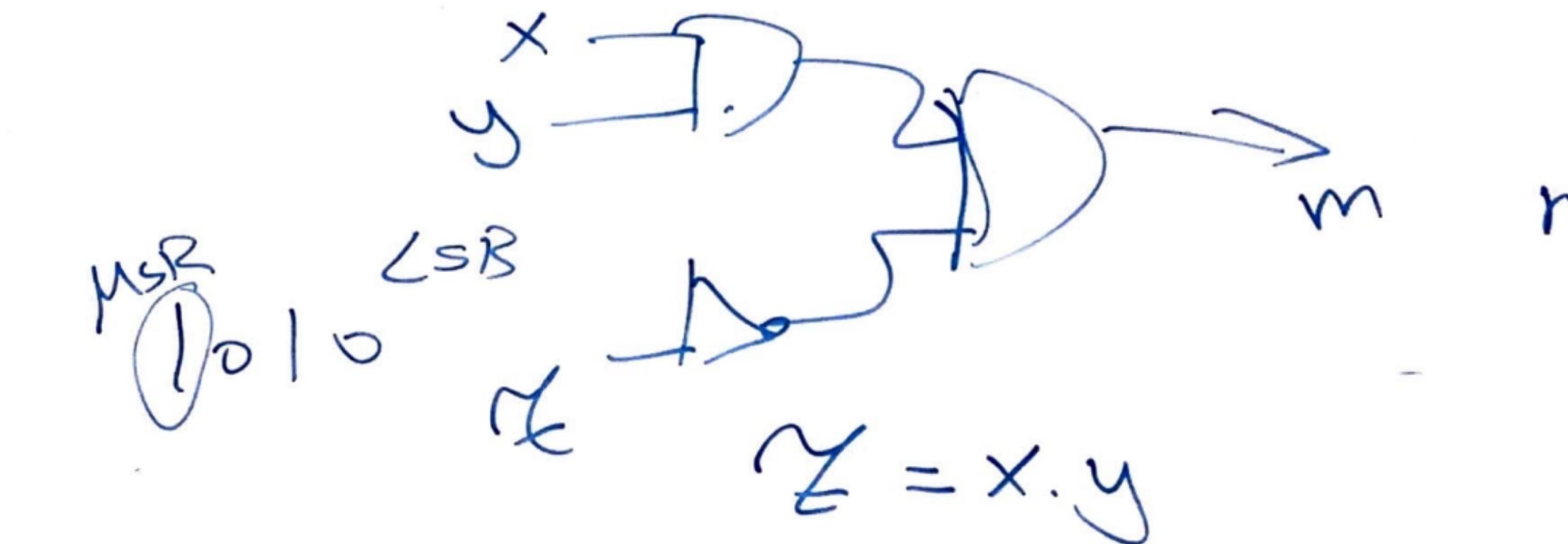
begin

$z \leftarrow x \text{ AND } y;$

end rtl;

$m \leftarrow (x \text{ AND } y) \text{ XOR } (\text{NOT } z) ;$

entity AND_2 is
Port (x, y : in std-logic;
z : out std-logic);
end AND_2;
architecture rtl of AND_2 is
begin
 $z \leftarrow x \text{ AND } y;$
end rtl;



$$m \leftarrow (x \text{ AND } y) \text{ XOR } (\text{NOT } z);$$

1 entity

Ans

