Course Specification

# *Code:* ECE 312 *Course : Electronic circuits design Using Computer*

## *A- Affiliation:*

| | |
|---|---|
| **Relevant program:** | Electronics and Communication Engineering program (ECE) |
| **Department offering the program:** | Communications and Computer Engineering Dep. |
| **Department offering the course:** | Communications and Computer Engineering Dep. |
| **Date of specifications approval:** | 2020-2021 |
| **Year of regulation approval:** | 2013 |

## B - BASIC INFORMATION

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|---|---|---|---|---|
| **Course Title:** Electronic circuits design using computer | | | **Code:** ECE 312 | **Year/level:** Third year<br>**Semester:** 2nd term |
| **Teaching Hours:** | **Lecture:** 0hrs. | **Tutorial:0** | **Practical:** 6hrs | **Total:** 6hrs. |

## C - PROFESSIONAL INFORMATION

### 1 – Course Learning Objectives:

The main objective of this course is to learn the basics of digital circuit design and implementation through computer-aided design (CAD) tools.

### 2 - Intended Learning Outcomes (ILOS)

**K- Knowledge and understanding:**

By the end of the course the student should gain the following knowledge.

k1- State the basics of Field Programmable Gate Array (FPGA) Technique for circuit design and implementation (K4,K13,K20).

k2- Illustrate the way in which digital circuits are designed today, using CAD tools (K4,K20,K13).

k3-State basics of circuit design with VHDL programming language(K4,K13,K20).

**I- Intellectual skills:**

By the end of the course the student should be able to:

i1- Analyze, simulate, and Synthesis digital circuits using CAD Software.(I14, I18, I15)

i2- Develop VHDL Design Programs (I15).

**P - Professional and practical skills:**
By the end of the course the student should be able to:
p1- Prepare models and implement digital circuits for certain specific function using relevant laboratory equipment and analyze the results correctly (P13).
p2-Practice VHDL programming language for the design of digital circuits (P15).
p3- Use appropriate analysis and design tools (P17).

**T - General and transferable skills:**
By the end of the course the student should be able to:
t1-Works under pressure (T2).

## 3 – Contents

| Week No. | Topic | Lecture hours | Tutorial hours | Practical hours |
|---|---|---|---|---|
| 1 | ▪ Introduction<br>▪ FPGA structure<br>▪ Introduction to CAD tools | - | - | 6 |
| 2 | ▪ Fundamental VHDL units<br>▪ Data Types<br>▪ Operators<br>▪ Assignment Statements | - | - | 6 |
| 3 | ▪ Multiplexers | - | - | 6 |
| 4 | ▪ Decoders<br>▪ Encoders | - | - | 6 |
| 5 | ▪ Latches<br>▪ Flip Flop<br>▪ Parallel register<br>▪ Shift register | - | - | 6 |
| 6 | ▪ Counters | - | - | 6 |
| 7 | ▪ Half Adder, Full Adder, Parallel Adder<br>▪ Half, Full, Parallel subtractor using Parallel Adders | - | - | 6 |
| 8 | ▪ Introduction to Finite State Machines | - | - | 6 |
| 9 | ▪ Mid Term | | | |
| 10 | ▪ Traffic Light Controller example | - | - | 6 |
| 11 | ▪ FSM as Sequence Detectors | - | - | 6 |
| 12 | ▪ Timing Simulation, Synthesis, Place and Route | - | - | 6 |
| 13 | ▪ Pin Assignments, FPGA configuration | - | - | 6 |
| 14 | ▪ Oral/Practical | - | - | |

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|---|---|---|---|---|
| 15 | ▪ Final Exam | - | - | - |
| | Total | - | - | 72 |

## 4 - Teaching and Learning methods:

| Course Intended learning Outcomes (ILOs) | Teaching and Learning Methods | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Lectures/Online Lectures | Presentation | Discussions | Tutorials | Practical and lab. experiments | Problem Solving | Brain Storming | Projects and Team Working | Site Visits | Researches and Reports | Self-Study | Modeling and Simulation |
| Knowledge & Understanding | √ | √ | √ | √ | √ | | √ | √ | | √ | | |
| Intellectual Skills | √ | √ | √ | √ | √ | √ | √ | √ | | √ | | √ |
| Professional Skills | √ | √ | | √ | √ | √ | | √ | | √ | √ | √ |
| General Skills | | √ | √ | √ | √ | √ | | √ | | √ | √ | √ |

## 5.Course Contents/ILOS:

| Course Contents | k | i | p | T |
|---|---|---|---|---|
| FPGA technique for digital circuit design | k1 | | | |
| Basics of VHDL language | K3 | | | |
| Multiplexers | K2,3 | i1,2 | p1,2,3 | t1 |
| Decoder/Encoder | K2,3 | i1,2 | p1,2,3 | t1 |
| Latch, Flip Flop, Parallel register, and Shift Register | K2,3 | i1,2 | p1,2,3 | t1 |
| Counters | K2,3 | i1,2 | p1,2,3 | t1 |
| Half Adder, Full Adder, Parallel Adder Half, Full, Parallel subtractor using Parallel Adders | K2,3 | i1,2 | p1,2,3 | t1 |
| Introduction to Finite State Machines | K2 | i1 | p1,3 | t1 |
| Traffic Light Controller example | | i1 | p1,3 | t1 |
| FSM as Sequence Detectors | | i1 | p1,3 | t1 |
| Timing Simulation, Synthesis, Place and Route | k2 | i1 | p1,3 | |
| Pin Assignments, FPGA configuration | k2 | i1 | p1,3 | |

## 6- Students' Assessment Methods:

| 6-1 Tools | |
|---|---|
| **Attendance & Quizzes & reports to measure** | Content of k1to k3, i1 to i2, p1 to p3, and t1. |
| **Mid-Term exam to measure** | Content of k1to k3, i2, and p2. |
| **Oral / practical exam to measure** | Content of k1to k3, i1 to i2, p1 to p3, and t1. |
| **Final exam to measure** | Content of k1 to k3, i2, and p2. |

| 6-2, Time schedule: | |
|---|---|
| **Attendance** | Weekly |
| **Reports and sheets** | Bi-weekly |
| **Quizzes** | At the 6th week of 1stsemester |
| **Oral /practical Exam** | At the 14h week of 1stsemester |
| **Mid-term exam** | At the 9th week of 1stsemester |
| **Final exam** | At the 15th week of 1st semester |

## 6.3.Grading system

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|---|---|---|---|---|---|
| **Teacher Opinion** | Quizzes | 30% | 30 | 12 Marks | 40 % |
| | Mid-term exam | | | 18 Marks | 60 % |
| **Practical &Oral** | Lab Attendance | 30% | 30 | 3 Marks | 10% |
| | Lab Reports | | | 3 Marks | 10% |
| | Oral /Practical Exam | | | 24 Marks | 80 % |
| **Final Exam** | | 40% | 40 | | |
| **Total** | | 100% | 150 Marks | | |

## 7- List of references:

**7-1 Course notes**

**7-2 Essential books (text books)**


[1] Z. Navabi, "VHDL Analysis and Modeling Of Digital Systems," New York, N.Y. : McGraw-Hill, 2nd Ed.,1998.

[2] M. Zwolinski, "Digital System Design With VHDL," , Pearson Education Limited, 2006.

[3] S. Salivahanan and S. Arivazhagan ,"Digital Circuits& Design," Vikas Publishing House Pvt Ltd, 4th ed., 2012.

[4] S. Rammamurthy and V.P. Kothari , "VHDL Modeling For Digital Design Synthesis," Medtec, 1st ed., 2014.

[5] M. M. R. Mano and M. D. Ciletti, "Digital Design With an Introduction To The Verilog HDL, VHDL, & System Verilog," Pearson, 6th ed., 2019.

[6] S. Mazor and P. Langstraat, "Aguide to VHDL," Springer, 2nd ed., 2007.


## 8- Facilities required for teaching and learning:

- Black or white board
- Overhead projector or Data show
- Disk-top computers and simulation tools

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| **Course coordinator:** | Dr.Fatma Elfouly | |
| **Head of the Department:** | Prof.Dr.SalahElagouze | |
| **Date:** | | |