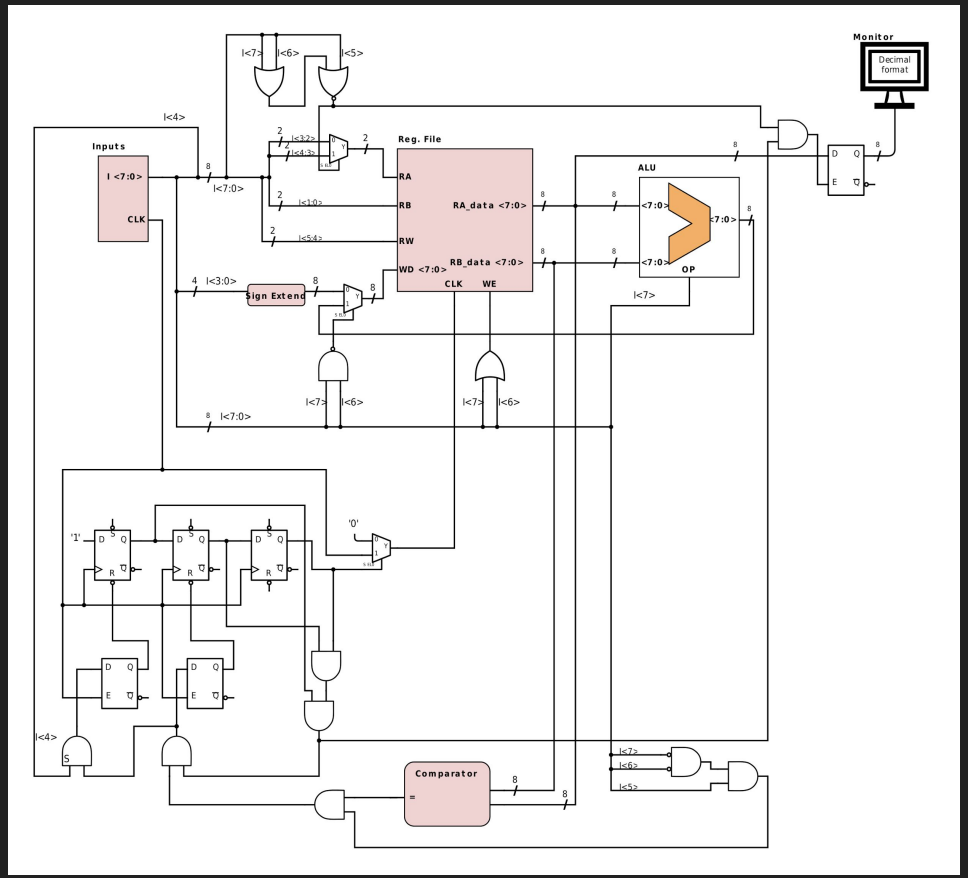
Lab 3 - A Single Cycle Calculator in VHDL

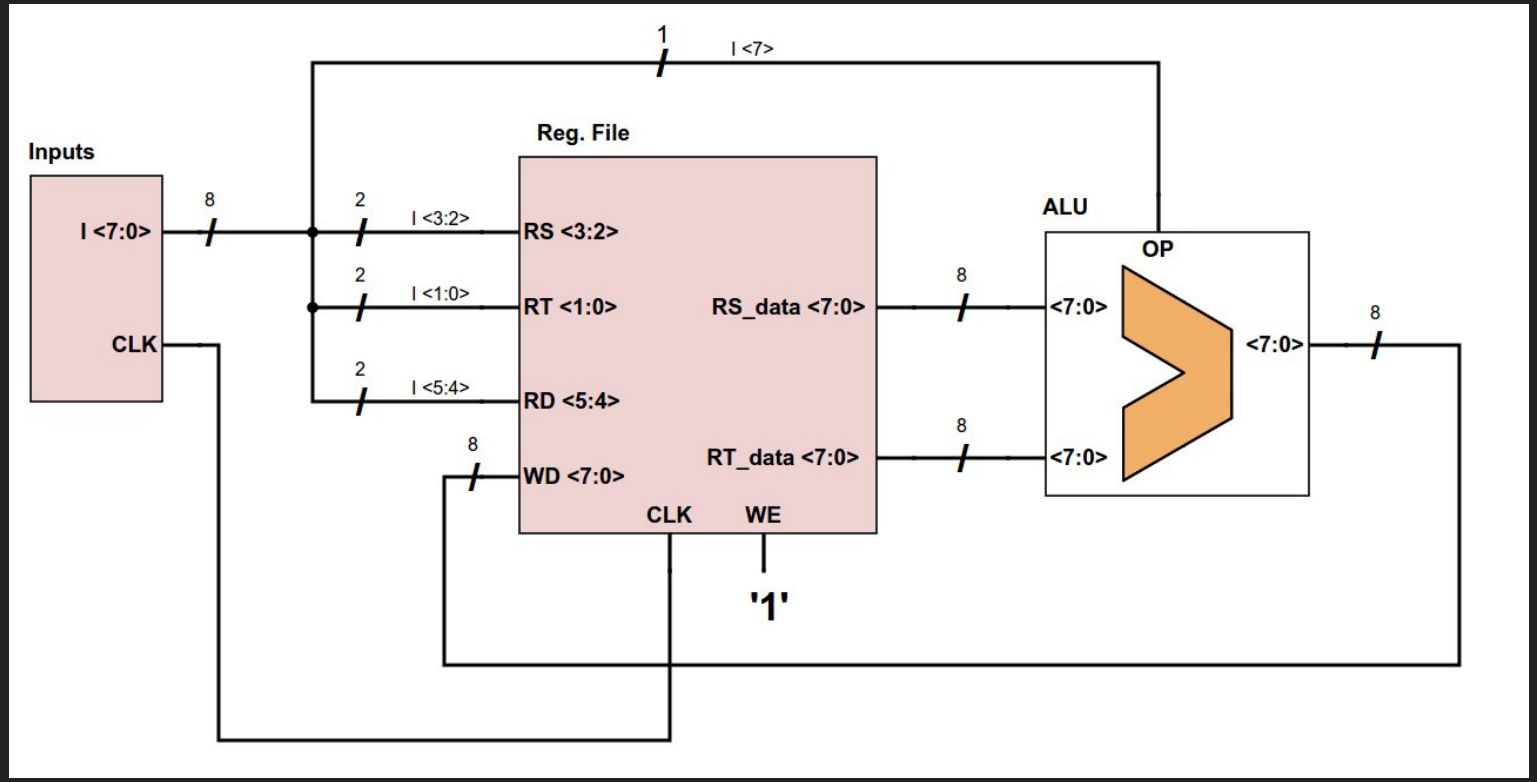
CPEG 324, 4/19/17

By: Abraham McIlvaine and Benjamin Steenkamer

Complete Datapath

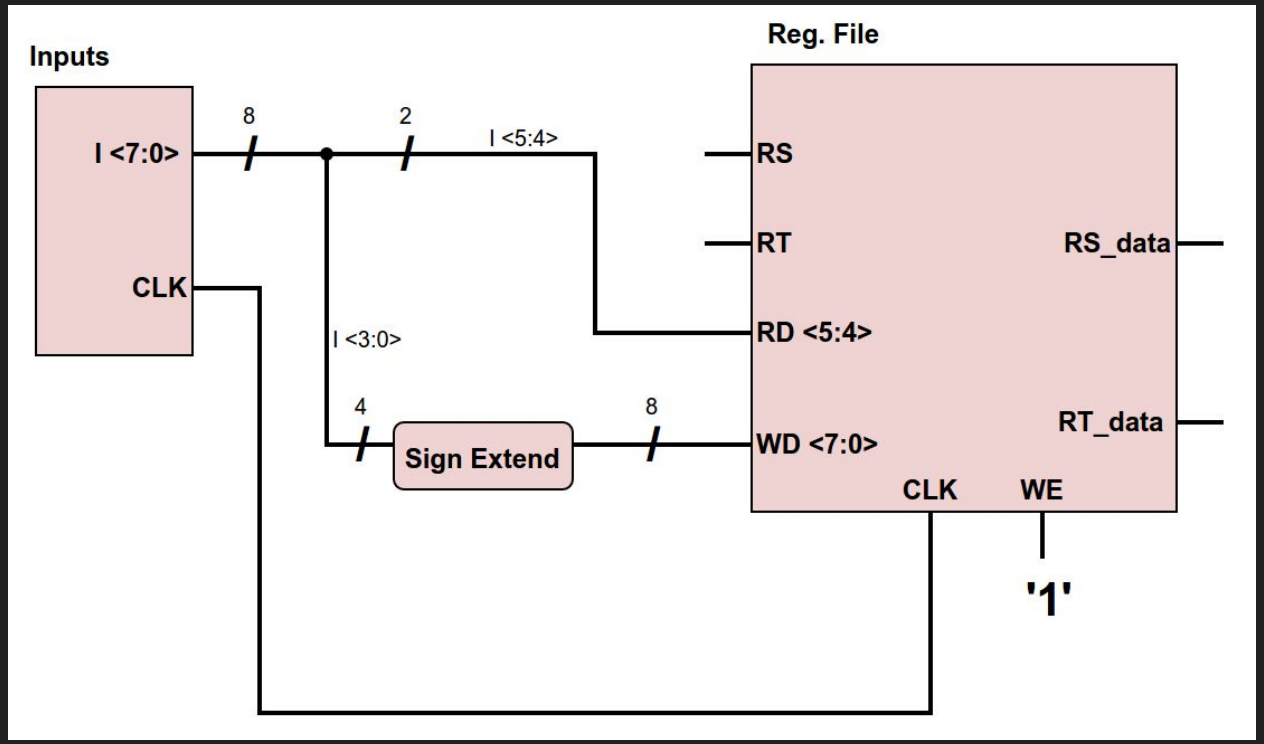


Add / Subtract Datapath



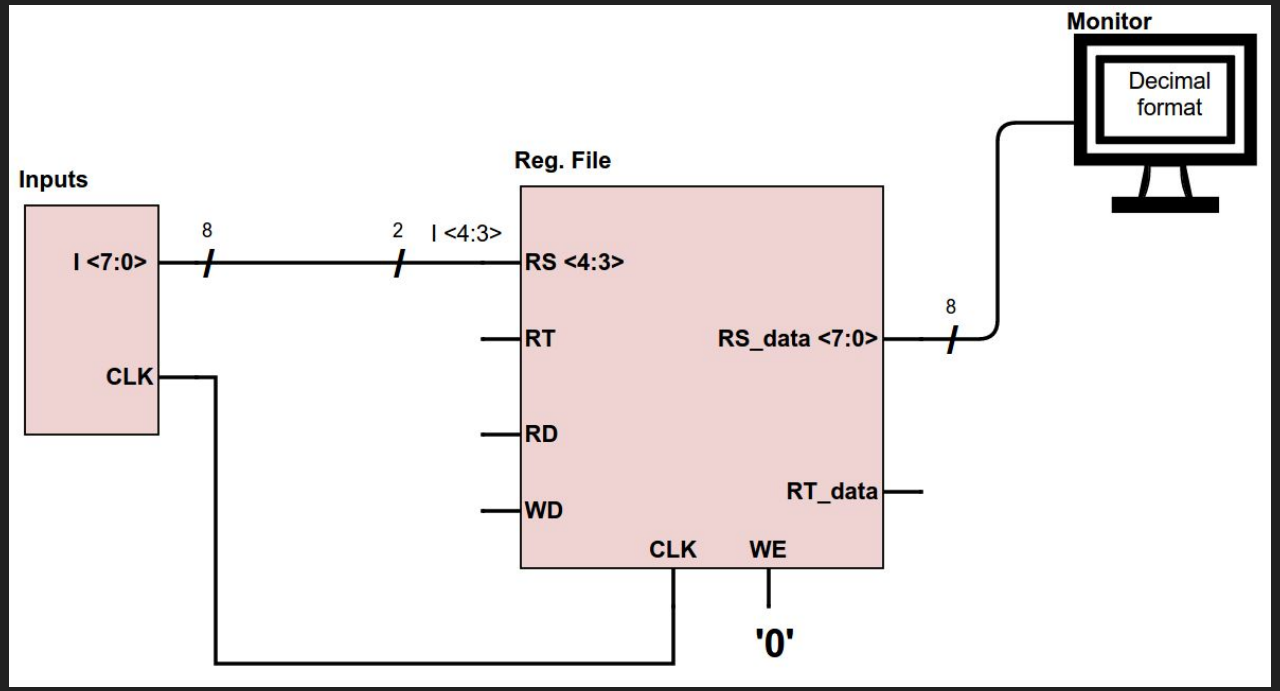
- Add: [0 1][RD RD][RS RS][RT RT]
- Subtract: [1 0][RD RD][RS RS][RT RT]
- If OP=0, RD[Data]=RS[Data]+RT[Data]; If OP=1, RD[Data]=RS[Data]-RT[Data]

Load Immediate Datapath



- Load Immediate: [1 1][RD RD][I_3 I_2 I_1 I_0]
- RD[Data] = 0b$I_3I_3I_3I_3I_2I_1I_0$

Display Register Contents Datapath

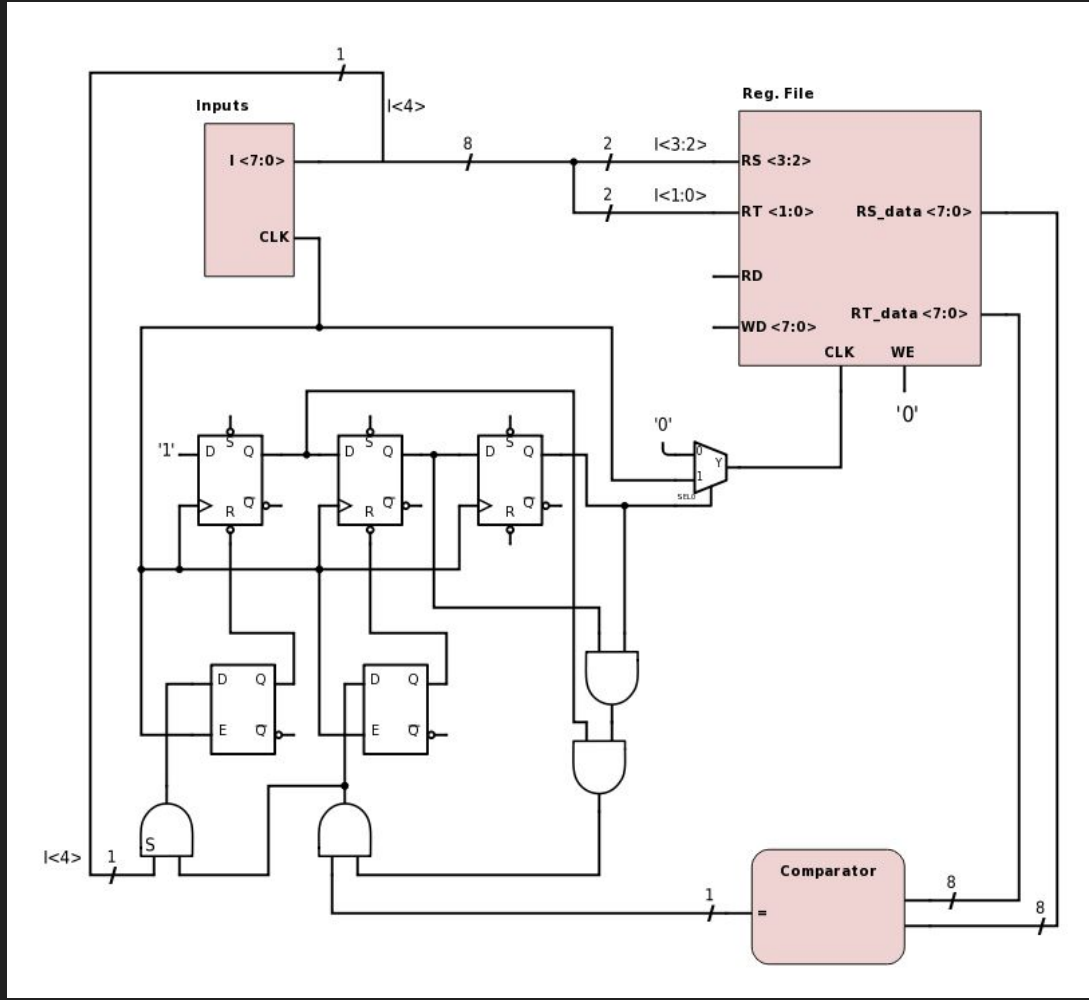


- Print: [0 0 0][RS RS][X X X]

- Originally, our ISA supported 3 output formats (decimal, hex, and ASCII) by setting the bottom 3 bits.
- Those last three bits are now dropped (i.e., don't care what they are), and the register contents are printed in decimal form always.

Skip Instruction(s) Datapath

- Skip Instruction: [0 0 1] [S] [RS RS] [RT RT]
- S + 1 instructions are skipped if RS[Data] = RT[Data].



Complete Datapath - Control Signals