Compas'2019

HARDWARE ASSISTED VIRTUAL MACHINE PAGE TRACKING

PhD Student : **Stella Bitchebe**[1]

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Anglet, June 2019

CONTEXT

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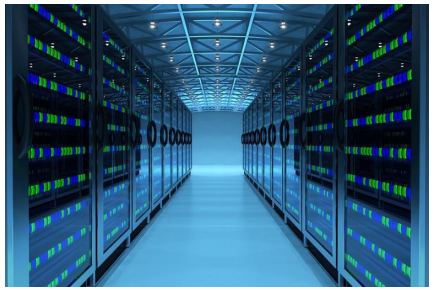
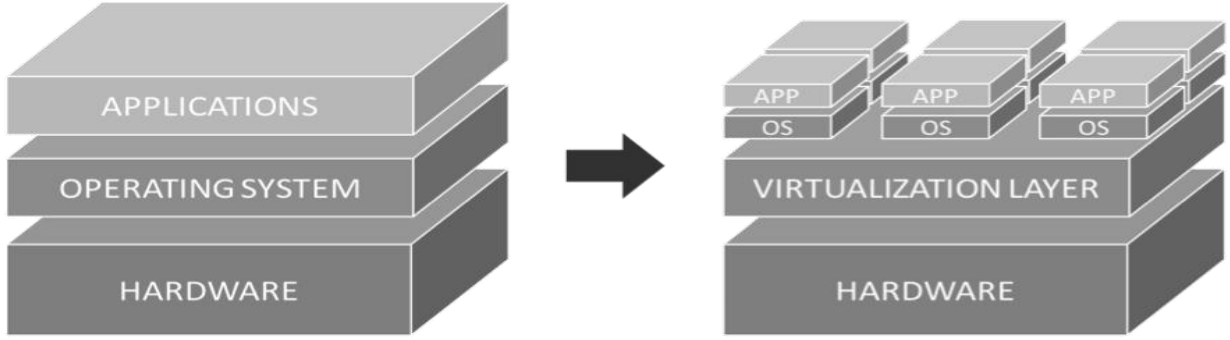
- Virtualization as the foundation of DataCenters.

Datacenter



50 - 70% of expenses

Energy saving



TRADITIONAL ARCHITECTURE

VIRTUAL ARCHITECTURE

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Page Modification Logging (PML)

PAGE MODIFICATION LOGGING

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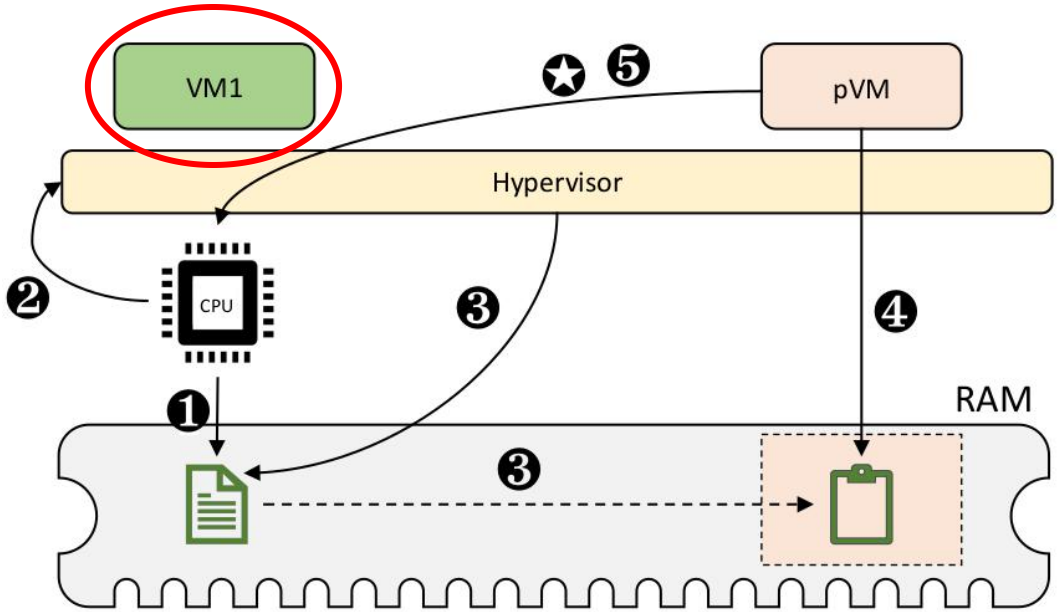
How does it work?



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- Backup / log buffer
- pVM's memory
- ✪ PML activation
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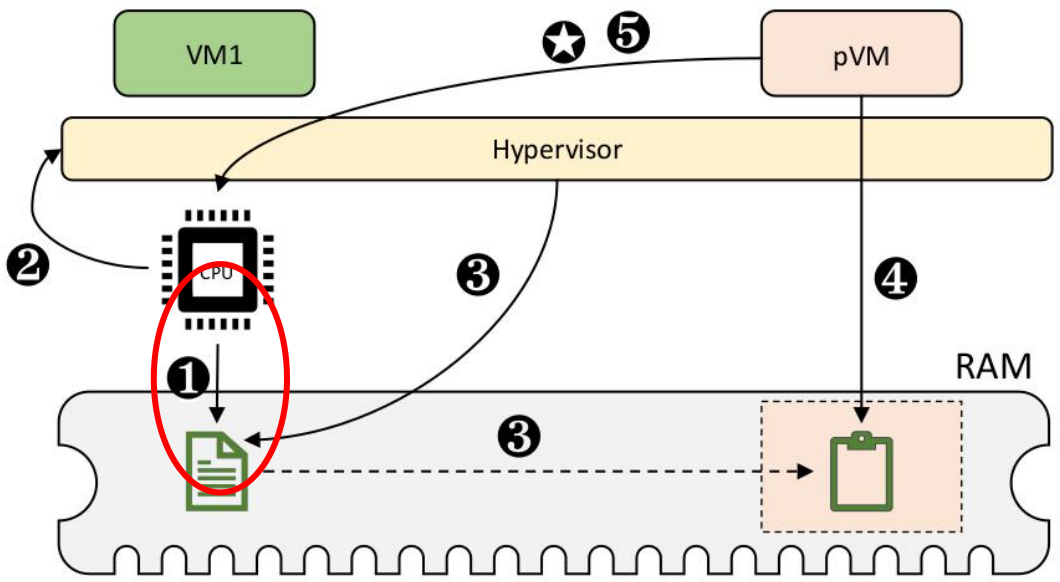

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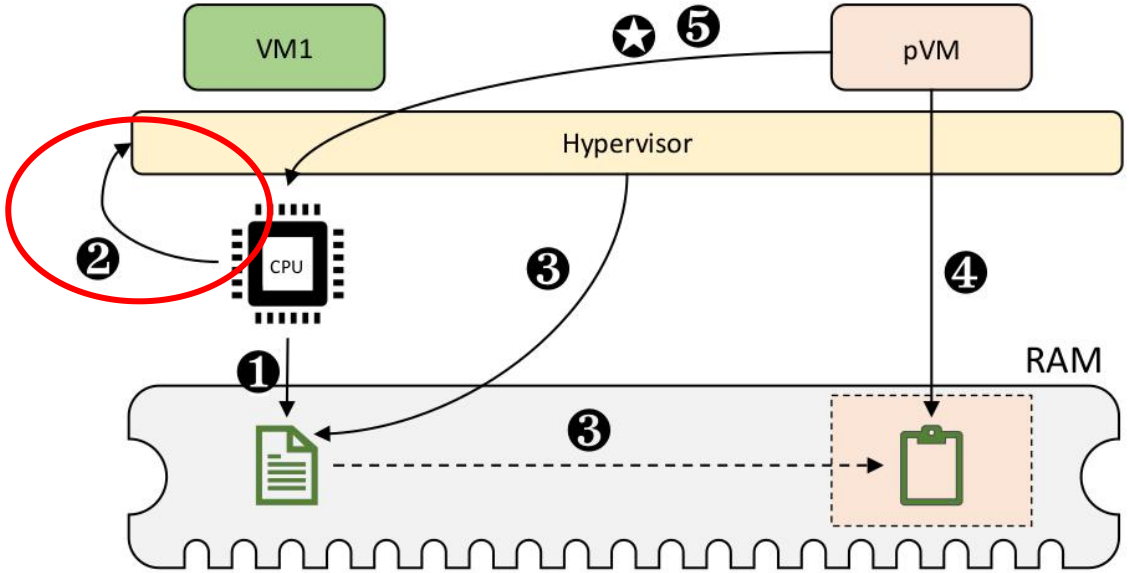

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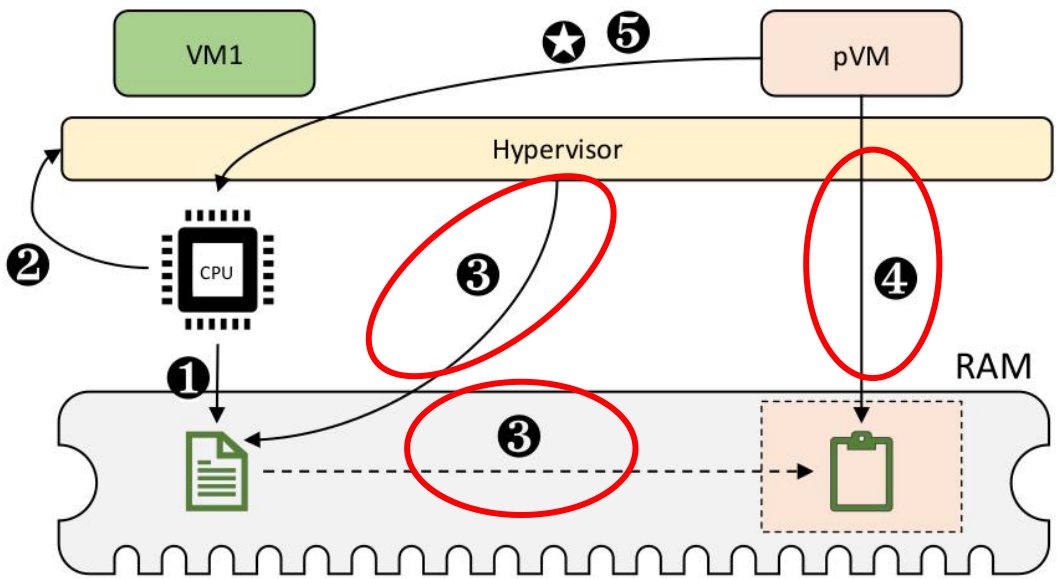

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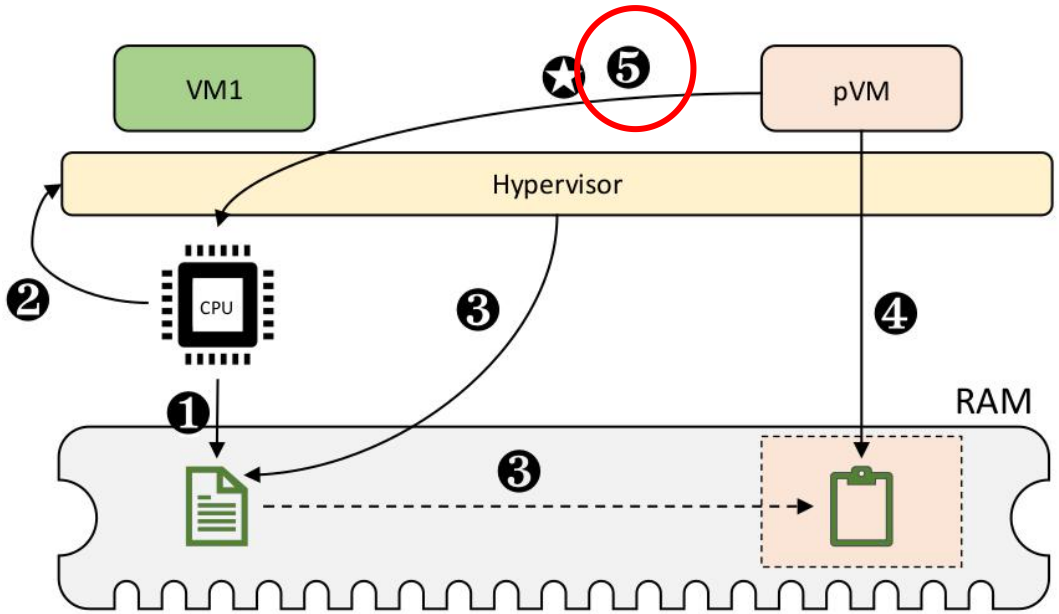

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PAGE MODIFICATION LOGGING (PML)

Study of PML from 3 angles

Energy consumption

Effectiveness

Performance overhead

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Study of Intel PML: Energy consumption

Workload: synthetic application that consists in parsing an array several time

- Each entry points to a 4KB data structure (size of a memory page).
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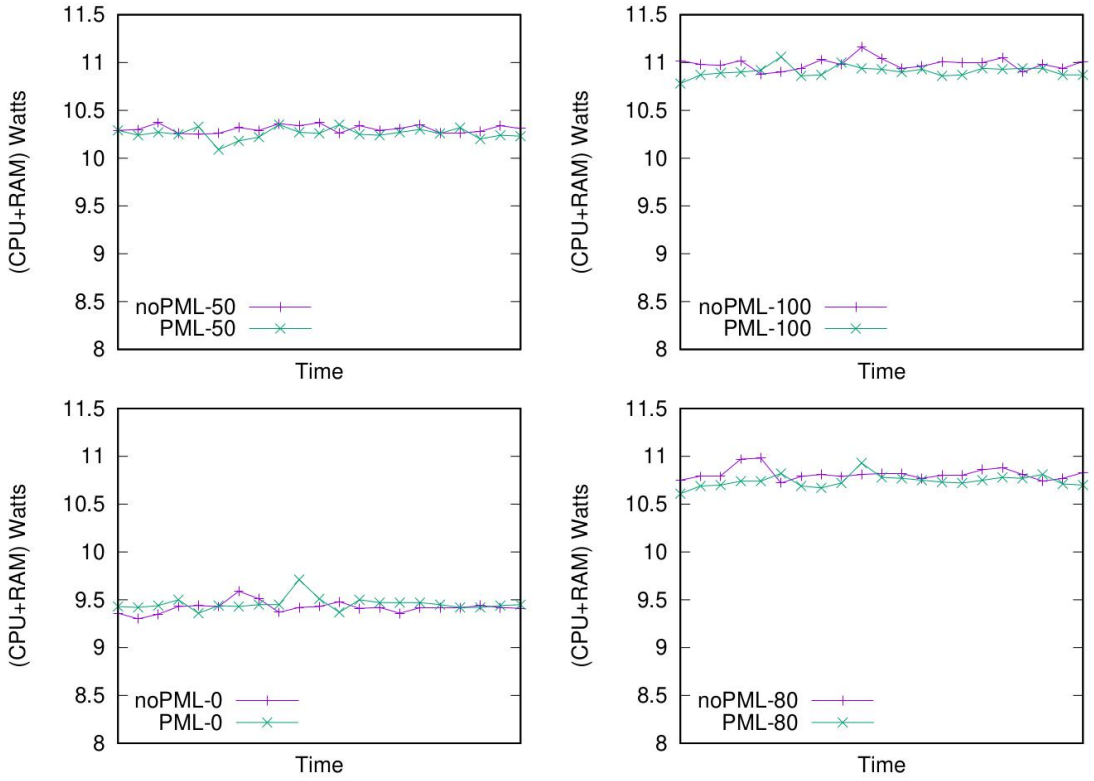

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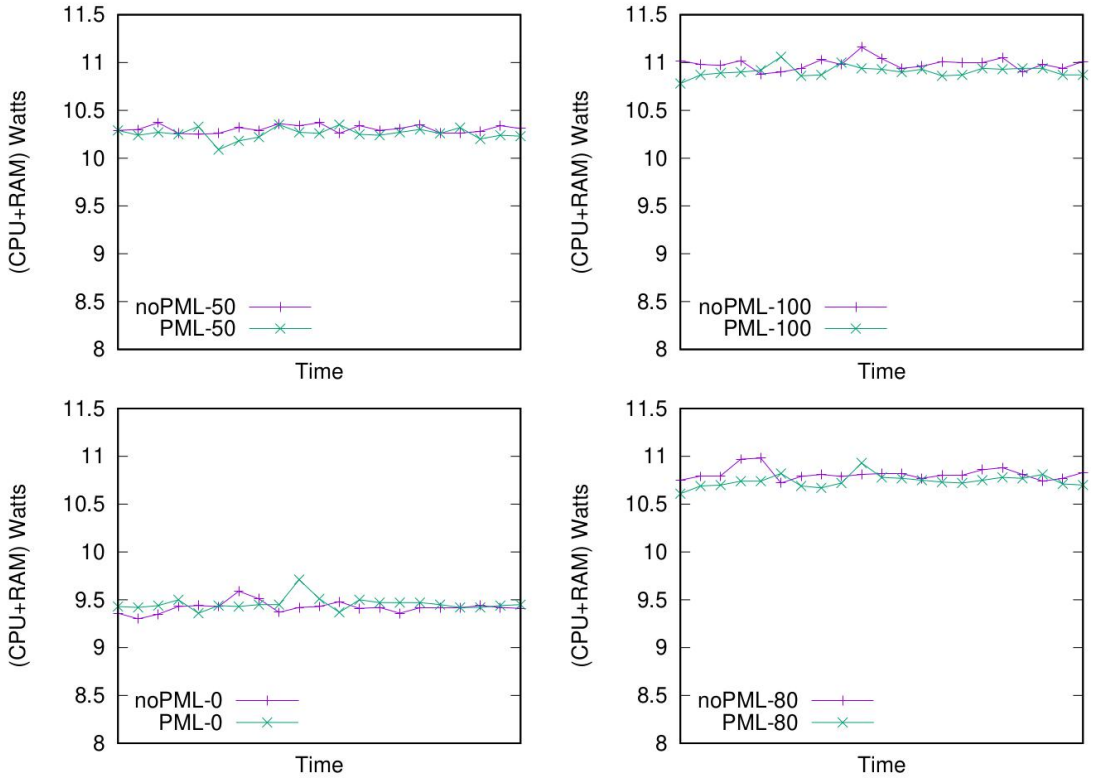

✓ The energy consumption incurred by PML is almost nil.

✓ The energy concumption slightly reduces when the write intensity increases (up to 0.02%): write intensive workloads lead to much VMExits due to *PML log buffer full*, thus reducing the utilization of the CPU.

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Study of Intel PML: Effectiveness for live migration and checkpointing

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- Base line: the classical memory page tracking approach which consists in write protecting memory pages so that next writes lead to page faults.
- Metrics:
  - m_1 the execution time of save(…) method. Tells whether PML accelerates checkpointing/migration
  - m_2 the performance of the user application. Allows to check whether PML reduces or increases the negative impact of these operations on the user application.

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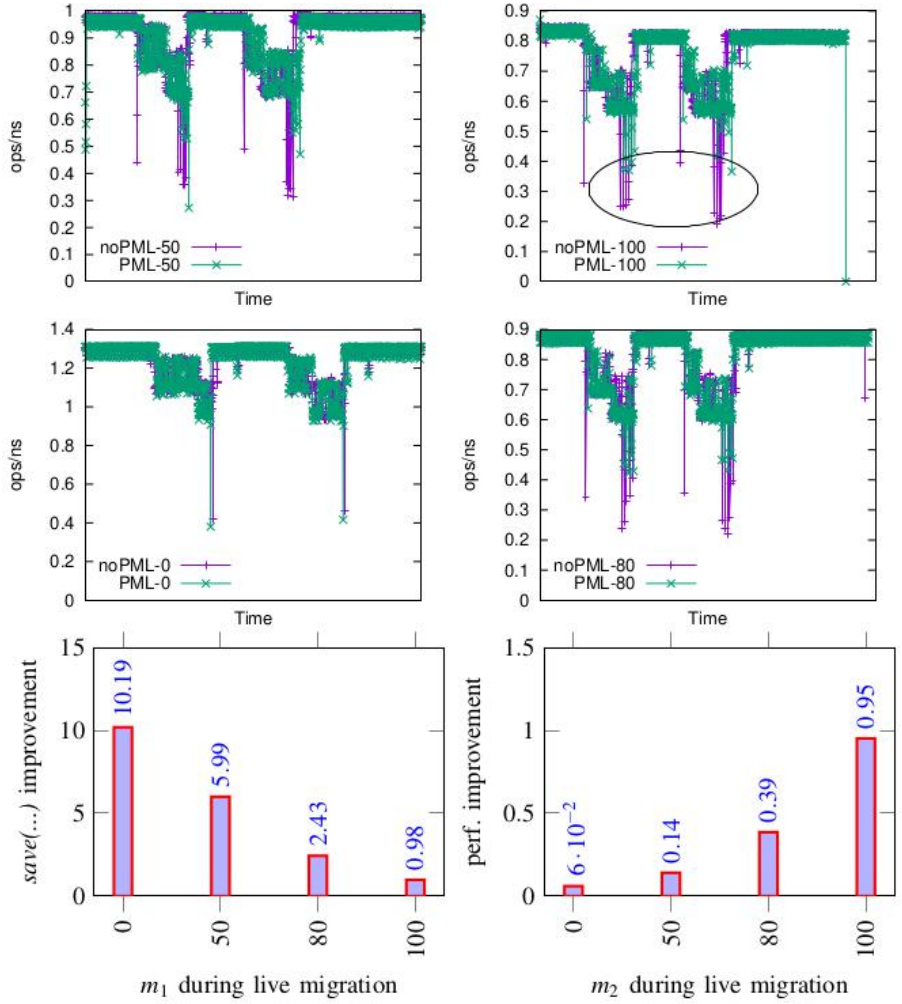
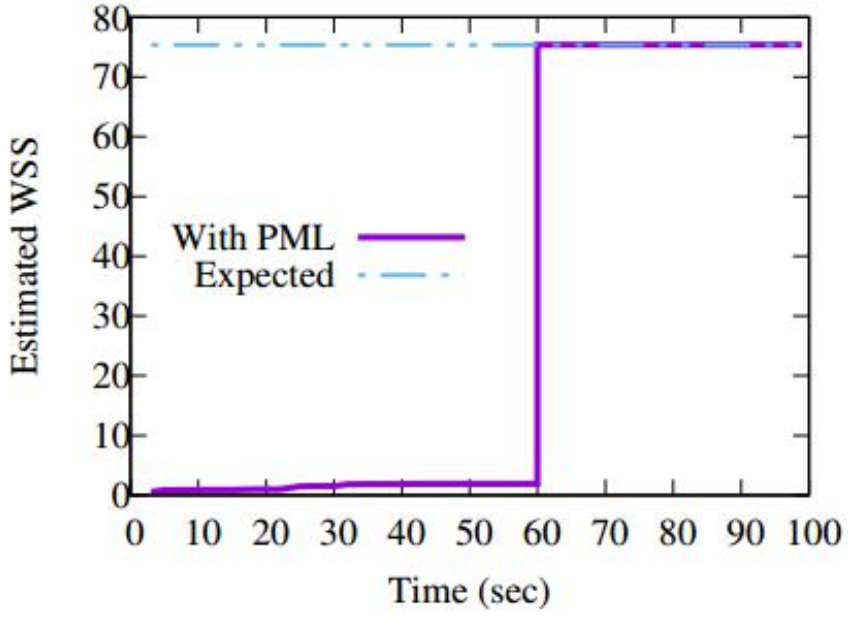
- Observations:
  - **PML reduces the duration of save(...) method by 0.98%-10.18% (the leftmost curve in line three of the figure)**.
  - **PML slightly reduces down to 0.95% the negative impact of live migration (the rightmost curve in line three of the figure)**.



PAGE MODIFICATION LOGGING (PML)

Study of Intel PML: Effectiveness for WSS estimation

- WSS estimation system which relies on PML (in the XEN hypervisor).
- The implemented system cannot be accurate in respect with the current PML design.
- Two reasons for this issue:
  - Only modified pages are recorded. However, the WSS of a VM should include both read and write pages.
  - It is not possible to track only hot pages. In respect with the current PML design, a page is logged only once.



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Study of Intel PML: Performance overhead

$$T = T_{PTW} + N \times (T_x + T_e + T_h):$$

- N: number of log full events. Depends on the workload type.
- T_{PTW}: overhead incurred by PML in the page table walker process.
- **T_x , T_e :** respectively the time needed for performing a VMExit, VMEnter. Are constant.
- **T_h**: time needed for performing *log full* handler. Depends on the virtualization operation for which PML is used and is very high.

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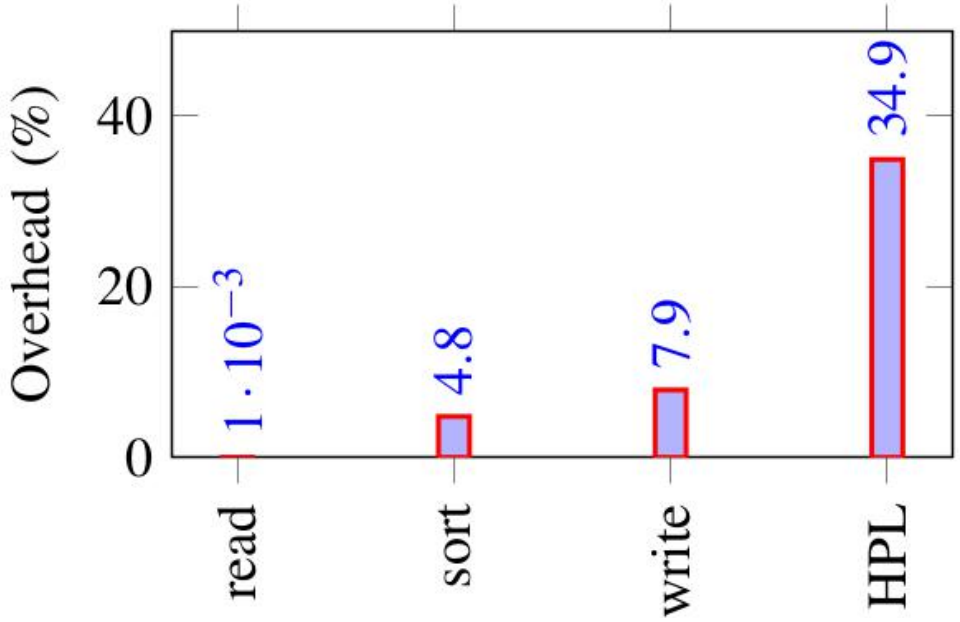


- Read intensive applications are not impacted (about 0.001% of overhead).
- For write intensive applications like HPL, the overhead is up to 34.8%.

PAGE MODIFICATION LOGGING (PML)

Study of Intel PML: Limits

The handling of PML *logging buffer full* events is done by the CPU that runs the VM.

The PML mechanism logs only modified pages.

Hot pages cannot be tracked.

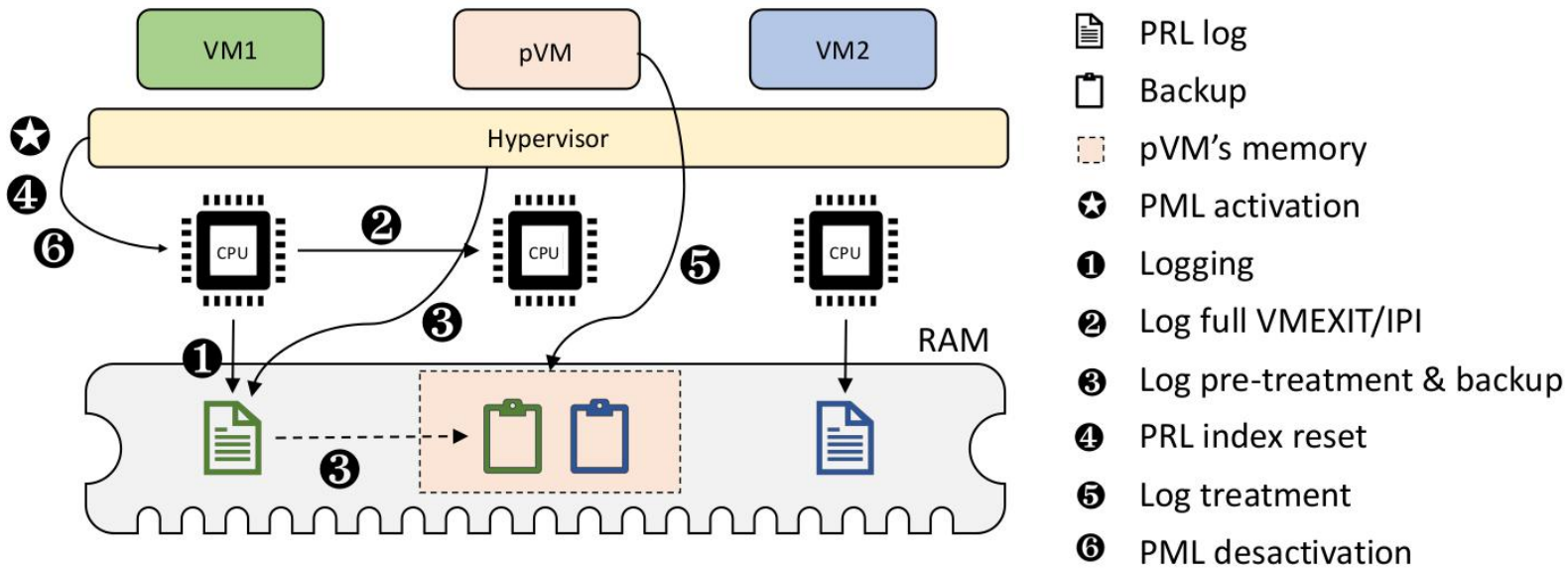
PAGE REFERENCE LOGGING

13/19

PAGE REFERENCE LOGGING (PRL)

Design implemented on Gem5

PRL is an extension of PML for making the latter usable for WSS estimation.



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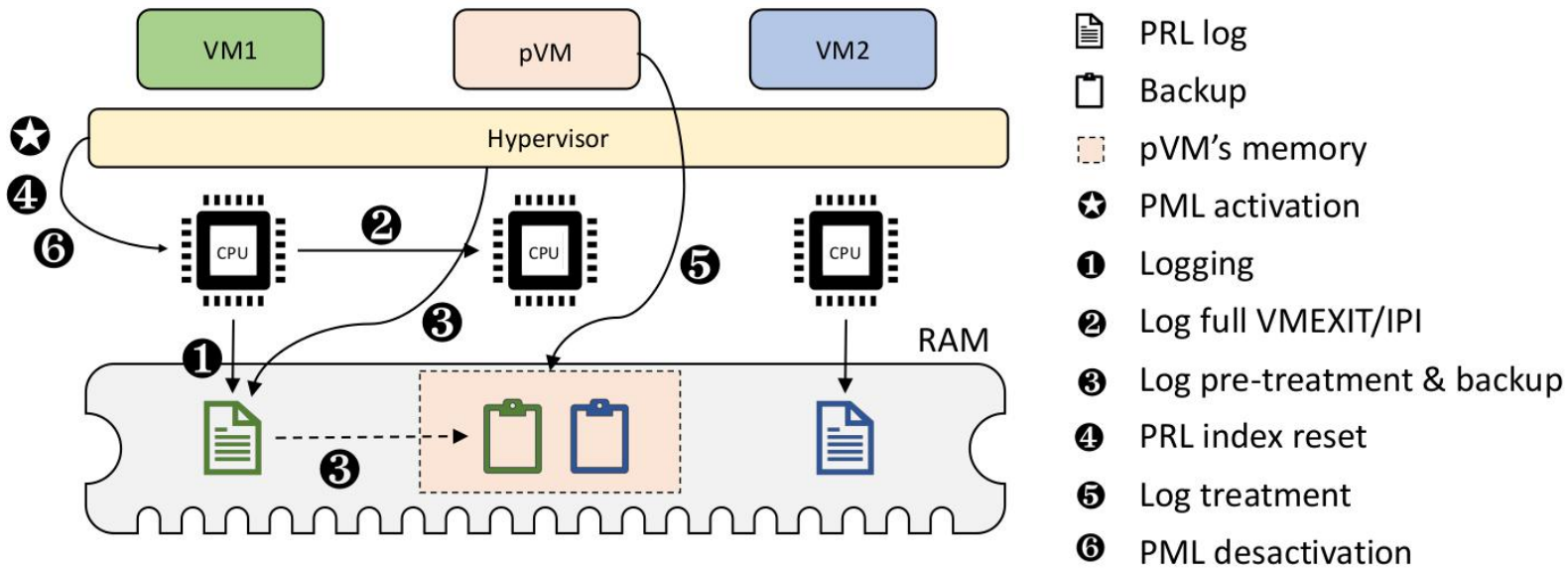

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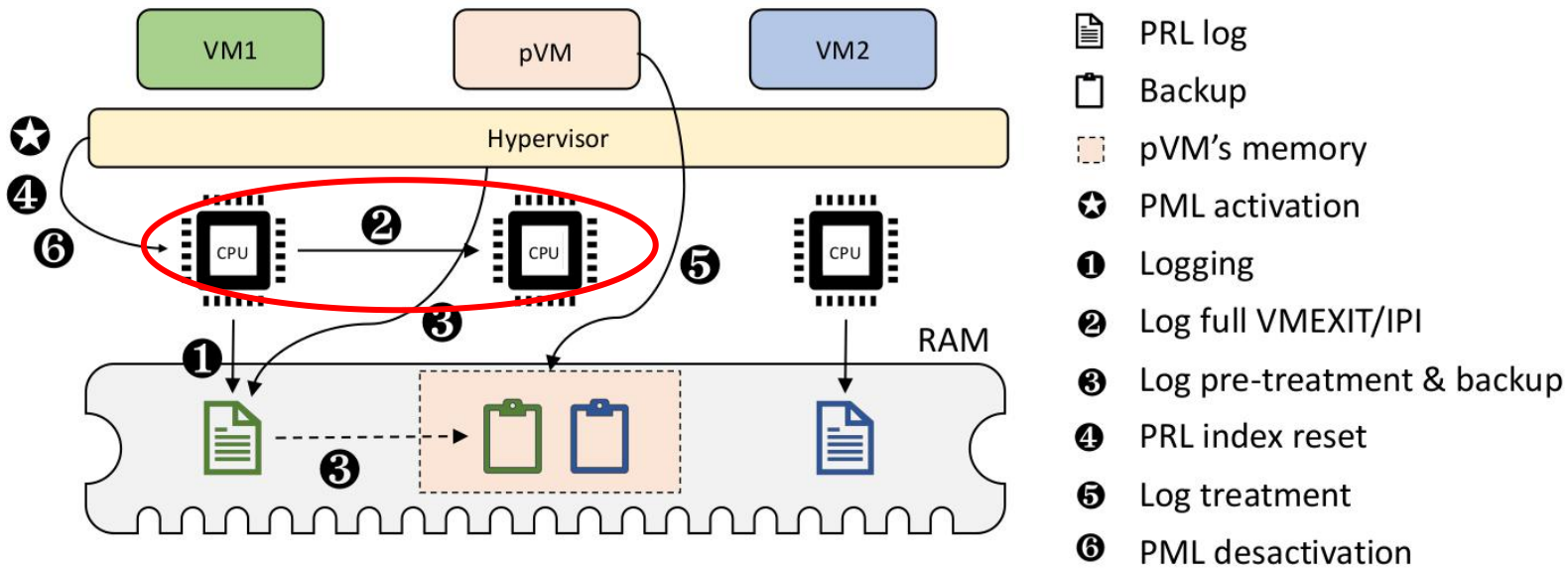

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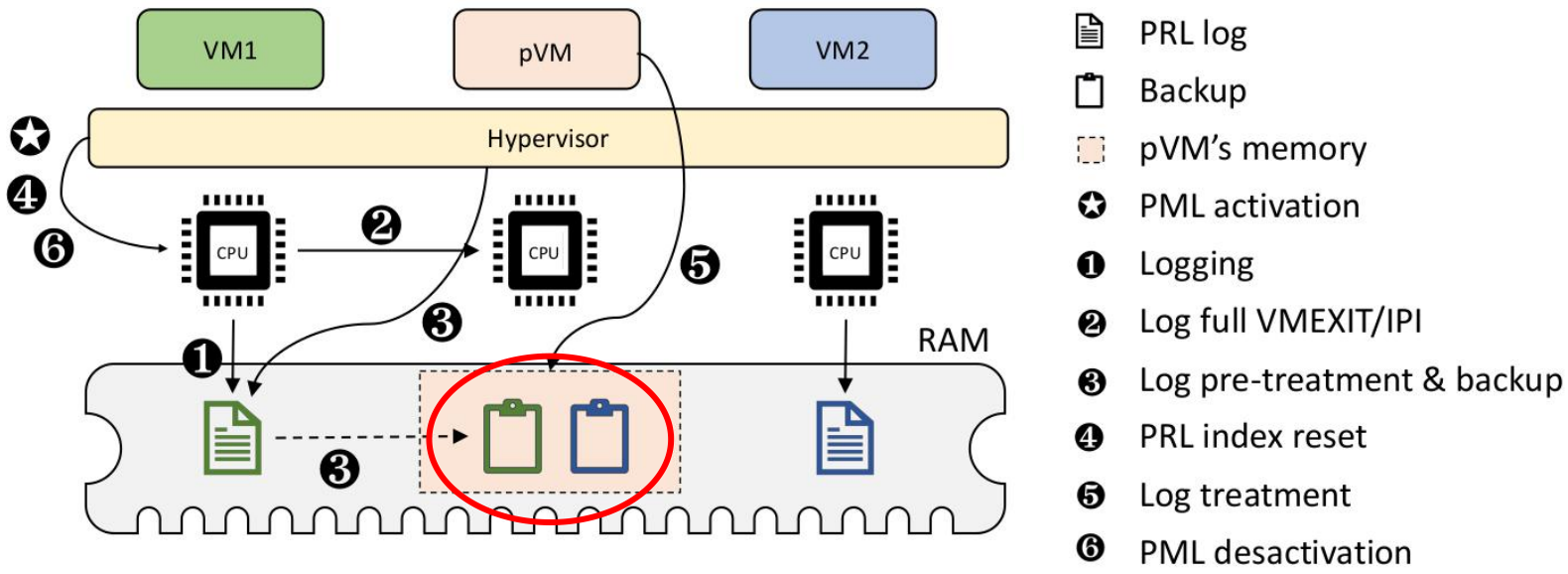

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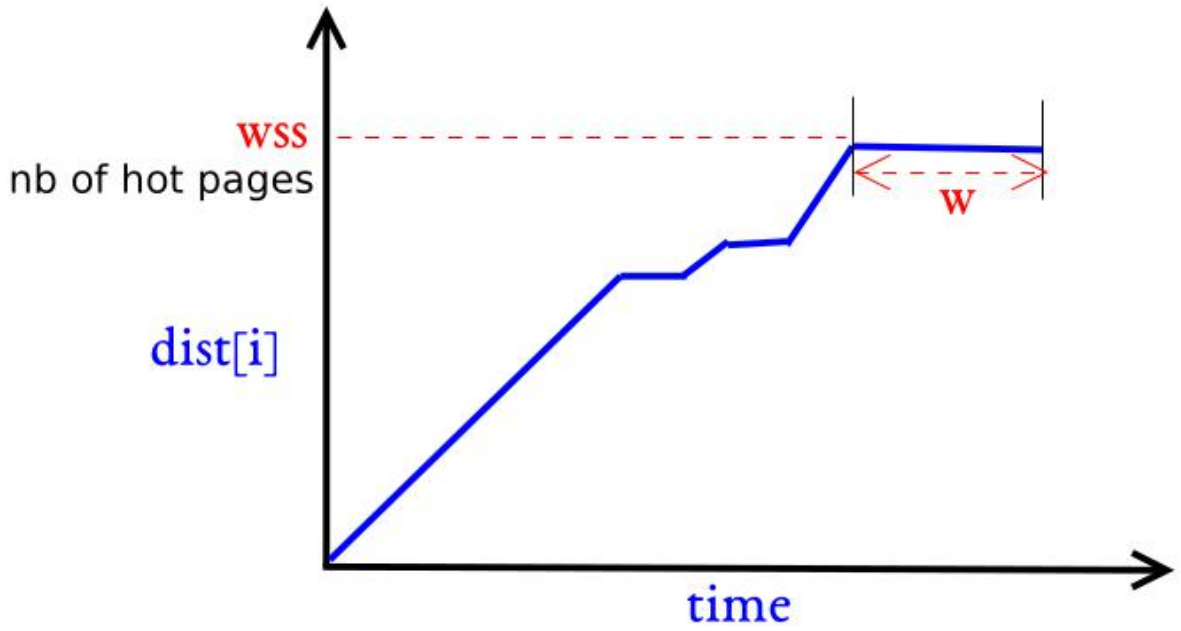

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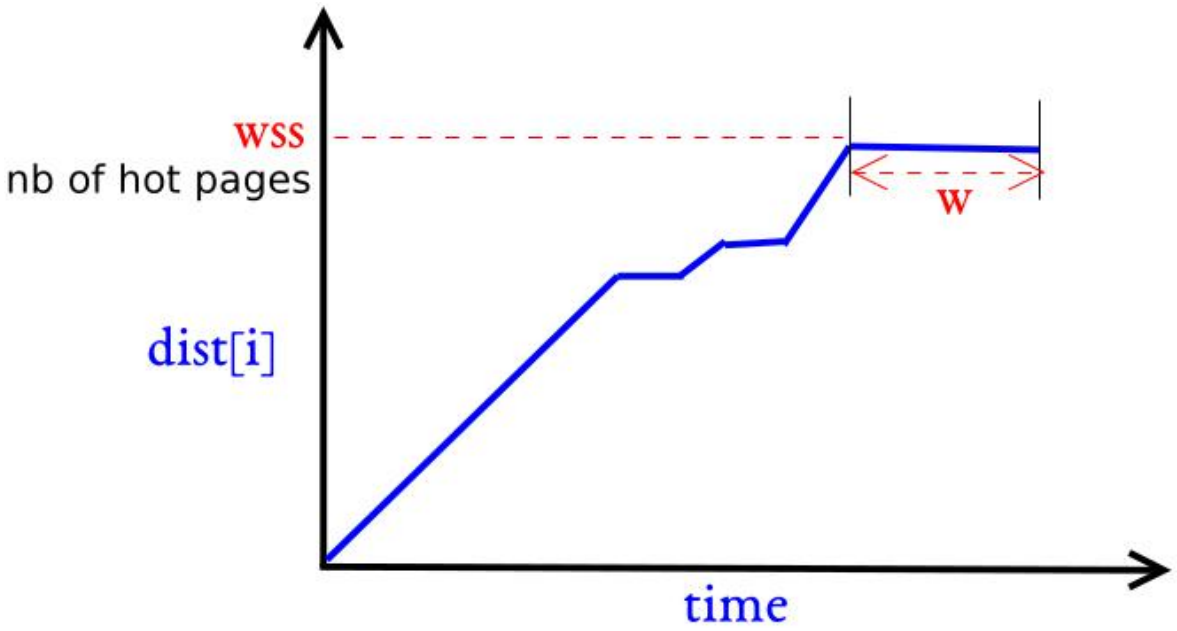

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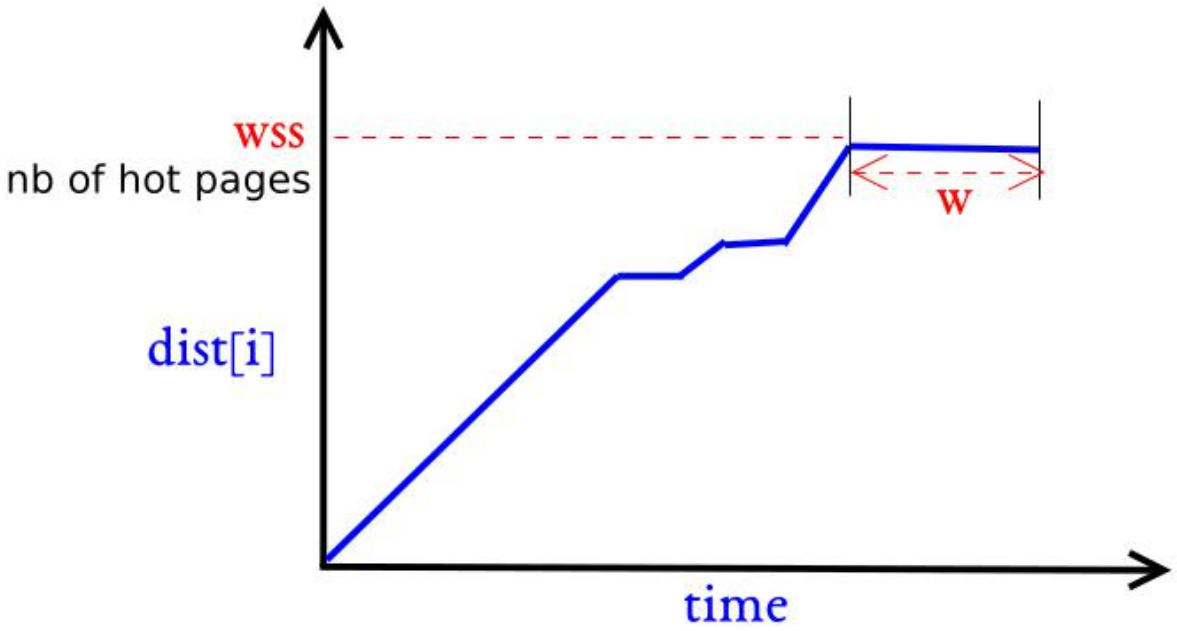

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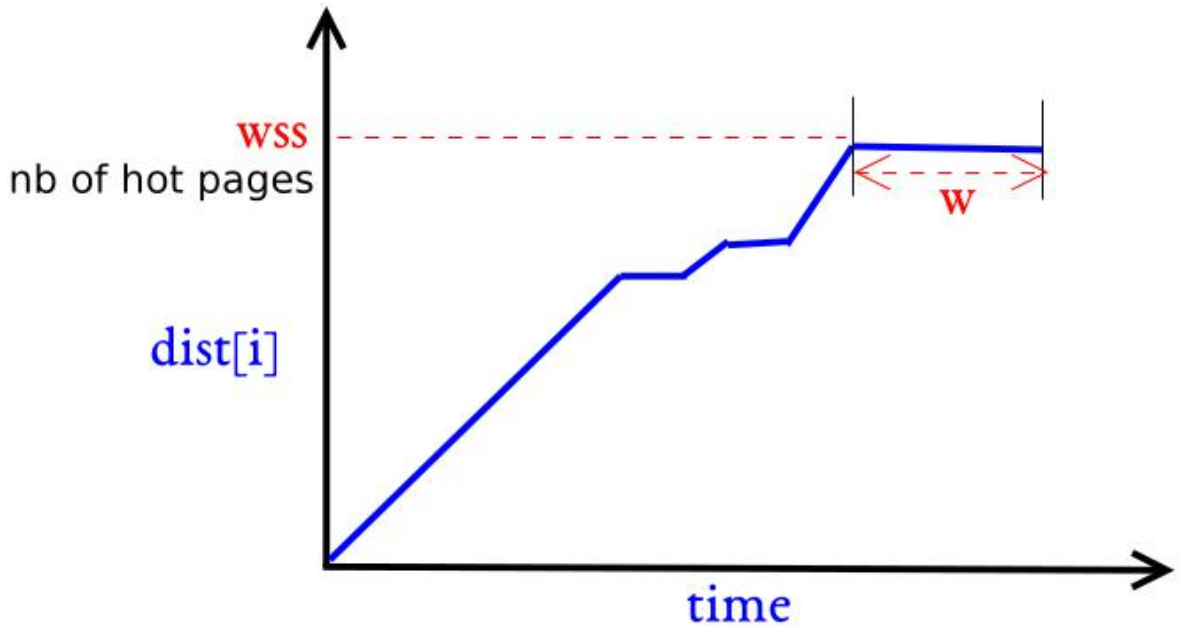

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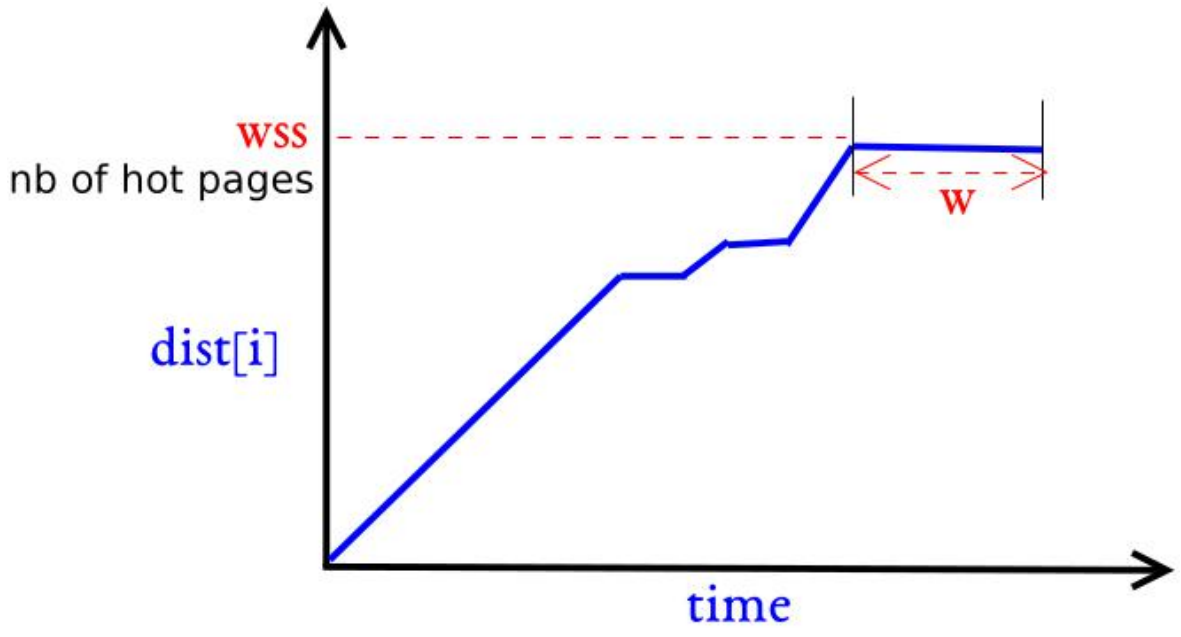

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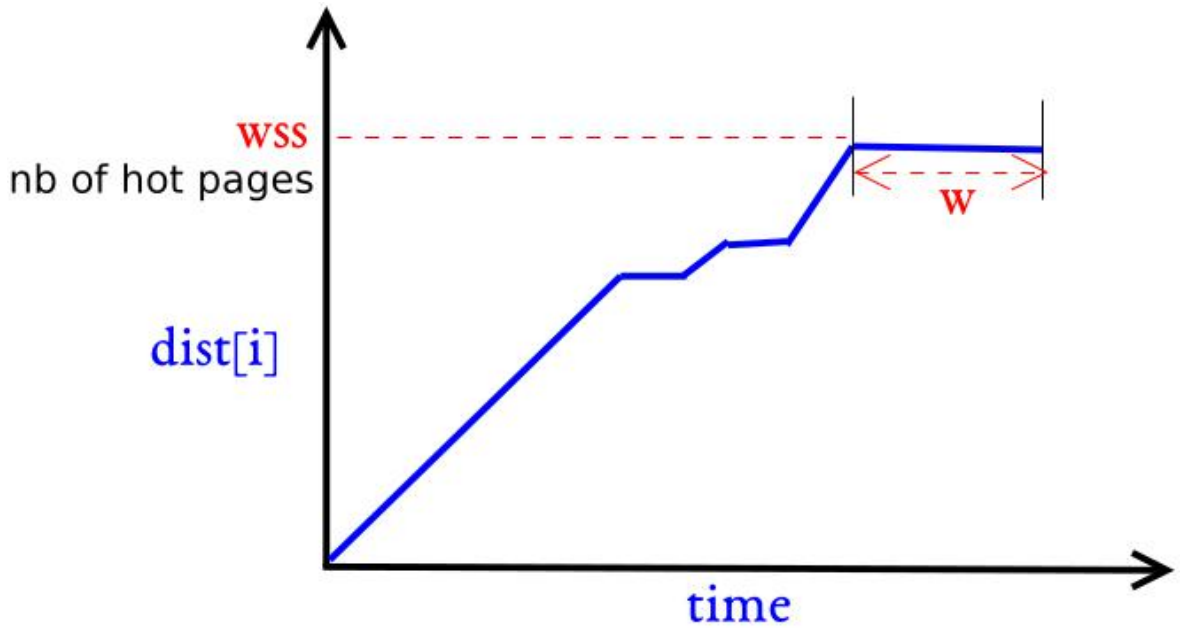

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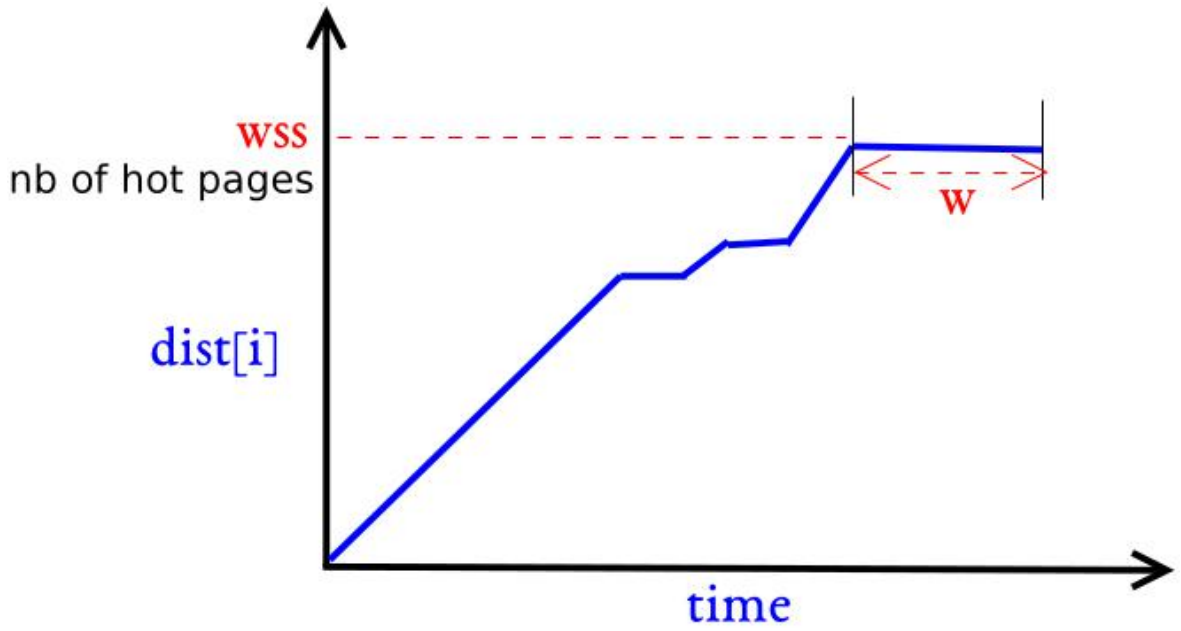

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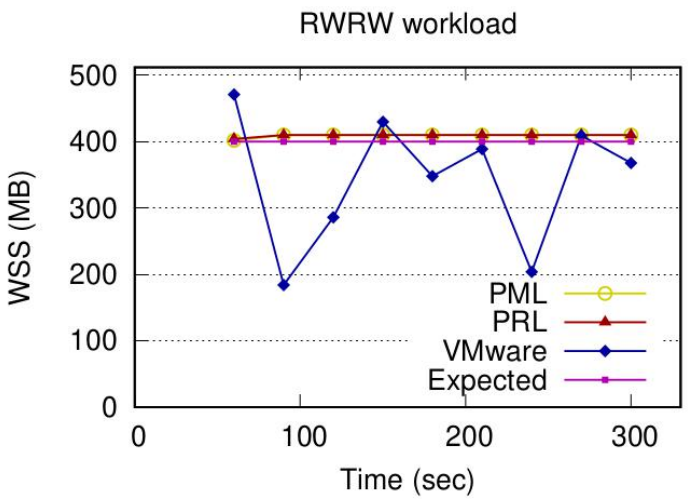
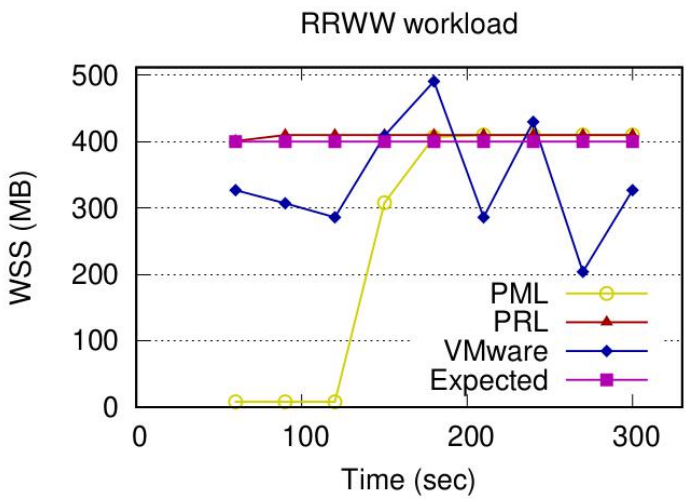
  - **dist[i]**: number of distincts GPAs present in the log which has been logged more than τ times

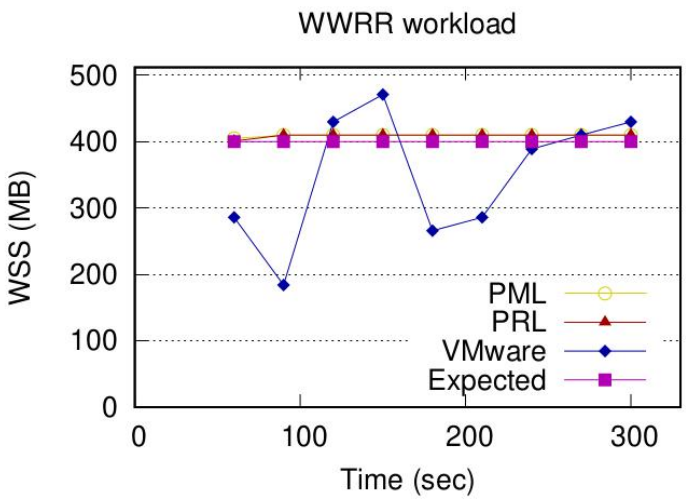
PAGE REFERENCE LOGGING (PRL)

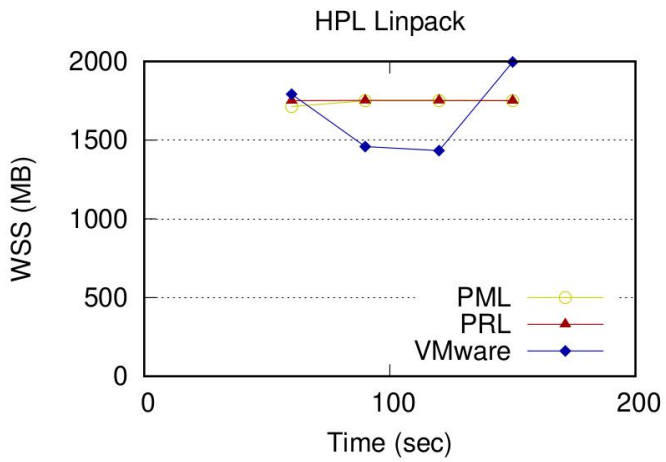
Evaluation of the accuracy

R: read W: write









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- ✓ We implemented PRL in Gem5, a popular hardware simulator and described a WSS estimation system which leverages PRL.
- ✓ We evaluated our solution using both real and synthetic applications, and compared it with VMware's WSS estimation solution. Our results demonstrate that, unlike VMware, our solution is both accurate and does not impact user VMs.

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