ELP718 Telecom Software Laboratory
1st Semester, 2016-18
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18 Oct 2016, 5pm
Assignment-11

Contents

0.1 Introduction

This assignment aims to provide a better understanding of the following topics:

1. **Xilinx**
You may know Xilinx because we invented the FPGA. Or maybe you know us because we turned the semiconductor world upside down and created the fabless model. With over 3500 patents and more than 60 industry firsts, we continue to pioneer new programmable technology putting our customers first. Today Xilinxs portfolio combines All Programmable devices in the categories of FPGAs, SoCs, and 3DICs, as well as All Programming models, including software-defined development environments. Our products are enabling smart, connected, and differentiated applications driven by 5G Wireless, Embedded Vision, Industrial IoT, and Cloud Computing.

2. **VHDL**
VHDL (VHSIC Hardware Description Language) is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits. VHDL can also be used as a general purpose parallel programming language.

0.2 Problem Statement 1

Model and simulate a 10 bit digital comparator with the following requirements: Active low reset,Active low Chip select Input- Two 10 bit words for comparison,a flip input bit/flag. Output- 4 LEDs at the output for greater than,less than,equal and flipped mode status.

0.2.1 Assumptions

The input bit streams do not change during testbench execution.

0.2.2 Structure Chart and Implementation

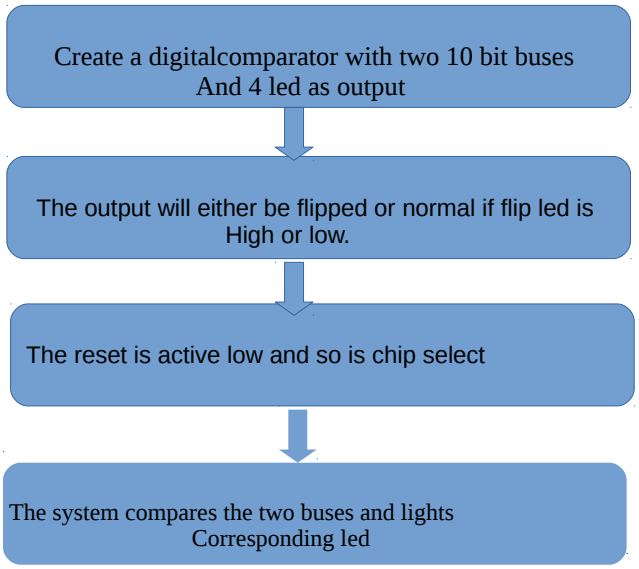

Figure 1: Structure chart for problem 1

0.2.3 Screenshots

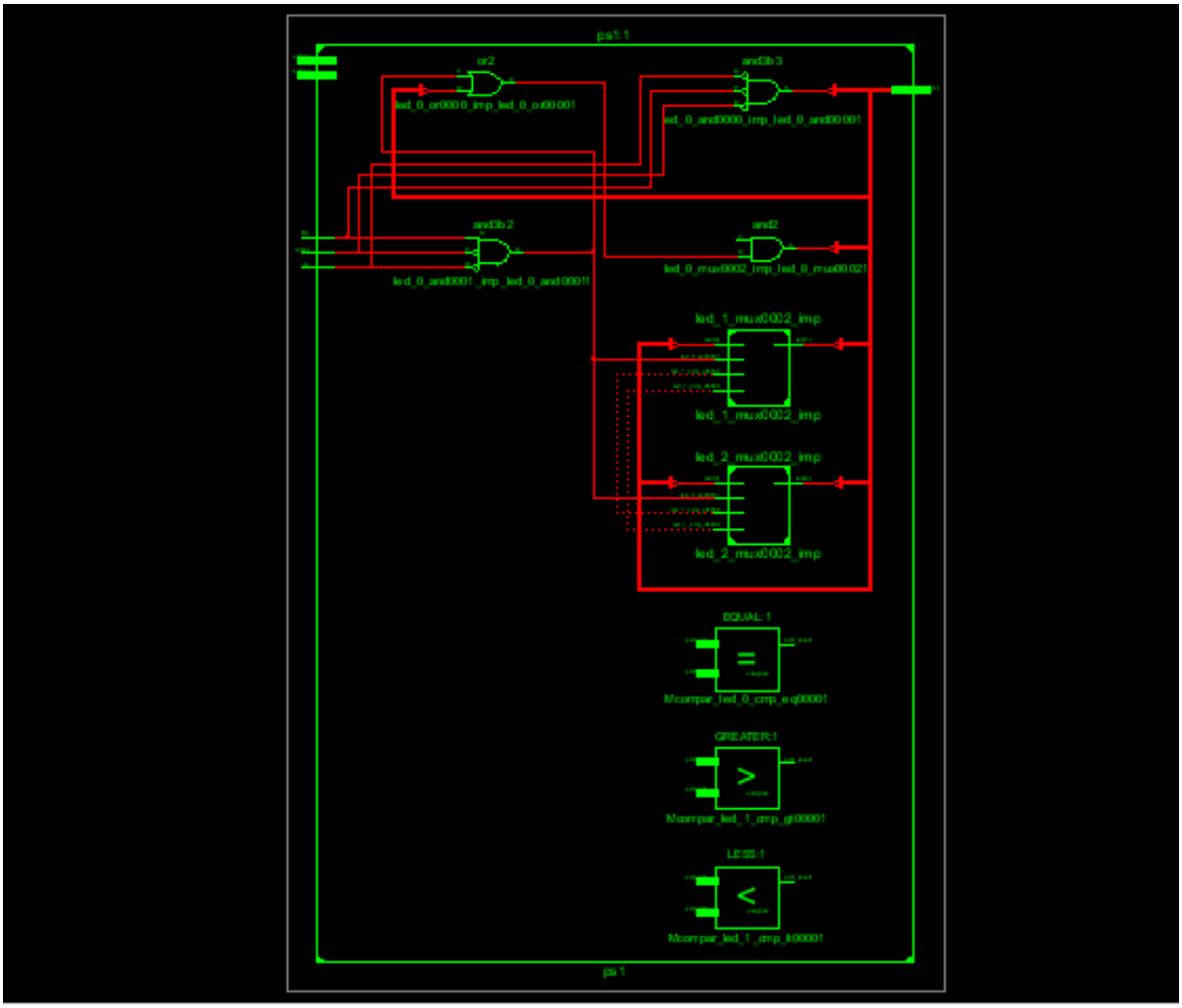

Figure 2: Screenshot for problem statement 1

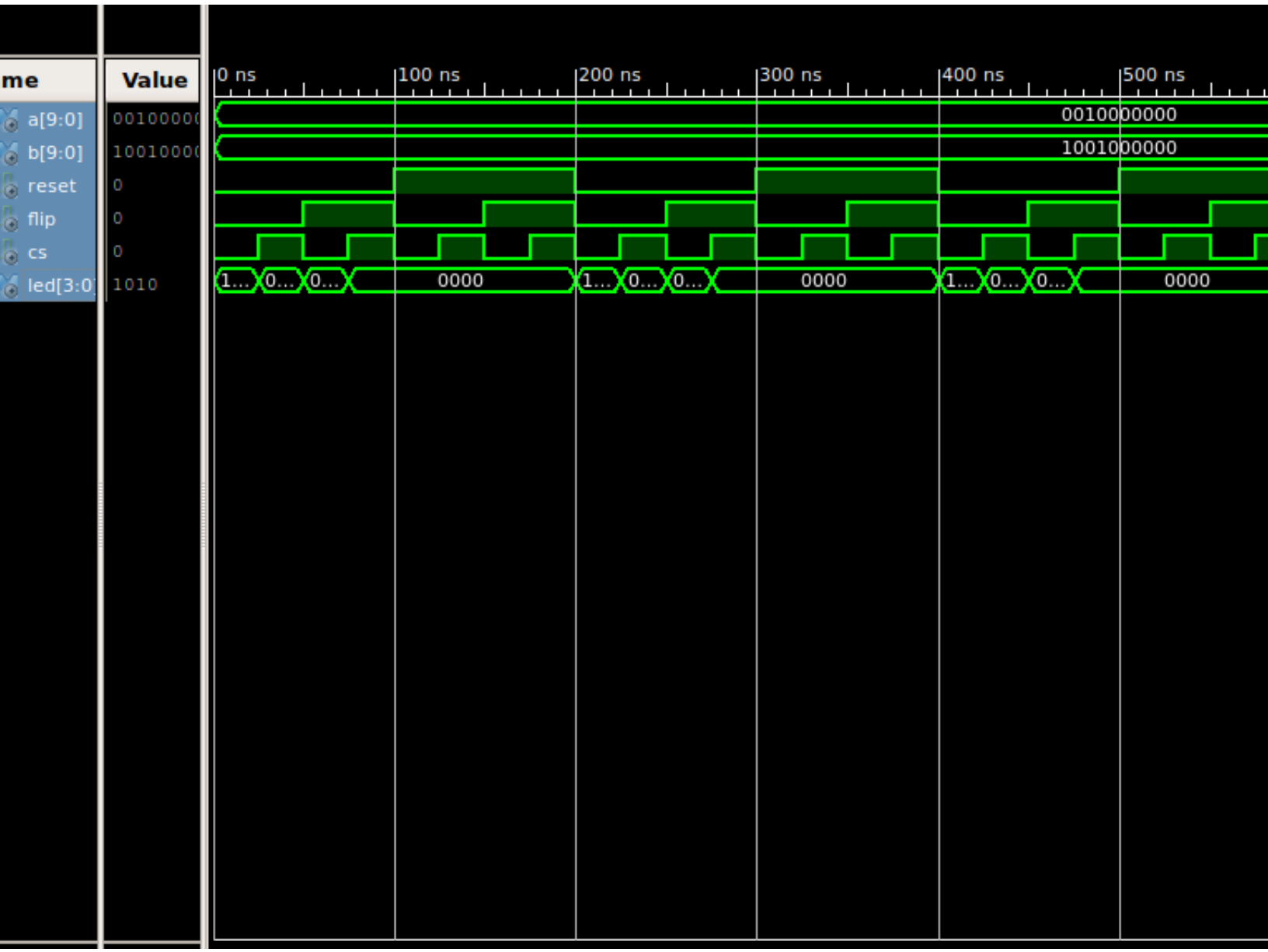

Figure 3: Screenshot for problem statement 1

0.3 Problem Statement 2

Model a hardware for detecting a pattern of bits 11001 in the input bit stream. The output LED must glow when the detection is successful.
Use Moore state machine for your design,simulate it in vhdl and generate the corresponding RTL for the same.Include an asynchronous reset input in the design for resetting to the initial state when the hardware is switched on.

0.3.1 Assumptions

Overlapping is possible.

0.3.2 Structure Chart

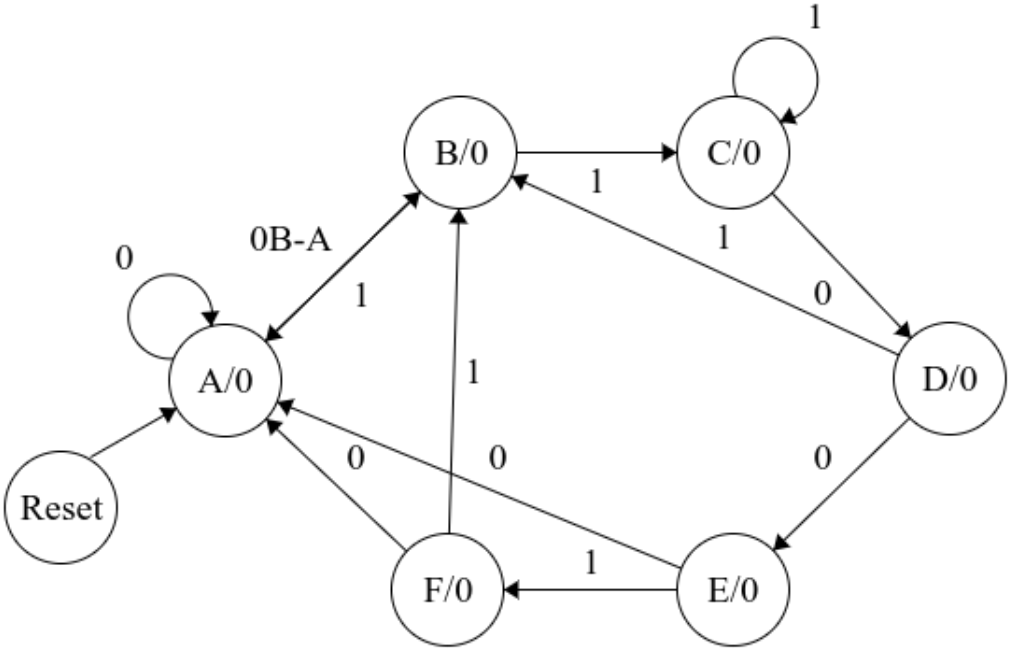

Figure 4: Structure chart for problem 2 - moore implementation

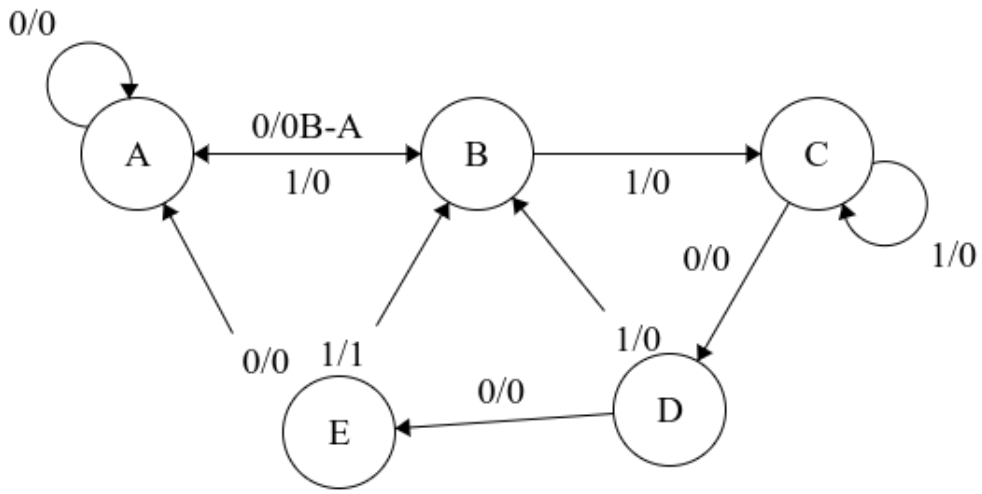

Figure 5: Structure chart for problem 2 - mealy mplementation

0.3.3 Screenshots

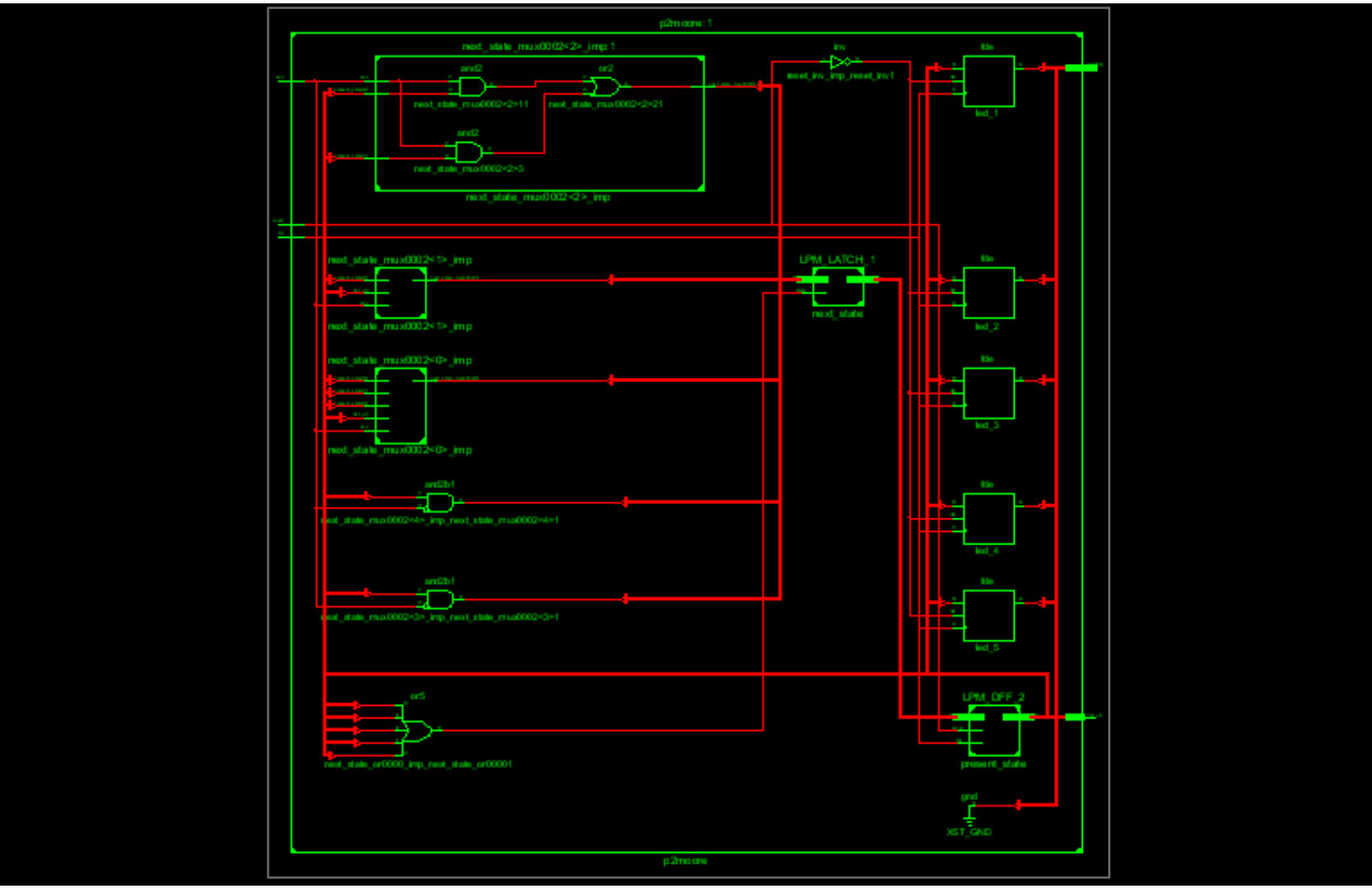

Figure 6: Screenshot for problem statement 2

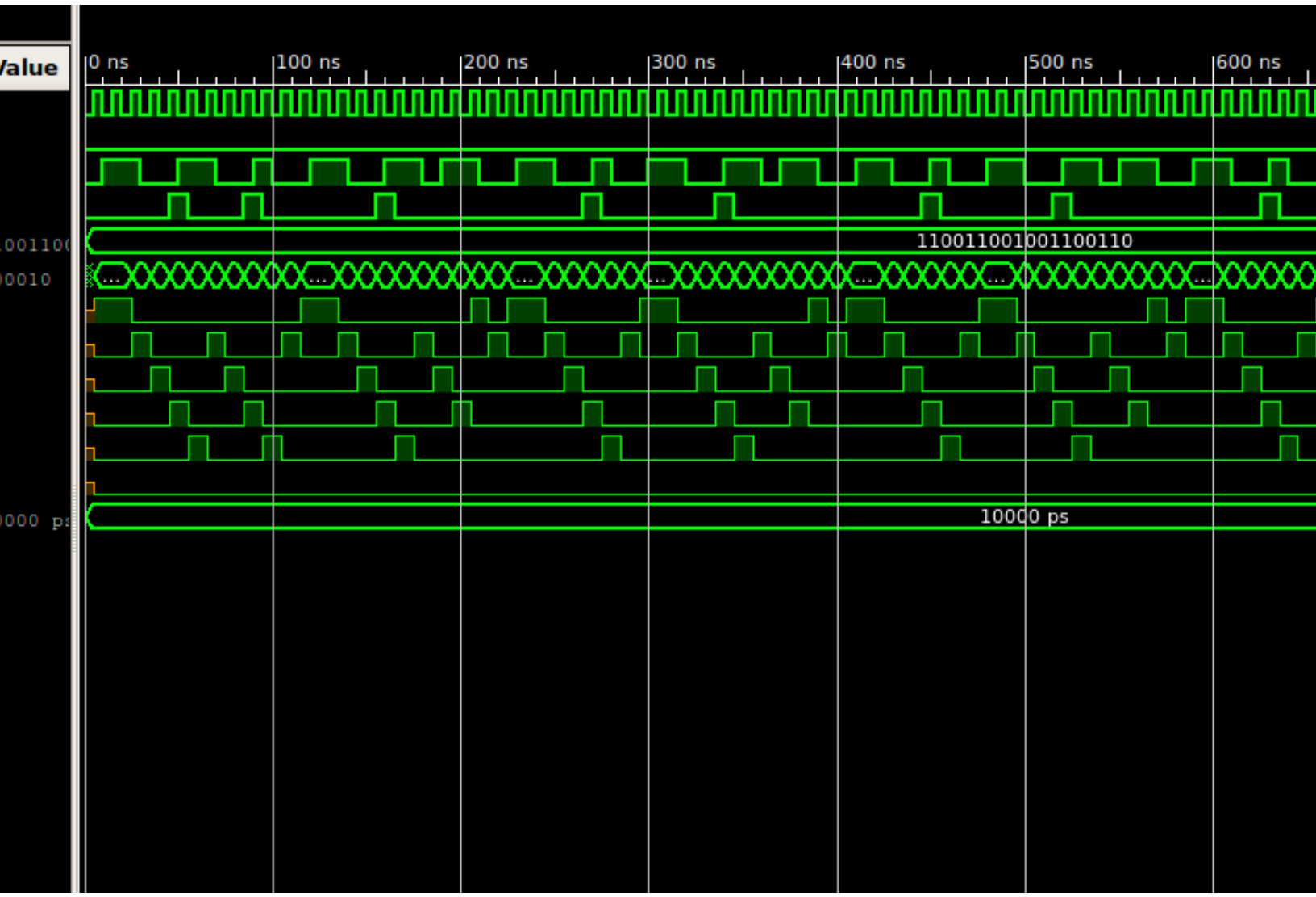

Figure 7: Screenshot for problem statement 2

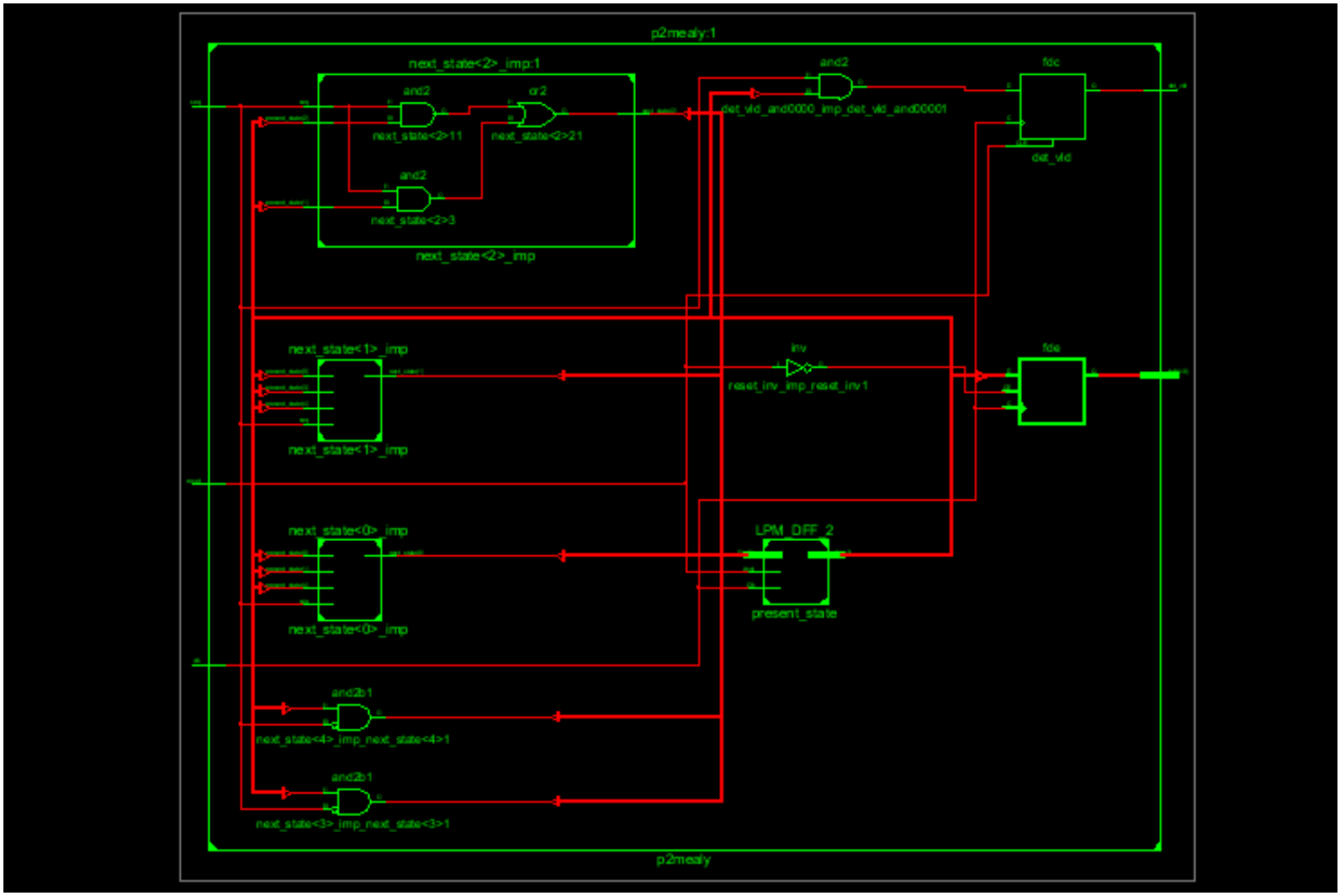

Figure 8: Screenshot for problem statement 2

Figure 9: Screenshot for problem statement 2

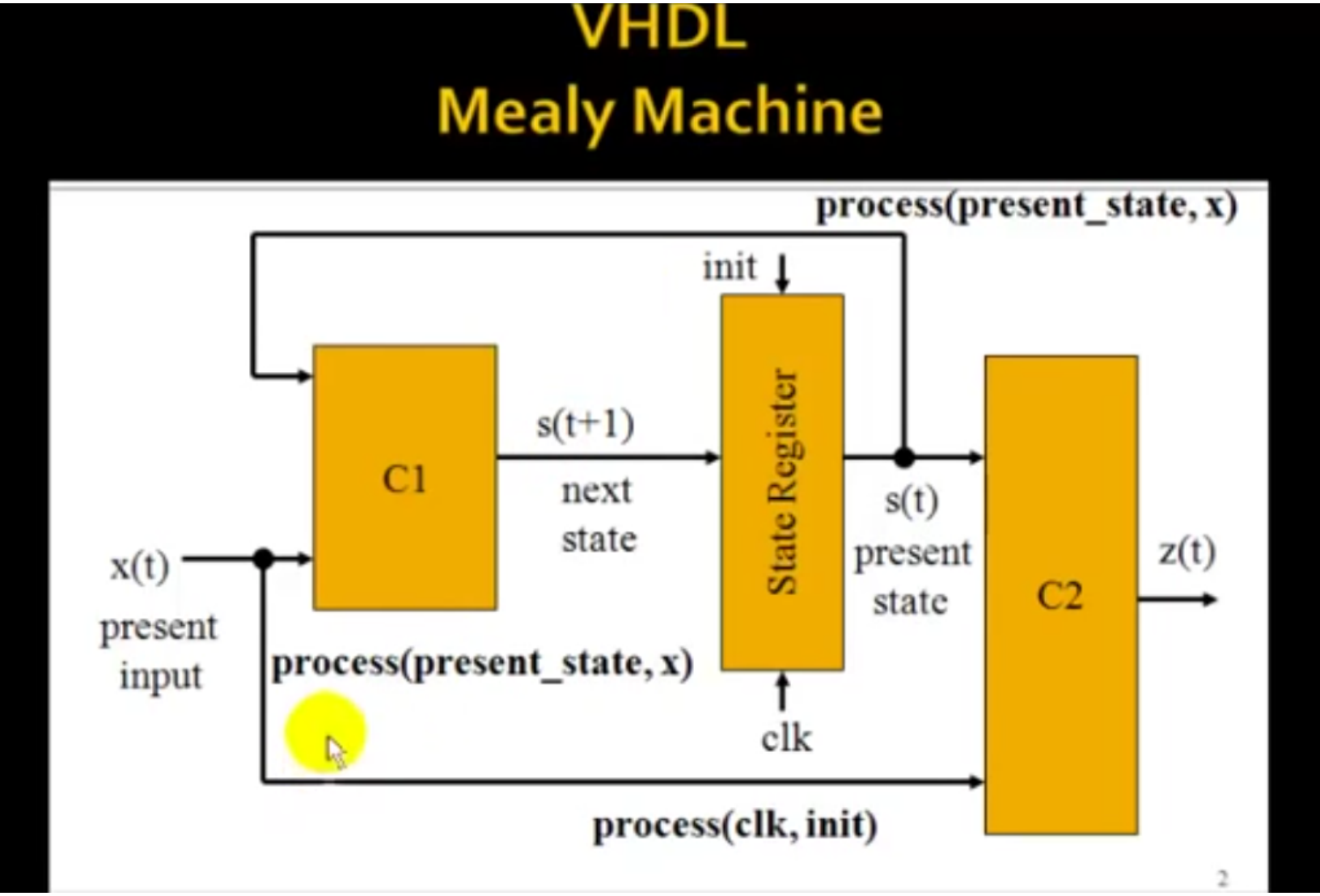

Figure 10: Screenshot for problem statement 2

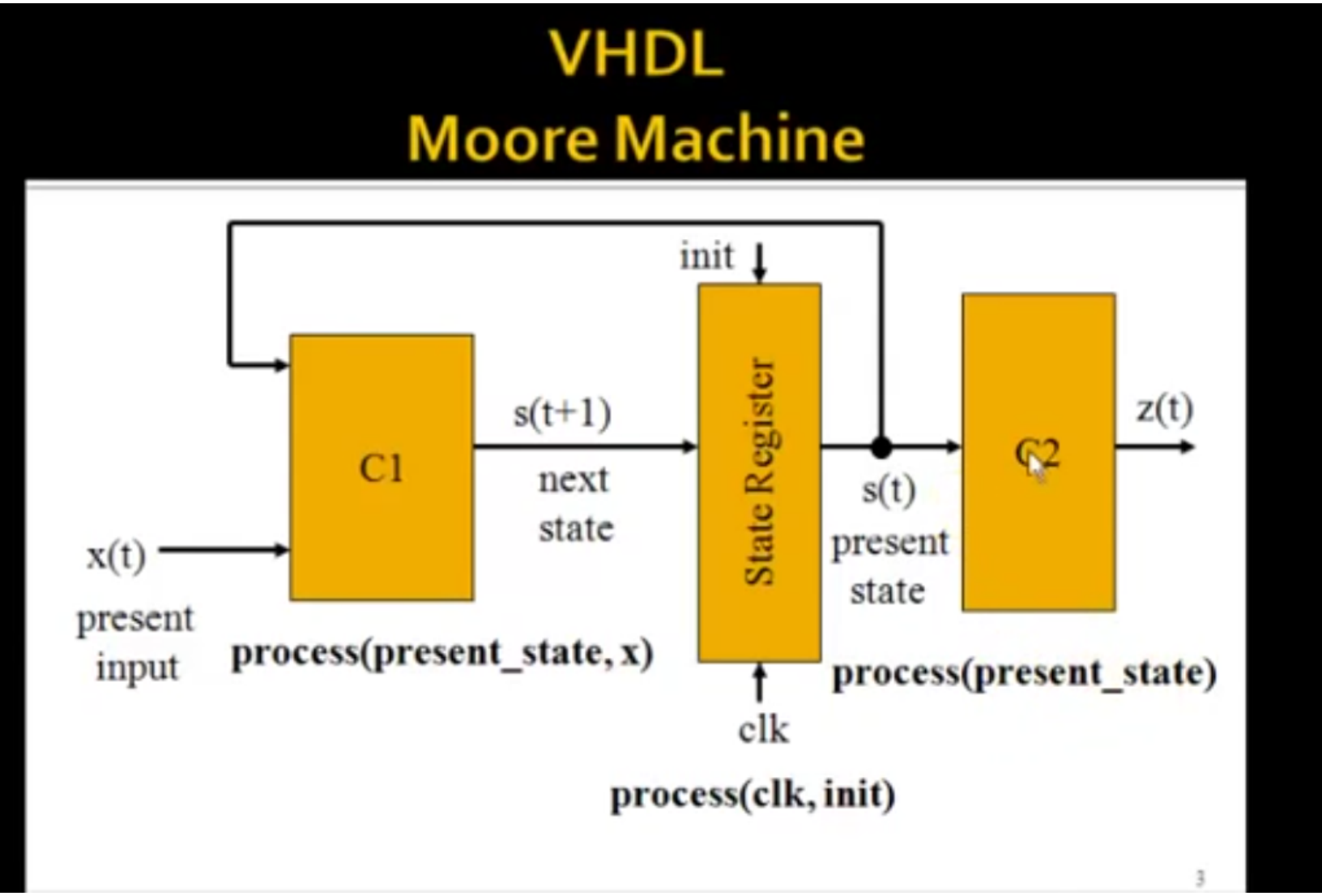

Figure 11: Screenshot for problem statement 2

0.4 Epilogue

The execution of the first problem involved writing of a vhdl module with a testbench.The module had two buses that were to be compared with each other. The execution of the second statement had been done in two ways - Moore machine and mealy machine.
Mealy machine : A Mealy Machine is an FSM whose output depends on the present state as well as the present input. The mealy machine has 5 finite states and the corresponding implementation has been shown here. Moore machine : Moore machine is an FSM whose outputs depend on only the present state. Moore machine has 6 finite states and the difference in implementation can be observed in the code.

Bibliography

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