8-Bit Dynamic-RAM Driver with Three-state Outputs

SN54/74S700/-1 SN54/74S730/-1 SN54/74S731/-1 SN54/74S734/-1

Features/Benefits:

- Provides MOS voltage levels for 16K and 64K DRAMs
- Undershoot of low-going output is less than -0.5 V
- Large capacitive drive capability
- Symmetric rise and fall times due to balanced output impedance
- Glitch-free outputs at power-up and power-down
- 20-pin SKINNYDIP® saves space
- 'S730/734 are exact replacement for the Am2965/66
- 'S700/730/731/734 are pin-compatible with 'S210/240/241/244, and can replace them in many applications
- 'S700-1/730-1/731-1/734-1 have a larger resistor in the output stage for better undershoot protection
- Commercial devices are specified at $V_{CC} \pm 10\%$.

Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54S700/-1	J,W,L	Mil	High-Low	Invert	S
SN74S700/-1	N,J	Com			
SN54S730/-1	J,W,L	Mil	Low		
SN74S730/-1	N,J	Com			
SN54S731/-1	J,W,L	Mil	High-Low	Non-Invert	
SN74S731/-1	N,J	Com			
SN54S734/-1	J,W,L	Mil	Low		
SN74S734/-1	N,J	Com			

Description:

The 'S700, 'S730, 'S731, and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S700 and 'S730 are inverting drivers, and the 'S731 and 'S734 are non-inverting drivers. The 'S700/731 are pin-compatible with the 'S210/241 and have complementary enables. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular 8-bit buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

The 'S700, 'S730, 'S731, and 'S734 have been designed to drive the highly-capacitive input lines of dynamic RAMs. The drivers provide a guaranteed V_{OH} of V_{CC} - 1.15 volts, limit undershoot to 0.5V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

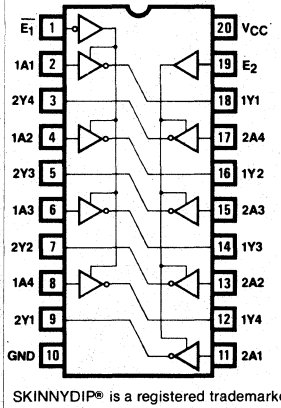
For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S700-1, 'S730-1, 'S731-1 and 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot voltage of -0.3 V is provided in the 'S700-1 series.

A typical fully-loaded-board dynamic-RAM array consists of 4 banks of dynamic-RAM memory. Each bank has its own $\overline{RAS}$ and $\overline{CAS}$, but has identical address lines. The $\overline{RAS}$ and $\overline{CAS}$ inputs to the array can come from one driver, reducing the skew between the $\overline{RAS}$ and $\overline{CAS}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50pf and 500pf load capacitances, and the commercial-range specifications are extended to $V_{CC} \pm 10\%$.

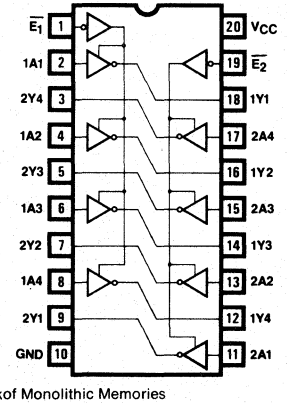
All of the octal devices are packaged in the popular 20-pin SKINNYDIP™.

Logic Symbols

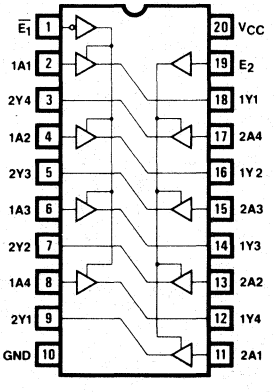
'S700/-1



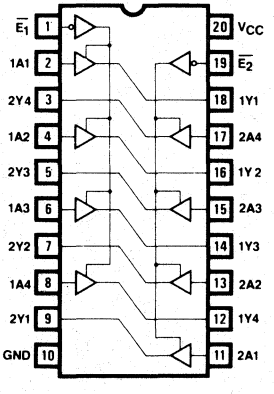
'S730 (Am2965)
'S730-1



'S731/-1



'S734 (Am2966)
'S734-1



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TWX: 910-338-2376
Monolithic Memories MMI

Function Tables

'S700/-1

$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	H	Z
L	L	H	X	L	Z
L	H	L	L	H	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	H	L	L
H	H	X	L	Z	H
H	H	X	H	Z	L
H	L	X	X	Z	Z

'S730/-1

$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	H	H
L	L	L	H	H	L
L	L	H	L	L	H
L	L	H	H	L	L
L	H	L	X	H	Z
L	H	H	X	L	Z
H	L	X	L	Z	H
H	L	X	H	Z	L
H	H	X	X	Z	Z

'S731/-1

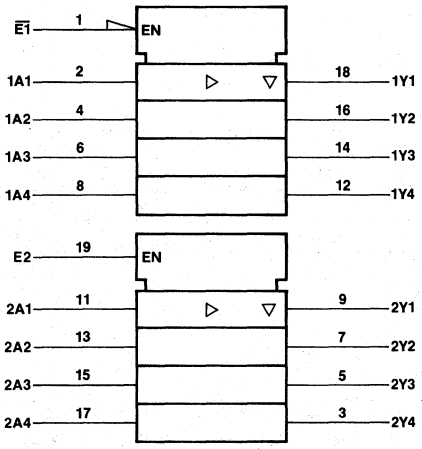
$\overline{E1}$	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L	L	H	X	H	Z
L	H	L	L	L	L
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	H
H	H	X	L	Z	L
H	H	X	H	Z	H
H	L	X	X	Z	Z

'S734/-1

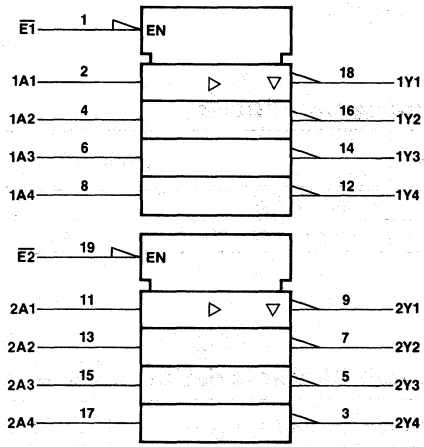
$\overline{E1}$	$\overline{E2}$	1A	2A	1Y	2Y
L	L	L	L	L	L
L	L	L	H	L	H
L	L	H	L	H	L
L	L	H	H	H	H
L	H	L	X	L	Z
L	H	H	X	H	Z
H	L	X	L	Z	L
H	L	X	H	Z	H
H	H	X	X	Z	Z

IEEE Symbol

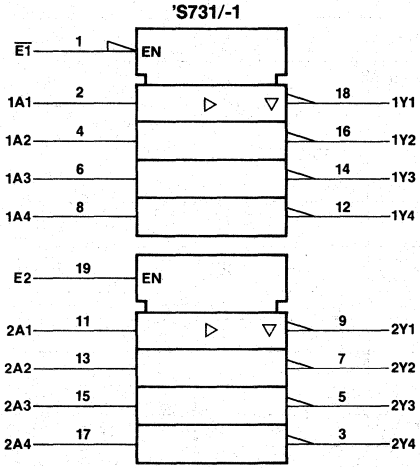
'S700/-1



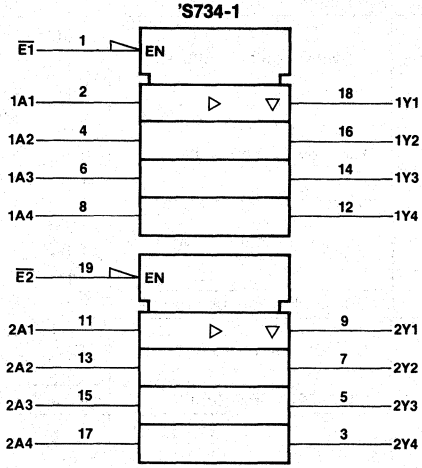
'S730-1



'S731/-1



'S734-1



8

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7.0 V
Input voltage ..... -1.5 V to 7.0 V
Off-state output voltage ..... -0.5 V to +V_{CC} max
Storage temperature range ..... -65° to +150°C
Output current ..... 200 mA

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
T_A	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS			MILITARY			COMMERCIAL			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}*	Low-level input voltage							0.8			0.8	V
V_{IH}*	High-level input voltage					2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18mA				-1.2			-1.2	V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.4V				-0.2			-0.2	mA
		Any E						-0.4			-0.4	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V				20			20	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 7V				0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 1mA				0.5			0.5	V
				I_{OL} = 12mA				0.8			0.8	
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = -1mA		V_{CC} -1.15	V_{CC} -.7		V_{CC} -1.15	V_{CC} -.7		V
I_{OZL}	Off-state output current		V_{CC} = MAX V_{IL} = 0.8V V_{IH} = 2V	V_O = 0.4V				-200			-200	μA
I_{OZH}				V_O = 2.7V				100			100	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX			-60		-200	-60		-200	mA
I_{OL}	Output sink current		V_{OL} = 2.0V	'S 7XX		50			50			mA
				'S 7XX-1		40			40			
I_{OH}	Output source current		V_{OH} = 2.0V			-35			-35			mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX Outputs open		S700/-1 S730/-1		24	50		24	50	mA
					S731/-1 S734/-1		53	75		53	75	
		Outputs Low			S700/-1 S730/-1		86	125		86	125	
					S731/-1 S734/-1		92	130		92	130	
		Outputs Disabled			S700/-1 S730/-1		86	125		86	125	
					S731/-1 S734/-1		116	150		116	150	

†Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

*These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or test noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S700, 'S730, 'S731, 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	30	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	12	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf		±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	−0.5	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S700, 'S730, 'S731, 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10%			COMMERCIAL V_{CC} = 5.0V ±10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		40	18		35	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			−0.5			−0.5	V

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

†† T_C = -55 to + 125°C for flatpack versions.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S700-1, 'S730-1, 'S731-1, 'S734-1

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	6	9	15	ns
			C_L = 500pf	18	22	30	
t_{PHL}			C_L = 50pf	5	7	15	
			C_L = 500pf	18	22	40	
t_{PZL}	Output enable delay	2 & 4	S = 1		12	20	ns
t_{PZH}			S = 2		12	20	
t_{PLZ}	Output disable delay	2 & 4	S = 1		11	20	ns
t_{PHZ}			S = 2		6.5	12	
t_{SKEW}	Output-to-output skew	1 & 3	C_L = 50pf	*	±0.5	±3.0	ns
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf		0	-0.3	V

*The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S700-1, 'S730-1, 'S731-1, 'S734-1

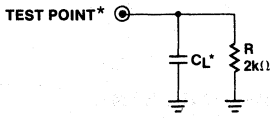
SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MILITARY †† V_{CC} = 5.0V ±10% MIN	TYP	MAX	COMMERCIAL V_{CC} = 5.0V ±10% MIN	TYP	MAX	UNIT
t_{PLH}	Data to output delay	1 & 3	C_L = 50pf	4		20	4		17	ns
			C_L = 500pf	18		40	18		35	
t_{PHL}			C_L = 50pf	4		20	4		17	
			C_L = 500pf	18		50	18		45	
t_{PZL}	Output enable delay	2 & 4	S = 1†			28			28	ns
t_{PZH}			S = 2†			28			28	
t_{PLZ}	Output disable delay	2 & 4	S = 1†			24			24	ns
t_{PHZ}			S = 2†			16			16	
V_{ONP}	Output voltage undershoot	1 & 3	C_L = 50pf			-0.3			-0.3	V

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

†"S = 1" and "S = 2" refer to the switch setting in Figure 2.

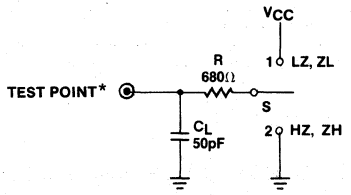
††T_C = -55 to + 125°C for flatpack versions.

Test Loads



*t_{pd} specified at C_L = 50 and 500pF

Figure 1. Capacitive Load Switching



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Figure 2. Three-State Enable/Disable

Typical Switching Characteristics

VOLTAGE WAVEFORMS

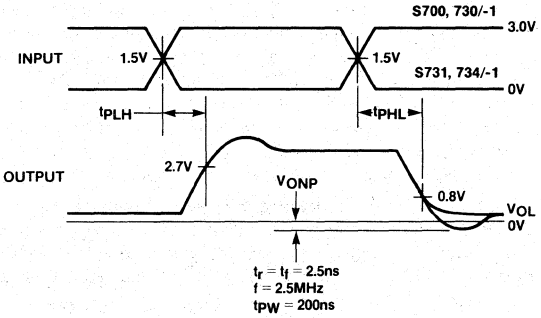


Figure 3. Output Voltage Levels

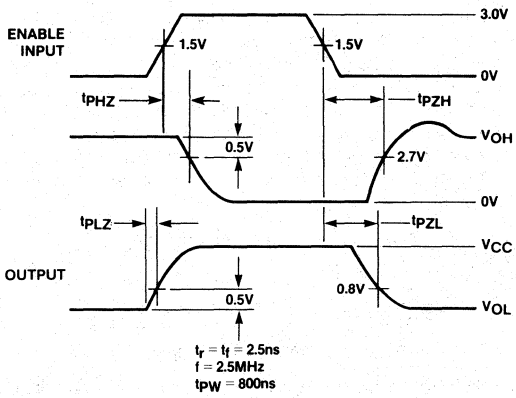
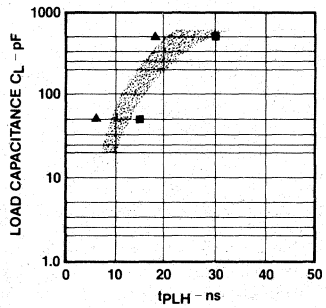


Figure 4. Three-State Control Levels

Typical Performance Characteristics:



▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5a. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S700 series

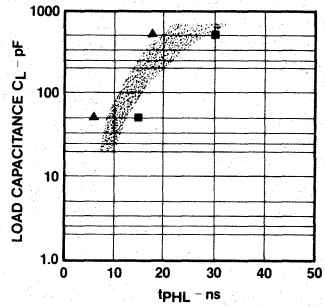
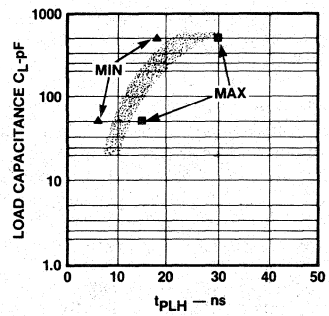


Figure 6a. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S700 series



▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5b. t_{PLH} for V_{OH} = 2.7 V vs. C_L, for the 'S700-1 series

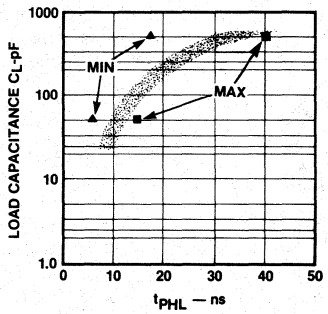


Figure 6b. t_{PHL} for V_{OL} = 0.8 V vs. C_L, for the 'S700-1 series

Applications

The'S700, 'S730, 'S731 and 'S734 are 8-bit bipolar dynamic RAM drivers and are pin-compatible with the 'S210, 'S240, 'S241 and 'S244 respectively.

The actual circuit conditions that arise for driving dynamic RAM memories are as follows: Typically, in dynamic RAM arrays address lines and control lines, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ have a fair amount of "daisy chaining." The daisy chaining causes an inductive effect due to the traces in the printed circuit board; the dominant factor in the RAM loading is input capacitance, and these two conditions contribute to the actual driver conditions shown in Figure 7. The result is a transmission line with distributed inductance and capacitance connected to the driver outputs.

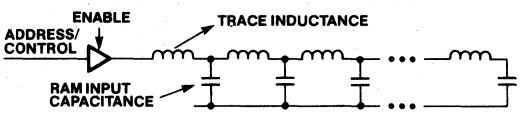


Figure 7. RAM Driver Output To Array

The transmission line effect can imply reflections, which in turn cause ringing, and it takes some time before the output settles from the low-to-high transition. On the high-to-low transition, along with ringing, a voltage undershoot can occur, and the circuit takes even longer to settle to an acceptable zero level. The main cause for the shorter high-to-low transition as compared to the low-to-high transition is the output impedance of typical Schottky drivers. Figure 8, shows a typical Schottky driver output stage and Figure 9 shows the output impedance for high and low output states.

Figure 8. Typical Schottky Driver Output

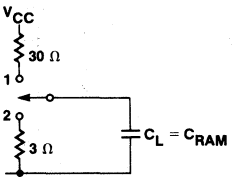


Figure 9. Driver Output Impedance

In Figure 9 when S=1, the output is high and the driver output impedance is approximately 30Ω. When S=2, the output is low and the driver output impedance is approximately 3Ω. There is a 10:1 ratio for the output impedances for the low and high states. The high-to-low transition causes a problem as the output transistor turns on fast due to the low impedance and undershoot results at the RAM inputs.

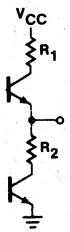


Figure 10. 'S700, 'S730, 'S731, and 'S734 Output Stage

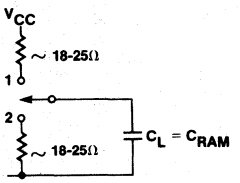


Figure 11. Driver Output Impedance For the 'S700, 'S730, 'S731, and 'S734

The 'S700, 'S730, 'S731, and 'S734 have a modification in their output stage, in that an internal resistor is added to the lower output stage as shown in Figure 10.

The 'S700-1, 'S730-1, 'S731-1 and 'S734-1 have a larger resistor, R2, comparted to the "non-dash" parts, which give better undershoot protection at a slightly slower switching performance.

The structure in Figure 10 provides a driver output impedance of approximately 18Ω to 25Ω in either high (S = 1) or low (S = 2) states as shown in Figure 11. In addition, this circuit limits undershoot to -0.5V, essentially eliminating that problem; provides a symmetrical rise and fall time; and guarantees output levels of V_{CC} -1.15V needed for MOS High levels. Also, when using the 'S700, 'S730, 'S731 and 'S734, no external resistors are needed. 'S240-series parts used with external resistors to provide drive capability, but the rise times and fall times are unsymmetrical due to higher impedance for low-to-high transitions.

Figure 12 shows the undershoot problem using a 'S240 without external resistors and the elimination of the problem by using the 'S730. Thus from a dynamic-RAM system-design viewpoint, the 'S700, 'S730, 'S731 and 'S734 are very effective RAM drivers.

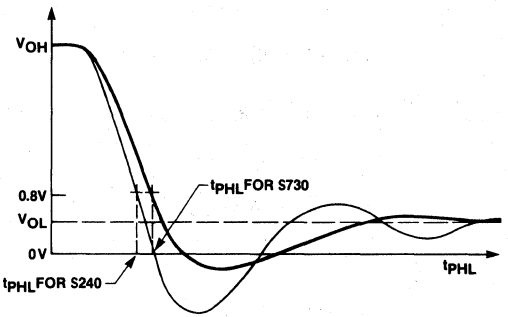


Figure 12. Comparison of Undershoots and t_{PHL}

An application using these 8-bit drivers to interface address and control lines (and data lines) to a dynamic RAM array using 64K DRAMs is discussed. The signals needed for the controls are $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The address lines are A0-A7 and the data lines are shown as the high and low byte. The array is shown in Figure 13. It consists of four rows of DRAMs; each row has individual $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ lines. However, all four rows have common address lines A0-A7. The RAM capacitive loading for $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ is about 10 pf per input. The loading of the address lines is about 5 to 7 pf per input. The loading of the $\overline{RAS}_i$, $\overline{CAS}_i$ and $\overline{WE}_i$ inputs to each row of memories is 160 pf. Note that $\overline{RAS}_i$ and $\overline{CAS}_i$ come from the same driver, which reduces timings skews which might arise if they were output from separate drivers. The address lines are outputs from another driver, and the loading on each line is 320 pf (5 pf loading times 64 DRAMs). At this point it is worth noting that if a 320-pf loading affects performance unduly, then the address lines can be split between two drivers with each having a load of 160 pf, reducing overall signal delay.

If an error-detection-and-correction scheme is used, then typically the row size expands to 22 bits from the 16 bits shown in the example. The 'S700, 'S730, 'S731 and 'S734 drivers lend themselves to such expansion, as their propagation delays are specified at 50 pF and also at 500 pF.

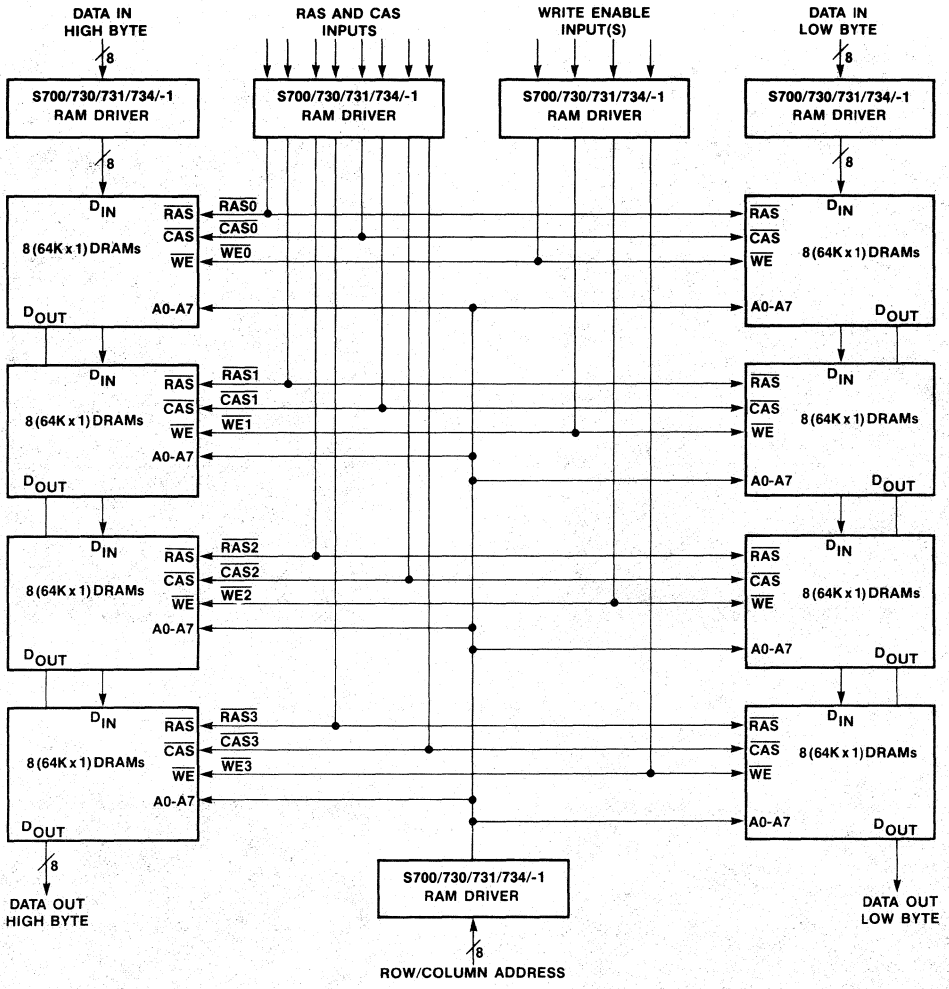
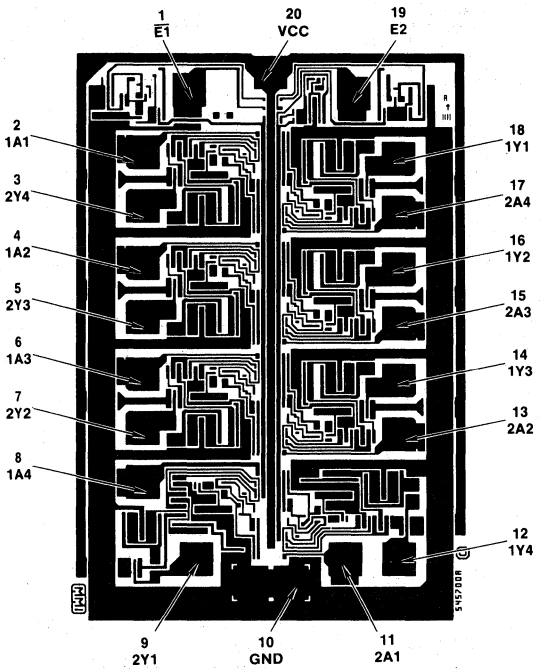


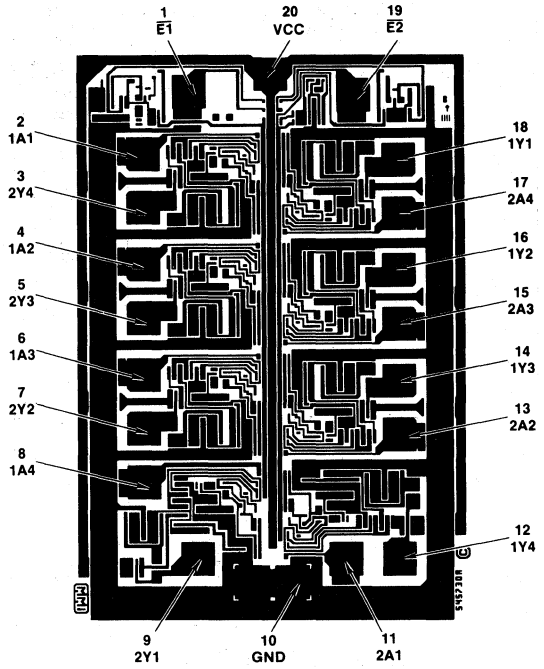
Figure 13. 256K X 16 Dynamic RAM Array with RAM Drivers

Die Configurations

SN54/74S700/-1

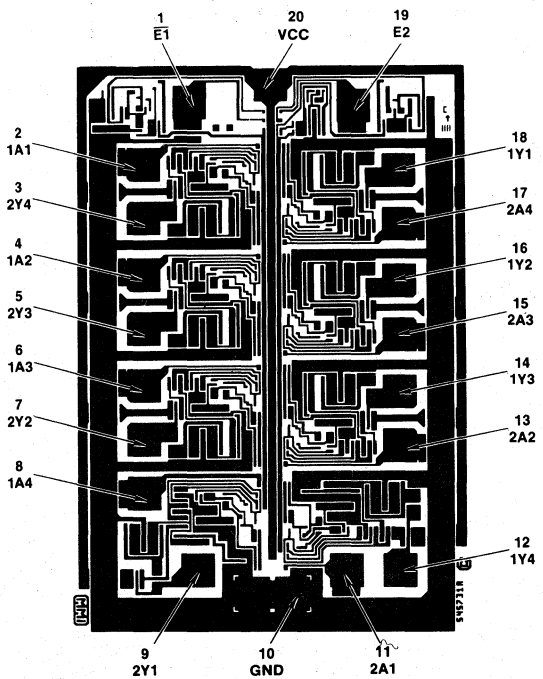


SN54/74S730/-1



Die Size: 62x87 mil^2

SN54/74S731/-1



SN54/74S734/-1