

MIMXRT1020-EVK

Table of Content


Page 1	COVER
Page 2	BLOCK DIAGRAM
Page 3	MAIN POWER
Page 4	POWER DOMAIN
Page 5	MIMXRT1021DAG5A
Page 6	USB
Page 7	CAN
Page 8	AUDIO
Page 9	ETHERNET
Page 10	SD/FLASH
Page 11	ARDUINO/JTAG
Page 12	SDRAM
Page 13	FREELINK
Page 14	BOOT
Page 15	MISC
Page 16	
Page 17	
Page 18	
Page 19	
Page 20	
Page 21	
Page 22	
Page 23	
Page 24	
Page 25	
Page 26	
Page 26	
Page 27	
Page 28	

1. Unless Otherwise Specified:
 - All resistors are in ohms, 1/16 Watt, 0402
 - All capacitors are in uF, 0402
 - All voltages are DC
 - All polarized capacitors are aluminum electrolytic
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

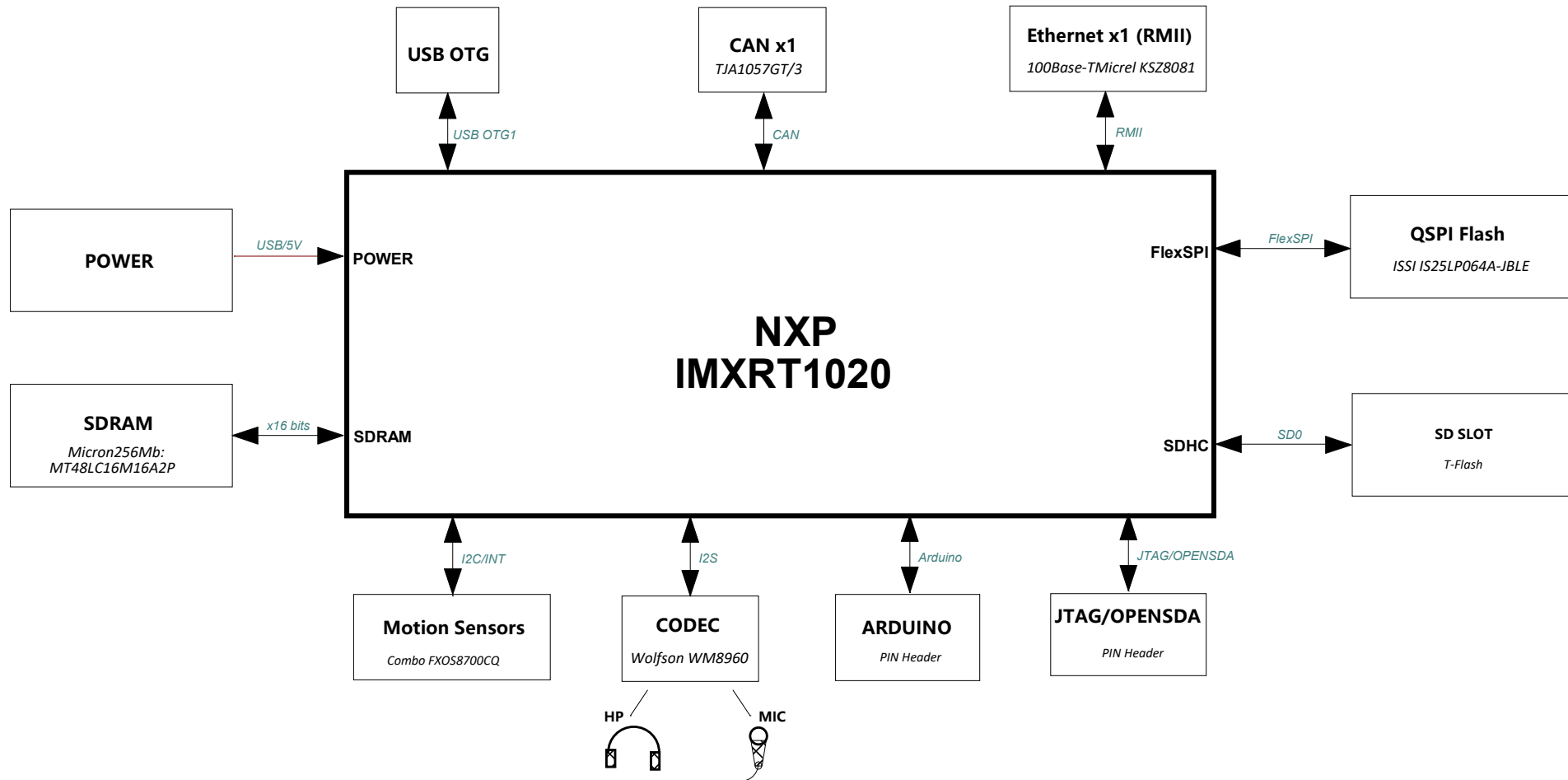
Revision History

[illegible]

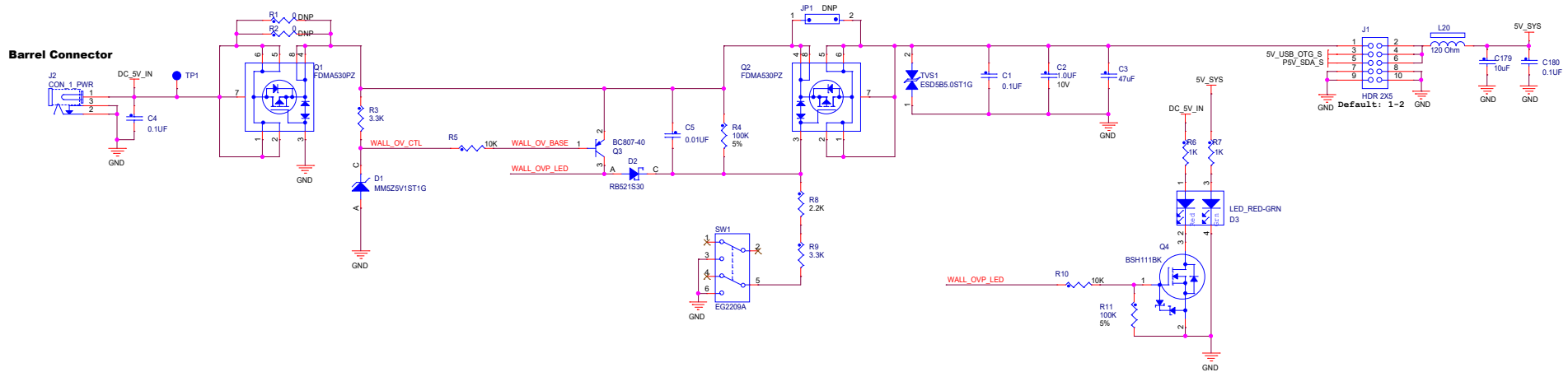
3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
 - _B Denotes - Active-Low Signal
 - <> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

				
ICAP Classification: CP: _____ IUG: X PUBI: _____				
Drawing Title: MIMXRT1020-EVK				
Page Title: COVER				
Size C	Document Number	SCH-29856, PDF: SPF-29856		Rev B1
Date:	Monday, October 22, 2018	Sheet	1	of 15

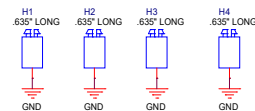
MIMXRT1020-EVK



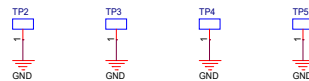
Main Power



Board Mounting Holes

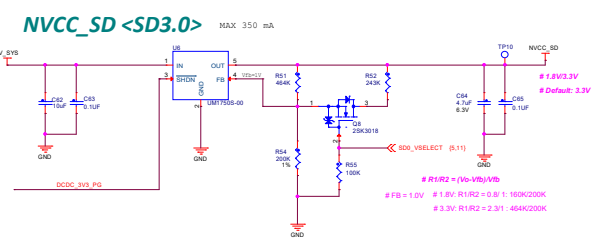
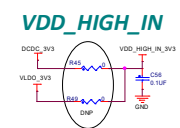
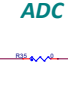
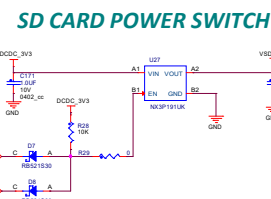
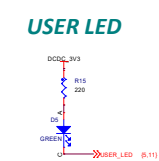


Ground TPs

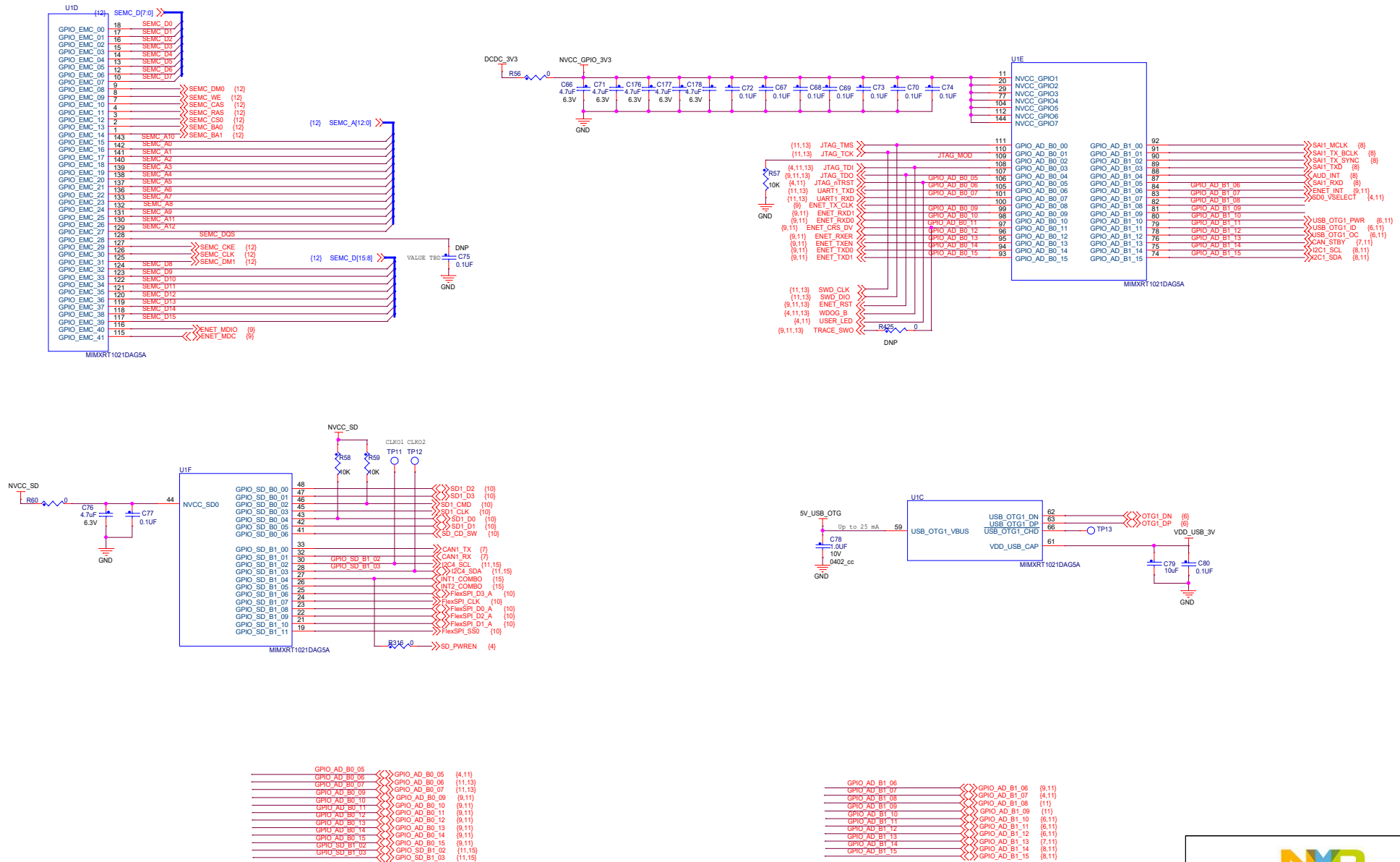


Layout Note: Place Ground TPs to assist signal measurement.

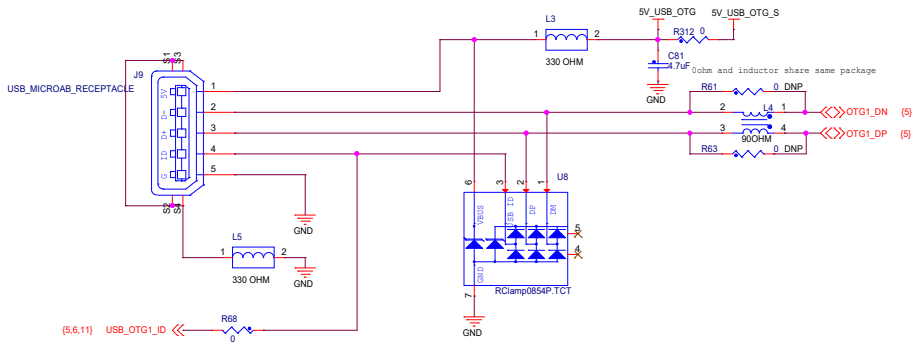
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Drawing Title: MIMXRT1020-EVK			
Page Title: MAIN POWER			
Size C	Document Number	SCH-29856, PDF: SPF-29856	Rev B1
Date: Monday, October 22 2018	Sheet 3	of 15	



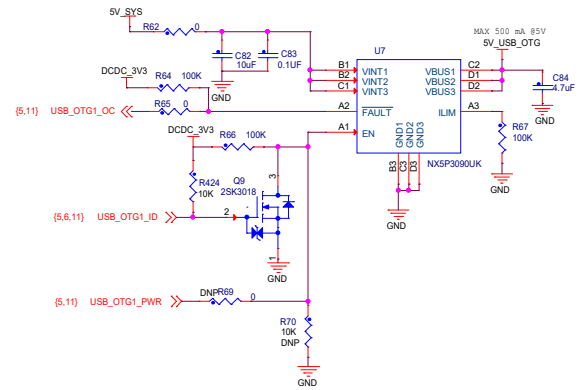
MCU PINOUT



USB OTG

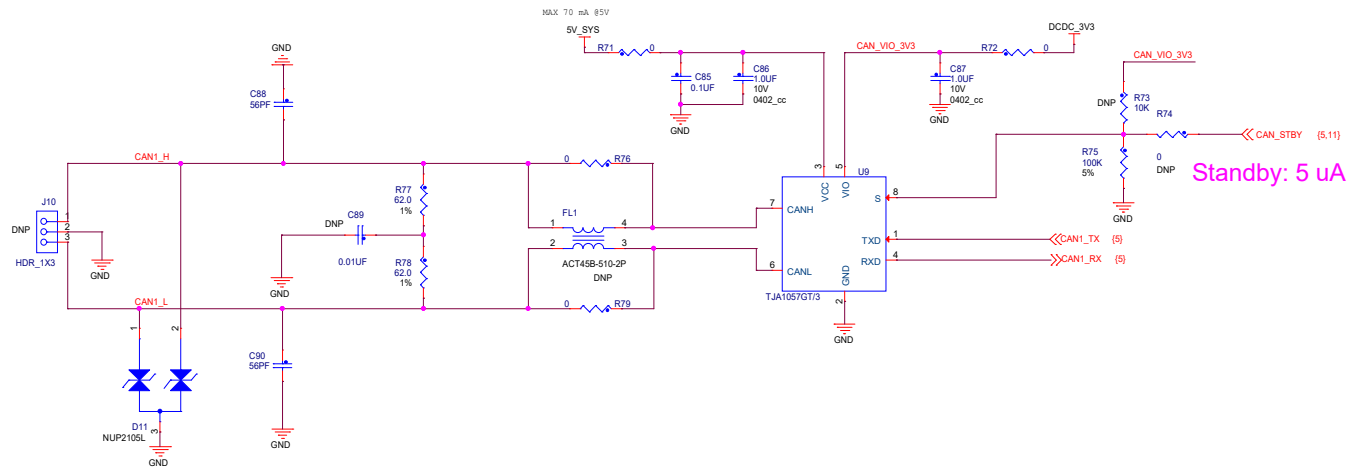


USB POWER

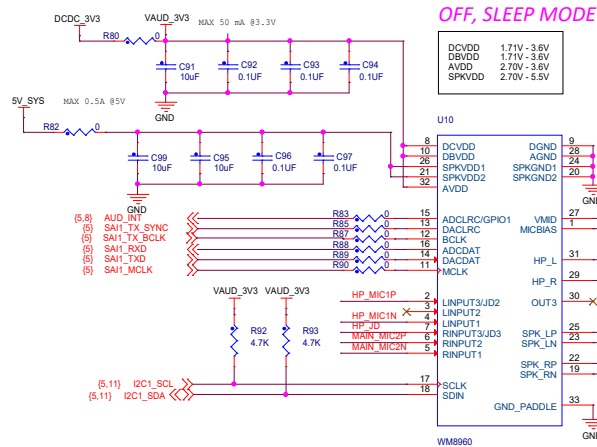


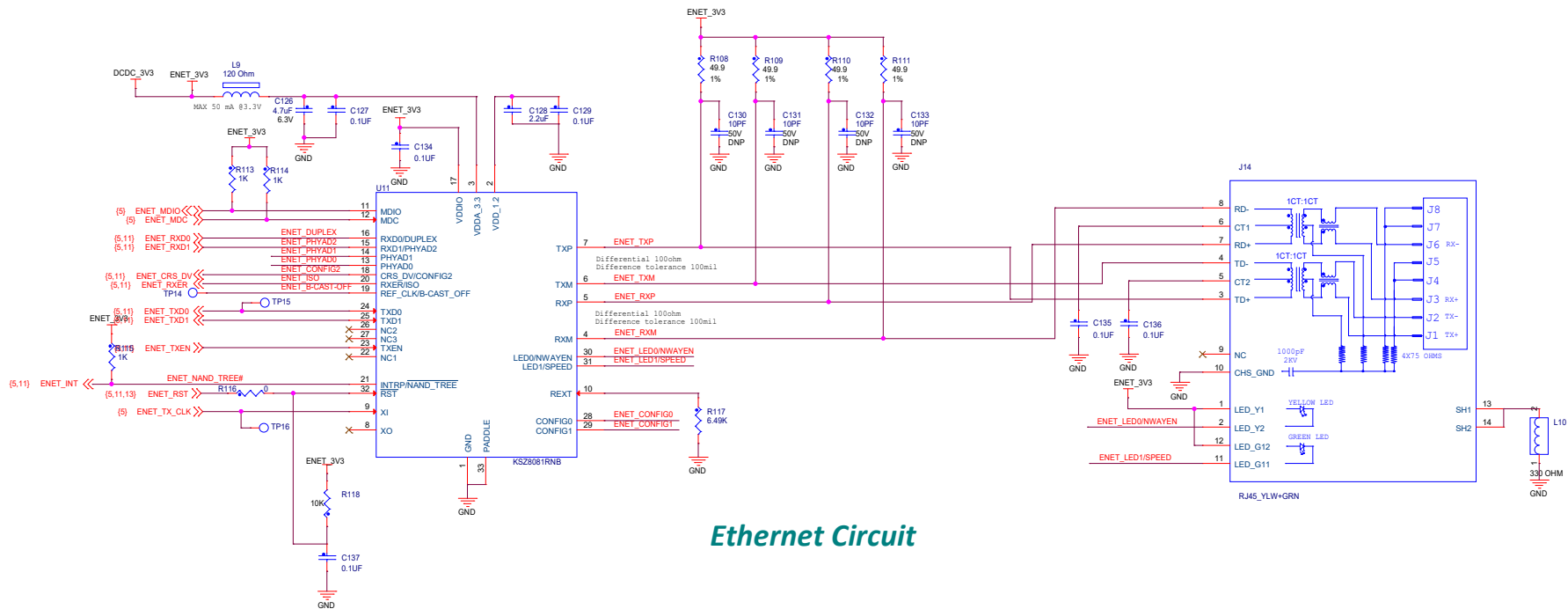
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MIMXRT1020-EVK				
Page Title:				
USB				
Size C	Document Number			Rev B1
	SCH-29856, PDF: SPF-29856			
Date:	Monday, October 22, 2018	Sheet	6	of 14

CAN BUS

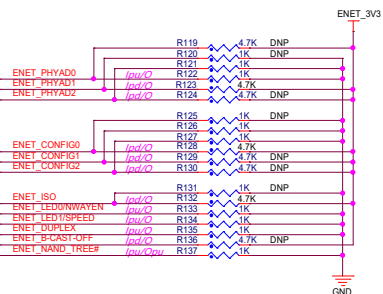


ICAP Classification: CP: IUX: X PUB:			
Drawing Title: MIMXRT1020-EVK			
Page Title: CAN			
Size C	Document Number SCH-29856, PDF: SPF-29856	Rev B1	
Date: Monday, October 22 2018	Sheet 7 of 15		



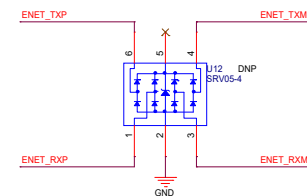


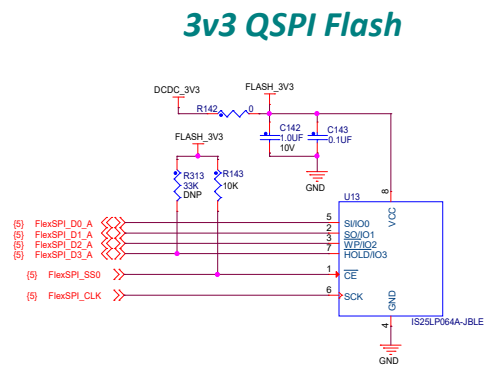
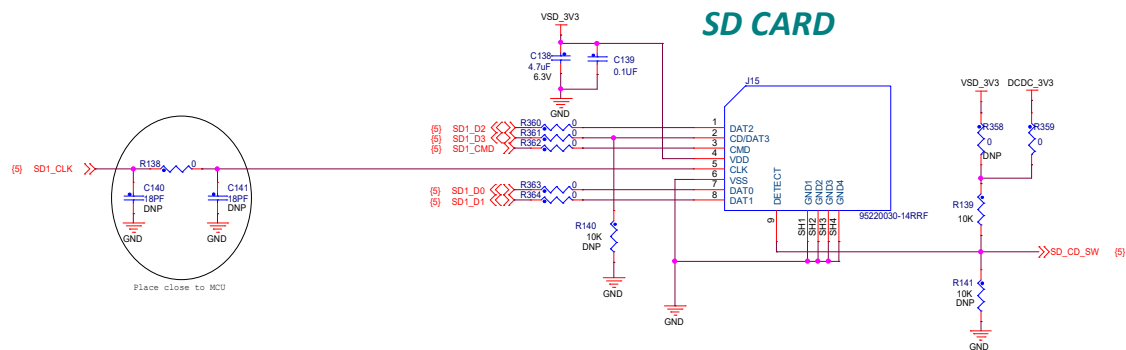
Ethernet Circuit



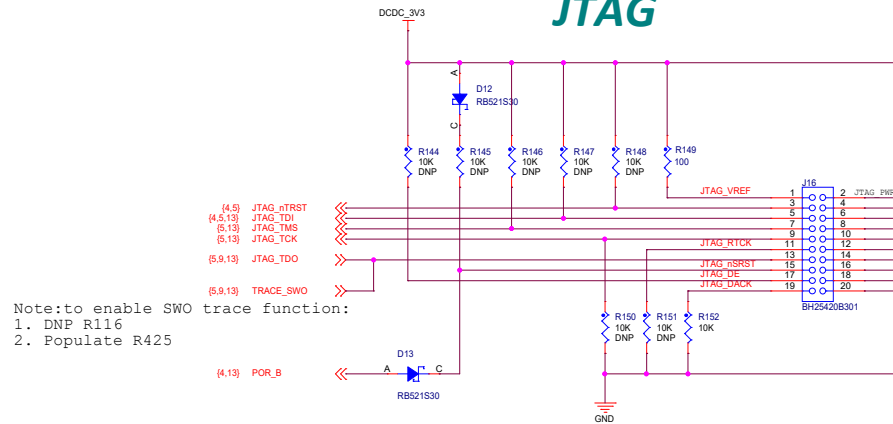
# CFG	Description	# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT) IF MODE	DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
CONFIG[2:0]	001 RMII 101 RMII Back-to-Back xxx Reserved-not used	NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable	B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps	NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION

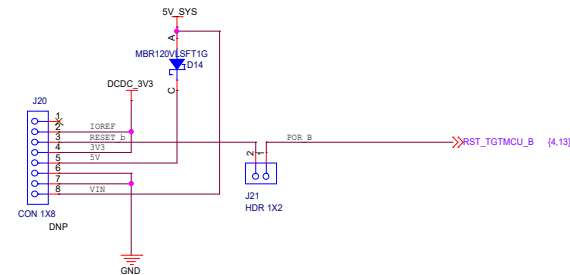
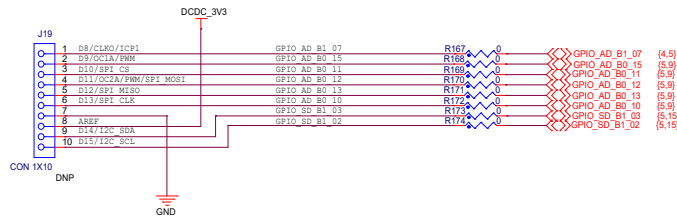
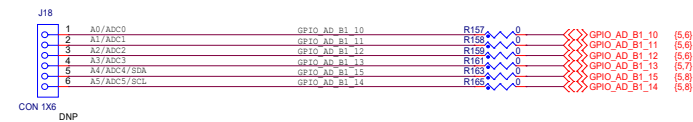
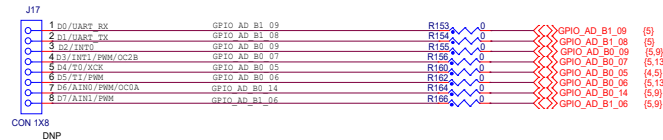




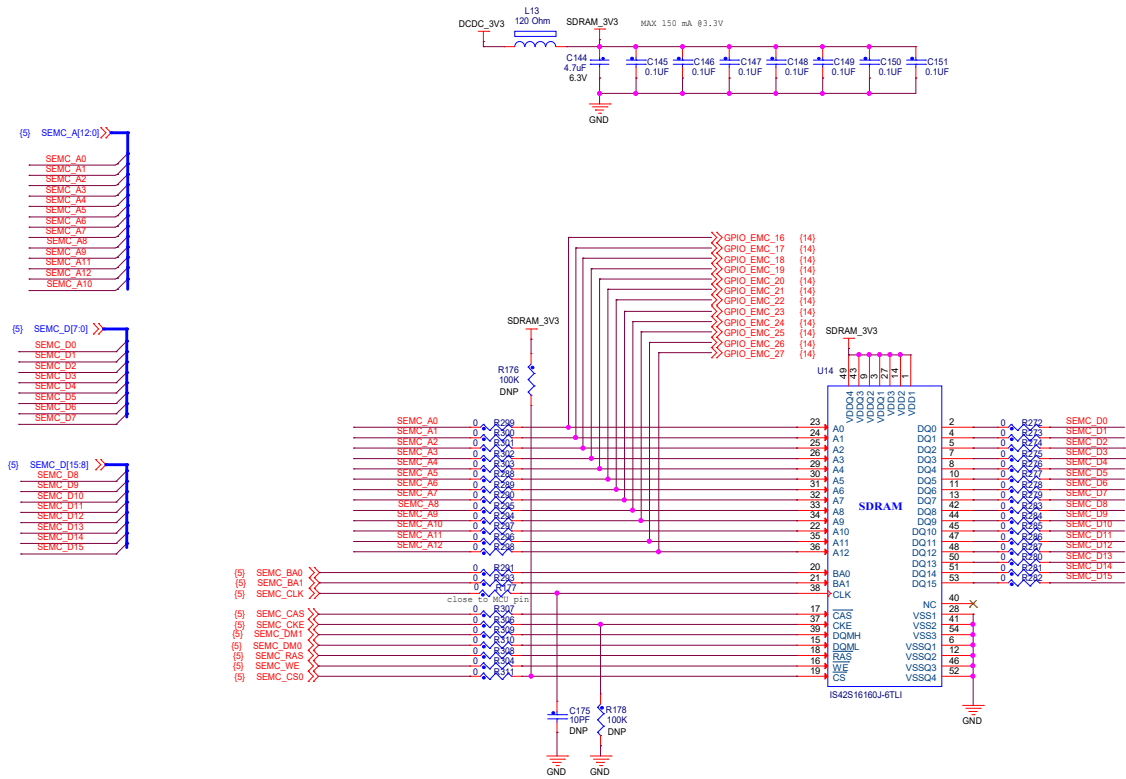
JTAG



Arduino Interface



SDRAM

ICAP Classification: CP: ____ IUO: X PUBL: ____
Division Title:

Drawing Title: **MIMXRT1020-EVK**

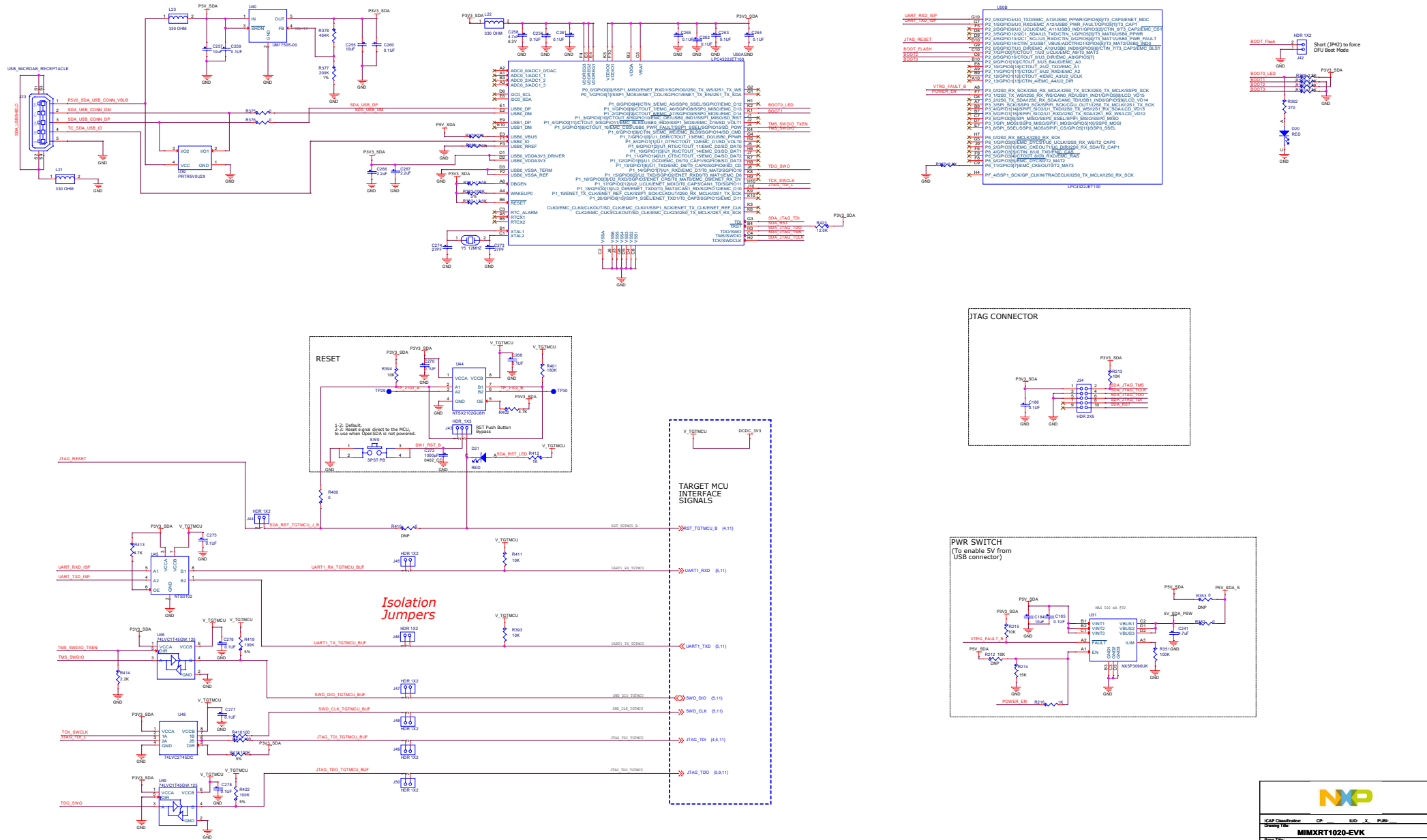
Page Title: **SDRAM**

Size C	Document Number SCH-29856, PDF: SPF-29856
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Date:	Monday, October 22, 2018	Sheet	12	of	15
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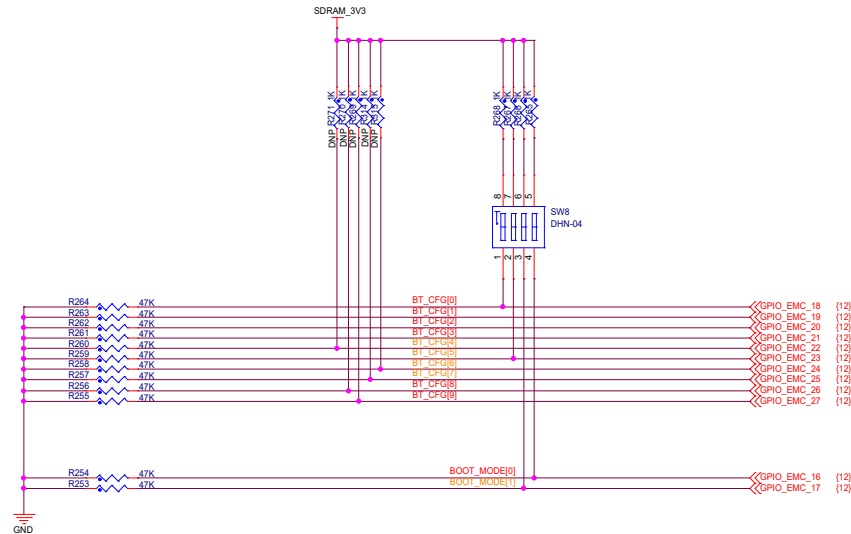
Rev
B1

Freelink Interface

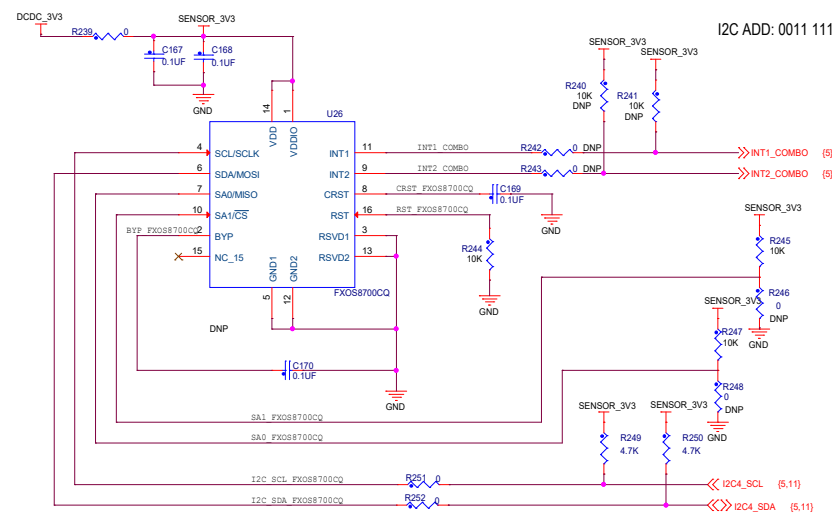


FUSE MAP

TYPE	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
FlexSPI1 - Serial NOR	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		0	0	0	0	FLASH_TYPE: 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR 101 - Micron Octal DDR 111 - QSPI device supports 3B read by default (on secondary pinmux option)			EncryptedXIP 0 - Disabled 1 - Enabled
SD	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		0	0	1	Bus Width: 0 - 1-bit 1 - 4-bit	SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Fast Boot: 0 - Regular 1 - Fast Boot
FlexSPI1 - Serial NAND	"CS_INTERVAL: CS de-asserted interval between two commands 0 - 100ns 1 - 200ns 2 - 400ns 3 - 50ns"		1	1	BOOT_SEARCH _COUNT: 0 - 1 1 - 2	COL_ADDRESS _WIDTH: 0 - 12bits 1 - 13bits	SPI NAND HOLD TIME 00 - 0 us 01 - 500us 10 - 1ms 11 - 3ms		BOOT_SEARCH_STRIDE: Search Stride for FCB and DBBT (in terms of pages) 0 - 64 1 - 128 2 - 256 3 - 32	



COMBO SENSOR



FXOS8700CQ COMBO SENSOR