

```
graph TD; RAM[RAM] --- L2[L2 Cache]; L2 --- L1_1[L1 Cache]; L2 --- L1_2[L1 Cache]; L1_1 --- Core1[Core 1]; L1_2 --- Core2[Core 2];
```

RAM

L2 Cache

L1 Cache

Core 1

L1 Cache

Core 2