CSE-1102

Analog Electronics

BANGLADESH UNIVERSITY

Outlines

- Transistor Biasing
- Methods of Transistor Biasing

Transistor Biasing

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as transistor biasing.

Essentials of a Transistor Biasing Circuit:

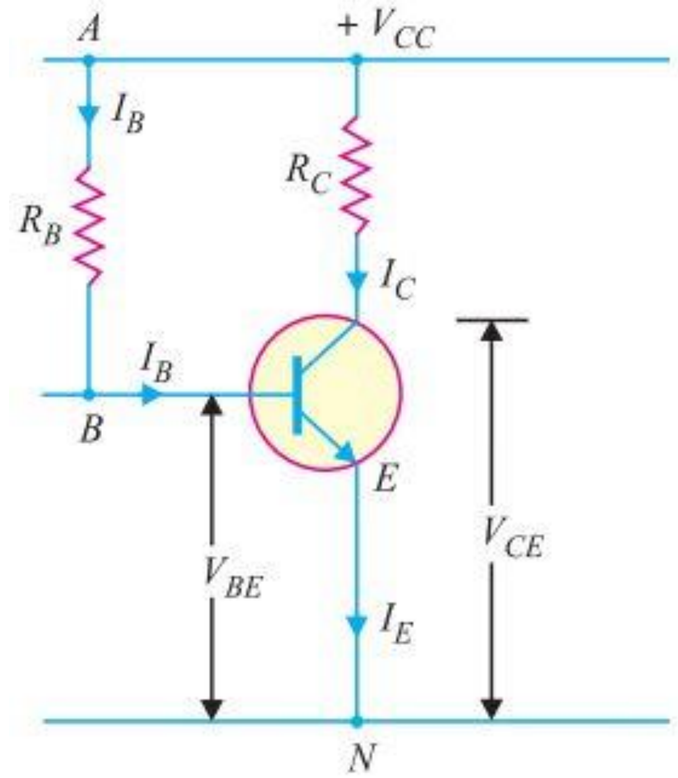
a) It should ensure proper zero signal collector current.
b) It should ensure that V_{CE} does not fall below 0.5 V for Ge transistors and 1 V for silicon transistors at any instant.
c) It should ensure the stabilization of operating point.

Methods of Transistor Biasing

(i) Base resistor method
(ii) Emitter bias method
(iii) Biasing with collector-feedback resistor
(iv) Voltage-divider bias

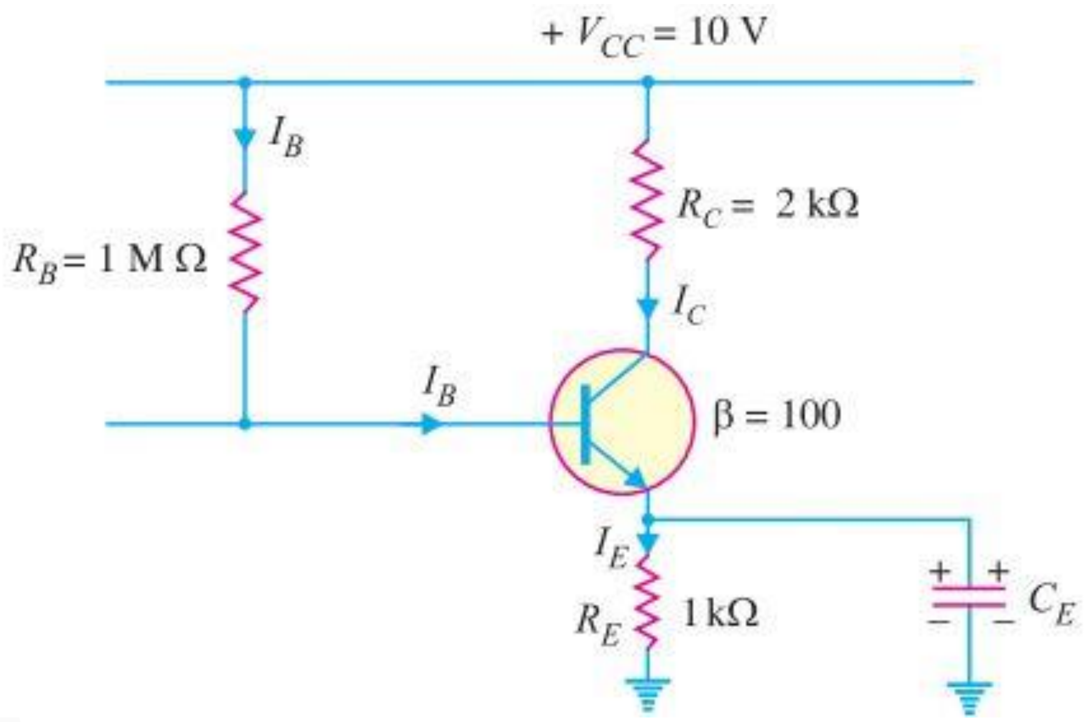
(i) Base Resistor Method

- A high resistance R_B is connected between the base and +ve end of supply for npn transistor.
- The required value of zero signal base current I_B can be made to flow by selecting the proper value of base resistor R_B.



Problem 14.1

Example 9.6. *Calculate the values of three currents in the circuit shown in Fig. 9.9.*



Example 9.6. *Calculate the values of three currents in the circuit shown in Fig. 9.9.*

Solution. Applying Kirchhoff's voltage law to the base side and taking resistances in kΩ and currents in mA, we have,

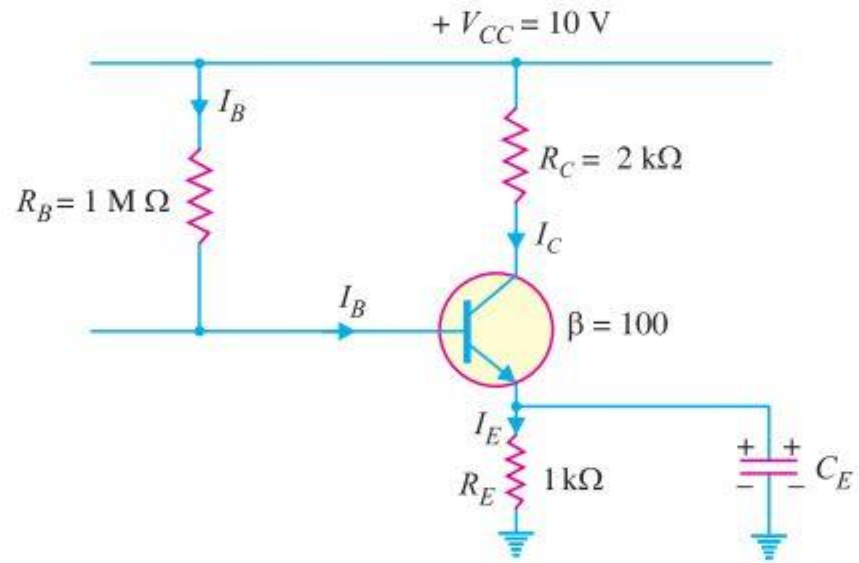


Fig. 9.9

$$V_{CC} = I_B R_B + V_{BE} + I_E \times 1$$

or $$10 = 1000\, I_B + {}^{*}0 + (I_C + I_B)$$

or $$10 = 1000\, I_B + (\beta\, I_B + I_B)$$

or $$10 = 1000\, I_B + (100\, I_B + I_B)$$

or $$10 = 1101\, I_B$$

∴ $$I_B = 10/1101 = \mathbf{0.0091\ mA}$$

$$I_C = \beta\, I_B = 100 \times 0.0091 = \mathbf{0.91\ mA}$$

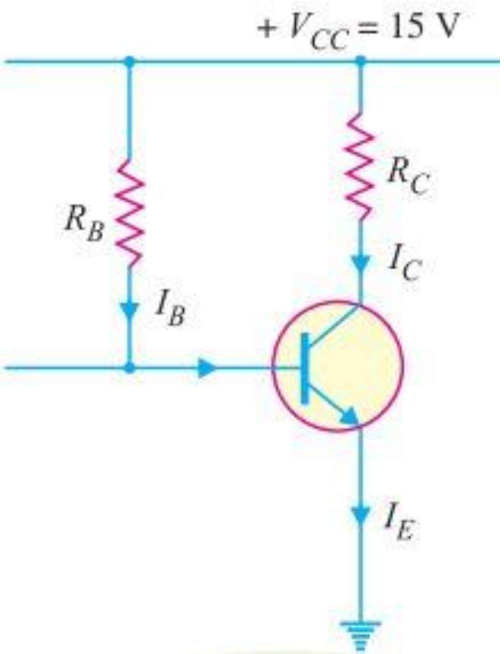
$$I_E = I_C + I_B = 0.91 + 0.0091 = \mathbf{0.919\ mA}$$

Problem 14.2

Example 9.7. *Design base resistor bias circuit for a CE amplifier such that operating point is $V_{CE} = 8V$ and $I_C = 2\ mA$. You are supplied with a fixed 15V d.c. supply and a silicon transistor with $\beta = 100$. Take base-emitter voltage $V_{BE} = 0.6V$. Calculate also the value of load resistance that would be employed.*

Example 9.7. *Design base resistor bias circuit for a CE amplifier such that operating point is V_{CE} = 8V and I_C = 2 mA. You are supplied with a fixed 15V d.c. supply and a silicon transistor with β = 100. Take base-emitter voltage V_{BE} = 0.6V. Calculate also the value of load resistance that would be employed.*

Solution. Fig. 9.10 shows *CE* amplifier using base resistor method of biasing.



$$V_{CC} = 15\text{ V};\ \beta = 100;\ V_{BE} = 0.6\text{V}$$

$$V_{CE} = 8\text{ V};\ I_C = 2\text{ mA};\ R_C = ?;\ R_B = ?$$

$$V_{CC} = V_{CE} + I_C R_C$$

or $$15\text{ V} = 8\text{ V} + 2\text{ mA} \times R_C$$

$$\therefore \quad R_C = \frac{(15-8)\text{ V}}{2\text{mA}} = \mathbf{3.5\ k\Omega}$$

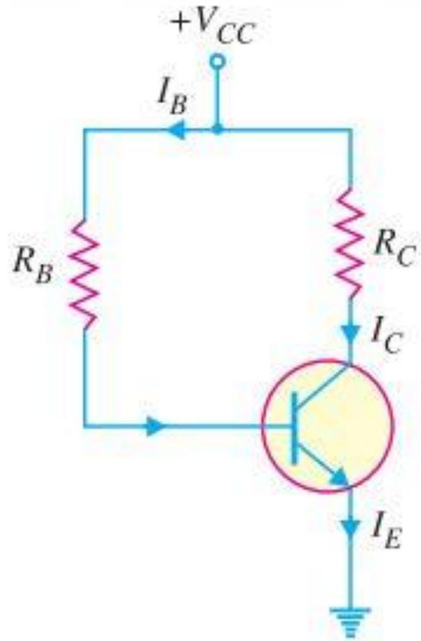
$$I_B = I_C/\beta = 2/100 = 0.02\text{ mA}$$

$$V_{CC} = I_B R_B + V_{BE}$$

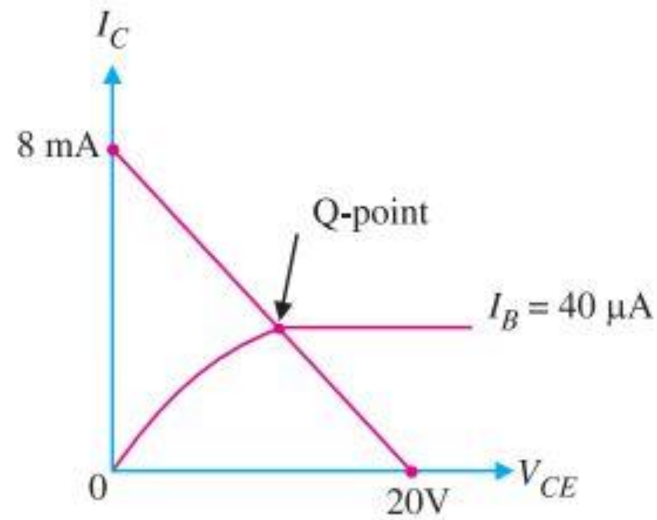
$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{(15-0.6)\text{ V}}{0.02\text{ mA}} = \mathbf{720\ k\Omega}$$

Problem 14.3

Example 9.10. *Fig. 9.13 (i) shows the base resistor transistor circuit. The device (i.e. transistor) has the characteristics shown in Fig. 9.13 (ii). Determine V_{CC}, R_C and R_B.*



(i)



(ii)

Example 9.10. *Fig. 9.13 (i) shows the base resistor transistor circuit. The device (i.e. transistor) has the characteristics shown in Fig. 9.13 (ii). Determine V_{CC}, R_C and R_B.*

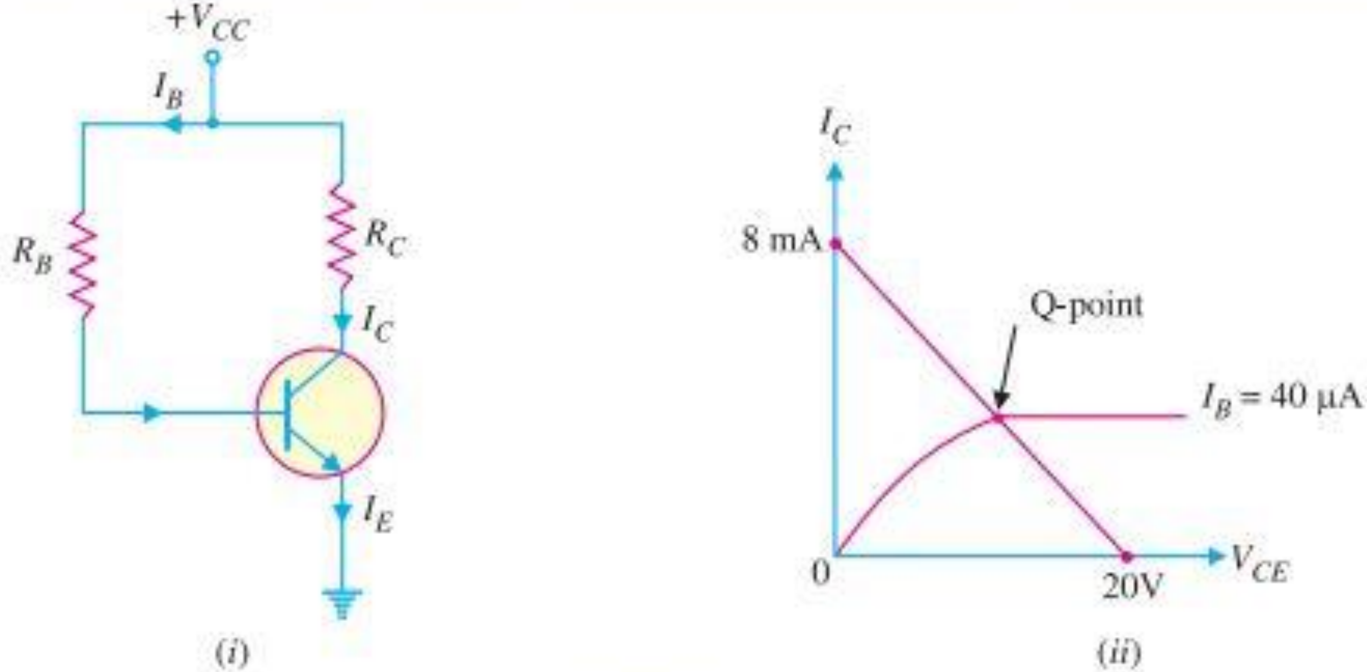


Fig. 9.13

Solution. From the d.c load line, V_{CC} = **20V.**

$$\text{Max. } I_C = \frac{V_{CC}}{R_C} \text{ (when } V_{CE} = 0\text{V)}$$

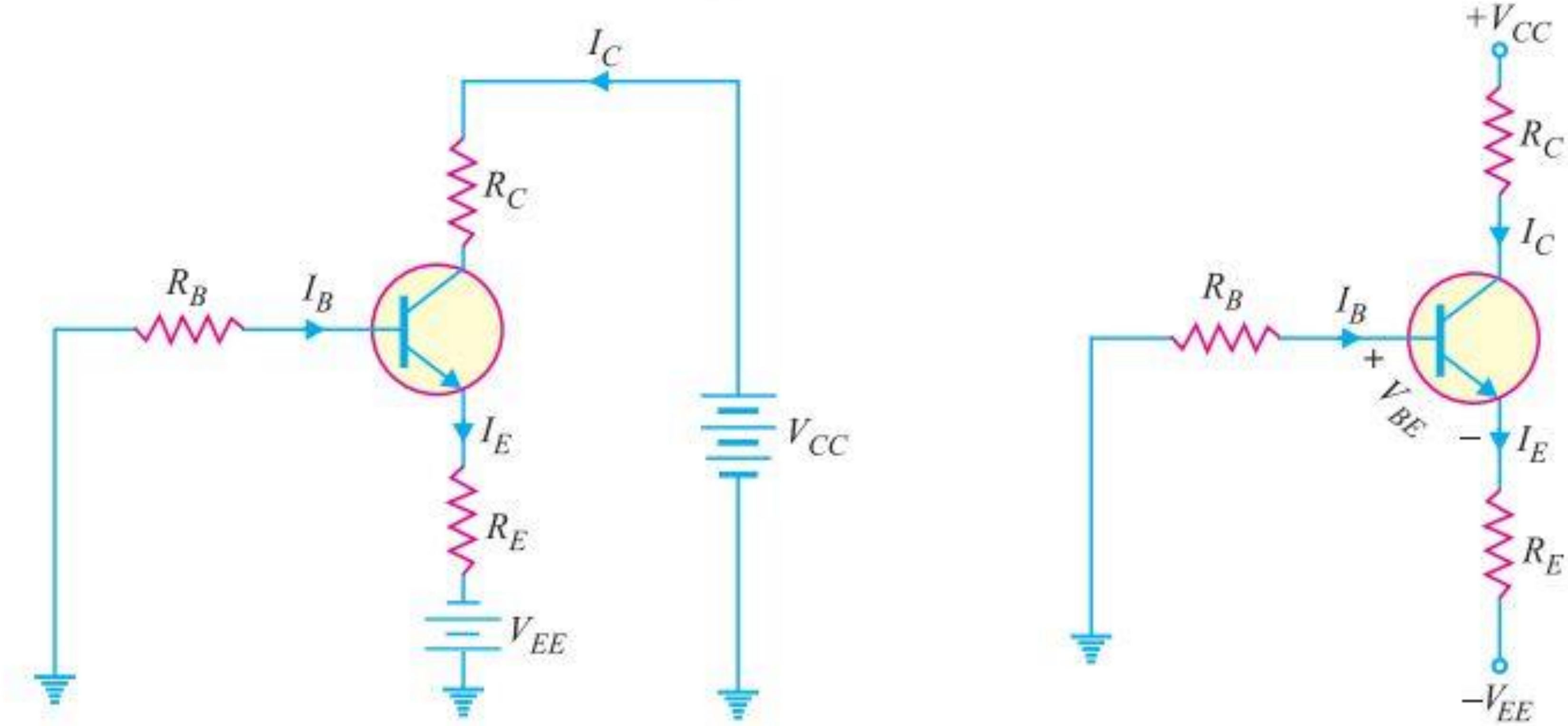
$$\therefore \quad R_C = \frac{V_{CC}}{\text{Max. } I_C} = \frac{20\text{V}}{8\text{mA}} = \mathbf{2.5\ k\Omega}$$

$$\text{Now} \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{V} - 0.7\text{V}}{40\ \mu\text{A}} = \frac{19.3\text{V}}{40\ \mu\text{A}} = \mathbf{482.5\ k\Omega}$$

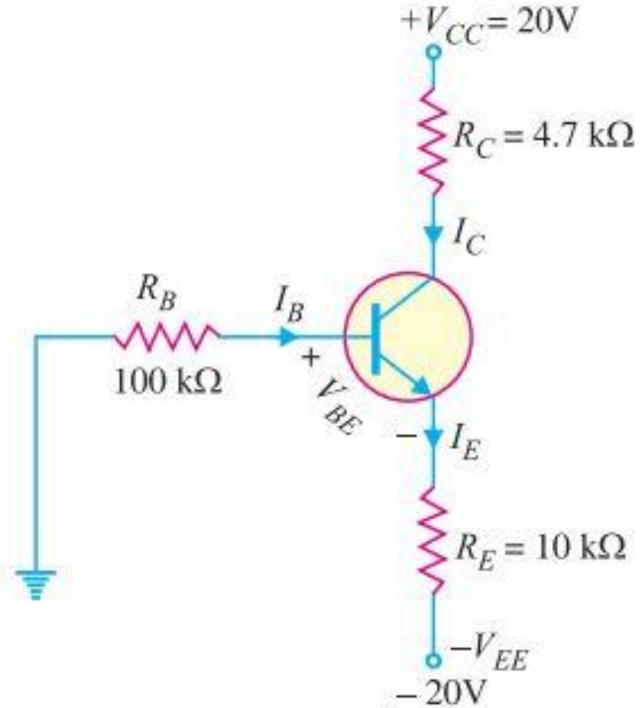
(ii) **Emitter Bias Circuit**

Fig. 9.15 shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources ; one positive ($+V_{CC}$) and the other negative ($-V_{EE}$). Normally, the two supply voltages will be equal. For example, if $V_{CC} = +20$V (d.c.), then $V_{EE} = -20$V (d.c.). Secondly, there is a resistor R_E in the emitter circuit.

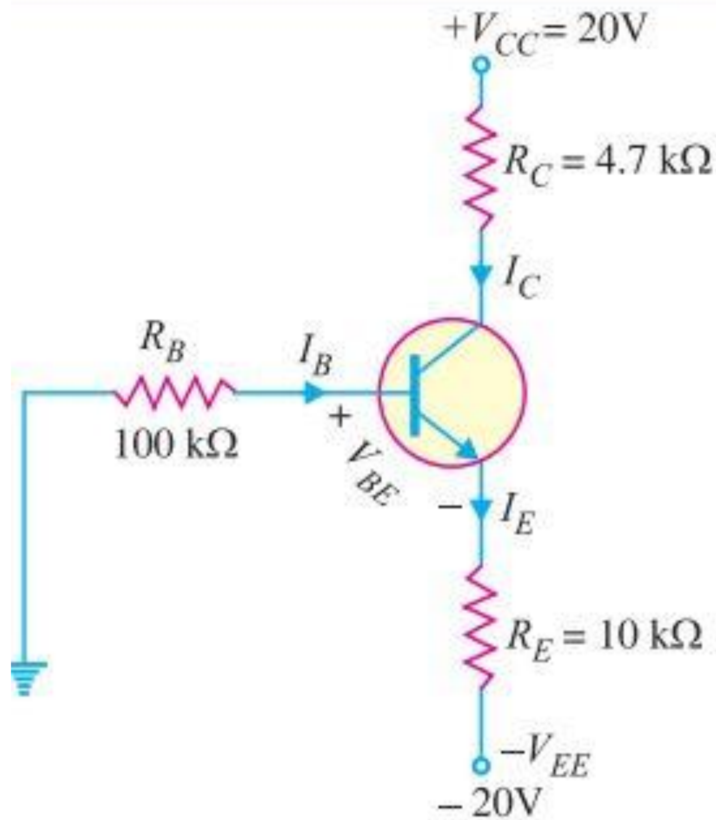


Problem 14.4

Example 9.12. *For the emitter bias circuit shown in Fig. 9.18, find I_E, I_C, V_C and V_{CE} for $\beta = 85$ and $V_{BE} = 0.7V$.*



Example 9.12. *For the emitter bias circuit shown in Fig. 9.18, find I_E, I_C, V_C and V_{CE} for $\beta = 85$ and $V_{BE} = 0.7V$.*



$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

Now $\quad I_C \simeq I_E$ and $I_C = \beta I_B \quad \therefore I_B \simeq \dfrac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or
$$V_{EE} - V_{BE} = I_E (R_B/\beta + R_E)$$

$\therefore$
$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.7V}{10\ k\Omega + 100\ k\Omega/85} = \mathbf{1.73\ mA}$$

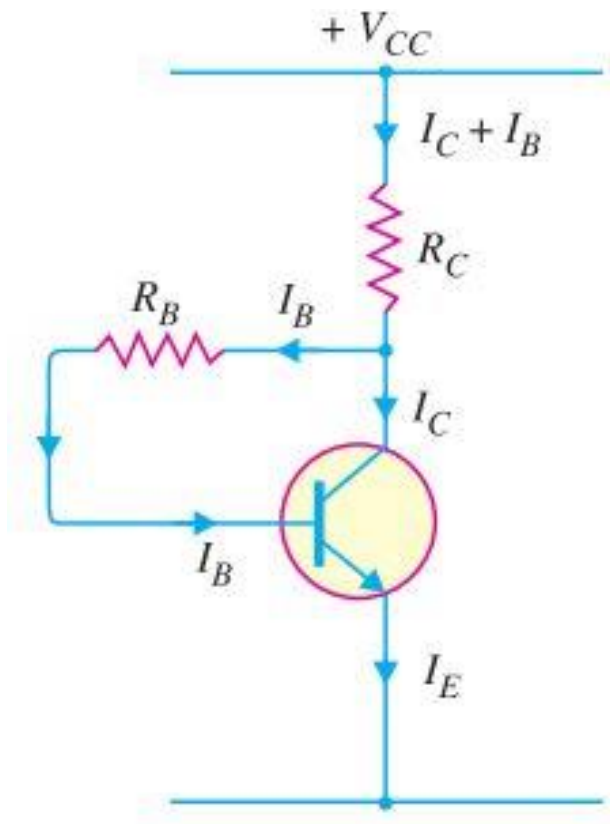
$$V_C = V_{CC} - I_C R_C = 20V - (1.73\ mA)(4.7\ k\Omega) = \mathbf{11.9V}$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.73\ mA)(10\ k\Omega) = -2.7V$$

$\therefore$
$$V_{CE} = V_C - V_E = 11.9 - (-2.7V) = \mathbf{14.6V}$$

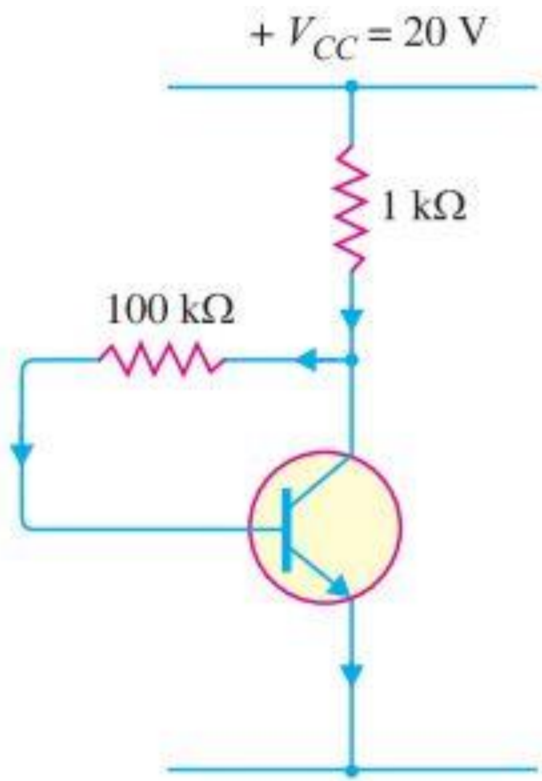
Note that operating point (or Q – point) of the circuit is 14.6V, 1.73 mA.

(iii) Biasing with Collector Feedback Resistor



Problem 14.5

Example 9.14. *Fig. 9.20 shows a silicon transistor biased by collector feedback resistor method. Determine the operating point. Given that* β = *100.*



Example 9.14. *Fig. 9.20 shows a silicon transistor biased by collector feedback resistor method. Determine the operating point. Given that $\beta = 100$.*

Solution. $V_{CC} = 20\text{V}, R_B = 100\ \text{k}\Omega, R_C = 1\text{k}\Omega$

Since it is a silicon transistor, $V_{BE} = 0.7$ V.

Assuming I_B to be in mA and using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B}$$

or $$100 \times I_B = 20 - 0.7 - 100 \times I_B \times 1$$

or $$200\ I_B = 19.3$$

or $$I_B = \frac{19.3}{200} = 0.096 \text{ mA}$$

$\therefore$ Collector current, $I_C = \beta\, I_B = 100 \times 0.096 = 9.6$ mA

Collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 20 - 9.6 \text{ mA} \times 1 \text{ k}\Omega$$
$$= 10.4 \text{ V}$$

$\therefore$ Operating point is **10.4 V, 9.6 mA.**

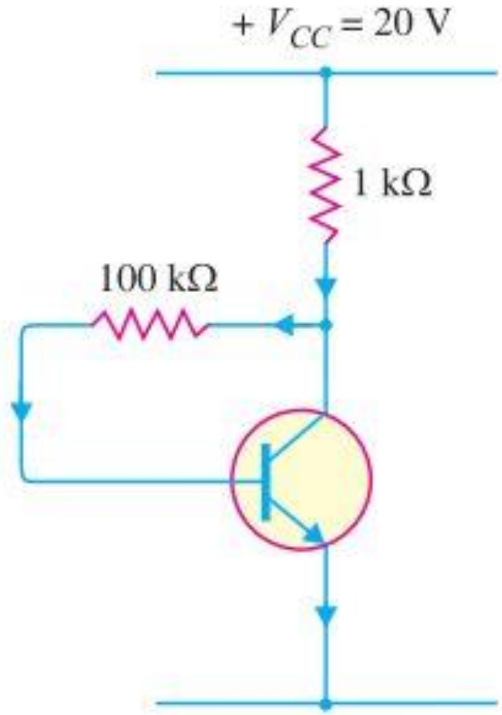
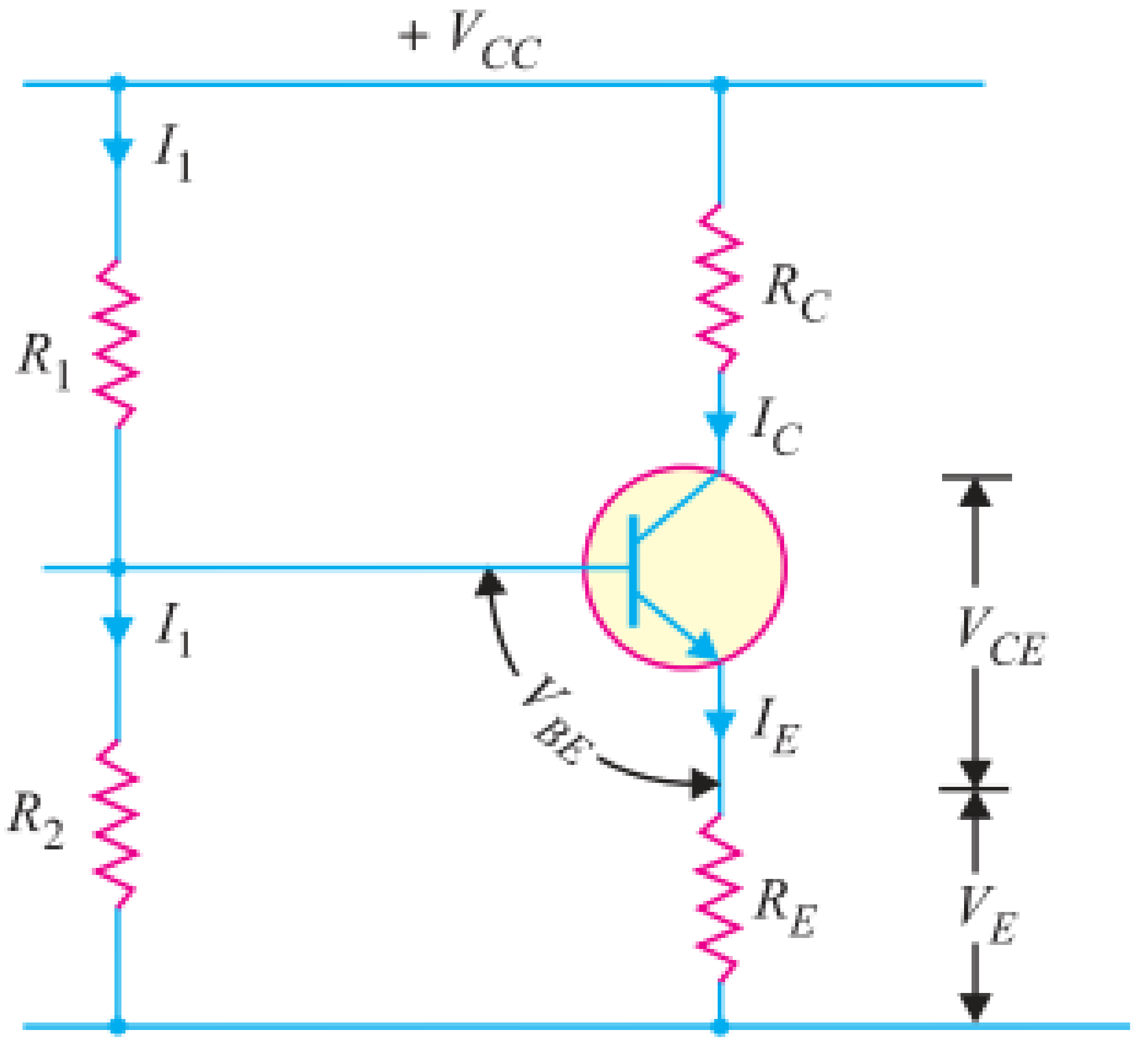


Fig. 9.20

(iv) Voltage-divider bias



(iv) Voltage-divider bias

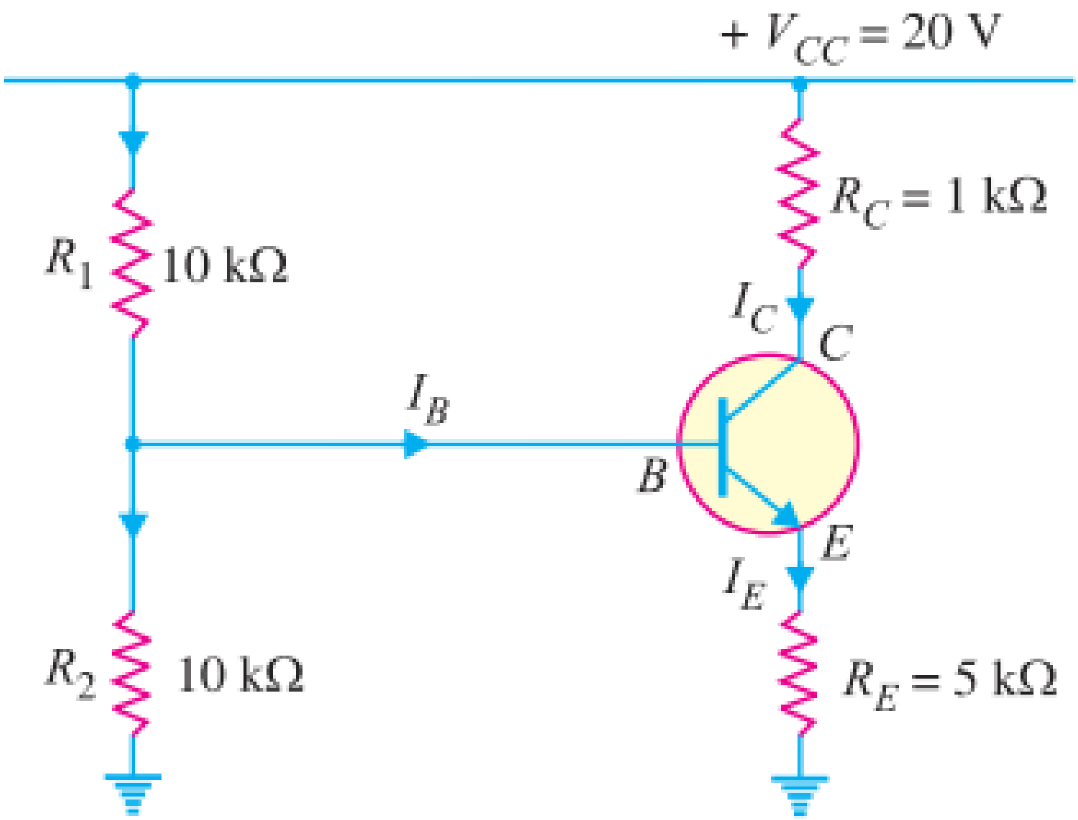
(i) Two resistors R_1 and R_2 are connected across the supply voltage V_{cc} and provide biasing.

(ii) The voltage drop across R_2 forward biases the base-emitter junction.

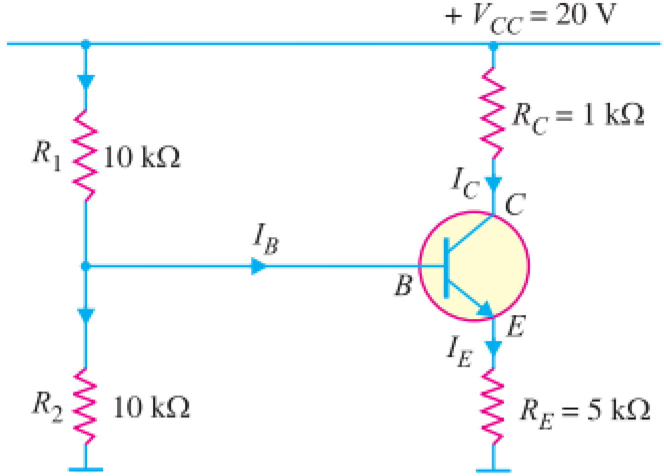
(iii) This causes the base current and hence collector current flow in the zero signal conditions.

Problem 14.6

Calculate the emitter current in the voltage divider circuit shown in Fig. Also find the value of V_{CE} and collector potential V_C.



Calculate the emitter current in the voltage divider circuit shown in Fig. Also find the value of V_{CE} and collector potential V_C.



$$\text{Voltage across } R_2,\ V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 = \left(\frac{20}{10 + 10}\right) 10 = 10 \text{ V}$$

Now $\quad V_2 = V_{BE} + I_E R_E$

As V_{BE} is generally small, therefore, it can be neglected.

$$\therefore \quad I_E = \frac{V_2}{R_E} = \frac{10 \text{ V}}{5 \text{ k}\Omega} = \mathbf{2\ mA}$$

Now $\quad I_C \simeq I_E = 2$ mA

$$\therefore \quad V_{CE} = V_{CC} - I_C(R_C + R_E) = 20 - 2 \text{ mA } (6 \text{ k}\Omega)$$
$$= 20 - 12 = \mathbf{8\ V}$$

$$\text{Collector potential, } V_C = V_{CC} - I_C R_C = 20 - 2 \text{ mA} \times 1 \text{ k}\Omega$$
$$= 20 - 2 = \mathbf{18\ V}$$

Thank You All