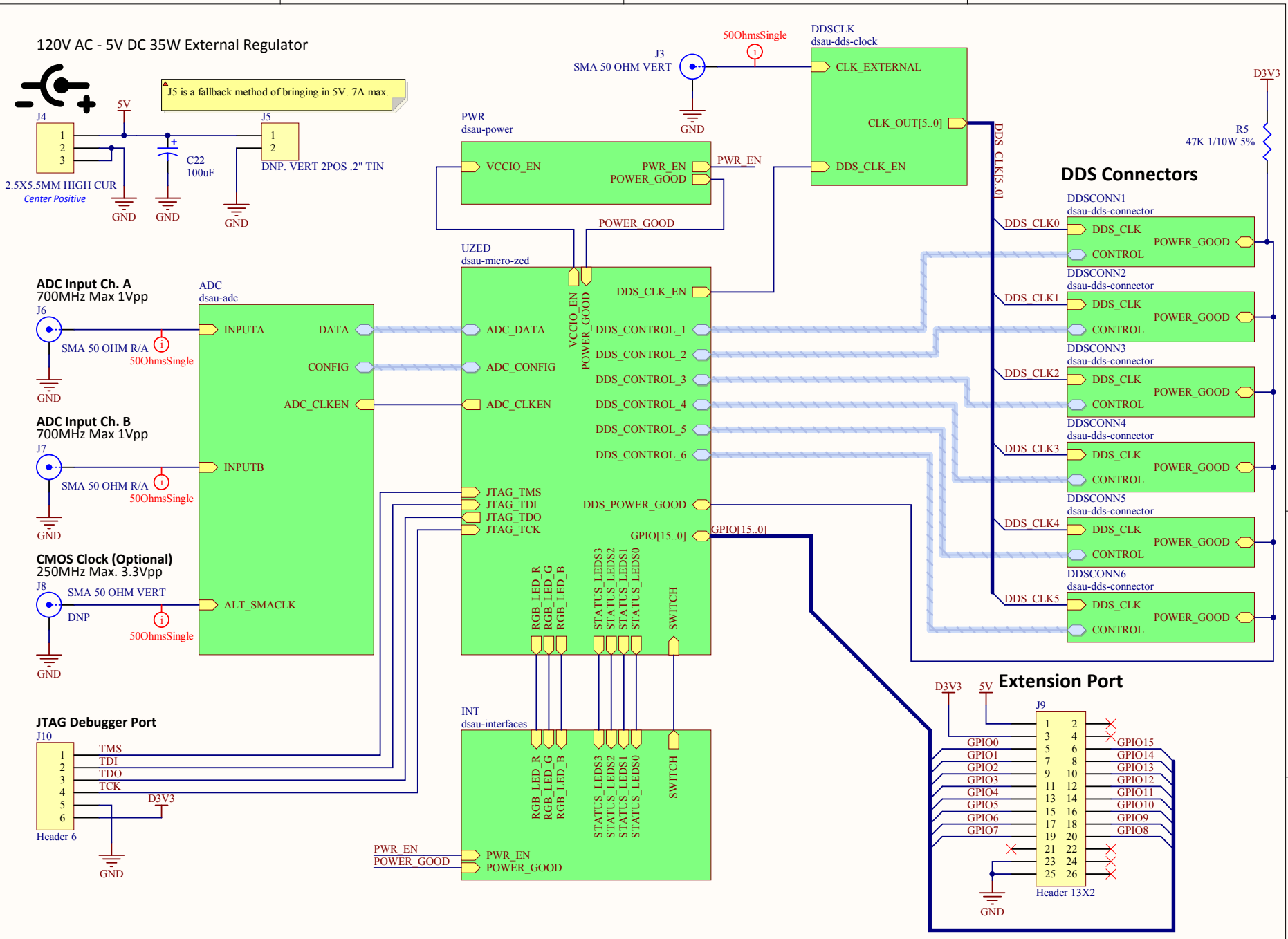
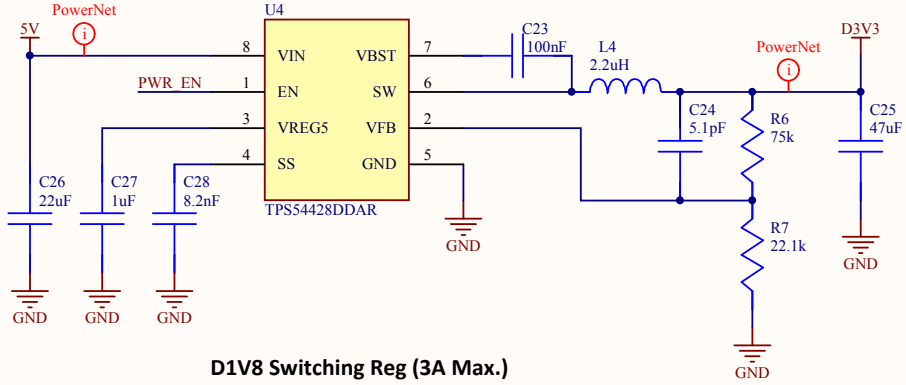
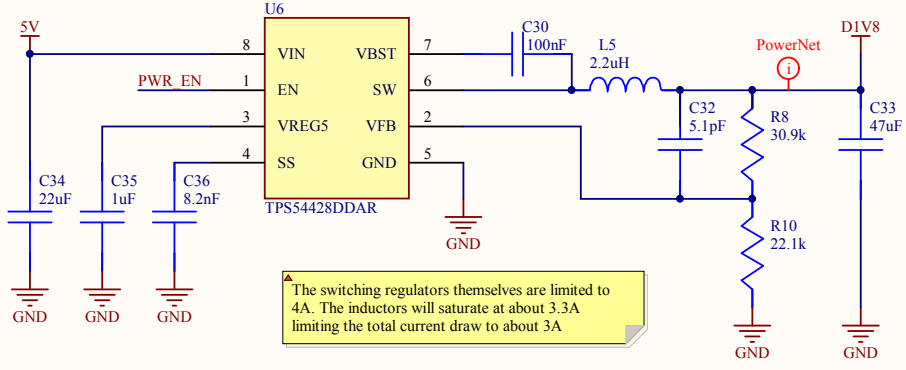

120V AC - 5V DC 35W External Regulator
J5 is a fallback method of bringing in 5V. 7A max.
J4
2.5X5.5MM HIGH CUR
Center Positive
5V
GND
C22
100uF
J5
DNP. VERT 2POS .2" TIN
J3
SMA 50 OHM VERT
50OhmsSingle
DDSCLK
dsau-dds-clock
CLK_EXTERNAL
CLK_OUT[5..0]
DDS_CLK_EN
D3V3
R5
47K 1/10W 5%
PWR
dsau-power
VCCIO_EN
PWR_EN
POWER_GOOD
DDS Connectors
DDSCONN1
dsau-dds-connector
DDSCONN2
DDSCONN3
DDSCONN4
DDSCONN5
DDSCONN6
DDS_CLK
CONTROL
DDS_CLK0
DDS_CLK1
DDS_CLK2
DDS_CLK3
DDS_CLK4
DDS_CLK5
UZED
dsau-micro-zed
ADC Input Ch. A
700MHz Max 1Vpp
J6
SMA 50 OHM R/A
ADC
dsau-adc
INPUTA
DATA
CONFIG
ADC_CLKEN
ADC_DATA
ADC_CONFIG
ADC_CLKEN
DDS_CONTROL_1
DDS_CONTROL_2
DDS_CONTROL_3
DDS_CONTROL_4
DDS_CONTROL_5
DDS_CONTROL_6
ADC Input Ch. B
700MHz Max 1Vpp
J7
INPUTB
CMOS Clock (Optional)
250MHz Max. 3.3Vpp
J8
DNP
ALT_SMACLK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TCK
DDS_POWER_GOOD
GPIO[15..0]
RGB_LED_R
RGB_LED_G
RGB_LED_B
STATUS_LEDS3
STATUS_LEDS2
STATUS_LEDS1
STATUS_LEDS0
SWITCH
JTAG Debugger Port
J10
TMS
TDI
TDO
TCK
Header 6
INT
dsau-interfaces
PWR_EN
POWER_GOOD
Extension Port
J9
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
Header 13X2
Title dSAU Motherboard - Top
Size: Letter
Number: 1
Revision: A
Date: 3/5/2014
Time: 3:43:16 PM
Sheet 1 of 10
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-motherboard-top.SchDoc
Boston University EDF/ECE
Team 19
Christopher J. Woodall
cwoodall@bu.edu
dDOS

D3V3 Switching Reg (3A Max.)

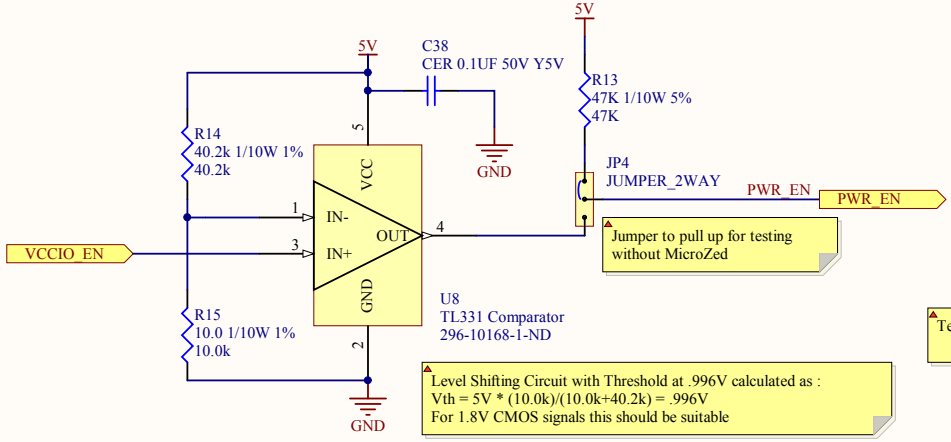


D1V8 Switching Reg (3A Max.)



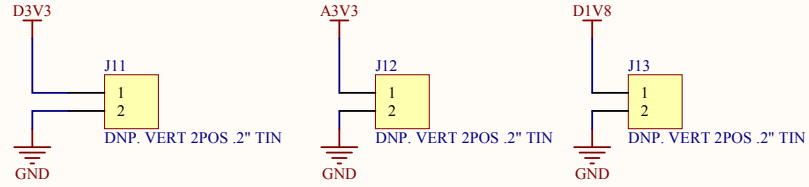
The switching regulators themselves are limited to 4A. The inductors will saturate at about 3.3A limiting the total current draw to about 3A

1.8V to 5V Level Shifter



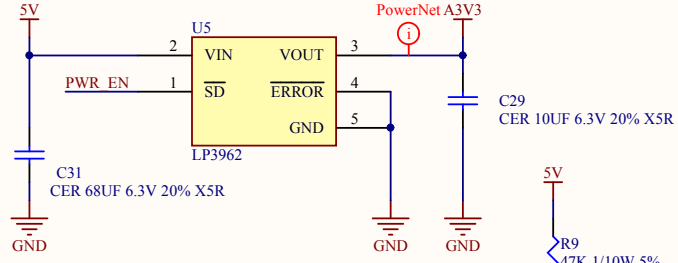
Jumper to pull up for testing without MicroZed

Level Shifting Circuit with Threshold at .996V calculated as :
Vth = 5V * (10.0k)/(10.0k+40.2k) = .996V
For 1.8V CMOS signals this should be suitable

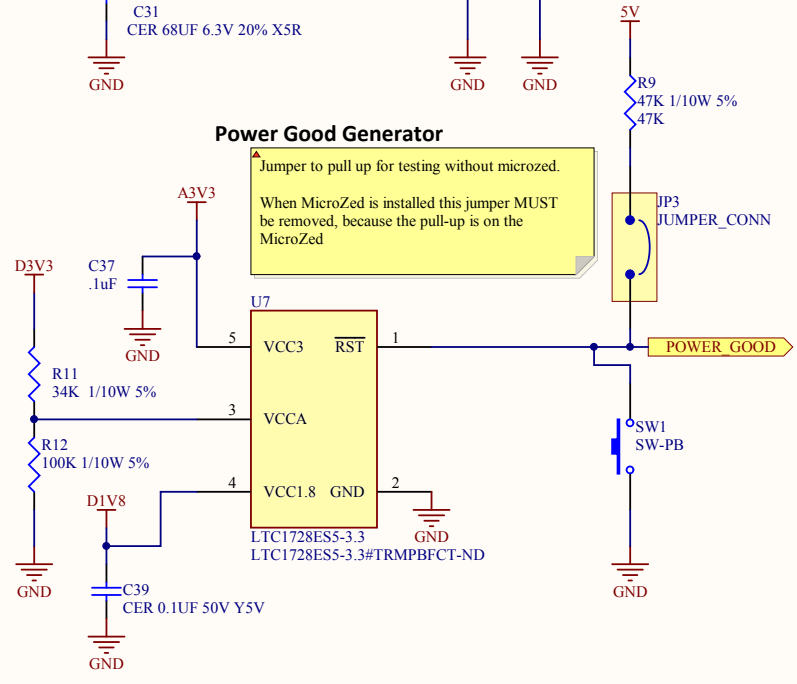


J10, J12, and J11 are fallback methods for bringing in power (DNP).
7A MAX.

A3V3 LDO



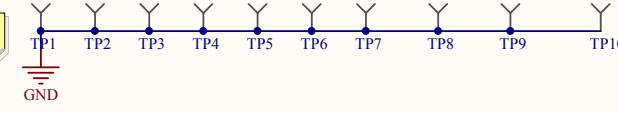
Power Good Generator



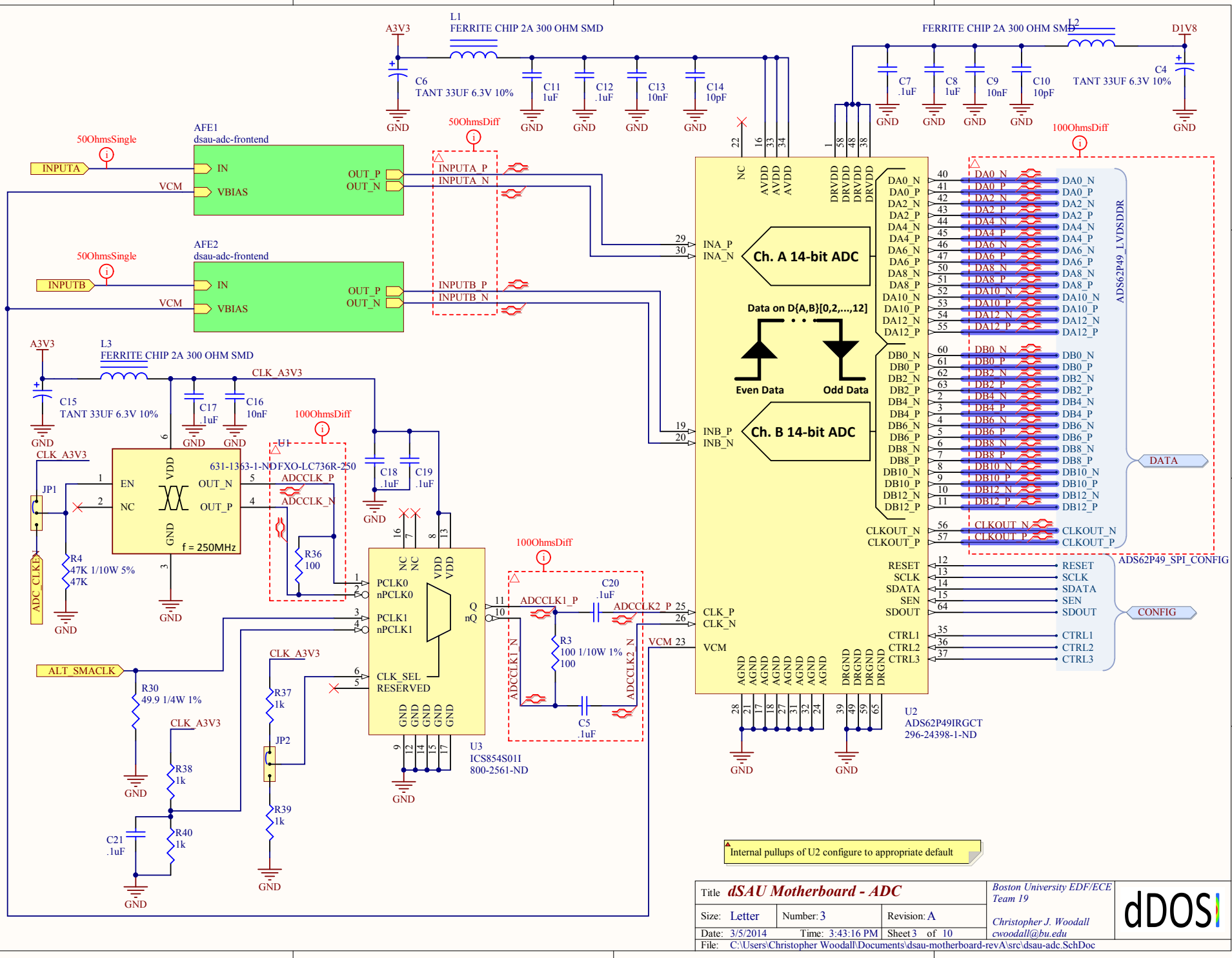
Jumper to pull up for testing without microzed.

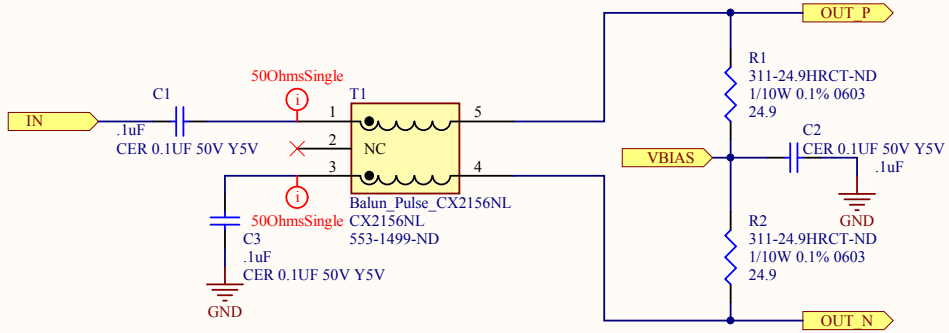
When MicroZed is installed this jumper MUST be removed, because the pull-up is on the MicroZed

Testpoint Grounds. Scatter at will.



Title: *dSAU Motherboard - Power*			*Boston University EDF/ECE Team 19*
Size: Letter	Number: 2	Revision: A	*Christopher J. Woodall* *cwoodall@bu.edu*
Date: 3/5/2014	Time: 3:43:16 PM	Sheet 2 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-power.SchDoc			


A3V3
L1
FERRITE CHIP 2A 300 OHM SMD
C6
TANT 33UF 6.3V 10%
C11
1uF
C12
.1uF
C13
10nF
C14
10pF
GND
L2
FERRITE CHIP 2A 300 OHM SMD
D1V8
C7
.1uF
C8
1uF
C9
10nF
C10
10pF
C4
TANT 33UF 6.3V 10%
50OhmsSingle
AFE1
dsau-adc-frontend
INPUTA
VCM
IN
VBIAS
OUT_P
OUT_N
50OhmsDiff
INPUTA_P
INPUTA_N
AFE2
dsau-adc-frontend
INPUTB
INPUTB_P
INPUTB_N
100OhmsDiff
NC
AVDD
DRVDD
INA_P
INA_N
Ch. A 14-bit ADC
Data on D{A,B}[0,2,...,12]
Even Data
Odd Data
INB_P
INB_N
Ch. B 14-bit ADC
DA0_N
DA0_P
DA2_N
DA2_P
DA4_N
DA4_P
DA6_N
DA6_P
DA8_N
DA8_P
DA10_N
DA10_P
DA12_N
DA12_P
DB0_N
DB0_P
DB2_N
DB2_P
DB4_N
DB4_P
DB6_N
DB6_P
DB8_N
DB8_P
DB10_N
DB10_P
DB12_N
DB12_P
CLKOUT_N
CLKOUT_P
ADS62P49_LVDSDDR
DATA
RESET
SCLK
SDATA
SEN
SDOUT
CTRL1
CTRL2
CTRL3
ADS62P49_SPI_CONFIG
CONFIG
CLK_P
CLK_N
VCM
AGND
DRGND
U2
ADS62P49IRGCT
296-24398-1-ND
L3
FERRITE CHIP 2A 300 OHM SMD
CLK_A3V3
C15
TANT 33UF 6.3V 10%
C17
.1uF
C16
10nF
C18
.1uF
C19
.1uF
U1
631-13363-1-ND
FXO-LC736R-250
f = 250MHz
EN
NC
VDD
OUT_N
OUT_P
GND
JP1
R4
47K 1/10W 5%
47K
ADC_CLKD
ADCCLK_P
ADCCLK_N
R36
100
U3
ICS854S01I
800-2561-ND
PCLK0
nPCLK0
PCLK1
nPCLK1
CLK_SEL
RESERVED
Q
nQ
ADCCLK1_P
ADCCLK2_P
ADCCLK1_N
ADCCLK2_N
C20
.1uF
R3
100 1/10W 1%
100
C5
.1uF
ALT_SMACLK
R30
49.9 1/4W 1%
R37
1k
JP2
R38
1k
R39
1k
R40
1k
C21
.1uF
Internal pullups of U2 configure to appropriate default
Title dSAU Motherboard - ADC
Size: Letter
Number: 3
Revision: A
Date: 3/5/2014
Time: 3:43:16 PM
Sheet 3 of 10
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-adc.SchDoc
Boston University EDF/ECE
Team 19
Christopher J. Woodall
cwoodall@bu.edu
dDOS

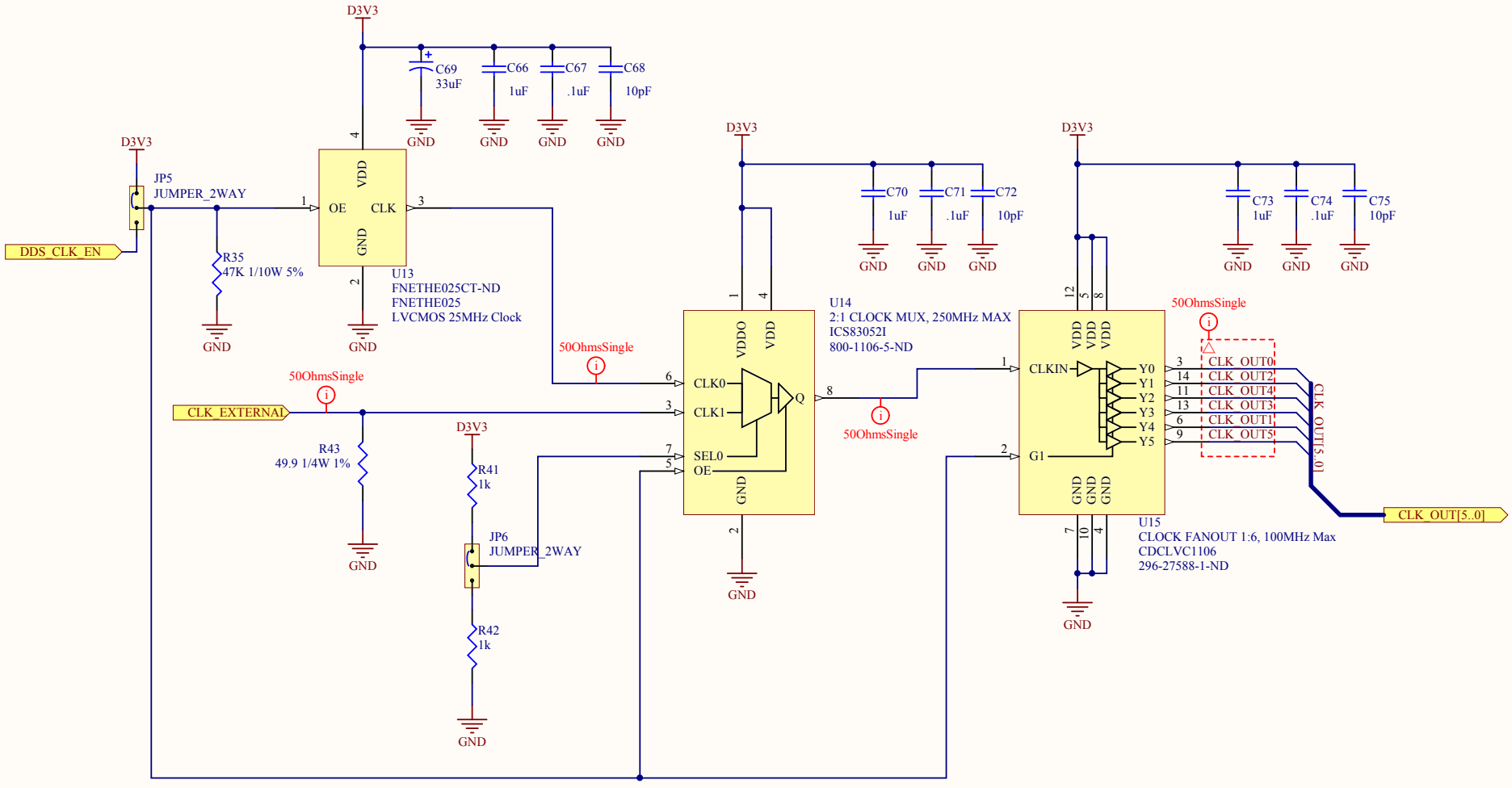


This frontend's main responsibility is converting from an unbalanced 50-Ohm input to a balanced 50-Ohm signal for interactions into the ADC.

This particular configuration is taken from the ADS62P49 datasheet and is expected to rely on the ADCs internal filter with a cutoff of 700MHz.

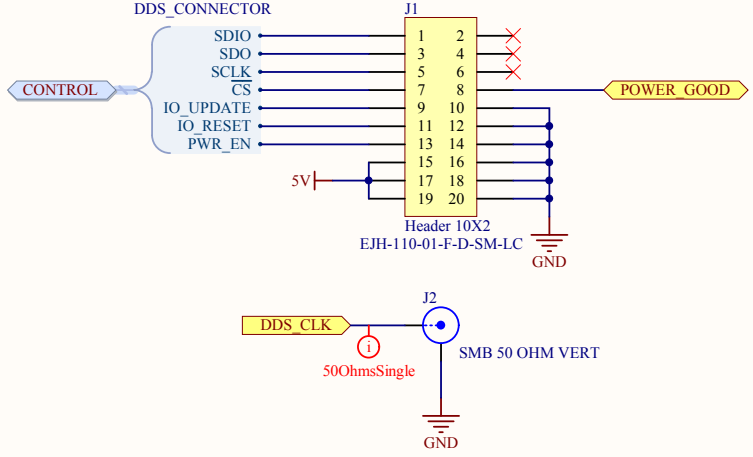
External filters are suggested for best performance.

Title	***dSAU Motherboard - ADC Frontend***		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 4	Revision: A	*Christopher J. Woodall* *cwoodall@bu.edu*
Date: 3/5/2014	Time: 3:43:16 PM	Sheet 4 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-adc-frontend.SchDoc			



Title	*dSAU Motherboard - DDS Clock Gen.*		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 5	Revision: A	*Christopher J. Woodall cwoodall@bu.edu*
Date: 3/5/2014	Time: 3:43:16 PM	Sheet 5 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-dds-clock.SchDoc			

Standard Connector to Single Channel DDS Board.



Title	***dSAU Motherboard - DDS Connector***		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 6	Revision: A	*Christopher J. Woodall cwoodall@bu.edu*
Date: 3/5/2014	Time: 3:43:16 PM	Sheet 6 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-dds-connector.SchDoc			

BANK13 is NOT available with the Z7010.

U9E

MicroZed (TM) Bank13

Z7020 Only

BANK13_LVDS_0_N (Bank 13, V7) 89
BANK13_LVDS_0_P (Bank 13, U7) 87
BANK13_LVDS_2_N (Bank 13, W8) 93
BANK13_LVDS_2_P (Bank 13, V8) 91
BANK13_LVDS_1_N (Bank 13, U10) 90
BANK13_LVDS_1_P (Bank 13, T9) 88
BANK13_LVDS_3_N (Bank 13, U5) 94
BANK13_LVDS_3_P (Bank 13, T5) 92
BANK13_LVDS_4_N (Bank 13, Y13) 195
BANK13_LVDS_4_P (Bank 13, Y12) 193
BANK13_LVDS_6_N (Bank 13, W6) 199
BANK13_LVDS_6_P (Bank 13, V6) 197
BANK13_LVDS_5_N (Bank 13, V10) 196
BANK13_LVDS_5_P (Bank 13, V11) 194
BANK13_SE_0 (Bank 13, V5) 200

MicroZed (Z7010)

D3V3 L6 FERRITE CHIP 2A 300 OHM SMD PowerNet

C40 TANT 33UF 6.3V 10% 33uF
C46 .1uF
C47 .1uF
C48 10nF
C49 10pF

GND

L7 FERRITE CHIP 2A 300 OHM SMD PowerNet

C55 33uF
C56 .1uF
C57 .1uF
C58 10nF
C59 10pF

5V

C41 100uF
C42 .1uF
C43 .1uF
C44 .1uF
C45 .1uF
C50 10pF
C51 10pF
C52 10nF
C53 10nF
C54 10nF

198 79 78 80 179 178 180 57 59 58 60 157 159 112 158 160

VCCO_13 VCCO_34 VCCO_34 VCCO_34 VCCO_35 VCCO_35 VCCO_35 VIN_HDR VIN_HDR VIN_HDR VIN_HDR VIN_HDR VIN_HDR VIN_HDR VIN_HDR

U9A

MicroZed (Z7010)

MicroZed (TM) Power Block

POWER_GOOD 111 PG_MODULE (Bank 500, C7)

VCCIO_EN 110 VCCIO_EN

DXN_0_N (Bank 0, M10) 100
DXP_0_P (Bank 0, M9) 98
VN_0_N (Bank 0, K9) 99
VP_0_P (Bank 0, L10) 97

Note: Pins 10X corresponds to jx2 pin X

GND 15 21 27 33 39 45 51 65 71 77 85 95 16 22 28 34 40 46 52 66 72 86 96 115 121 127 133 139 145 151 165 171 177 185 191 116 122 128 134 140 146 152 166 172 186 192

UZEDB34

dsau-micro-zed-bank34

ADC_DATA ADC_DATA ADC_CLKEN ADC_CLKEN

ADC_CONFIG ADC_CONFIG RGB_LED_B RGB_LED_R
RGB_LED_G RGB_LED_G
RGB_LED_R RGB_LED_B

STATUS_LEDS0 STATUS_LEDS0
STATUS_LEDS1 STATUS_LEDS1
STATUS_LEDS3 STATUS_LEDS2
SWITCH SWITCH STATUS_LEDS2 STATUS_LEDS3

UZEDB35

dsau-micro-zed-bank35

DDS_POWER_GOOD DDS_POWER_GOOD DDS_CONTROL_1 DDS_CONTROL_1
DDS_CONTROL_2 DDS_CONTROL_2
DDS_CONTROL_3 DDS_CONTROL_3
DDS_CONTROL_4 DDS_CONTROL_4
DDS_CONTROL_5 DDS_CONTROL_5
DDS_CONTROL_6 DDS_CONTROL_6

GPIO[15..0] GPIO[15..0] GPIO[15..0]

DDS_CLK_EN DDS_CLK_EN

U9B

MicroZed (TM) Control Block

JTAG_TCK 1 JTAG_TCK (Bank 0, F9)
JTAG_TDI 4 JTAG_TDI (Bank 0, G6)
JTAG_TDO 3 JTAG_TDO (Bank 0, F6)
JTAG_TMS 2 JTAG_TMS (Bank 0, J6)
TP1 5 PWR_ENABLE
TP1 6 CARRIER_SRST
TP1 109 INIT (Bank 0, R10)
TP1 8 FPGA_DONE (Bank 0, R11)
7 FPGA_VBATT

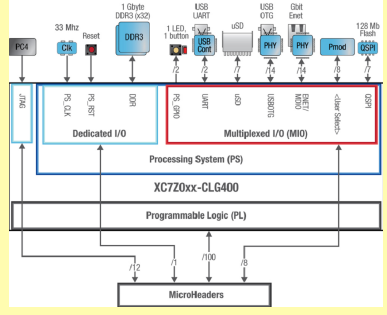


Image From zedboard.org

Pins 1-100 correspond to JX1 1-100

Pins 101-200 correspond to JX2 1-100

101 PMOD_D0 (Bank 500, E6)
102 PMOD_D1 (Bank 500, B5)
103 PMOD_D2 (Bank 500, E9)
104 PMOD_D3 (Bank 500, C6)
105 PMOD_D4 (Bank 500, D9)
106 PMOD_D5 (Bank 500, E8)
107 PMOD_D6 (Bank 500, C5)
108 PMOD_D7 (Bank 500, C8)

MicroZed (Z7010)

BANK500/PMOD is hooked up to the PS directly.

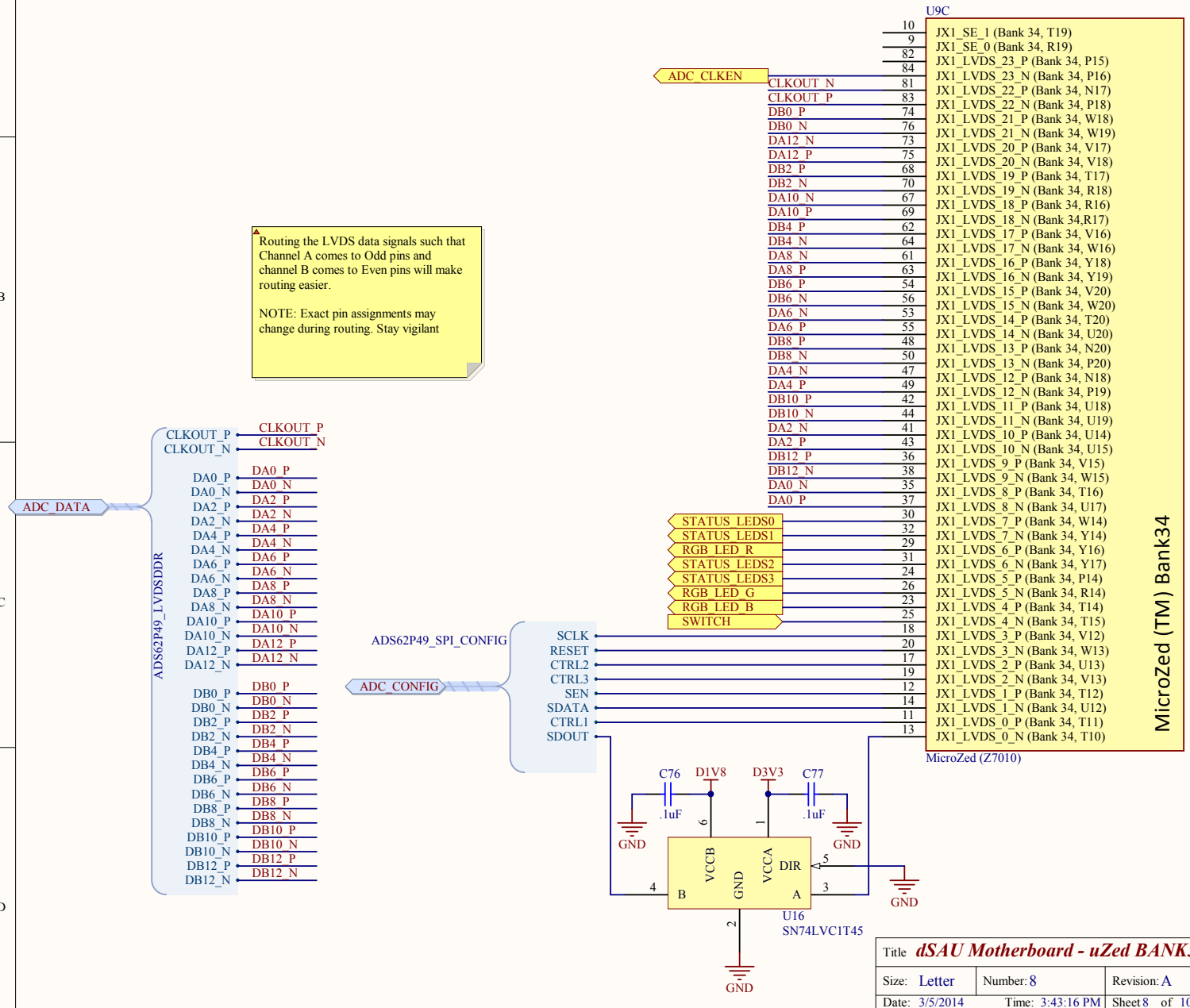
Title: *dSAU Motherboard - MicroZed*			*Boston University EDF/ECE Team 19*
Size: Letter	Number: 7	Revision: A	*Christopher J. Woodall cwoodall@bu.edu*
Date: 3/5/2014	Time: 3:43:16 PM	Sheet 7 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed.SchDoc			

BANK34 (1.8V)

BANK34 (1.8V) is used soley for connections to the 1.8V 7bit DDR (time multiplexed) LVDS inputs from the ADS62P49 ADC, and for Control Signals (an SPI port) to and from the ADS62P49.

Routing the LVDS data signals such that Channel A comes to Odd pins and channel B comes to Even pins will make routing easier.

NOTE: Exact pin assignments may change during routing. Stay vigilant

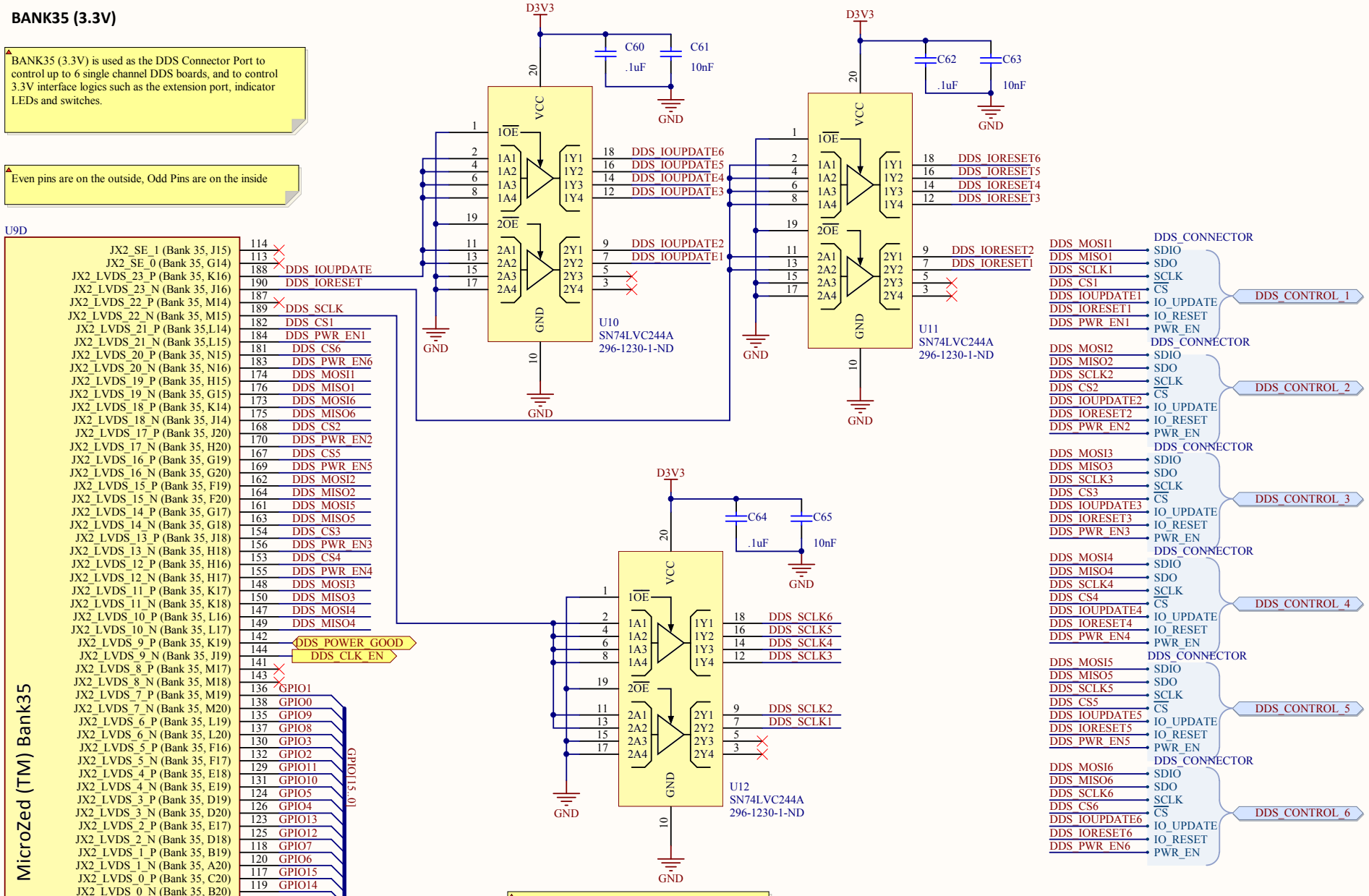


Title	dSAU Motherboard - uZed BANK34		Boston University EDF/ECE Team 19
Size: Letter	Number: 8	Revision: A	Christopher J. Woodall cwoodall@bu.edu
Date: 3/5/2014	Time: 3:43:16 PM	Sheet 8 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed-bank34.SchDoc			

BANK35 (3.3V)

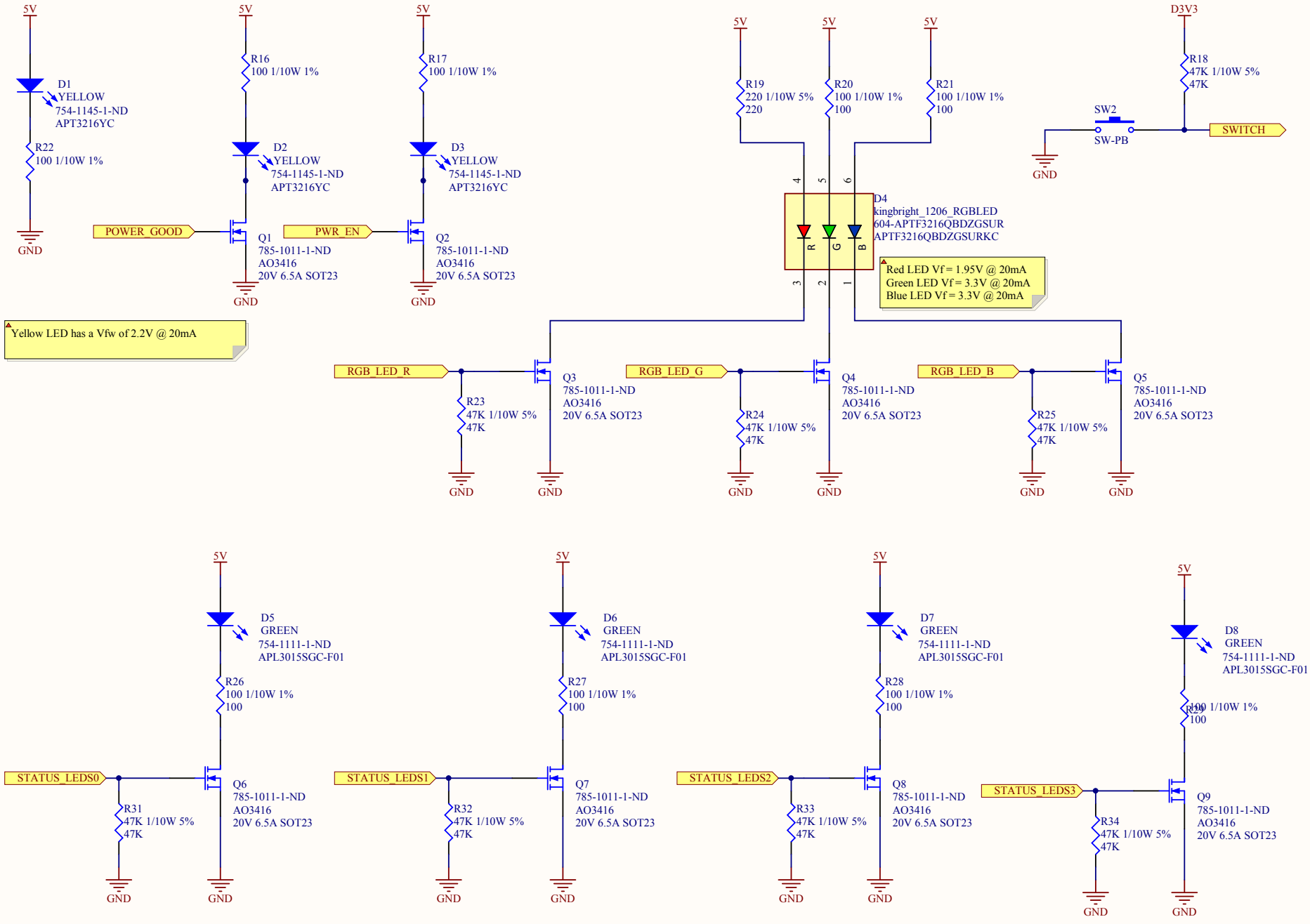
BANK35 (3.3V) is used as the DDS Connector Port to control up to 6 single channel DDS boards, and to control 3.3V interface logics such as the extension port, indicator LEDs and switches.

Even pins are on the outside, Odd Pins are on the inside



Buffer Common Signals (SCLK, IOUPDATE and IORESET) to drive over the 6 connectors.

Title	dSAU Motherboard - uZed BANK35		Boston University EDF/ECE Team 19
Size: Letter	Number: 9	Revision: A	Christopher J. Woodall cwoodall@bu.edu
Date: 3/5/2014	Time: 3:43:16 PM	Sheet 9 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed-bank35.SchDoc			


5V
D1
YELLOW
754-1145-1-ND
APT3216YC
R22
100 1/10W 1%
GND
R16
100 1/10W 1%
D2
YELLOW
754-1145-1-ND
APT3216YC
POWER_GOOD
Q1
785-1011-1-ND
AO3416
20V 6.5A SOT23
R17
100 1/10W 1%
D3
YELLOW
754-1145-1-ND
APT3216YC
PWR_EN
Q2
785-1011-1-ND
AO3416
20V 6.5A SOT23
Yellow LED has a Vfw of 2.2V @ 20mA
R19
220 1/10W 5%
220
R20
100 1/10W 1%
100
R21
100 1/10W 1%
100
D4
kingbright_1206_RGBLED
604-APTF3216QBDZGSUR
APTF3216QBDZGSURKC
R
G
B
Red LED Vf = 1.95V @ 20mA
Green LED Vf = 3.3V @ 20mA
Blue LED Vf = 3.3V @ 20mA
D3V3
R18
47K 1/10W 5%
47K
SW2
SW-PB
SWITCH
RGB_LED_R
Q3
785-1011-1-ND
AO3416
20V 6.5A SOT23
R23
47K 1/10W 5%
47K
RGB_LED_G
Q4
785-1011-1-ND
AO3416
20V 6.5A SOT23
R24
47K 1/10W 5%
47K
RGB_LED_B
Q5
785-1011-1-ND
AO3416
20V 6.5A SOT23
R25
47K 1/10W 5%
47K
D5
GREEN
754-1111-1-ND
APL3015SGC-F01
R26
100 1/10W 1%
100
STATUS_LEDS0
Q6
785-1011-1-ND
AO3416
20V 6.5A SOT23
R31
47K 1/10W 5%
47K
D6
GREEN
754-1111-1-ND
APL3015SGC-F01
R27
100 1/10W 1%
100
STATUS_LEDS1
Q7
785-1011-1-ND
AO3416
20V 6.5A SOT23
R32
47K 1/10W 5%
47K
D7
GREEN
754-1111-1-ND
APL3015SGC-F01
R28
100 1/10W 1%
100
STATUS_LEDS2
Q8
785-1011-1-ND
AO3416
20V 6.5A SOT23
R33
47K 1/10W 5%
47K
D8
GREEN
754-1111-1-ND
APL3015SGC-F01
R29
100 1/10W 1%
100
STATUS_LEDS3
Q9
785-1011-1-ND
AO3416
20V 6.5A SOT23
R34
47K 1/10W 5%
47K
Green LED has a Vfw of 2.2V @ 20mA
Title dSAU Motherboard - LEDs/Switches
Size: Letter
Number: 10
Revision: A
Date: 3/5/2014
Time: 3:43:16 PM
Sheet 10 of 10
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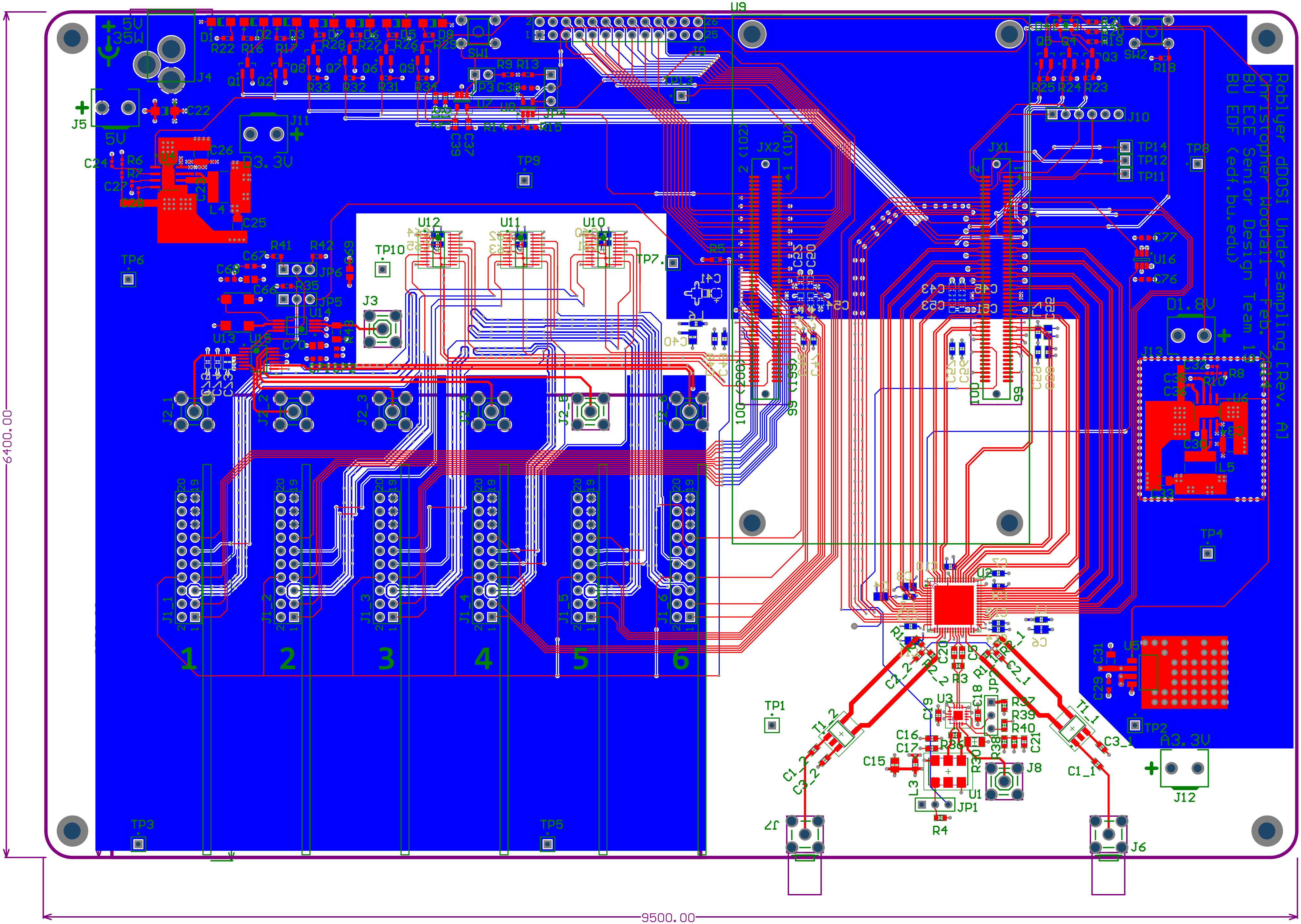
dDOS


Robiyer dDOSI Undersampling [Rev. A]
Christopher Woodall - Feb. 2014
BU ECE Senior Design Team 19
BU EDF (edf.bu.edu)
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