

Title **dSAU Motherboard - Top**

Boston University EDF/ECE  
Team 19

Size: Letter

Number: 1

Revision: A

Date: 3/12/2014

Time: 4:26:24 PM

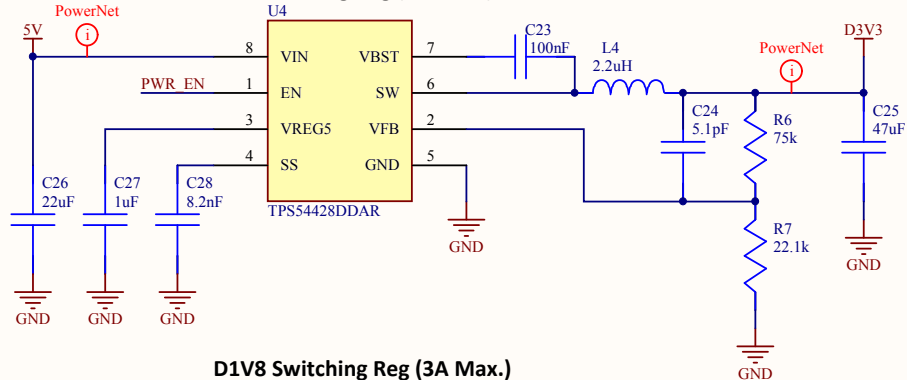
Sheet 1 of 10

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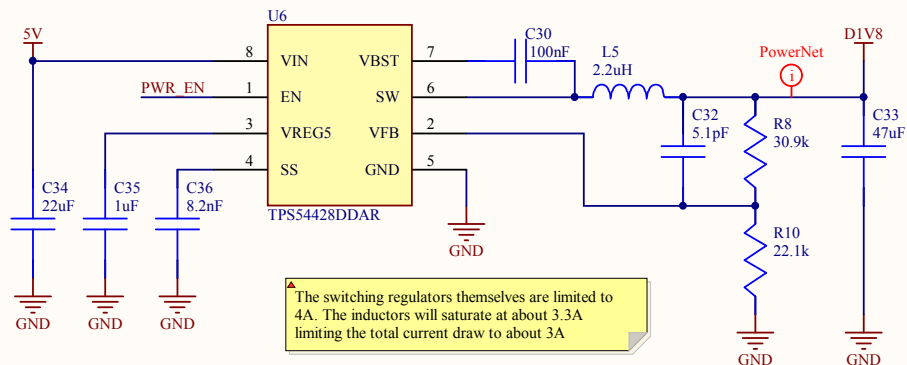
**dDOS**

File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-motherboard-top.SchDoc

### D3V3 Switching Reg (3A Max.)

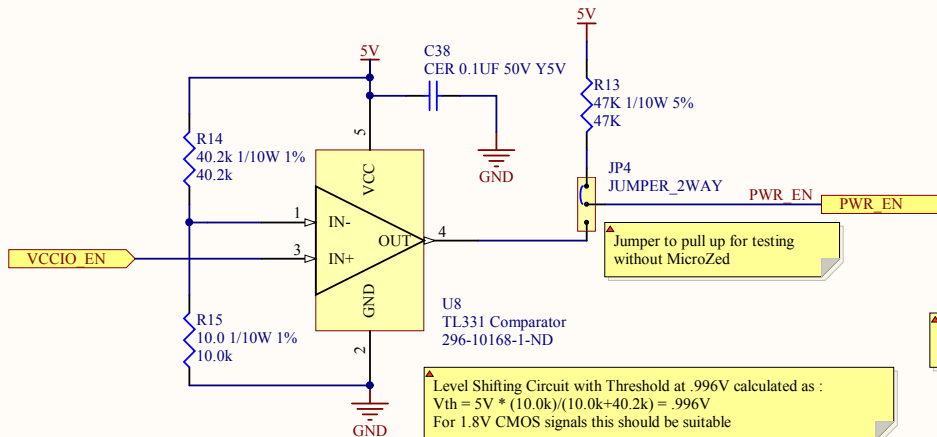


### D1V8 Switching Reg (3A Max.)

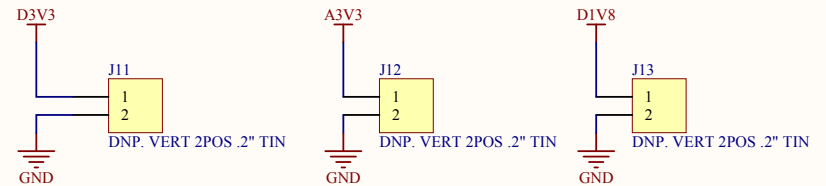


The switching regulators themselves are limited to 4A. The inductors will saturate at about 3.3A limiting the total current draw to about 3A

### 1.8V to 5V Level Shifter

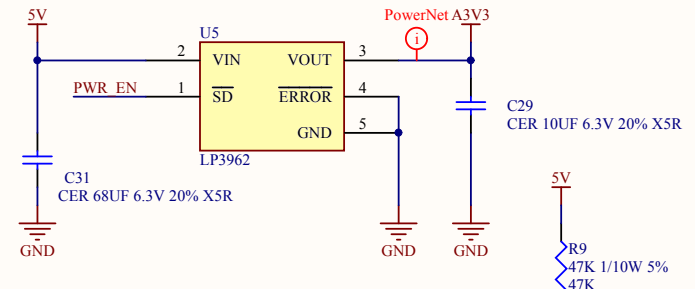


Level Shifting Circuit with Threshold at .996V calculated as :  
 $V_{th} = 5V * (10.0k) / (10.0k + 40.2k) = .996V$   
 For 1.8V CMOS signals this should be suitable



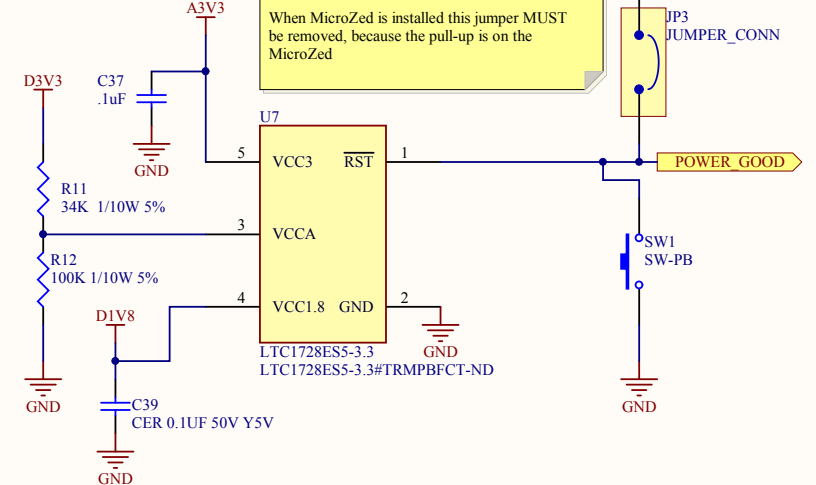
J10, J12, and J11 are fallback methods for bringing in power (DNP). 7A MAX.

### A3V3 LDO

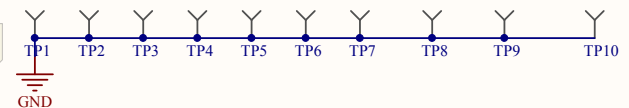


### Power Good Generator

Jumper to pull up for testing without microzed.  
 When MicroZed is installed this jumper MUST be removed, because the pull-up is on the MicroZed



Testpoint Grounds. Scatter at will.



Title **dSAU Motherboard - Power**

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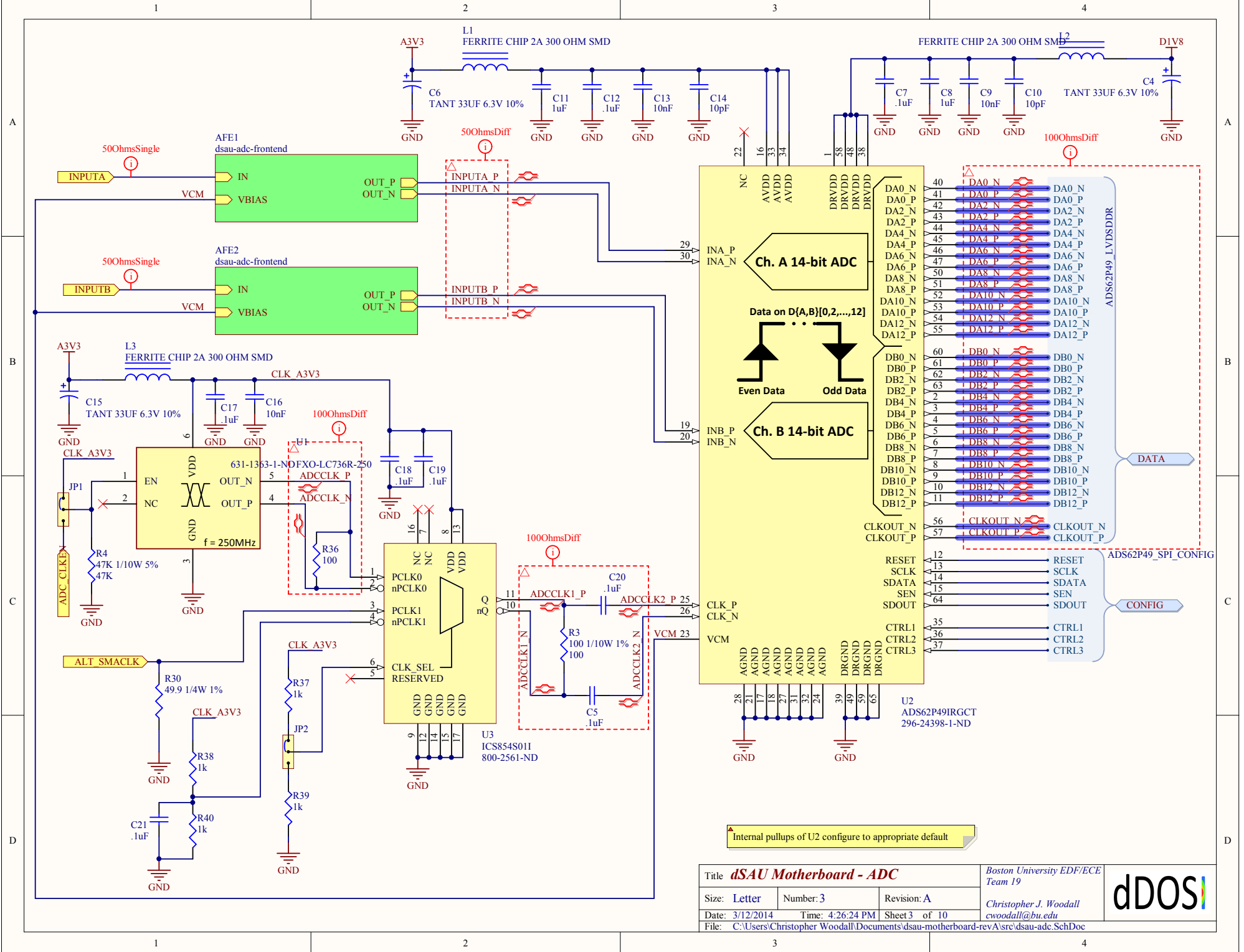
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File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-power.SchDoc

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**dDOS**

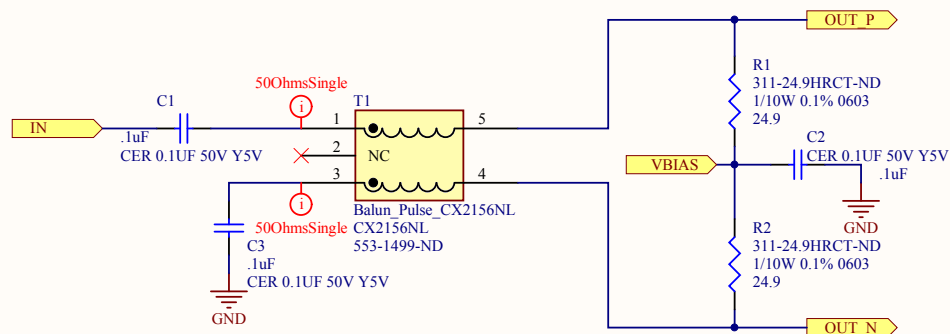


# Title **dSAU Motherboard - ADC**

Size: **Letter**    Number: **3**    Revision: **A**  
Date: **3/12/2014**    Time: **4:26:24 PM**    Sheet **3** of **10**  
File: **C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-adc.SchDoc**

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**dDOS**

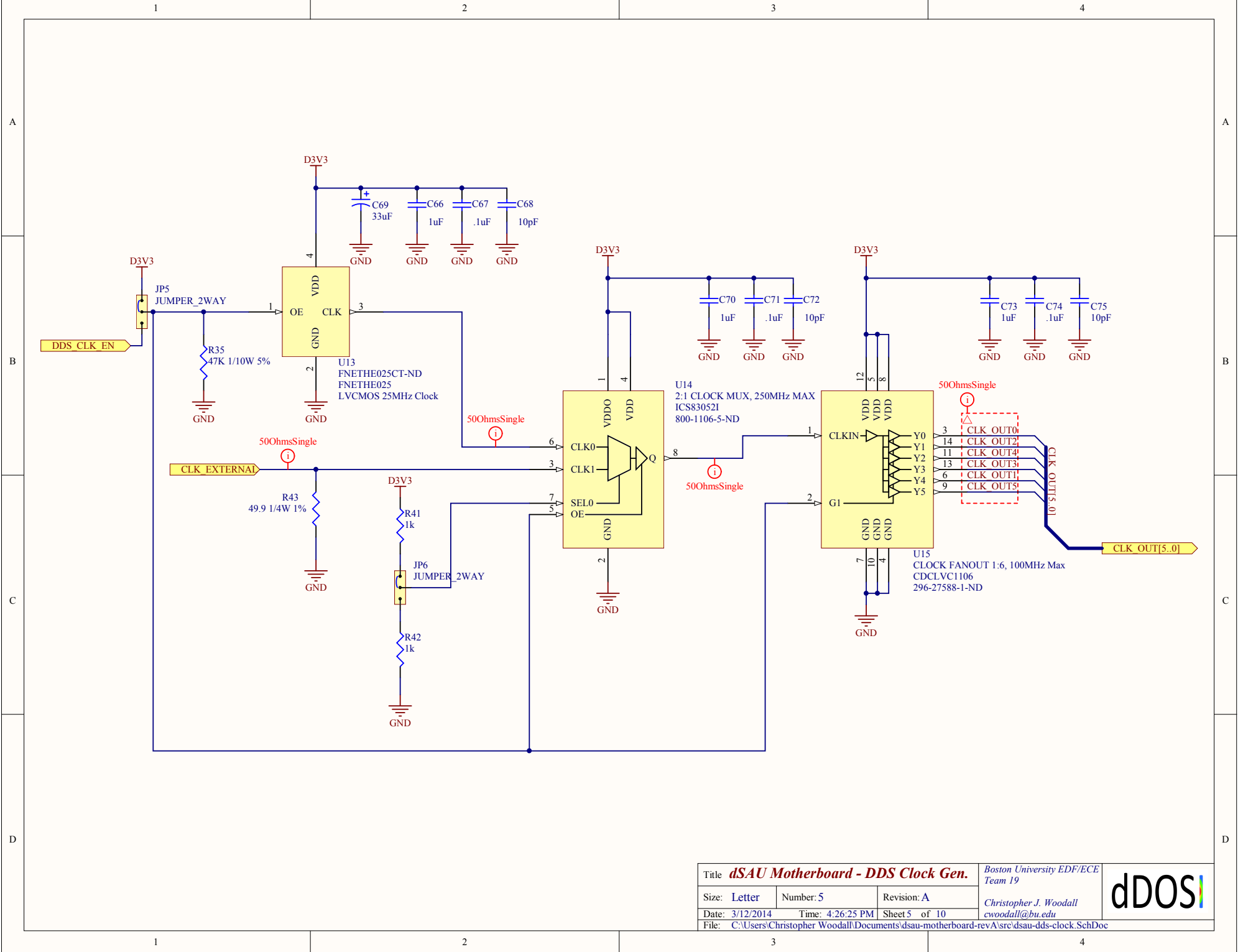


This frontend's main responsibility is converting from an unbalanced 50-Ohm input to a balanced 50-Ohm signal for interactions into the ADC.

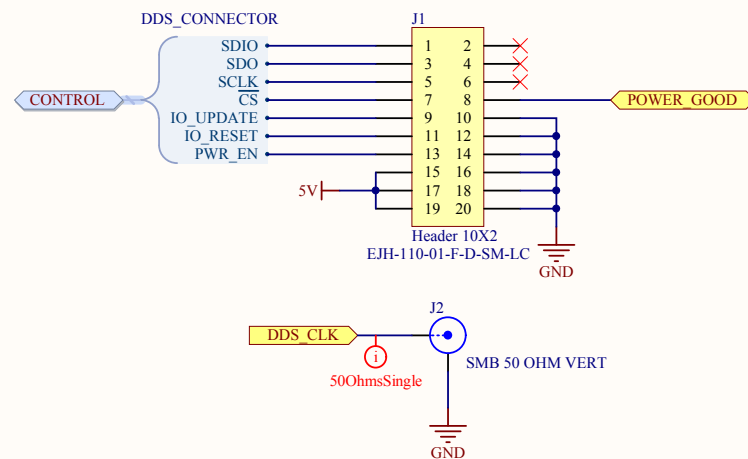
This particular configuration is taken from the ADS62P49 datasheet and is expected to rely on the ADCs internal filter with a cutoff of 700MHz.

External filters are suggested for best performance.

Title <b><i>dSAU Motherboard - ADC Frontend</i></b>			Boston University EDF/ECE Team 19  Christopher J. Woodall cwoodall@bu.edu	
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File: <b>C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\srs\dsau-adc-frontend.SchDoc</b>				



### Standard Connector to Single Channel DDS Board.



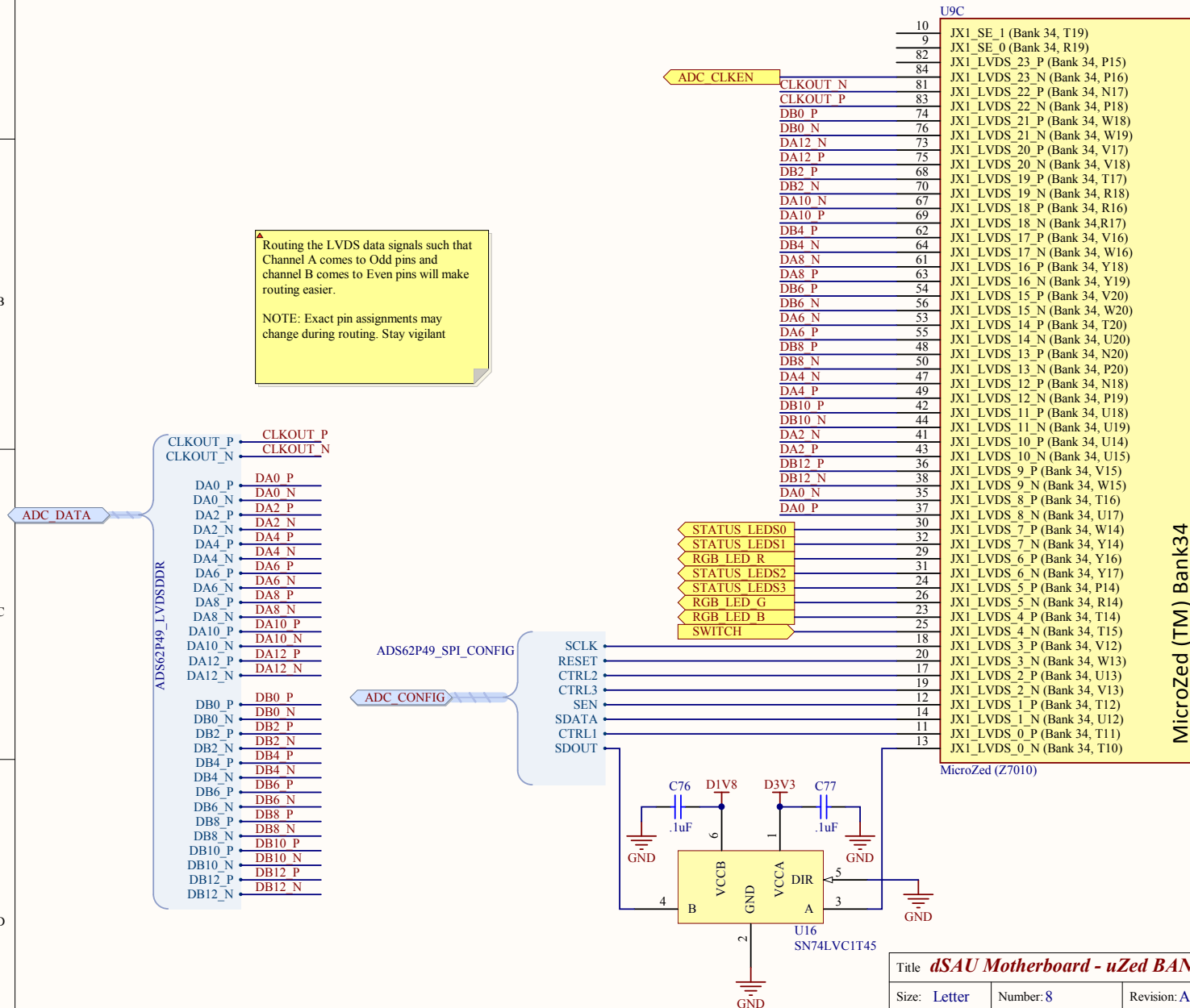


## BANK34 (1.8V)

▲ BANK34 (1.8V) is used solely for connections to the 1.8V 7bit DDR (time multiplexed) LVDS inputs from the ADS62P49 ADC, and for Control Signals (an SPI port) to and from the ADS62P49.

▲ Routing the LVDS data signals such that Channel A comes to Odd pins and channel B comes to Even pins will make routing easier.

NOTE: Exact pin assignments may change during routing. Stay vigilant



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File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed-bank34.SchDoc

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**dDOS**



# BANK35 (3.3V)

BANK35 (3.3V) is used as the DDS Connector Port to control up to 6 single channel DDS boards, and to control 3.3V interface logics such as the extension port, indicator LEDs and switches.

Even pins are on the outside, Odd Pins are on the inside

U9D

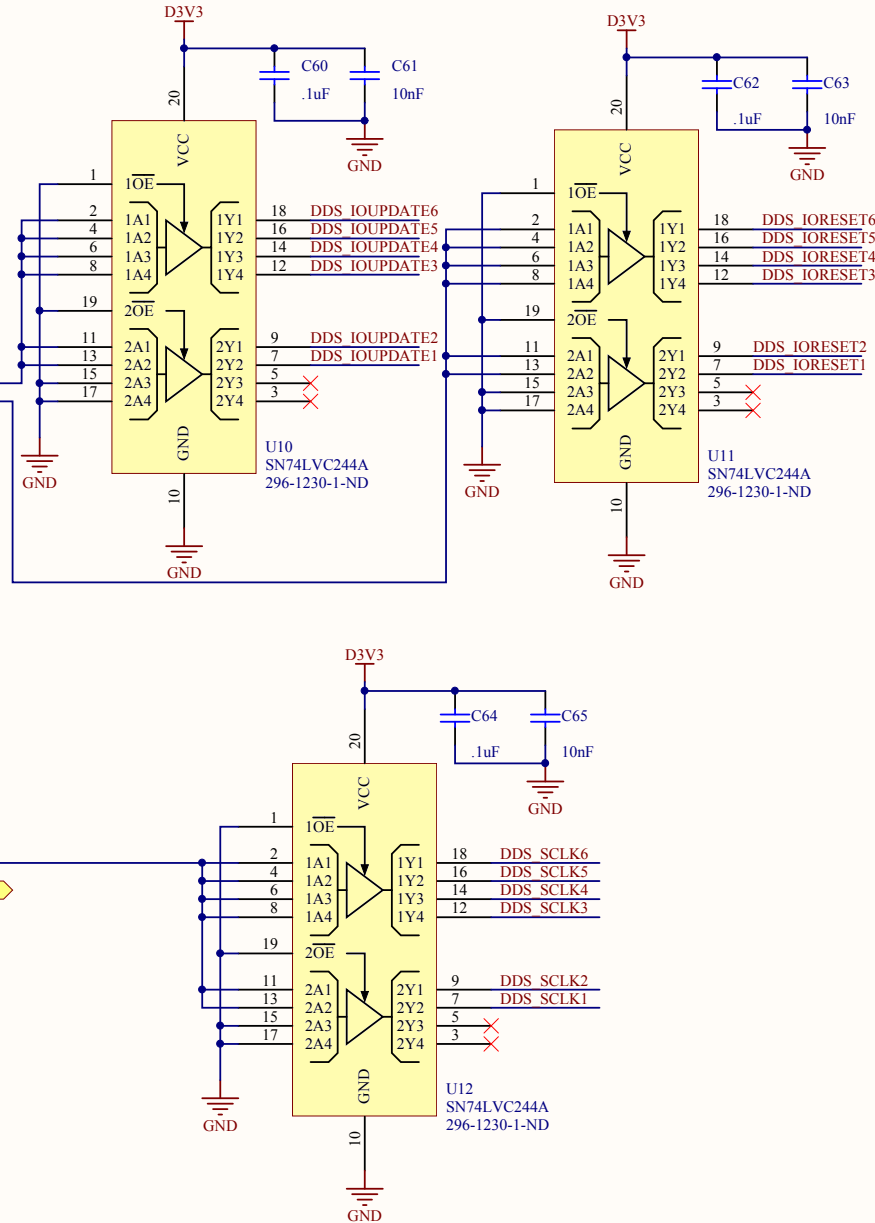
JX2_SE_1 (Bank 35, J15)	114	X
JX2_SE_0 (Bank 35, G14)	113	X
JX2_LVDS_23_P (Bank 35, K16)	188	X
JX2_LVDS_23_N (Bank 35, J16)	190	X
JX2_LVDS_22_P (Bank 35, M14)	187	X
JX2_LVDS_22_N (Bank 35, M15)	189	X
JX2_LVDS_21_P (Bank 35, L14)	184	X
JX2_LVDS_21_N (Bank 35, L15)	181	X
JX2_LVDS_20_P (Bank 35, N15)	183	X
JX2_LVDS_20_N (Bank 35, N16)	174	X
JX2_LVDS_19_P (Bank 35, H15)	176	X
JX2_LVDS_19_N (Bank 35, G15)	173	X
JX2_LVDS_18_P (Bank 35, K14)	175	X
JX2_LVDS_18_N (Bank 35, J14)	168	X
JX2_LVDS_17_P (Bank 35, J20)	170	X
JX2_LVDS_17_N (Bank 35, H20)	167	X
JX2_LVDS_16_P (Bank 35, G19)	169	X
JX2_LVDS_16_N (Bank 35, G20)	162	X
JX2_LVDS_15_P (Bank 35, F19)	164	X
JX2_LVDS_15_N (Bank 35, F20)	161	X
JX2_LVDS_14_P (Bank 35, G17)	163	X
JX2_LVDS_14_N (Bank 35, G18)	154	X
JX2_LVDS_13_P (Bank 35, J18)	156	X
JX2_LVDS_13_N (Bank 35, H18)	153	X
JX2_LVDS_12_P (Bank 35, H16)	155	X
JX2_LVDS_12_N (Bank 35, H17)	148	X
JX2_LVDS_11_P (Bank 35, K17)	150	X
JX2_LVDS_11_N (Bank 35, K18)	147	X
JX2_LVDS_10_P (Bank 35, L16)	149	X
JX2_LVDS_10_N (Bank 35, L17)	142	X
JX2_LVDS_9_P (Bank 35, K19)	144	X
JX2_LVDS_9_N (Bank 35, J19)	141	X
JX2_LVDS_8_P (Bank 35, M17)	143	X
JX2_LVDS_8_N (Bank 35, M18)	136	X
JX2_LVDS_7_P (Bank 35, M19)	138	X
JX2_LVDS_7_N (Bank 35, M20)	135	X
JX2_LVDS_6_P (Bank 35, L19)	137	X
JX2_LVDS_6_N (Bank 35, L20)	130	X
JX2_LVDS_5_P (Bank 35, F16)	132	X
JX2_LVDS_5_N (Bank 35, F17)	129	X
JX2_LVDS_4_P (Bank 35, E18)	131	X
JX2_LVDS_4_N (Bank 35, E19)	124	X
JX2_LVDS_3_P (Bank 35, D19)	126	X
JX2_LVDS_3_N (Bank 35, D20)	123	X
JX2_LVDS_2_P (Bank 35, E17)	125	X
JX2_LVDS_2_N (Bank 35, D18)	118	X
JX2_LVDS_1_P (Bank 35, B19)	120	X
JX2_LVDS_1_N (Bank 35, A20)	117	X
JX2_LVDS_0_P (Bank 35, C20)	119	X
JX2_LVDS_0_N (Bank 35, B20)		

MicroZed (Z7010)

MicroZed (TM) Bank35

GPIO15..0

GPIO[15..0]



Buffer Common Signals (SCLK, IOUPDATE and IORESET) to drive over the 6 connectors.

DDS MOSI1	DDS CONNECTOR	SDIO
DDS MISO1	SDO	
DDS SCLK1	SCLK	
DDS CS1	CS	
DDS IOUPDATE1	IO_UPDATE	
DDS IORESET1	IO_RESET	
DDS PWR_EN1	PWR_EN	
DDS MOSI2	DDS CONNECTOR	SDIO
DDS MISO2	SDO	
DDS SCLK2	SCLK	
DDS CS2	CS	
DDS IOUPDATE2	IO_UPDATE	
DDS IORESET2	IO_RESET	
DDS PWR_EN2	PWR_EN	
DDS MOSI3	DDS CONNECTOR	SDIO
DDS MISO3	SDO	
DDS SCLK3	SCLK	
DDS CS3	CS	
DDS IOUPDATE3	IO_UPDATE	
DDS IORESET3	IO_RESET	
DDS PWR_EN3	PWR_EN	
DDS MOSI4	DDS CONNECTOR	SDIO
DDS MISO4	SDO	
DDS SCLK4	SCLK	
DDS CS4	CS	
DDS IOUPDATE4	IO_UPDATE	
DDS IORESET4	IO_RESET	
DDS PWR_EN4	PWR_EN	
DDS MOSI5	DDS CONNECTOR	SDIO
DDS MISO5	SDO	
DDS SCLK5	SCLK	
DDS CS5	CS	
DDS IOUPDATE5	IO_UPDATE	
DDS IORESET5	IO_RESET	
DDS PWR_EN5	PWR_EN	
DDS MOSI6	DDS CONNECTOR	SDIO
DDS MISO6	SDO	
DDS SCLK6	SCLK	
DDS CS6	CS	
DDS IOUPDATE6	IO_UPDATE	
DDS IORESET6	IO_RESET	
DDS PWR_EN6	PWR_EN	

Title **dSAU Motherboard - uZed BANK35**

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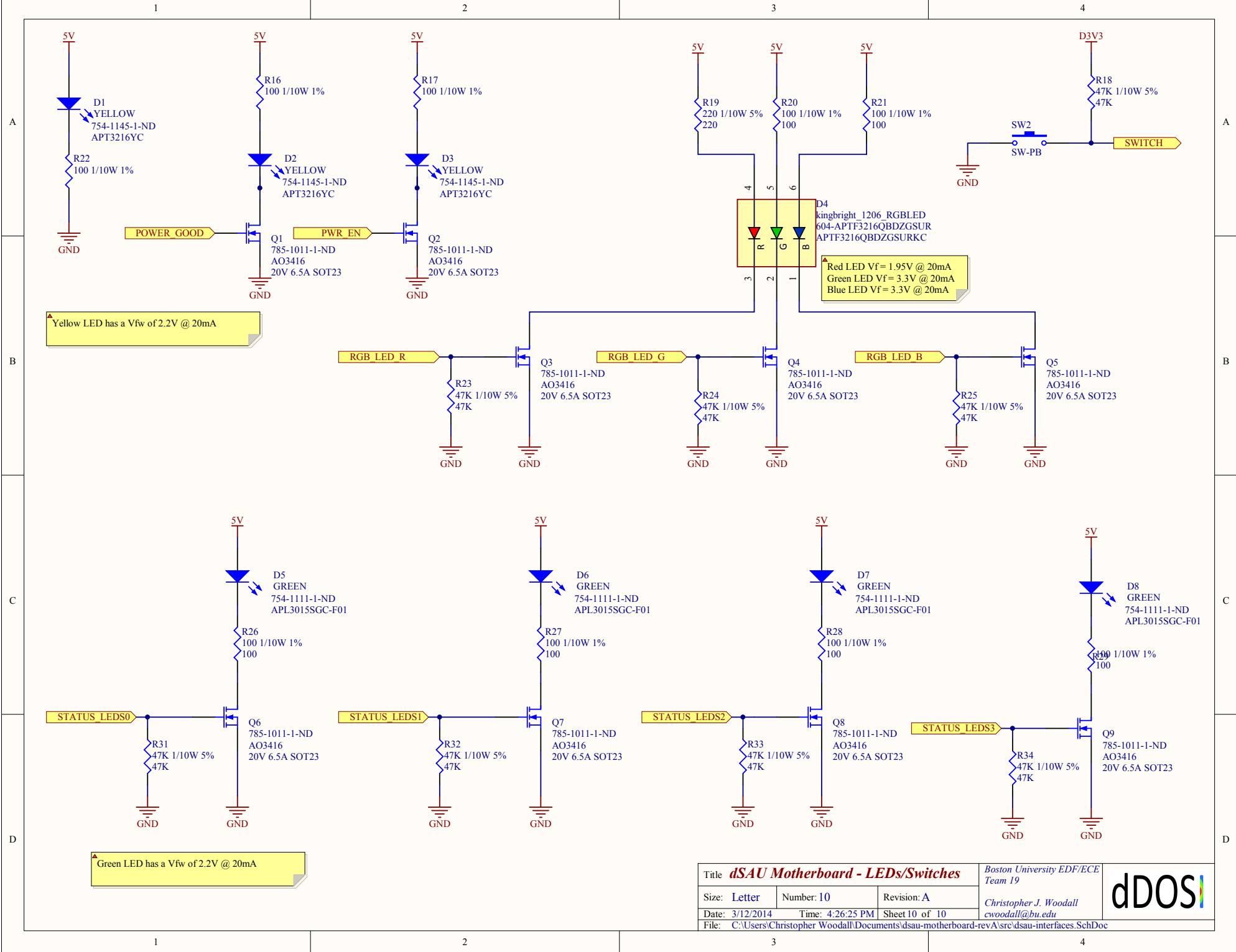
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dDOS



Robyler d00SI Under-sampling [Rev. A]  
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