

▲ This frontend's main responsibility is converting from an unbalanced 50-Ohm input to a balanced 50-Ohm signal for interactions into the ADC.

This particular configuration is taken from the ADS62P49 datasheet and is expected to rely on the ADC's internal filter with a cutoff of 700MHz.

External filters are suggested for best performance.

DDS_CONNECTOR

CONTROL

SDIO

SDO

SCLK

CS

IO_UPDATE

IO_RESET

PWR_EN

EN

5V

POWER_GOOD

Header 10X2

EJH-110-01-F-D-SM-LC


GND

J2

DDS_CLK

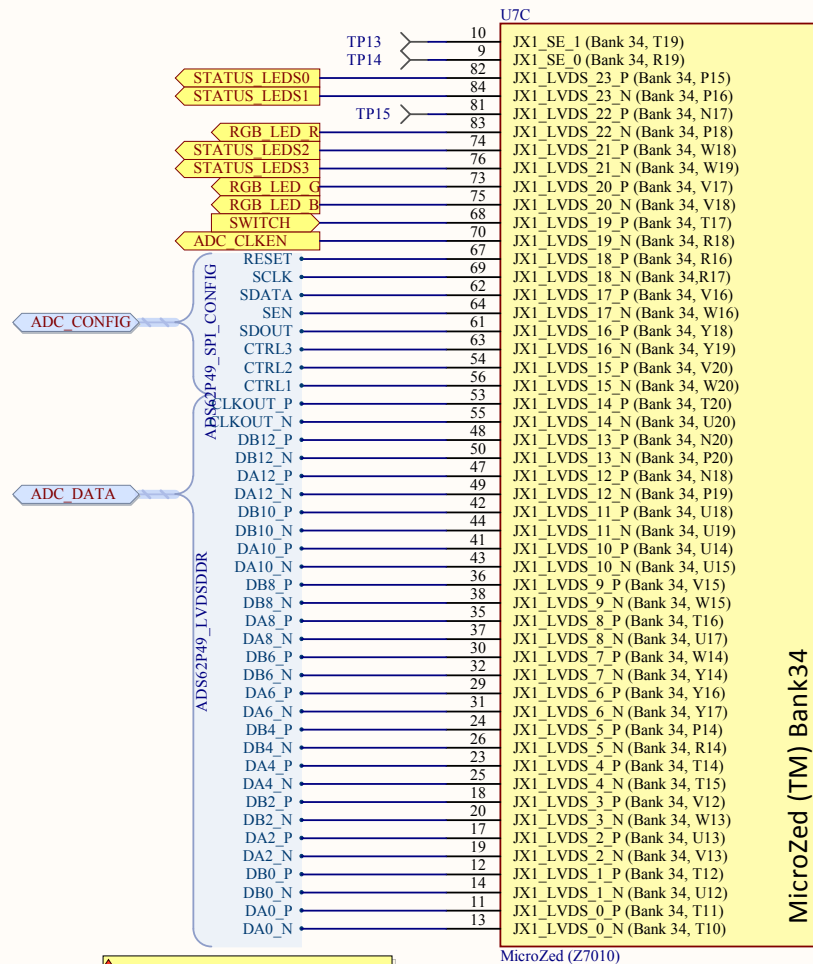
SMB Vertical

GND

Title <i>dSAU Motherboard - DDS Connector</i>			Boston University EDF/ECE Team 19 Christopher J. Woodall cwoodall@bu.edu 
Size: Letter	Number: 5	Revision: A	
Date: 2/12/2014	Time: 8:31:34 AM	Sheet 5 of 10	
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-dds-connector.SchDoc			

BANK34 (1.8V)

▲ BANK34 (1.8V) is used solely for connections to the 1.8V 7bit DDR (time multiplexed) LVDS inputs from the ADS62P49 ADC, and for Control Signals (an SPI port) to and from the ADS62P49.



▲ Routing the LVDS data signals such that Channel A comes to Odd pins and channel B comes to Even pins will make routing easier.

NOTE: Exact pin assignments may change during routing. Stay vigilant

Title **dSAU Motherboard - uZed BANK34**

Boston University EDF/ECE
Team 19

Size: Letter

Number: 7

Revision: A

Date: 2/12/2014

Time: 8:31:34 AM Sheet 7 of 10

Christopher J. Woodall
cwoodall@bu.edu

dDOS

File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed-bank34.SchDoc

Even pins are on the outside, Odd Pins are on the inside

BANK35 (3.3V)

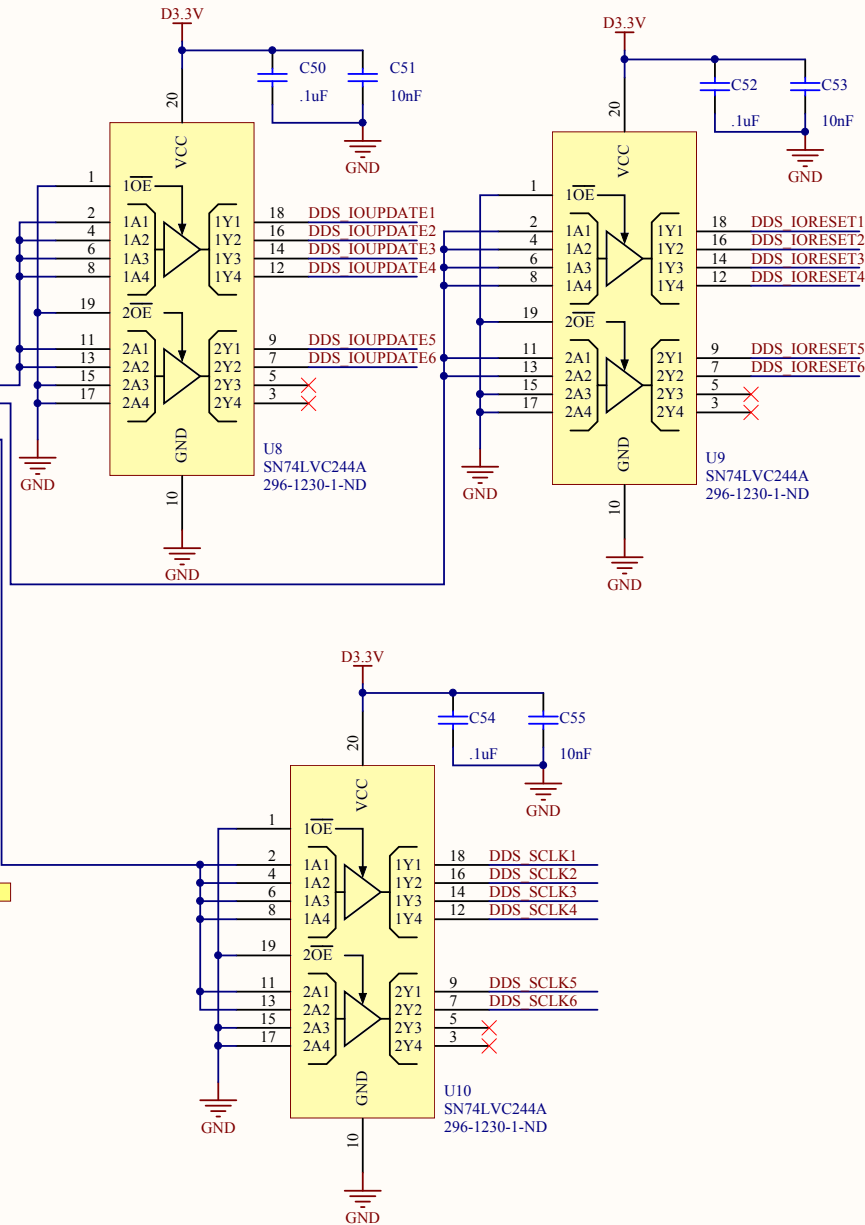
BANK35 (3.3V) is used as the DDS Connector Port to control up to 6 single channel DDS boards, and to control 3.3V interface logics such as the extension port, indicator LEDs and switches.

U7D

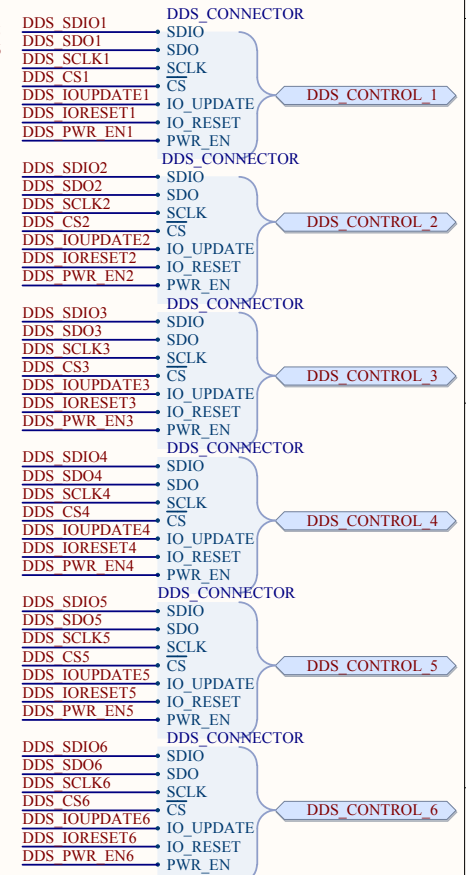
JX2_SE_1 (Bank 35, J15)	114	X
JX2_SE_0 (Bank 35, G14)	113	X
JX2_LVDS_23_P (Bank 35, K16)	188	X
JX2_LVDS_23_N (Bank 35, J16)	190	X
JX2_LVDS_22_P (Bank 35, M14)	187	X
JX2_LVDS_22_N (Bank 35, M15)	189	X
JX2_LVDS_21_P (Bank 35, L14)	182	X
JX2_LVDS_21_N (Bank 35, L15)	184	X
JX2_LVDS_20_P (Bank 35, N15)	181	X
JX2_LVDS_20_N (Bank 35, N16)	183	X
JX2_LVDS_19_P (Bank 35, H15)	174	X
JX2_LVDS_19_N (Bank 35, G15)	176	X
JX2_LVDS_18_P (Bank 35, K14)	173	X
JX2_LVDS_18_N (Bank 35, J14)	175	X
JX2_LVDS_17_P (Bank 35, J20)	168	X
JX2_LVDS_17_N (Bank 35, H20)	170	X
JX2_LVDS_16_P (Bank 35, G19)	167	X
JX2_LVDS_16_N (Bank 35, G20)	169	X
JX2_LVDS_15_P (Bank 35, F19)	162	X
JX2_LVDS_15_N (Bank 35, F20)	164	X
JX2_LVDS_14_P (Bank 35, G17)	161	X
JX2_LVDS_14_N (Bank 35, G18)	163	X
JX2_LVDS_13_P (Bank 35, J18)	154	X
JX2_LVDS_13_N (Bank 35, H18)	156	X
JX2_LVDS_12_P (Bank 35, H16)	153	X
JX2_LVDS_12_N (Bank 35, H17)	155	X
JX2_LVDS_11_P (Bank 35, K17)	148	X
JX2_LVDS_11_N (Bank 35, K18)	150	X
JX2_LVDS_10_P (Bank 35, L16)	147	X
JX2_LVDS_10_N (Bank 35, L17)	149	X
JX2_LVDS_9_P (Bank 35, K19)	142	X
JX2_LVDS_9_N (Bank 35, J19)	144	X
JX2_LVDS_8_P (Bank 35, M17)	141	X
JX2_LVDS_8_N (Bank 35, M18)	143	X
JX2_LVDS_7_P (Bank 35, M19)	136	X
JX2_LVDS_7_N (Bank 35, M20)	138	X
JX2_LVDS_6_P (Bank 35, L19)	135	X
JX2_LVDS_6_N (Bank 35, L20)	137	X
JX2_LVDS_5_P (Bank 35, F16)	130	X
JX2_LVDS_5_N (Bank 35, F17)	132	X
JX2_LVDS_4_P (Bank 35, E18)	129	X
JX2_LVDS_4_N (Bank 35, E19)	131	X
JX2_LVDS_3_P (Bank 35, D19)	124	X
JX2_LVDS_3_N (Bank 35, D20)	126	X
JX2_LVDS_2_P (Bank 35, E17)	123	X
JX2_LVDS_2_N (Bank 35, D18)	125	X
JX2_LVDS_1_P (Bank 35, B19)	118	X
JX2_LVDS_1_N (Bank 35, A20)	120	X
JX2_LVDS_0_P (Bank 35, C20)	117	X
JX2_LVDS_0_N (Bank 35, B20)	119	X

MicroZed (Z7010)

GPIO[15..0]



Buffer Common Signals (SCLK, IOUPDATE and IORESET) to drive over the 6 connectors.



Title **dSAU Motherboard - uZed BANK35**

Boston University EDF/ECE
Team 19

Size: Letter Number: 8 Revision: A

Date: 2/12/2014 Time: 8:31:34 AM Sheet 8 of 10

File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed-bank35.SchDoc

Christopher J. Woodall
cwoodall@bu.edu

dDOS

