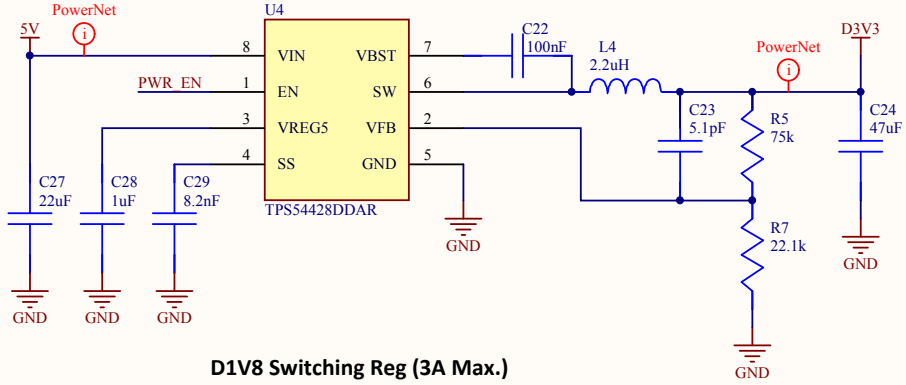
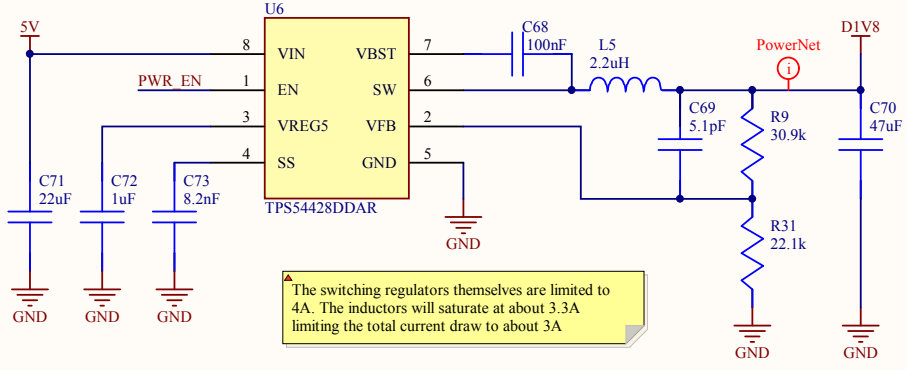
D3V3 Switching Reg (3A Max.)

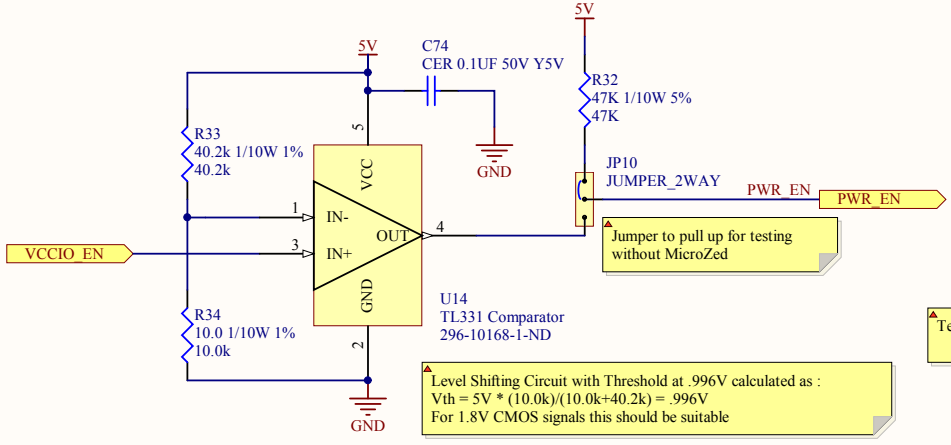


D1V8 Switching Reg (3A Max.)



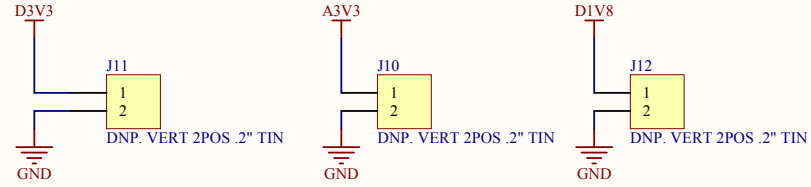
The switching regulators themselves are limited to 4A. The inductors will saturate at about 3.3A limiting the total current draw to about 3A

1.8V to 5V Level Shifter



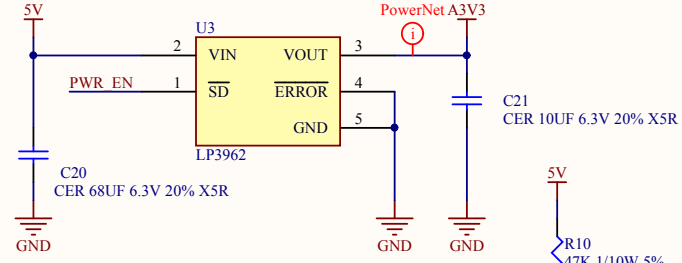
Jumper to pull up for testing without MicroZed

Level Shifting Circuit with Threshold at .996V calculated as :
Vth = 5V * (10.0k)/(10.0k+40.2k) = .996V
For 1.8V CMOS signals this should be suitable

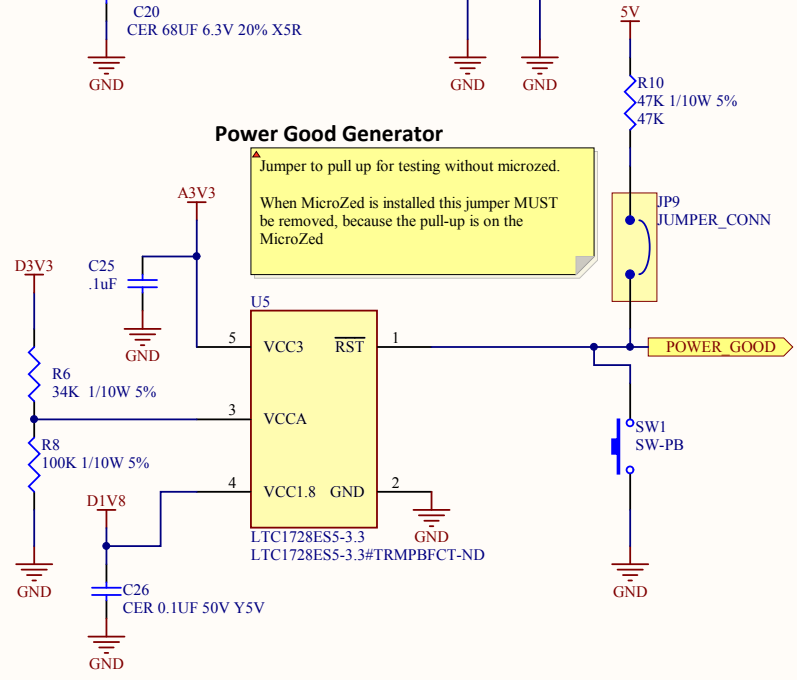


J10, J12, and J11 are fallback methods for bringing in power (DNP).
7A MAX.

A3V3 LDO



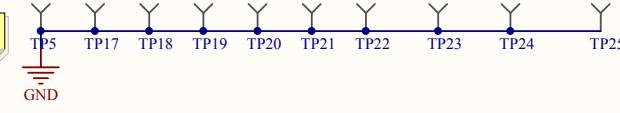
Power Good Generator



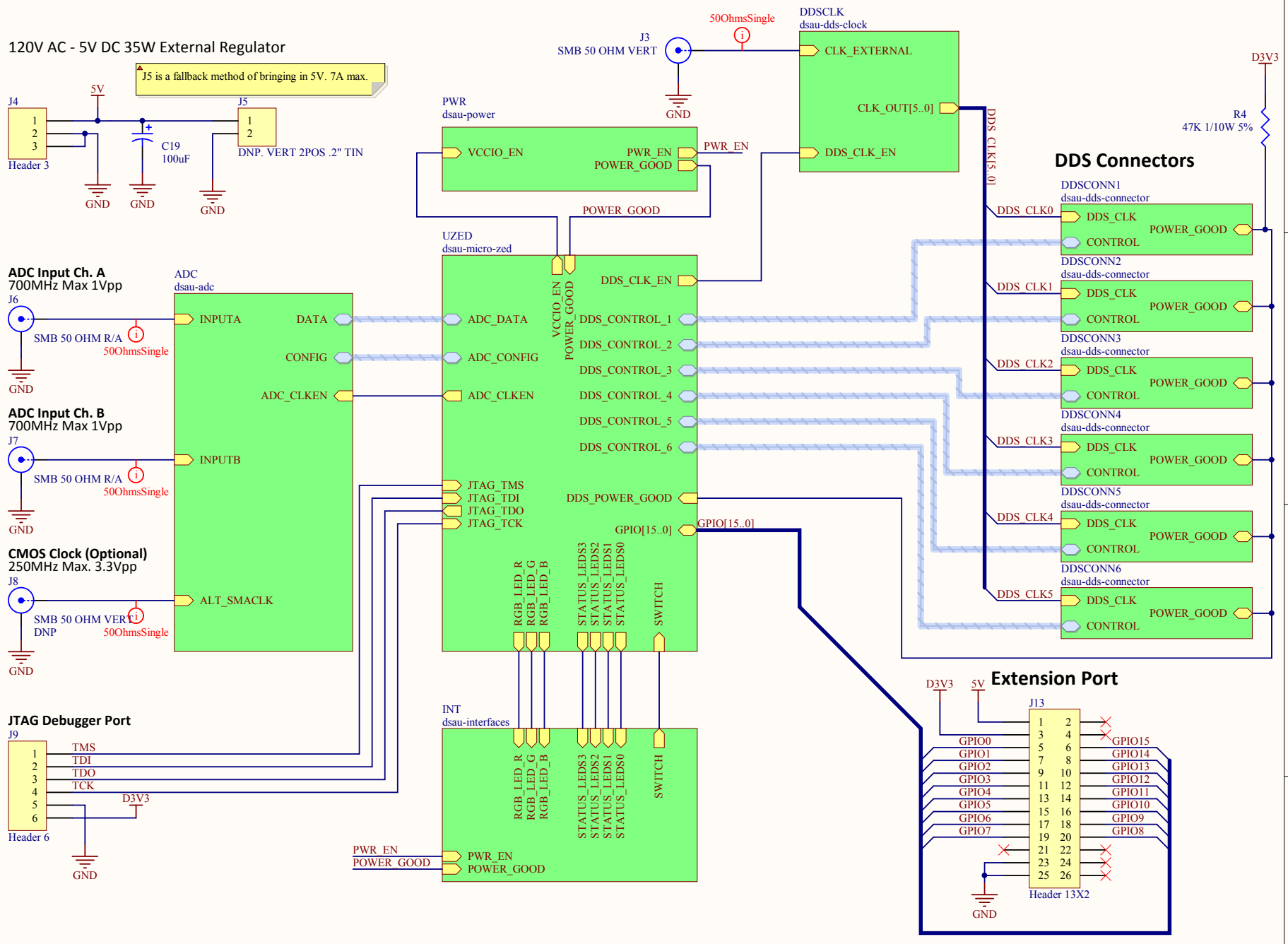
Jumper to pull up for testing without microzed.

When MicroZed is installed this jumper MUST be removed, because the pull-up is on the MicroZed

Testpoint Grounds. Scatter at will.



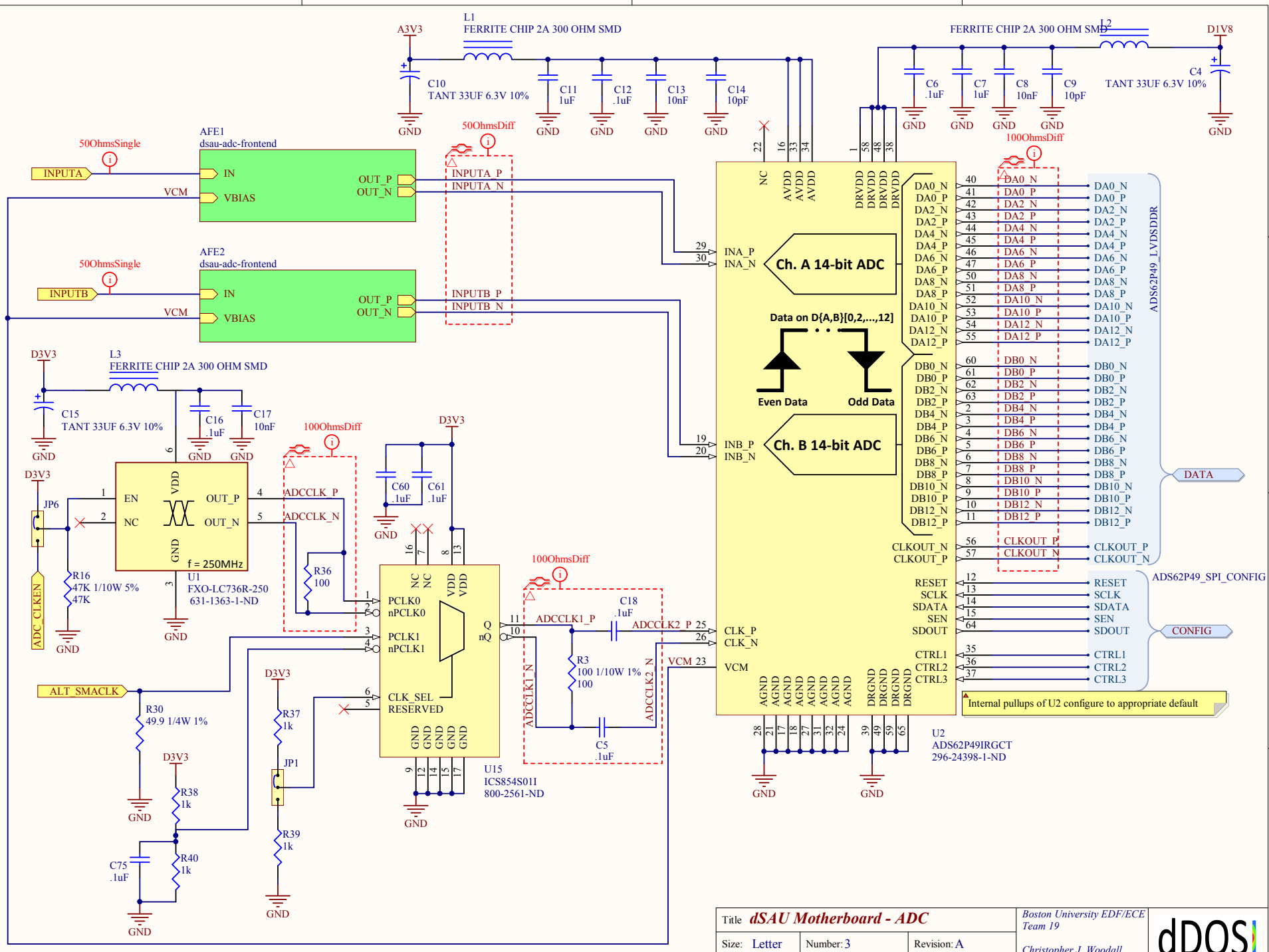
Title: *dSAU Motherboard - Power*			*Boston University EDF/ECE Team 19*
Size: Letter	Number: 1	Revision: A	*Christopher J. Woodall cwoodall@bu.edu*
Date: 2/13/2014	Time: 11:58:25 PM	Sheet 1 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-power.SchDoc			

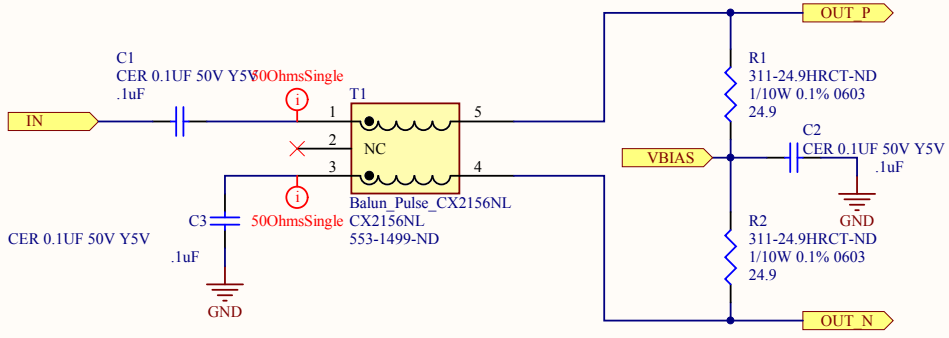


Title	*dSAU Motherboard - Top*	
Size: Letter	Number: 2	Revision: A
Date: 2/13/2014	Time: 11:58:25 PM	Sheet 2 of 10
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-motherboard-top.SchDoc		

Boston University EDF/ECE Team 19
Christopher J. Woodall
cwoodall@bu.edu

dDOS


A3V3
L1
FERRITE CHIP 2A 300 OHM SMD
C10
TANT 33UF 6.3V 10%
C11
1uF
C12
.1uF
C13
10nF
C14
10pF
GND
L2
FERRITE CHIP 2A 300 OHM SMD
D1V8
C6
.1uF
C7
1uF
C8
10nF
C9
10pF
C4
TANT 33UF 6.3V 10%
50OhmsSingle
AFE1
dsau-adc-frontend
INPUTA
VCM
IN
VBIAS
OUT_P
OUT_N
50OhmsDiff
INPUTA_P
INPUTA_N
AFE2
dsau-adc-frontend
INPUTB
INPUTB_P
INPUTB_N
100OhmsDiff
NC
AVDD
DRVDD
INA_P
INA_N
Ch. A 14-bit ADC
Data on D{A,B}[0,2,...,12]
Even Data
Odd Data
INB_P
INB_N
Ch. B 14-bit ADC
DA0_N
DA0_P
DA2_N
DA2_P
DA4_N
DA4_P
DA6_N
DA6_P
DA8_N
DA8_P
DA10_N
DA10_P
DA12_N
DA12_P
DB0_N
DB0_P
DB2_N
DB2_P
DB4_N
DB4_P
DB6_N
DB6_P
DB8_N
DB8_P
DB10_N
DB10_P
DB12_N
DB12_P
CLKOUT_N
CLKOUT_P
ADS62P49_LVDSDDR
DATA
D3V3
L3
FERRITE CHIP 2A 300 OHM SMD
C15
TANT 33UF 6.3V 10%
C16
.1uF
C17
10nF
JP6
ADC_CLKEN
EN
NC
VDD
OUT_P
OUT_N
GND
f = 250MHz
U1
FXO-LC736R-250
631-1363-1-ND
R16
47K 1/10W 5%
47K
R36
100
ADCCLK_P
ADCCLK_N
C60
.1uF
C61
.1uF
PCLK0
nPCLK0
PCLK1
nPCLK1
CLK_SEL
RESERVED
Q
nQ
U15
ICS854S01I
800-2561-ND
ADCCLK1_P
ADCCLK1_N
ADCCLK2_P
ADCCLK2_N
C18
.1uF
C5
.1uF
R3
100 1/10W 1%
100
CLK_P
CLK_N
VCM
ALT_SMACLK
R30
49.9 1/4W 1%
R37
1k
JP1
R38
1k
R39
1k
R40
1k
C75
.1uF
RESET
SCLK
SDATA
SEN
SDOUT
CTRL1
CTRL2
CTRL3
ADS62P49_SPI_CONFIG
CONFIG
Internal pullups of U2 configure to appropriate default
U2
ADS62P49IRGCT
296-24398-1-ND
Title dSAU Motherboard - ADC
Size: Letter
Number: 3
Revision: A
Date: 2/13/2014
Time: 11:58:25 PM
Sheet 3 of 10
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-adc.SchDoc
Boston University EDF/ECE
Team 19
Christopher J. Woodall
cwoodall@bu.edu
dDOS



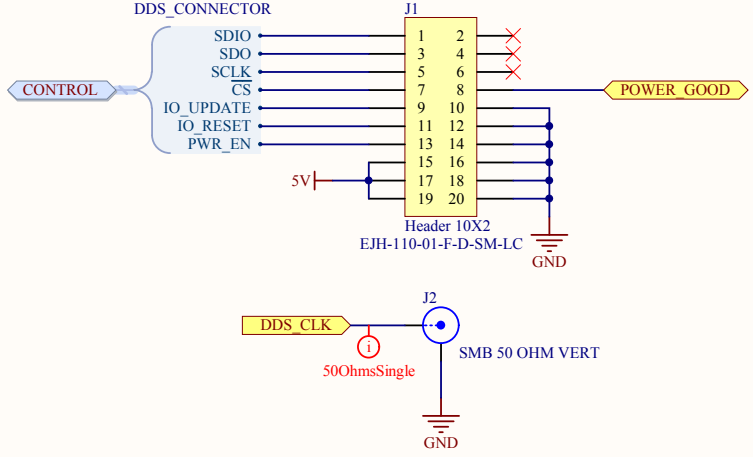
This frontend's main responsibility is converting from an unbalanced 50-Ohm input to a balanced 50-Ohm signal for interactions into the ADC.

This particular configuration is taken from the ADS62P49 datasheet and is expected to rely on the ADCs internal filter with a cutoff of 700MHz.

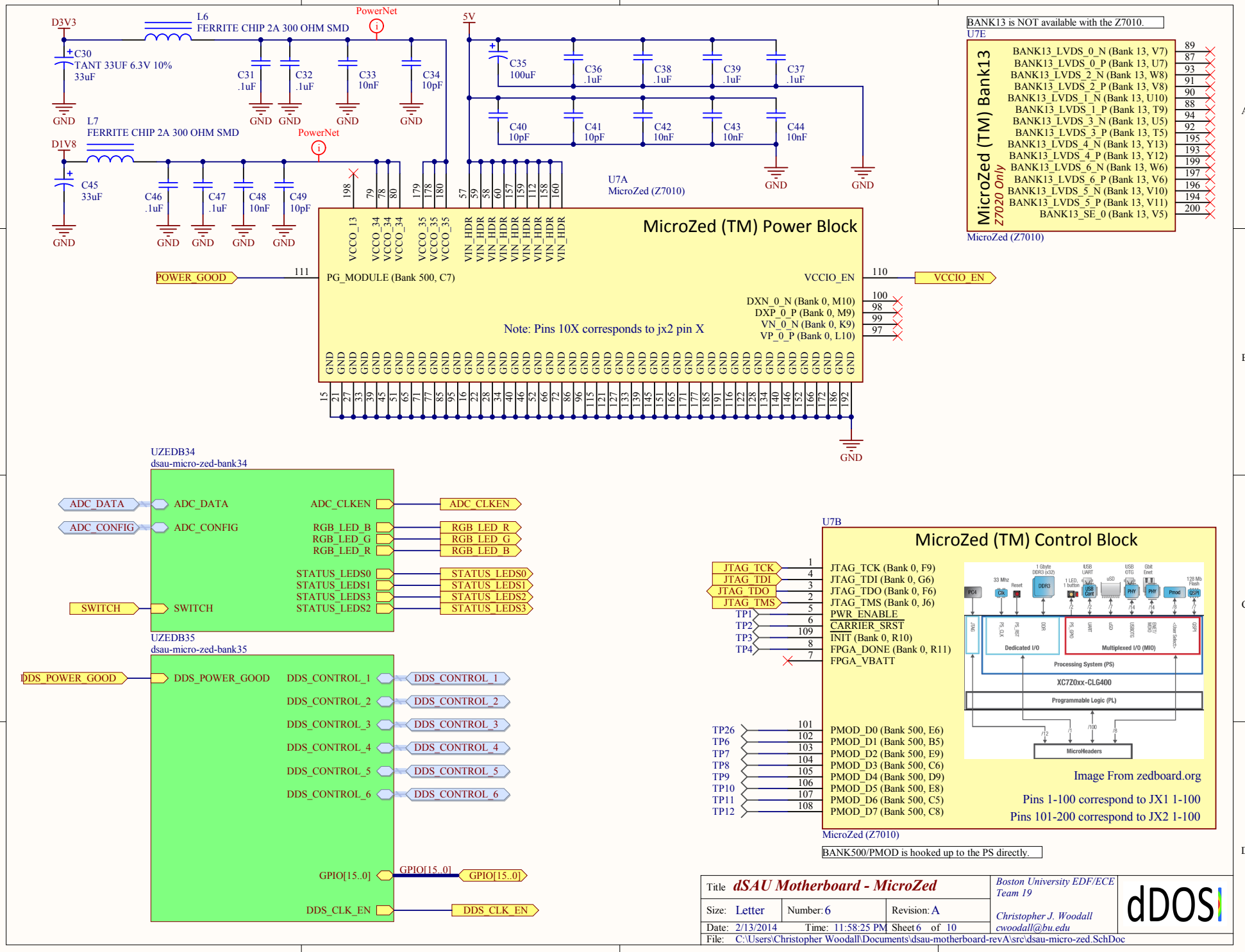
External filters are suggested for best performance.

Title	***dSAU Motherboard - ADC Frontend***		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 4	Revision: A	*Christopher J. Woodall* *cwoodall@bu.edu*
Date: 2/13/2014	Time: 11:58:25 PM	Sheet 4 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-adc-frontend.SchDoc			

Standard Connector to Single Channel DDS Board.

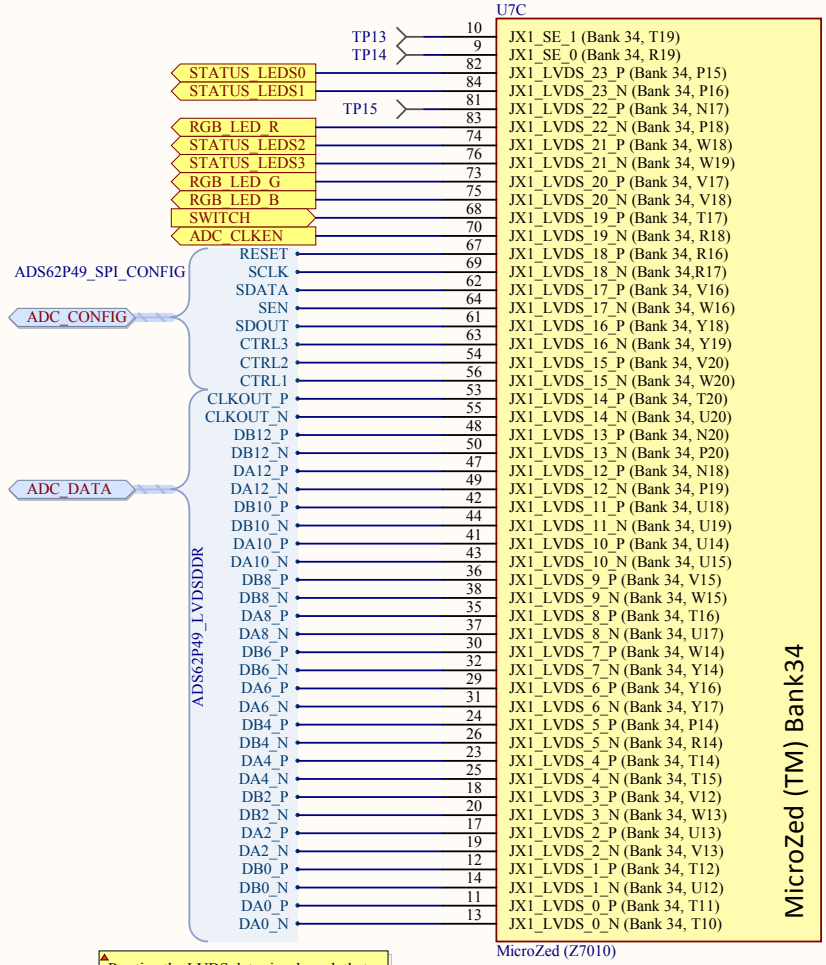


Title	***dSAU Motherboard - DDS Connector***		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 5	Revision: A	*Christopher J. Woodall cwoodall@bu.edu*
Date: 2/13/2014	Time: 11:58:25 PM	Sheet 5 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-dds-connector.SchDoc			


D3V3
L6
FERRITE CHIP 2A 300 OHM SMD
PowerNet
5V
C30
TANT 33UF 6.3V 10%
33uF
C31 .1uF
C32 .1uF
C33 10nF
C34 10pF
C35 100uF
C36 .1uF
C38 .1uF
C39 .1uF
C37 .1uF
C40 10pF
C41 10pF
C42 10nF
C43 10nF
C44 10nF
GND
L7
FERRITE CHIP 2A 300 OHM SMD
PowerNet
D1V8
C45 33uF
C46 .1uF
C47 .1uF
C48 10nF
C49 10pF
U7A
MicroZed (Z7010)
MicroZed (TM) Power Block
VCCO_13
VCCO_34
VCCO_34
VCCO_34
VCCO_35
VCCO_35
VCCO_35
VIN_HDR
POWER_GOOD
111
PG_MODULE (Bank 500, C7)
VCCIO_EN
110
VCCIO_EN
DXN_0_N (Bank 0, M10)
DXP_0_P (Bank 0, M9)
VN_0_N (Bank 0, K9)
VP_0_P (Bank 0, L10)
Note: Pins 10X corresponds to jx2 pin X
BANK13 is NOT available with the Z7010.
U7E
MicroZed (TM) Bank13
Z7020 Only
BANK13_LVDS_0_N (Bank 13, V7)
BANK13_LVDS_0_P (Bank 13, U7)
BANK13_LVDS_2_N (Bank 13, W8)
BANK13_LVDS_2_P (Bank 13, V8)
BANK13_LVDS_1_N (Bank 13, U10)
BANK13_LVDS_1_P (Bank 13, T9)
BANK13_LVDS_3_N (Bank 13, U5)
BANK13_LVDS_3_P (Bank 13, T5)
BANK13_LVDS_4_N (Bank 13, Y13)
BANK13_LVDS_4_P (Bank 13, Y12)
BANK13_LVDS_6_N (Bank 13, W6)
BANK13_LVDS_6_P (Bank 13, V6)
BANK13_LVDS_5_N (Bank 13, V10)
BANK13_LVDS_5_P (Bank 13, V11)
BANK13_SE_0 (Bank 13, V5)
MicroZed (Z7010)
UZEDB34
dsau-micro-zed-bank34
ADC_DATA
ADC_CONFIG
SWITCH
ADC_CLKEN
RGB_LED_B
RGB_LED_G
RGB_LED_R
STATUS_LEDS0
STATUS_LEDS1
STATUS_LEDS3
STATUS_LEDS2
UZEDB35
dsau-micro-zed-bank35
DDS_POWER_GOOD
DDS_CONTROL_1
DDS_CONTROL_2
DDS_CONTROL_3
DDS_CONTROL_4
DDS_CONTROL_5
DDS_CONTROL_6
GPIO[15..0]
DDS_CLK_EN
U7B
MicroZed (TM) Control Block
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
TP1
TP2
TP3
TP4
PWR_ENABLE
CARRIER_SRST
INIT (Bank 0, R10)
FPGA_DONE (Bank 0, R11)
FPGA_VBATT
TP26
TP6
TP7
TP8
TP9
TP10
TP11
TP12
PMOD_D0 (Bank 500, E6)
PMOD_D1 (Bank 500, B5)
PMOD_D2 (Bank 500, E9)
PMOD_D3 (Bank 500, C6)
PMOD_D4 (Bank 500, D9)
PMOD_D5 (Bank 500, E8)
PMOD_D6 (Bank 500, C5)
PMOD_D7 (Bank 500, C8)
Dedicated I/O
Multiplexed I/O (MIO)
Processing System (PS)
XC7Z0xx-CLG400
Programmable Logic (PL)
MicroHeaders
Image From zedboard.org
Pins 1-100 correspond to JX1 1-100
Pins 101-200 correspond to JX2 1-100
MicroZed (Z7010)
BANK500/PMOD is hooked up to the PS directly.
Title dSAU Motherboard - MicroZed
Size: Letter
Number: 6
Revision: A
Date: 2/13/2014
Time: 11:58:25 PM
Sheet 6 of 10
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed.SchDoc
Boston University EDF/ECE Team 19
Christopher J. Woodall
cwoodall@bu.edu
dDOS

BANK34 (1.8V)

BANK34 (1.8V) is used soley for connections to the 1.8V 7bit DDR (time multiplexed) LVDS inputs from the ADS62P49 ADC, and for Control Signals (an SPI port) to and from the ADS62P49.



Routing the LVDS data signals such that Channel A comes to Odd pins and channel B comes to Even pins will make routing easier.

NOTE: Exact pin assignments may change during routing. Stay vigilant

Title	***dSAU Motherboard - uZed BANK34***		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 7	Revision: A	*Christopher J. Woodall cwoodall@bu.edu*
Date: 2/13/2014	Time: 11:58:25 PM	Sheet 7 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed-bank34.SchDoc			

Even pins are on the outside, Odd Pins are on the inside

BANK35 (3.3V)

BANK35 (3.3V) is used as the DDS Connector Port to control up to 6 single channel DDS boards, and to control 3.3V interface logics such as the extension port, indicator LEDs and switches.

U7D

MicroZed (TM) Bank35

JX2_SE_1 (Bank 35, J15)	114	
JX2_SE_0 (Bank 35, G14)	113	
JX2_LVDS_23_P (Bank 35, K16)	188	DDS_IOUPDATE
JX2_LVDS_23_N (Bank 35, J16)	190	DDS_IORESET
JX2_LVDS_22_P (Bank 35, M14)	187	
JX2_LVDS_22_N (Bank 35, M15)	189	DDS_SCLK
JX2_LVDS_21_P (Bank 35,L14)	182	DDS_MOSI1
JX2_LVDS_21_N (Bank 35,L15)	184	DDS_MISO1
JX2_LVDS_20_P (Bank 35, N15)	181	DDS_MOSI4
JX2_LVDS_20_N (Bank 35, N16)	183	DDS_MISO4
JX2_LVDS_19_P (Bank 35, H15)	174	DDS_CS1
JX2_LVDS_19_N (Bank 35, G15)	176	DDS_PWR_EN1
JX2_LVDS_18_P (Bank 35, K14)	173	DDS_CS4
JX2_LVDS_18_N (Bank 35, J14)	175	DDS_PWR_EN4
JX2_LVDS_17_P (Bank 35, J20)	168	DDS_MOSI2
JX2_LVDS_17_N (Bank 35, H20)	170	DDS_MISO2
JX2_LVDS_16_P (Bank 35, G19)	167	DDS_MOSI5
JX2_LVDS_16_N (Bank 35, G20)	169	DDS_MISO5
JX2_LVDS_15_P (Bank 35, F19)	162	DDS_CS2
JX2_LVDS_15_N (Bank 35, F20)	164	DDS_PWR_EN2
JX2_LVDS_14_P (Bank 35, G17)	161	DDS_CS5
JX2_LVDS_14_N (Bank 35, G18)	163	DDS_PWR_EN5
JX2_LVDS_13_P (Bank 35, J18)	154	DDS_MOSI3
JX2_LVDS_13_N (Bank 35, H18)	156	DDS_MISO3
JX2_LVDS_12_P (Bank 35, H16)	153	DDS_MOSI6
JX2_LVDS_12_N (Bank 35, H17)	155	DDS_MISO6
JX2_LVDS_11_P (Bank 35, K17)	148	DDS_CS3
JX2_LVDS_11_N (Bank 35, K18)	150	DDS_PWR_EN3
JX2_LVDS_10_P (Bank 35, L16)	147	DDS_CS6
JX2_LVDS_10_N (Bank 35, L17)	149	DDS_PWR_EN6
JX2_LVDS_9_P (Bank 35, K19)	142	
JX2_LVDS_9_N (Bank 35, J19)	144	DDS_POWER_GOOD
JX2_LVDS_8_P (Bank 35, M17)	141	DDS_CLK_EN
JX2_LVDS_8_N (Bank 35, M18)	143	
JX2_LVDS_7_P (Bank 35, M19)	136	GPIO7
JX2_LVDS_7_N (Bank 35, M20)	138	GPIO6
JX2_LVDS_6_P (Bank 35, L19)	135	GPIO15
JX2_LVDS_6_N (Bank 35, L20)	137	GPIO14
JX2_LVDS_5_P (Bank 35, F16)	130	GPIO5
JX2_LVDS_5_N (Bank 35, F17)	132	GPIO4
JX2_LVDS_4_P (Bank 35, E18)	129	GPIO13
JX2_LVDS_4_N (Bank 35, E19)	131	GPIO12
JX2_LVDS_3_P (Bank 35, D19)	124	GPIO3
JX2_LVDS_3_N (Bank 35, D20)	126	GPIO2
JX2_LVDS_2_P (Bank 35, E17)	123	GPIO11
JX2_LVDS_2_N (Bank 35, D18)	125	GPIO10
JX2_LVDS_1_P (Bank 35, B19)	118	GPIO1
JX2_LVDS_1_N (Bank 35, A20)	120	GPIO0
JX2_LVDS_0_P (Bank 35, C20)	117	GPIO9
JX2_LVDS_0_N (Bank 35, B20)	119	GPIO8

GPIO[15..0]

MicroZed (Z7010)

U8 SN74LVC244A 296-1230-1-ND

U9 SN74LVC244A 296-1230-1-ND

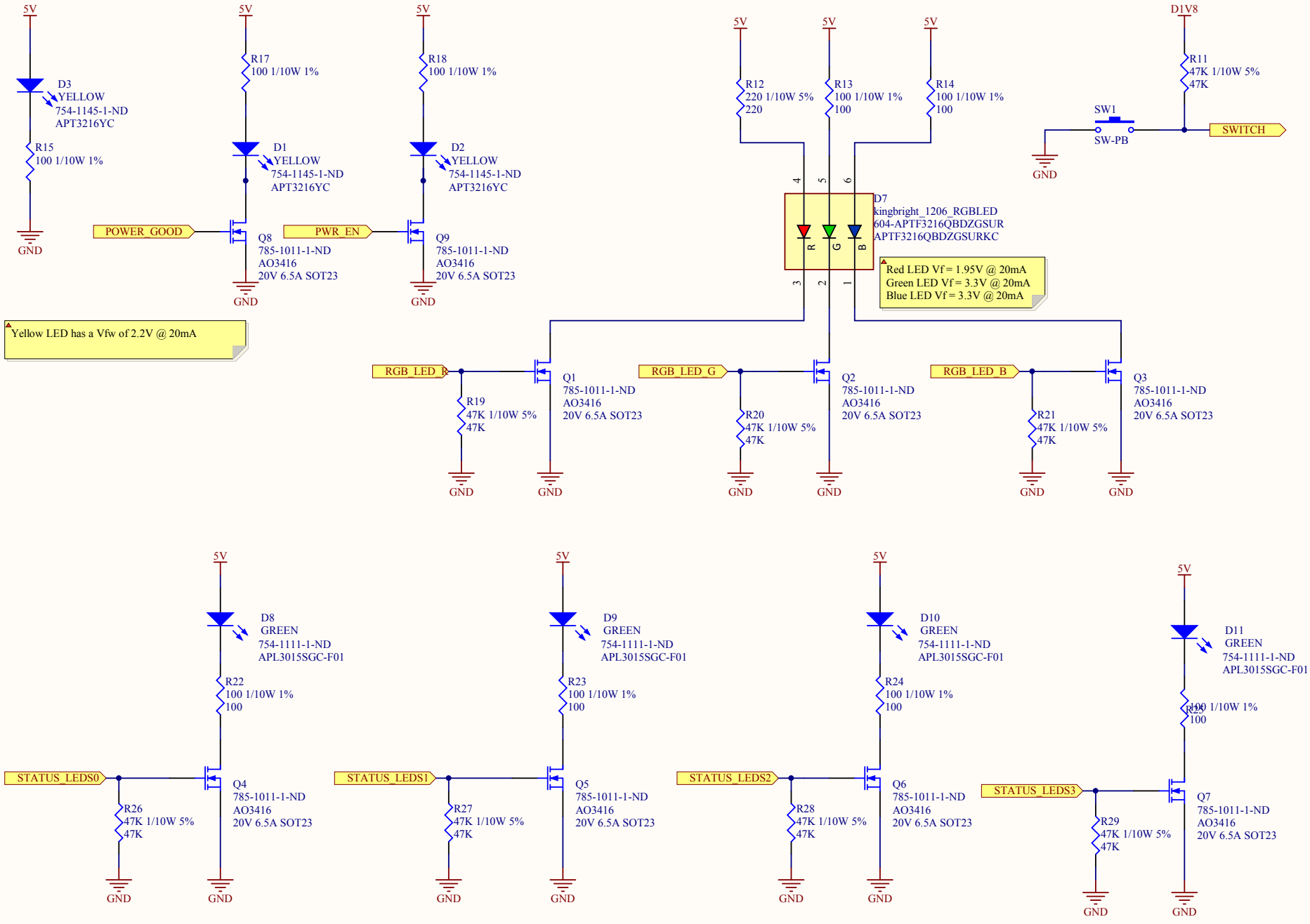
U10 SN74LVC244A 296-1230-1-ND

Buffer Common Signals (SCLK, IOUPDATE and IORESET) to drive over the 6 connectors.

DDS_CONNECTOR

DDS_SDIO1	SDIO	DDS_CONTROL_1
DDS_SDO1	SDO	
DDS_SCLK1	SCLK	
DDS_CS1	CS	
DDS_IOUPDATE1	IO_UPDATE	
DDS_IORESET1	IO_RESET	
DDS_PWR_EN1	PWR_EN	
DDS_SDIO2	SDIO	DDS_CONTROL_2
DDS_SDO2	SDO	
DDS_SCLK2	SCLK	
DDS_CS2	CS	
DDS_IOUPDATE2	IO_UPDATE	
DDS_IORESET2	IO_RESET	
DDS_PWR_EN2	PWR_EN	
DDS_SDIO3	SDIO	DDS_CONTROL_3
DDS_SDO3	SDO	
DDS_SCLK3	SCLK	
DDS_CS3	CS	
DDS_IOUPDATE3	IO_UPDATE	
DDS_IORESET3	IO_RESET	
DDS_PWR_EN3	PWR_EN	
DDS_SDIO4	SDIO	DDS_CONTROL_4
DDS_SDO4	SDO	
DDS_SCLK4	SCLK	
DDS_CS4	CS	
DDS_IOUPDATE4	IO_UPDATE	
DDS_IORESET4	IO_RESET	
DDS_PWR_EN4	PWR_EN	
DDS_SDIO5	SDIO	DDS_CONTROL_5
DDS_SDO5	SDO	
DDS_SCLK5	SCLK	
DDS_CS5	CS	
DDS_IOUPDATE5	IO_UPDATE	
DDS_IORESET5	IO_RESET	
DDS_PWR_EN5	PWR_EN	
DDS_SDIO6	SDIO	DDS_CONTROL_6
DDS_SDO6	SDO	
DDS_SCLK6	SCLK	
DDS_CS6	CS	
DDS_IOUPDATE6	IO_UPDATE	
DDS_IORESET6	IO_RESET	
DDS_PWR_EN6	PWR_EN	

Title	dSAU Motherboard - uZed BANK35		Boston University EDF/ECE Team 19
Size: Letter	Number: 8	Revision: A	Christopher J. Woodall cwoodall@bu.edu
Date: 2/13/2014	Time: 11:58:26 PM	Sheet 8 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-micro-zed-bank35.SchDoc			


5V
D3
YELLOW
754-1145-1-ND
APT3216YC
R15
100 1/10W 1%
GND
R17
100 1/10W 1%
D1
YELLOW
754-1145-1-ND
APT3216YC
POWER_GOOD
Q8
785-1011-1-ND
AO3416
20V 6.5A SOT23
R18
100 1/10W 1%
D2
YELLOW
754-1145-1-ND
APT3216YC
PWR_EN
Q9
785-1011-1-ND
AO3416
20V 6.5A SOT23
Yellow LED has a Vfw of 2.2V @ 20mA
R12
220 1/10W 5%
220
R13
100 1/10W 1%
100
R14
100 1/10W 1%
100
D7
kingbright_1206_RGBLED
604-APTF3216QBDZGSUR
APTF3216QBDZGSURKC
R
G
B
Red LED Vf = 1.95V @ 20mA
Green LED Vf = 3.3V @ 20mA
Blue LED Vf = 3.3V @ 20mA
D1V8
R11
47K 1/10W 5%
47K
SW1
SW-PB
SWITCH
RGB_LED_R
Q1
785-1011-1-ND
AO3416
20V 6.5A SOT23
R19
47K 1/10W 5%
47K
RGB_LED_G
Q2
785-1011-1-ND
AO3416
20V 6.5A SOT23
R20
47K 1/10W 5%
47K
RGB_LED_B
Q3
785-1011-1-ND
AO3416
20V 6.5A SOT23
R21
47K 1/10W 5%
47K
D8
GREEN
754-1111-1-ND
APL3015SGC-F01
R22
100 1/10W 1%
100
STATUS_LEDS0
Q4
785-1011-1-ND
AO3416
20V 6.5A SOT23
R26
47K 1/10W 5%
47K
D9
GREEN
754-1111-1-ND
APL3015SGC-F01
R23
100 1/10W 1%
100
STATUS_LEDS1
Q5
785-1011-1-ND
AO3416
20V 6.5A SOT23
R27
47K 1/10W 5%
47K
D10
GREEN
754-1111-1-ND
APL3015SGC-F01
R24
100 1/10W 1%
100
STATUS_LEDS2
Q6
785-1011-1-ND
AO3416
20V 6.5A SOT23
R28
47K 1/10W 5%
47K
D11
GREEN
754-1111-1-ND
APL3015SGC-F01
R25
100 1/10W 1%
100
STATUS_LEDS3
Q7
785-1011-1-ND
AO3416
20V 6.5A SOT23
R29
47K 1/10W 5%
47K
Green LED has a Vfw of 2.2V @ 20mA
Title dSAU Motherboard - LEDs/Switches
Size: Letter
Number: 9
Revision: A
Date: 2/13/2014
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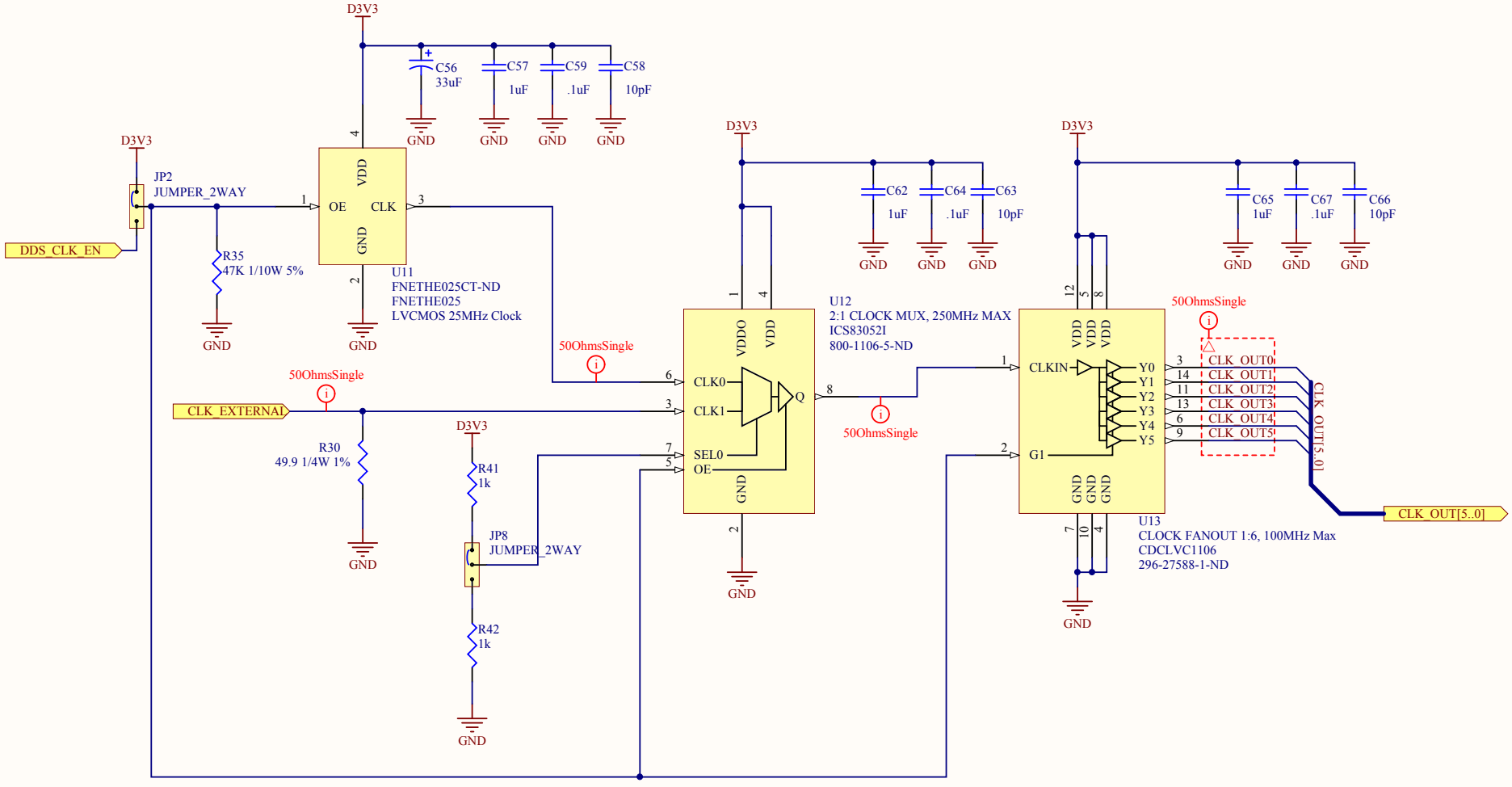
Sheet 9 of 10
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-interfaces.SchDoc
Boston University EDF/ECE Team 19
Christopher J. Woodall
cwoodall@bu.edu
dDOS



Title	***dSAU Motherboard - DDS Clock Gen.***		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 10	Revision: A	*Christopher J. Woodall cwoodall@bu.edu*
Date: 2/13/2014	Time: 11:58:26 PM	Sheet 10 of 10	dDOS
File: C:\Users\Christopher Woodall\Documents\dsau-motherboard-revA\src\dsau-dds-clock.SchDoc			