Back to project **URL** https://opencores.org/ocsvn/can/can/trunk

can Go

Subversion Repositories can

[/] - Rev 161

Rev 161 Go

Go to most recent revision

Filtering Options

From rev	To rev	Max revs
161	1	200

Search for

Go Clear current filter

Rev	Log message	Author	Age	Path
161	New directory structure.	root	5938d 19h	/
160	New tests for testing the bus-off.	igorm	6988d 02h	/
159	*** empty log message ***	igorm	7276d 02h	/
158	Fixing overrun problems.	igorm	7276d 04h	/
157	In "Extended mode" when dual filter was used and standard frame received, upper nibble of the data was not filtered ok.	igorm	7370d 02h	/
156	Wake-up interrupt was generated in some cases.	igorm	7391d 00h	/
155	rd_info_pointer fixed (fifo_empty was used instead of info_empty).	igorm	7399d 06h	/

Rev	Log message	Author	Age	Path
154	irq is cleared after the release_buffer command. This bug was entered with changes for the edge triggered interrupts.	igorm	7499d 00h	/
153	Arbitration capture register changed. SW reset (setting the reset_mode bit) doesn't work as HW reset.	igorm	7506d 20h	/
152	Fixes for compatibility after the SW reset.	igorm	7511d 02h	/
151	When CAN was reset by setting the reset_mode signal in mode register, it was possible that CAN was blocked for a short period of time. Problem occured very rarly.	igorm	7513d 20h	/
150	This commit was manufactured by cvs2svn to create tag 'rel_24'.		7532d 20h	/
149	Fixed synchronization problem in real hardware when 0xf is used for TSEG1.	igorm	7532d 20h	/
148	This commit was manufactured by cvs2svn to create tag 'rel_23'.		7535d 03h	/
147	Interrupt is always cleared for one clock after the irq register is read. This fixes problems when CPU is using IRQs that are edge triggered.	igorm	7535d 03h	/
146	This commit was manufactured by cvs2svn to create tag 'rel_22'.		7535d 08h	/
145	Arbitration bug fixed.	igorm	7535d 08h	/
144	This commit was manufactured by cvs2svn to create tag 'rel_21'.		7682d 00h	/
143	Bit acceptance_filter_mode was inverted.	igorm	7682d 00h	/
142	This commit was manufactured by cvs2svn to create tag 'rel_20'.		7700d 23h	/
141	Core improved to pass all tests with the Bosch VHDL Reference system.	igorm	7700d 23h	/
140	I forgot to thange one signal name.	igorm	7755d 21h	/
139	Signal bus_off_on added.	igorm	7755d 22h	/
138	Header changed. Address latched to posedge. bus_off_on signal added.	mohor	7795d 00h	/
137	Header changed.	mohor	7795d 00h	/
136	Error counters changed.	mohor	7795d 00h	/
135	Header changed.	mohor	7795d 01h	/
134	Active high/low problem when Altera devices are used. Bug fixed by Rojhalat Ibrahim.	mohor	7902d 22h	/

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133	This commit was manufactured by cvs2svn to create tag 'rel_19'.		7909d 09h	/
132	This commit was manufactured by cvs2svn to create tag 'asyst_3'.		7909d 09h	/
131	This commit was manufactured by cvs2svn to create tag 'asyst_2'.		7909d 09h	/
130	mbist signals updated according to newest convention	markom	7909d 09h	/
129	Error counters changed.	mohor	7925d 18h	/
128	This commit was manufactured by cvs2svn to create tag 'rel_18'.		7925d 18h	/
127	Fixing the core to be Bosch VHDL Reference compatible.	mohor	7925d 18h	/
126	Error counters fixed to be compatible with Bosch VHDL reference model. Small synchronization changes.	mohor	7926d 14h	/
125	Synchronization changed, error counters fixed.	mohor	7930d 20h	/
124	ALTERA_RAM supported.	mohor	7951d 02h	/
123	This commit was manufactured by cvs2svn to create tag 'rel_17'.		7958d 08h	/
122	This commit was manufactured by cvs2svn to create tag 'rel_16'.		7958d 08h	/
121	When detecting bus-free, signal bus_free_cnt_en was cleared to zero although the last sampled bit was zero instead of one.	mohor	7958d 08h	/
120	This commit was manufactured by cvs2svn to create tag 'rel_15'.		7967d 05h	/
119	Artisan RAMs added.	mohor	7967d 05h	/
118	Artisan RAM fixed (when not using BIST).	mohor	7967d 05h	/
117	Tristate signal tx_o is separated to tx_o and tx_oen_o. Both signals need to be joined together on higher level.	mohor	7967d 05h	/
116	This commit was manufactured by cvs2svn to create tag 'rel_14'.		7972d 23h	/
115	Artisan ram instances added.	simons	7972d 23h	/
114	This commit was manufactured by cvs2svn to create tag 'rel_13'.		7999d 23h	/
113	This commit was manufactured by cvs2svn to create tag 'rel_12'.		7999d 23h	/

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112	Tx and rx length are limited to 8 bytes regardless to the DLC value.	tadejm	7999d 23h	/
111	Fixed according to the linter. Case statement for data_out joined.	mohor	8001d 23h	/
110	Fixed according to the linter.	mohor	8002d 00h	/
109	Fixed according to the linter.	mohor	8002d 01h	/
108	Fixed according to the linter.	mohor	8002d 01h	/
107	Fixed according to the linter.	mohor	8002d 02h	/
106	Unused signal removed.	mohor	8007d 23h	/
105	This commit was manufactured by cvs2svn to create tag 'rel_11'.		8008d 13h	/
104	Synchronization fixed. In some strange cases it didn't work according to the VHDL reference model.	tadejm	8008d 13h	/
103	This commit was manufactured by cvs2svn to create tag 'complete_1'.		8011d 03h	/
102	Little fixes (to fix warnings).	mohor	8011d 03h	/
101	This commit was manufactured by cvs2svn to create tag 'rel_10'.		8015d 05h	/
100	Synchronization changed.	mohor	8015d 05h	/
99	PCI_BIST replaced with CAN_BIST.	mohor	8015d 05h	/
98	This commit was manufactured by cvs2svn to create tag 'rel_9'.		8020d 17h	/
97	Overrun fifo implemented with FFs, because it is not possible to create such a memory.	simons	8020d 17h	/
96	This commit was manufactured by cvs2svn to create tag 'rel_8'.		8020d 18h	/
95	Virtual silicon ram instances added.	simons	8020d 18h	/
94	This commit was manufactured by cvs2svn to create tag 'rel_7'.		8026d 05h	/
93	synthesis full_case parallel_case fixed.	mohor	8026d 05h	/
92	clkout is clk/2 after the reset.	mohor	8026d 13h	/

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91	This commit was manufactured by cvs2svn to create tag 'rel_6'.		8027d 03h	/
90	paralel_case and full_case compiler directives added to case statements.	mohor	8027d 03h	/
89	This commit was manufactured by cvs2svn to create tag 'rel_5'.		8028d 00h	/
88	Previous change removed. When resynchronization occurs we go to seg1 stage. sync stage does not cause another start of seg1 stage.	mohor	8028d 00h	/
87	When hard_sync or resync occure we need to go to seg1 segment. Going to sync segment is in that case blocked.	mohor	8028d 00h	/
86	This commit was manufactured by cvs2svn to create tag 'rel_4'.		8029d 16h	/
85	Typo fixed.	mohor	8029d 16h	/
84	clk_cnt reduced from [8:0] to [6:0].	mohor	8030d 23h	/
83	cs_can_i is used only when WISHBONE interface is not used.	mohor	8031d 00h	/
82	Removed few signals.	mohor	8031d 00h	/
81	"chip select" signal cs_can_i is used only when not using WISHBONE interface.	mohor	8031d 00h	/
80	Form error was detected when stuff bit occured at the end of crc.	mohor	8031d 00h	/
79	Bit stuffing corrected when stuffing comes at the end of the crc.	tadejm	8032d 00h	/
78	tx_point generated one clk earlier. rx_i registered. Data corrected when using extended mode.	mohor	8032d 01h	/
77	Synchronization is also needed when transmitting a message.	mohor	8035d 00h	/
76	Counters width changed.	mohor	8035d 00h	/
75	When switching to tx, sync stage is overjumped.	mohor	8037d 00h	/
74	This commit was manufactured by cvs2svn to create tag 'rel_3'.		8037d 05h	/
73	overrun and length_info fifos are initialized at the end of reset.	mohor	8037d 05h	/
72	This commit was manufactured by cvs2svn to create tag 'rel_2'.		8039d 03h	/
71	Ports added for the CAN_BIST.	mohor	8039d 03h	/

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70	data_out is already registered in the can_top.v file.	mohor	8039d 03h	/
69	Some features are supported in extended mode only (listen_only_mode...).	mohor	8093d 23h	/
68	CAN inturrupt is active low.	mohor	8114d 03h	/
67	CAN interrupt is active low.	mohor	8114d 03h	/
66	unix.	mohor	8119d 22h	/
65	unix.	mohor	8119d 22h	/
64	*** empty log message ***	mohor	8119d 22h	/
63	ALE changes on negedge of clk.	mohor	8125d 19h	/
62	can_cs signal used for generation of the cs.	mohor	8125d 19h	/
61	Bidirectional port_0_i changed to port_0_io. input cs_can changed to cs_can_i.	mohor	8128d 09h	/
60	rd_i and wr_i are active high signals. If 8051 is connected, these two signals need to be negated one level higher.	mohor	8128d 10h	/
59	8051 interface added (besides WISHBONE interface). Selection is made in can_defines.v file.	mohor	8128d 10h	/
58	timescale.v is used for simulation only.	mohor	8128d 22h	/
57	Mux used for clkout to avoid "gated clocks warning".	mohor	8128d 22h	/
56	Doubled declarations removed.	mohor	8129d 21h	/
55	wire declaration added.	mohor	8129d 21h	/
54	This commit was manufactured by cvs2svn to create tag 'branch-release-1-0'.		8134d 23h	/
53	CAN pins located.	mohor	8134d 23h	/
52	tx_o is now tristated signal. tx_oen and tx_o combined together.	mohor	8134d 23h	/
51	Xilinx RAM added.	mohor	8135d 00h	/
50	Top level signal names changed.	mohor	8135d 00h	/

Rev	Log message	Author	Age	Path
49	Actel APA ram changed. Now synchronous read is used.	mohor	8138d 15h	/
48	Actel APA ram supported.	mohor	8138d 16h	/
47	Data is latched on read.	mohor	8138d 16h	/
46	This commit was manufactured by cvs2svn to create tag 'rel_1'.		8148d 14h	/
45	When a dominant bit was detected at the third bit of the intermission and node had a message to transmit, bit_stuff error could occur. Fixed.	mohor	8148d 14h	/
44	When bit error occured while active error flag was transmitted, counter was not incremented.	mohor	8148d 15h	/
43	Directory keeper.	mohor	8148d 22h	/
42	Initial version of the project.	mohor	8148d 22h	/
41	Incomplete sensitivity list fixed.	mohor	8149d 00h	/
40	Typo fixed.	mohor	8149d 00h	/
39	CAN core finished. Host interface added. Registers finished. Synchronization to the wishbone finished.	mohor	8149d 00h	/
38	Temporary backup version (still fully operable).	mohor	8150d 14h	/
37	Define CAN_CLOCK_DIVIDER_MODE not used any more. Deleted.	mohor	8150d 15h	/
36	Most of the registers added. Registers "arbitration lost capture", "error code capture" + few more still need to be added.	mohor	8150d 15h	/
35	Several registers added. Not finished, yet.	mohor	8153d 19h	/
34	Errors monitoring improved. arbitration_lost improved.	mohor	8156d 00h	/
33	abort_tx added.	mohor	8156d 00h	/
32	abort_tx added. Bit destuff fixed.	mohor	8156d 00h	/
31	Wishbone interface added.	mohor	8157d 14h	/
30	CAN is working according to the specification. WB interface and more registers (status, IRQ, ...) needs to be added.	mohor	8157d 23h	/
29	Overload fixed. Hard synchronization also enabled at the last bit of interframe.	mohor	8158d 20h	/

Rev	Log message	Author	Age	Path
28	Bosch license warning added. Error counters finished. Overload frames still need to be fixed.	mohor	8159d 12h	/
27	This file is not used.	mohor	8163d 21h	/
26	Backup.	mohor	8163d 21h	/
25	*** empty log message ***	mohor	8164d 00h	/
24	backup.	mohor	8168d 14h	/
23	Fifo corrected to be synthesizable.	mohor	8181d 21h	/
22	Form error supported. When receiving messages, last bit of the end-of-frame does not generate form error. Receiver goes to the idle mode one bit sooner. (CAN specification ver 2.0, part B, page 57).	mohor	8183d 01h	/
21	Data is stored to fifo at the end of ack stage.	mohor	8183d 17h	/
20	CRC checking fixed (when bitstuff occurs at the end of a CRC sequence).	mohor	8183d 18h	/
19	RX state machine fixed to receive "remote request" frames correctly. No data bytes are written to fifo when such frames are received.	mohor	8184d 00h	/
18	When a frame with "remote request" is received, no data is stored to fifo, just the frame information (identifier, ...). Data length that is stored is the received data length and not the actual data length that is stored to fifo.	mohor	8184d 02h	/
17	Addresses corrected to decimal values (previously hex).	mohor	8184d 21h	/
16	rx_fifo is now working.	mohor	8185d 02h	/
15	Temporary version (backup).	mohor	8188d 21h	/
14	rx fifo added. Not 100 % verified, yet.	mohor	8189d 17h	/
13	Temporary files (backup).	mohor	8190d 00h	/
12	Temp version.	mohor	8191d 01h	/
11	Acceptance filter added.	mohor	8191d 13h	/
10	Backup version.	mohor	8202d 11h	/
9	Header changed, testbench improved to send a frame (crc still missing).	mohor	8203d 15h	/
8	Testbench define file added. Clock divider register added.	mohor	8203d 23h	/
7	Tripple sampling supported.	mohor	8204d 13h	/

Rev	Log message	Author	Age	Path
6	Commented lines removed.	mohor	8204d 15h	/
5	Synchronization working.	mohor	8205d 01h	/
4	Dir keeper.	mohor	8209d 22h	/
3	This commit was manufactured by cvs2svn to create tag 'initial'.		8209d 22h	/
2	Initial	mohor	8209d 22h	/
1	Standard project directories initialized by cvs2svn.		8209d 22h	/

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