Cyclone V FPGA Resources

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Cyclone V FPGA Architecture

Cyclone V FPGA architecture consists of:

- Adaptive Logic Modules (ALM) and Logic Array Blocks (LAB)
  - The logic array block (LAB) consists of 10 ALMs and a LAB-wide control block.
  - ALMs are the basic building blocks similar to logic elements (LE).
- Digital Signal Processing (DSP) Blocks
  - Cyclone V devices support DSP blocks for multiplication operations.
  - DSP blocks contain multipliers, adders, and internal coefficients.
  - Each block supports 9-bit, 18-bit, or 27-bit word length.
  - Multipliers can be inferred directly from the VHDL or Verilog source code or by instantiating the megafunctions.
- Memory Blocks
- Clock Networks and PLLs

Cyclone V Memory Blocks

- The Cyclone V device family has embedded memory structures to address the on-chip memory needs.
- The embedded memory structure consists of M10K memory blocks columns that can be configured as RAM, first-in first-out (FIFO) buffers, or ROM.
- M10K memory blocks provide ten kbits of on-chip memory capable of operating at up to 315 MHz for Cyclone V devices.
  - 8,192 memory bits per block (10,240 bits per block including parity)
  - The parity bit is the fifth bit associated with each 4 data bits in data widths of 5, 10, 20, and 40
- M10K blocks support variable port configurations

Memory Features in Cyclone V Devices

Feature	M10K
Maximum operating frequency	315 MHz
Total RAM bits (including parity bits)	10,240
Configuration (depth × width)	256 x 32, 256 x 40, 512 x 16, 512 x 20, 1K x 8, 1K x 10, 2K x 4, 2K x 5, 4K x 2, and 8K x 1

Cyclone V Memory Blocks

- The *rden* and *wren* control signals control the read and write operations for each port of M10K memory blocks.
- The clock-enable control signal controls the clock entering the input and output registers and the entire M10K memory block.
- M10K blocks feature byte enable control signals for data input masking during writes.
- M10K memory blocks support a parity bit for each 4 bits. This bit can be used as either a parity bit or as an additional data bit.

Cyclone V Memory Blocks

- Byte enables are active high signals. The LSB of the *byteena* signal corresponds to the least significant byte of the data bus.

byteena Controls in x20 Data Width

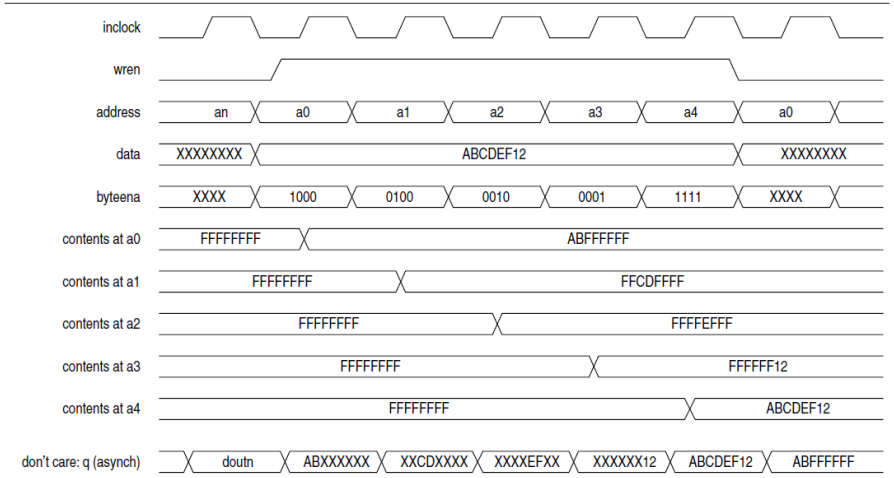
byteena[1:0]	Data Bits Written	
11 (default)	[19:10]	[9:0]
10	[19:10]	—
01	—	[9:0]

byteena Controls in x40 Data Width

byteena[3:0]	Data Bits Written			
1111 (default)	[39:30]	[29:20]	[19:10]	[9:0]
1000	[39:30]	—	—	—
0100	—	[29:20]	—	—
0010	—	—	[19:10]	—
0001	—	—	—	[9:0]

Cyclone V Memory Blocks

Byte Enable Functional Waveform

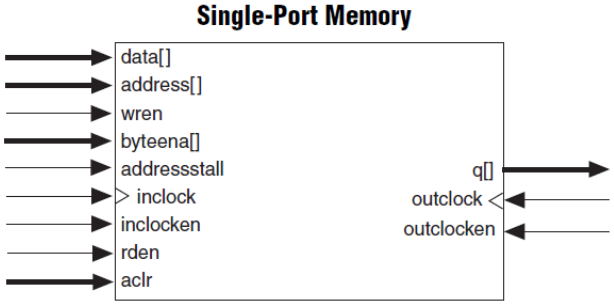


Cyclone V Memory Blocks

- Memory Modes
  - Single-port
  - Simple dual-port
  - True dual-port
  - Shift-register
  - ROM
  - FIFO

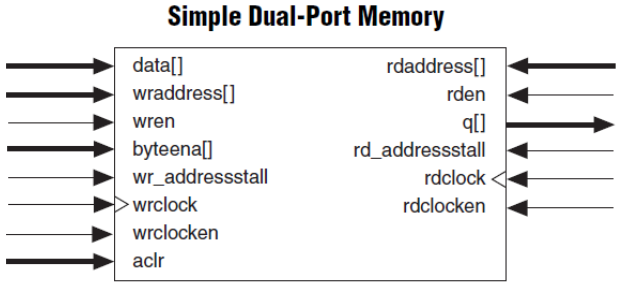
Cyclone V Memory Blocks - Single-Port Mode

- Single-port mode supports non-simultaneous read and write operations from a single address.



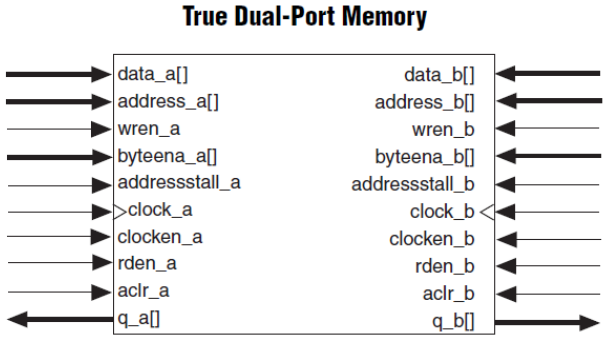
Cyclone V Memory Blocks - Simple Dual-Port Mode

- Simple dual-port mode supports simultaneous read and write operations to different locations.
- Mixed-width configurations, allowing different read and write port widths are supported.



Cyclone V Memory Blocks - True Dual-port Mode

- True dual-port mode supports any combination of two-port operations at two different clock frequencies:
  - two reads,
  - two writes,
  - or one read and one write
- The widest bit configuration of the M10K blocks in true dual-port mode is 512 x 16-bit (20-bit with parity).



Cyclone V Memory Blocks - Shift Register Mode

- DSP applications require shift registers for local data storage.
  - Using standard flip flops quickly exhaust many logic cells for large shift registers.
  - A more efficient alternative is using embedded memory as a shift register block.
- This is useful in DSP applications that require local data storage such as:
  - Finite impulse response (FIR) filters
  - Pseudo-random number generators
  - Multi-channel filtering
  - Auto-correlation and cross-correlation functions

Cyclone V Memory Blocks - ROM Mode

- Cyclone V device family M10K memory blocks support ROM mode.
- A .mif initializes the ROM contents of these blocks.
- The ROM read operation is identical to the read operation in the single-port RAM configuration.
  - The address lines of the ROM are registered.
  - The outputs can be registered or unregistered.

Cyclone V Memory Blocks - FIFO Mode

- Cyclone V device family M10K memory blocks support single-clock or dual-clock FIFO buffers.
  - Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain.
- Cyclone V device family M10K memory blocks do not support simultaneous read and write from an empty FIFO buffer.

Cyclone V Memory Blocks - Clocking Modes

Cyclone V device family M10K memory blocks support the following clocking modes:

- **Single-clock**
- **Read or write**
- **Input or output**
- **Independent**

Memory Blocks Clocking Modes for Each Memory Mode

Clocking Mode	Memory Mode				
	Single-Port	Simple Dual-Port	True Dual-Port	ROM	FIFO
Single clock mode	Yes	Yes	Yes	Yes	Yes
Read/write clock mode	—	Yes	—	—	Yes
Input/output clock mode	Yes	Yes	Yes	Yes	—
Independent clock mode	—	—	Yes	Yes	—

Cyclone V Memory Blocks - Clocking Modes

- Single-clock Mode
  - All registers of the M10K memory block can be controlled with a single clock together with clock enable.
  - Single-clock mode can be implemented for FIFO, ROM, true dual-port, simple dual-port, and single-port memories.

Cyclone V Memory Blocks - Clocking Modes

- Read/Write Clock Mode
  - This mode is used for FIFO and simple dual-port memories.
  - A write clock controls the data inputs, write address, and wren registers.
  - read clock controls the data outputs, read address, and rden registers.
  - Independent clock enables for both the read and write clocks are supported.

When using read or write mode, if you perform a simultaneous read or write to the same address location, the output read data is **unknown**.

Cyclone V Memory Blocks - Clocking Modes

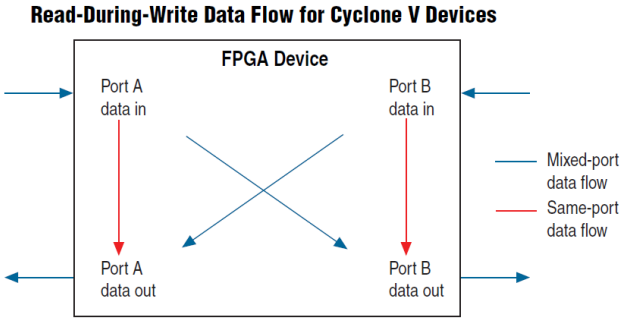
- Input/Output Clock Mode
  - An input clock controls all input registers to the memory block, including data, address, byteena, wren, and rden registers.
  - An output clock controls the data-output registers.
  - Each port supports independent clock enables for input and output registers.

Cyclone V Memory Blocks - Clocking Modes

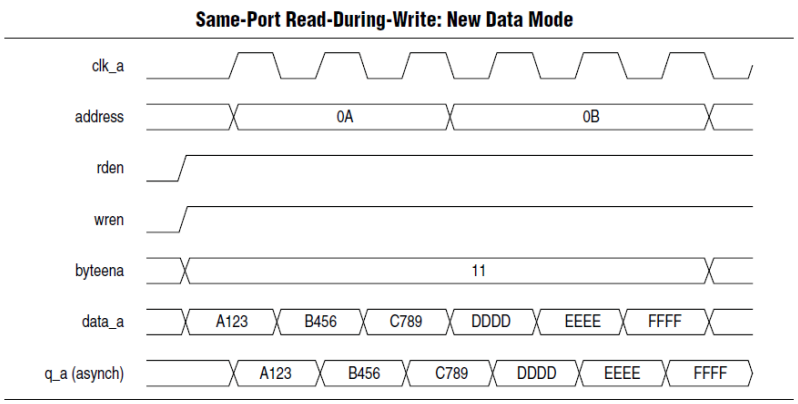
- Independent Clock Mode
  - A separate clock is available for each port (port A and port B).
  - clock A controls all registers on port A side, clock B controls all registers on port B side.
  - Each port supports independent clock enables for port A and B registers.

Cyclone V Memory Blocks - Design Considerations

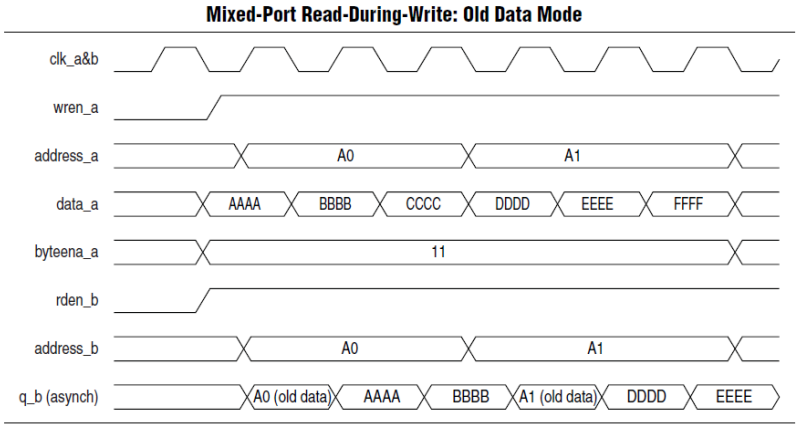
- There are two read-during-write data flows:
  - **Same-port**
    - ★ New Data Mode (Flow-through)
    - ★ Don't Care (Unknown)
  - **Mixed-port**
    - ★ Old Data Mode
    - ★ Don't Care (Unknown)



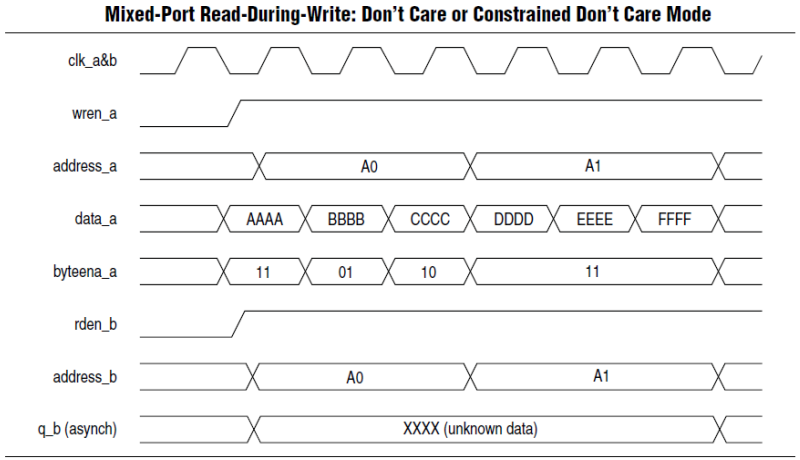
Cyclone V Memory Blocks - Design Considerations



Cyclone V Memory Blocks - Design Considerations



Cyclone V Memory Blocks - Design Considerations



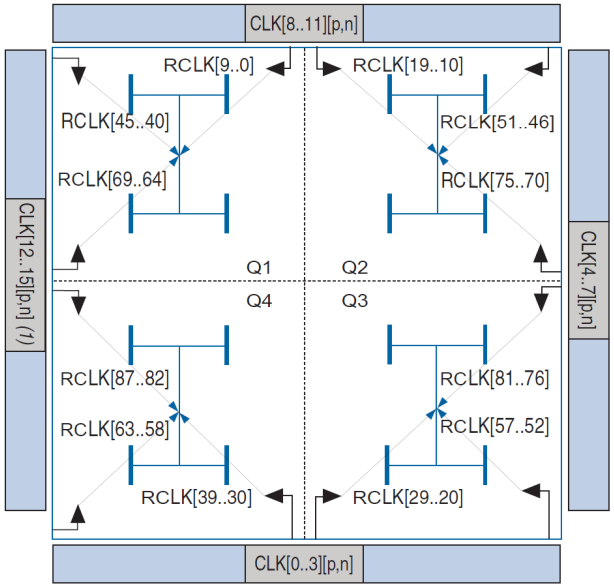
Cyclone V Clock Network

- Cyclone V device family includes:
  - 16 global clock networks (GCLK)
  - 88 regional clock networks (RCLK).
- All types of resources in the device can use GCLKs and RCLKs as clock sources.
  - I/O elements
  - Logic array blocks (LABs)
  - DSP blocks
  - M10K memory blocks
- The Cyclone V device family provides up to 32 single-ended or 16 differential clock input pins (CLK[15..0]p and CLK[15..0]n):
  - Four dedicated clock pins on each side of the device.
  - They can drive global clocks (GCLKs) and regional clocks (RCLKs).

Cyclone V Global and Regional Clock Networks

- Global clock signals
  - GCLK networks can drive throughout the device.
  - The GCLKs serve as low-skew clock sources for functional blocks.
- Regional clock signals
  - RCLK networks are only applicable to the quadrant they drive into.
  - The RCLKs provide the lowest clock delay and skew for logic contained in a single device quadrant.

Cyclone V Global and Regional Clock Networks



Cyclone V Clock Network

Global clock signals and regional clock signals can be driven from

- Dedicated clock inputs
- High-speed serial interface outputs
- PLL outputs
- Internal logic

Cyclone V Clock Network

- PLLs provide robust clock management and synthesis using $M/(N*\text{post-scale counter})$ scaling factors.
  - The input clock is divided by a pre-scale factor, N, and is then multiplied by the M feedback factor.
  - There is one pre-scale counter, N, and one multiply counter, M, per PLL, with a range of 1 to 512 for both M and N.
- There are four PLLs and each PLL generates two clock outputs.
- There are nine generic post-scale counters per PLL that can feed GCLKs or external clock outputs.
  - Post-scale counters range from 1 to 512 with a 50% duty cycle setting.
  - Post-scale counters range from 1 to 256 with any non-50% duty cycle setting.

Summary

- We discussed the Cyclone V FPGA family architecture.
- We looked at embedded memory blocks on Cyclone V FPGA.
- We discussed Cyclone V clock network and PLLs.

Acknowledgment

- Some figures/notes are taken from or inspired by the
  - Cyclone V Device Handbook, Volume 1, 2012