

ZHOU, QI

+44 07710 799432 ◊ +86 185 5254 1785

zhouqi008012@gmail.com ◊ Q.Zhou-24@sms.ed.ac.uk

EDUCATION

University of Edinburgh, Computer Science (BSc Hons)

2019 - 2023

WORK EXPERIENCE

Asteria

Sept 2020 - Feb 2021

<https://www.asteria-space.com/>

- Came up with possible solution for attaching a camera on a single-board computer which will be launched into space.

Codeplay

June 2022 - Sept 2022

<https://www.codeplay.com/>

- Worked on **ComputeArota (CA)**, a toolkit implementing heterogeneous cross-platform computing.
- Added **RV32** and **Zfh** extension (half float) support to the simulator in **CA**, such that **RV32** or **Float16** instructions can be generated by **CA** and simulated using **SPIKE**.
- Learnt about **Sollya's fpminimax** function that computes a polynomial approximation for float point operations, then investigated some test failures caused by float point precision issues.
- Implemented a faster and more intuitive replacement of **SPIKE** for **CA** using **RISCV-64 QEMU** with a Linux operating system, where the host (client) communicates with simulator (server) using sockets.

Teaching assistant

Sept 2022 - May 2023

Demonstrator in workshops and labs for these courses:

- Computer Architecture and Design (INFR10076),
- Compiling Techniques (INFR10065).

PROJECTS

SIMD Support for LLVM MLIR Presburger library - In progress

[llvm/llvm-project/blob/main/mlir/lib/Analysis/Presburger/Simplex.cpp](https://llvm.org/projects/llvm-project/blob/main/mlir/lib/Analysis/Presburger/Simplex.cpp)

- This library performs overflow-checked multiplication and addition on small and sparse matrix.
- Compute 52 bit integer using FPU could be fast, because:
 - Fraction part of double precision float point number is exactly 52 bits,
 - Exploits fused-multiply-add,
 - Sufficient for small data, not likely to trigger overflow exception and redirect to slow **BigInt** algorithms,
 - Float point overflow and imprecision checking is convenient.
- Discovered bugs in **llvm-mca** when it analysis **FMA** throughput on **zen3**.

RISC-V Processor

- Programs a Xilinx PYNQ demo board into a working **RV32IM** processor.
- Classic 5-stage pipeline and speculative result forwarding.
- Fast **int32** multiplication by utilizing FPGA's builtin **int16** multiplier in parallel.

Lorenz Attractor

<https://github.com/A0IDU0/LorenzAttractor/>

- A animated figure of Lorenz attractor written in Haskell.
- Demo: [https://homepages.inf.ed.ac.uk/wadler/fp-competition-2019/#\(16\)](https://homepages.inf.ed.ac.uk/wadler/fp-competition-2019/#(16)).

Turing Machine Emulator

<https://github.com/A0IDU0/RegisterMachineEmulator/>

- A emulator for the register variant of turing machine with only 2 instructions: **inc** and **decjz**.
- Has a parser that recognizes instruction source code in BNF style.
- Planning to complete the support of macro in the future.

SKILLS

- Have experience with GNU/Linux,
- Familiar with Java, Agda, Haskell, Python, Shell, Verilog and C++,
- Capable of building embedded widgets with single board computers and PCDIY.