CPE301 – FALL 2019

Design Assignment 2A

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Primary Github address: <https://github.com/buchaa2/103EPC>

Directory: <https://github.com/buchaa2/103EPC/tree/master/DA2A>

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

List of Components used

Block diagram with pins used in the Atmega328P

1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

; DA2A.asm

;

; Created: 9/28/2019 1:18:05 AM

; Author : ANDREW BUCHANAN

;

; Replace with your application code

; GPIOs\_Part1\_ASM.asm

.org 0

sbi DDRB, 3 ; set PORTB.3 as output

sbi PORTB, 3 ; set LED off

; generate waveform with 40% DC and .625 sec period

BEGIN:

sbi PORTB, 3 ; set LED on

rcall delay\_1

cbi PORTB, 3 ; set LED off

rcall delay\_2

jmp BEGIN

; Delay 4 000 000 cycles

; 250ms at 16 MHz

delay\_1:

ldi r18, 21

ldi r19, 75

ldi r20, 191

L1: dec r20

brne L1

dec r19

brne L1

dec r18

brne L1

nop

ret

; Delay 6 000 000 cycles

; 375ms at 16 MHz

delay\_2:

ldi r18, 31

ldi r19, 113

ldi r20, 31

L2: dec r20

brne L1

dec r19

brne L1

dec r18

brne L2

nop

ret

#define *F\_CPU* 16000000UL

#include <avr/io.h>

#include <util/delay.h>

int main(void)

{

DDRB |= (1<<3); // set PORTB.3 for output

while (1)

{

*\_delay\_ms*(250); // delay for 40% DC

PORTB &= ~(1<<3); // make port B LED high

*\_delay\_ms*(375); // the rest of the .650ms delay

PORTB |= (1<<3); // make port B LED low

}

}

; DA2A\_part2.asm

;

; Created: 9/30/2019 9:22:22 PM

; Author : ANDREW BUCHANAN

;

; GPIOs\_Part2\_ASM.asm

.org 0

cbi DDRC, 3 ; set PORTC.3 to be an input

sbi PORTC, 3 ; set PORTC.3 to be active high

sbi DDRB, 2 ; set PORTB.3 to be an output output

sbi PORTB, 2 ; set LED off

FUNC:

sbic PINC, 3 ; if PINC is low go to line 17

jmp SKIP ; jump to pin C

sbi PORTB, 2 ; turn LED on

; Delay 21 328 000 cycles

; 1s 333ms at 16 MHz

ldi r18, 109

ldi r19, 51

ldi r20, 106

L1: dec r20

brne L1

dec r19

brne L1

dec r18

brne L1

jmp FUNC

SKIP:

Cbi PORTB, 2 ; turn LED off

jmp FUNC

; DA2A\_part2.asm

;

; Created: 9/30/2019 9:22:22 PM

; Author : ANDREW BUCHANAN

;

; GPIOs\_Part2\_ASM.asm

.org 0

cbi DDRC, 3 ; set PORTC.3 to be an input

sbi PORTC, 3 ; set PORTC.3 to be active high

sbi DDRB, 2 ; set PORTB.3 to be an output output

sbi PORTB, 2 ; set LED off

FUNC:

sbic PINC, 3 ; if PINC is low go to line 17

jmp SKIP ; jump to pin C

sbi PORTB, 2 ; turn LED on

; Delay 21 328 000 cycles

; 1s 333ms at 16 MHz

ldi r18, 109

ldi r19, 51

ldi r20, 106

L1: dec r20

brne L1

dec r19

brne L1

dec r18

brne L1

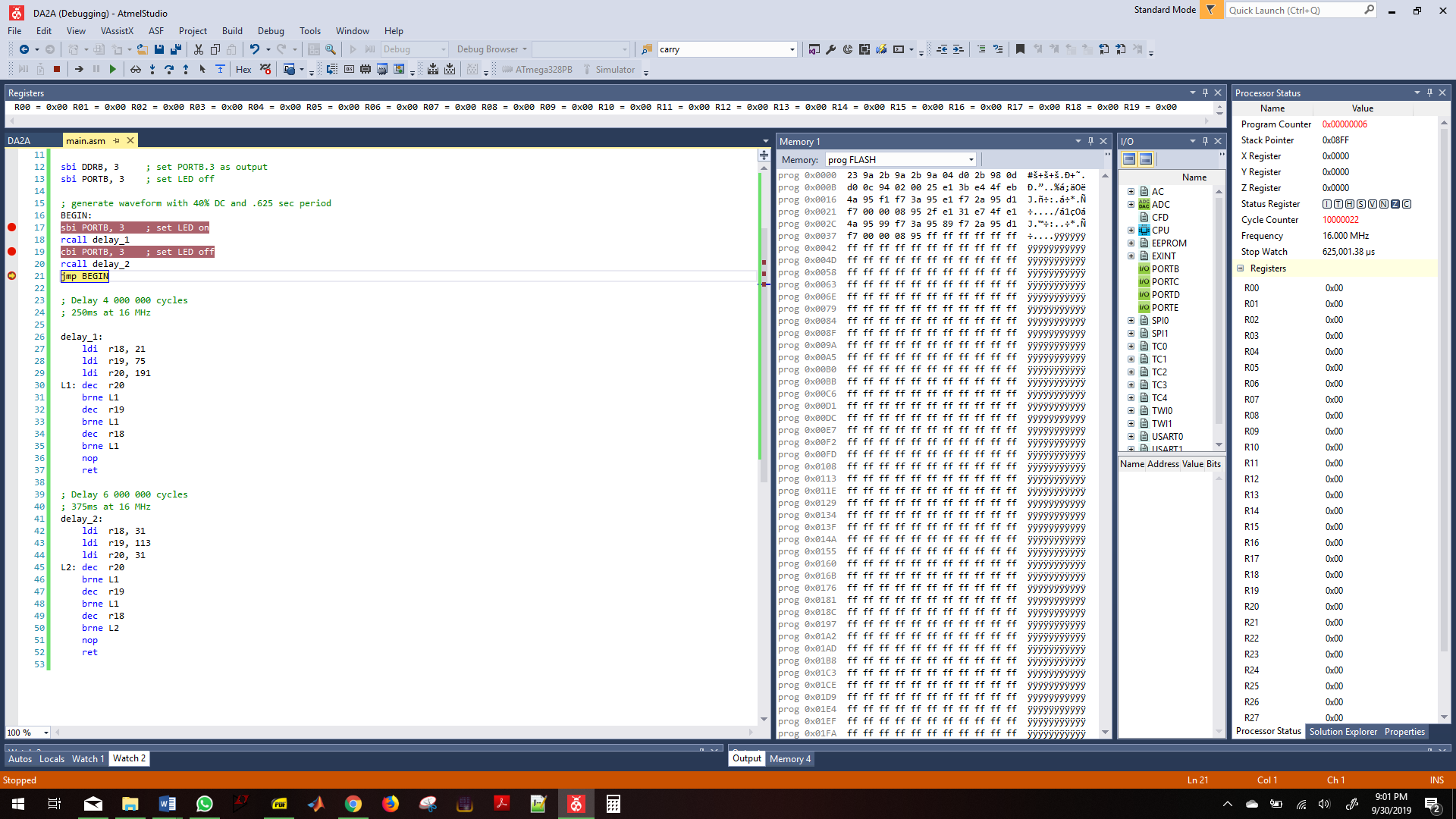
jmp FUNC

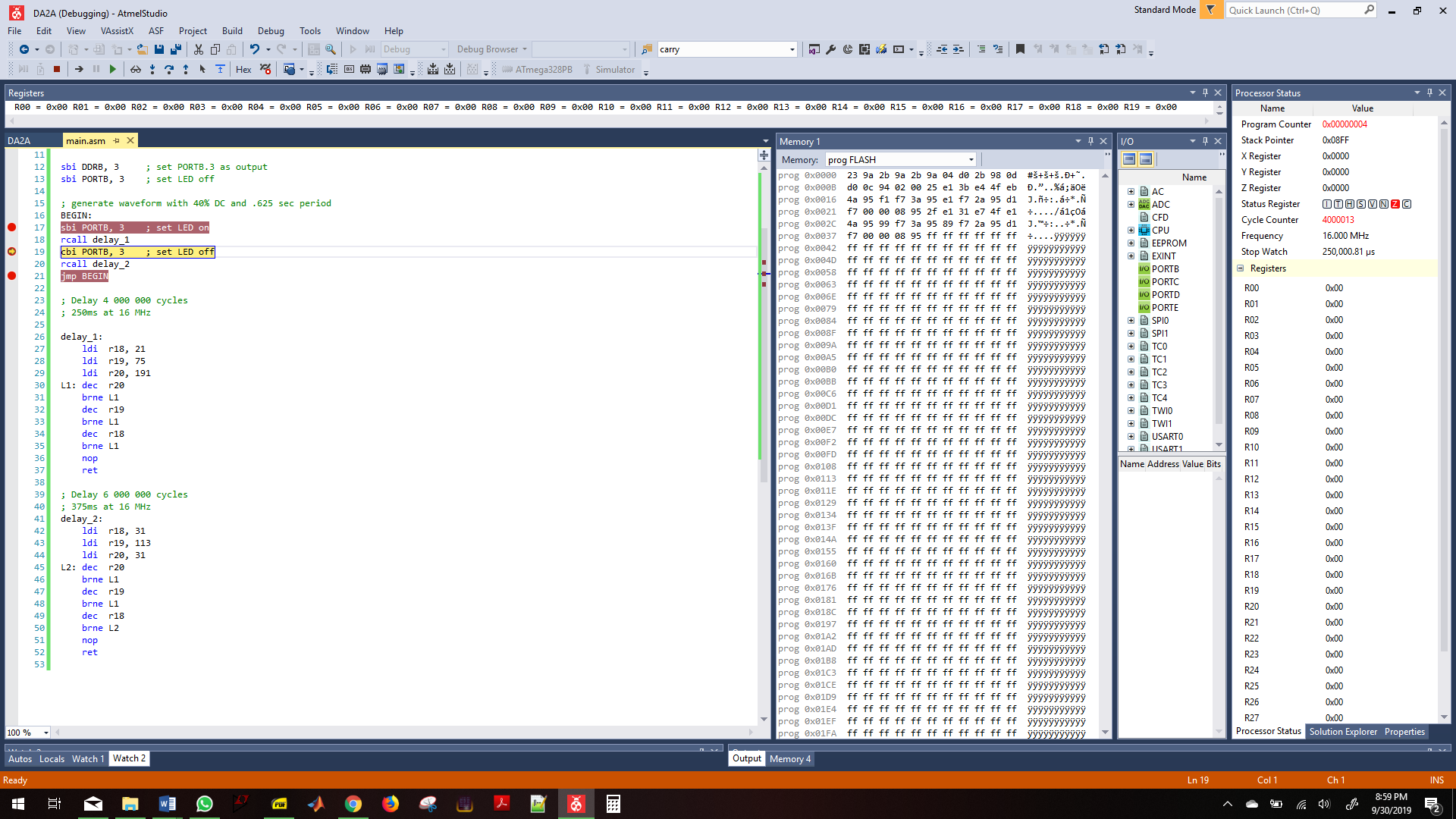
SKIP:

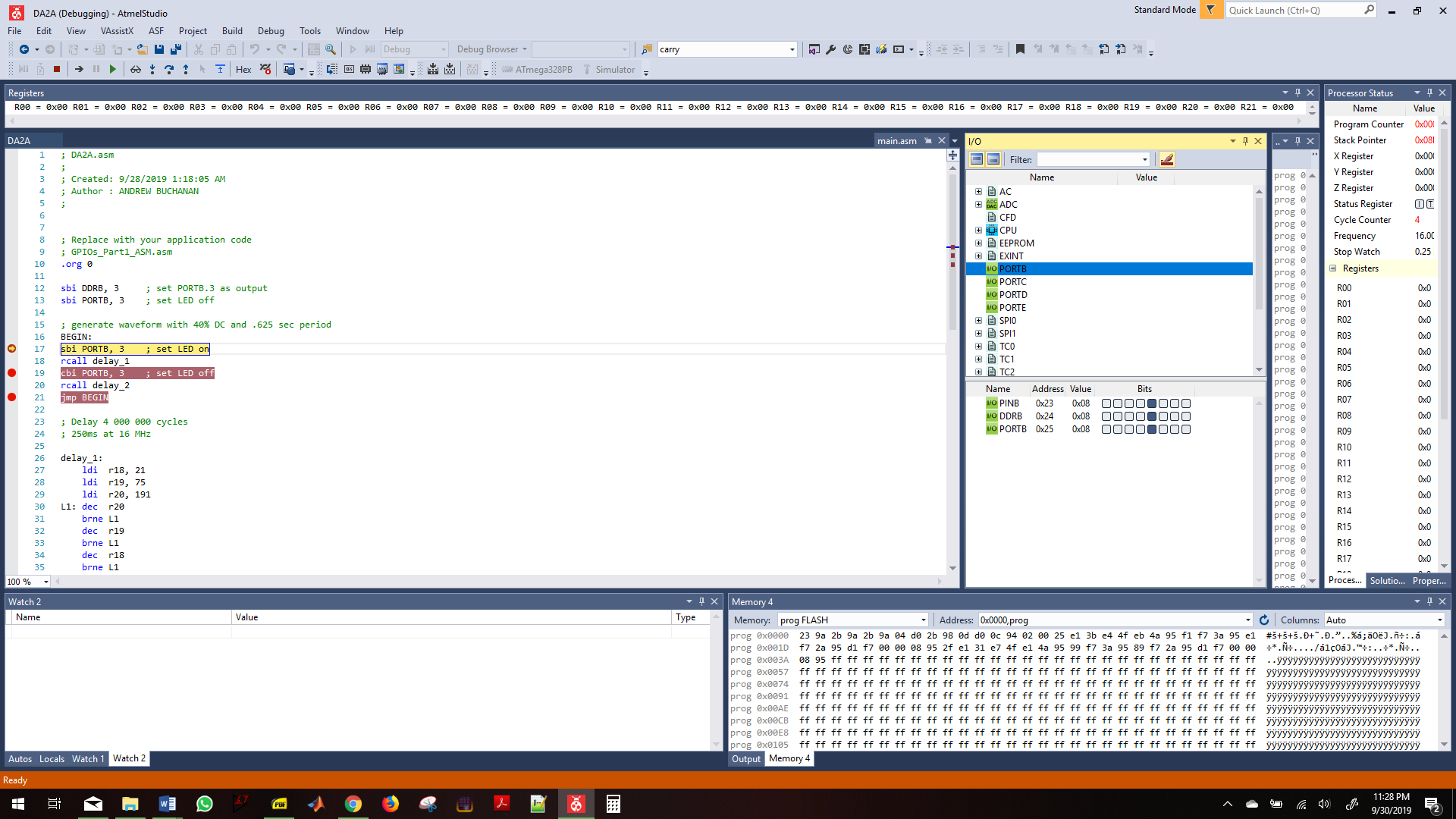
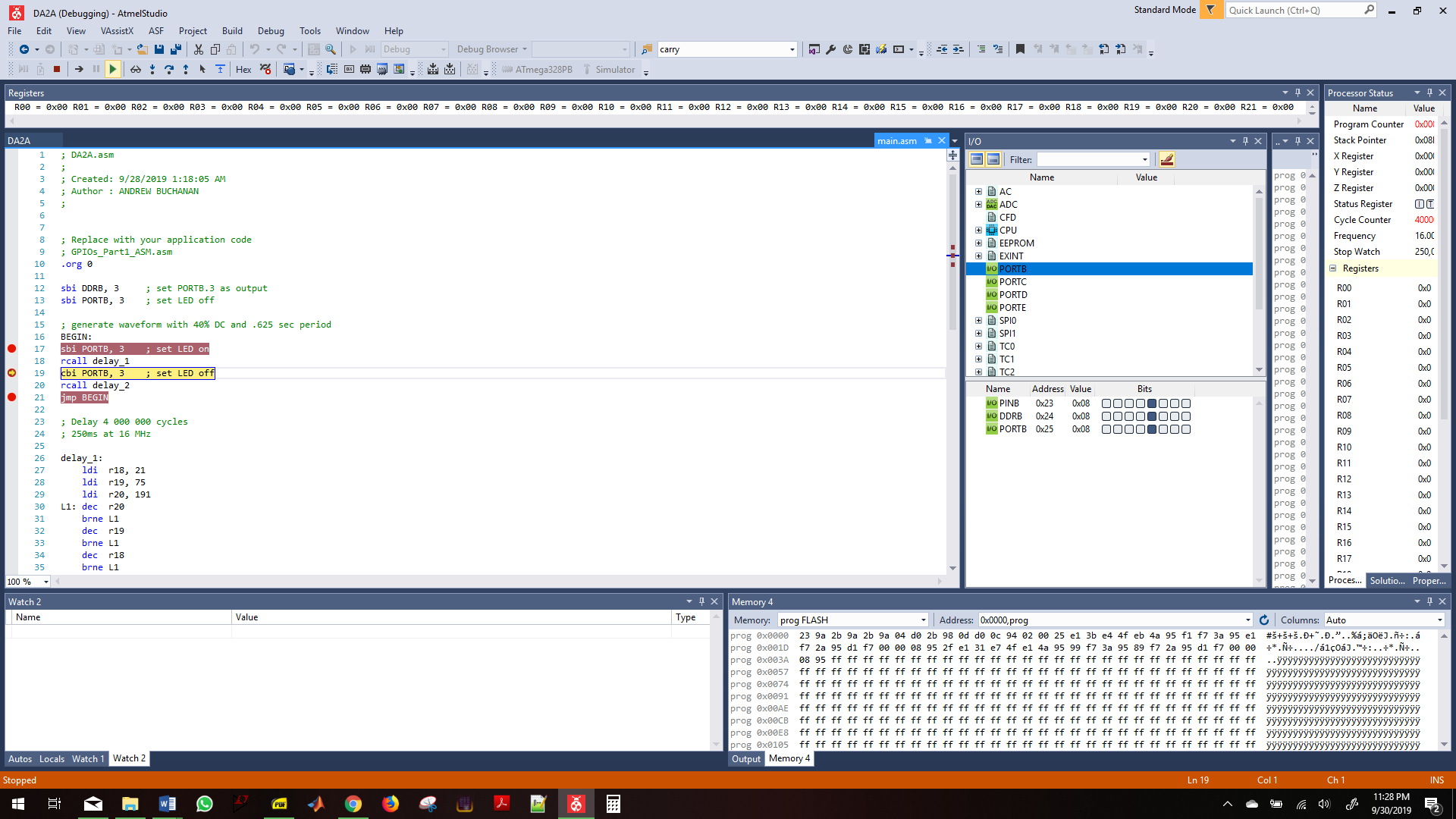
Cbi PORTB, 2 ; turn LED off

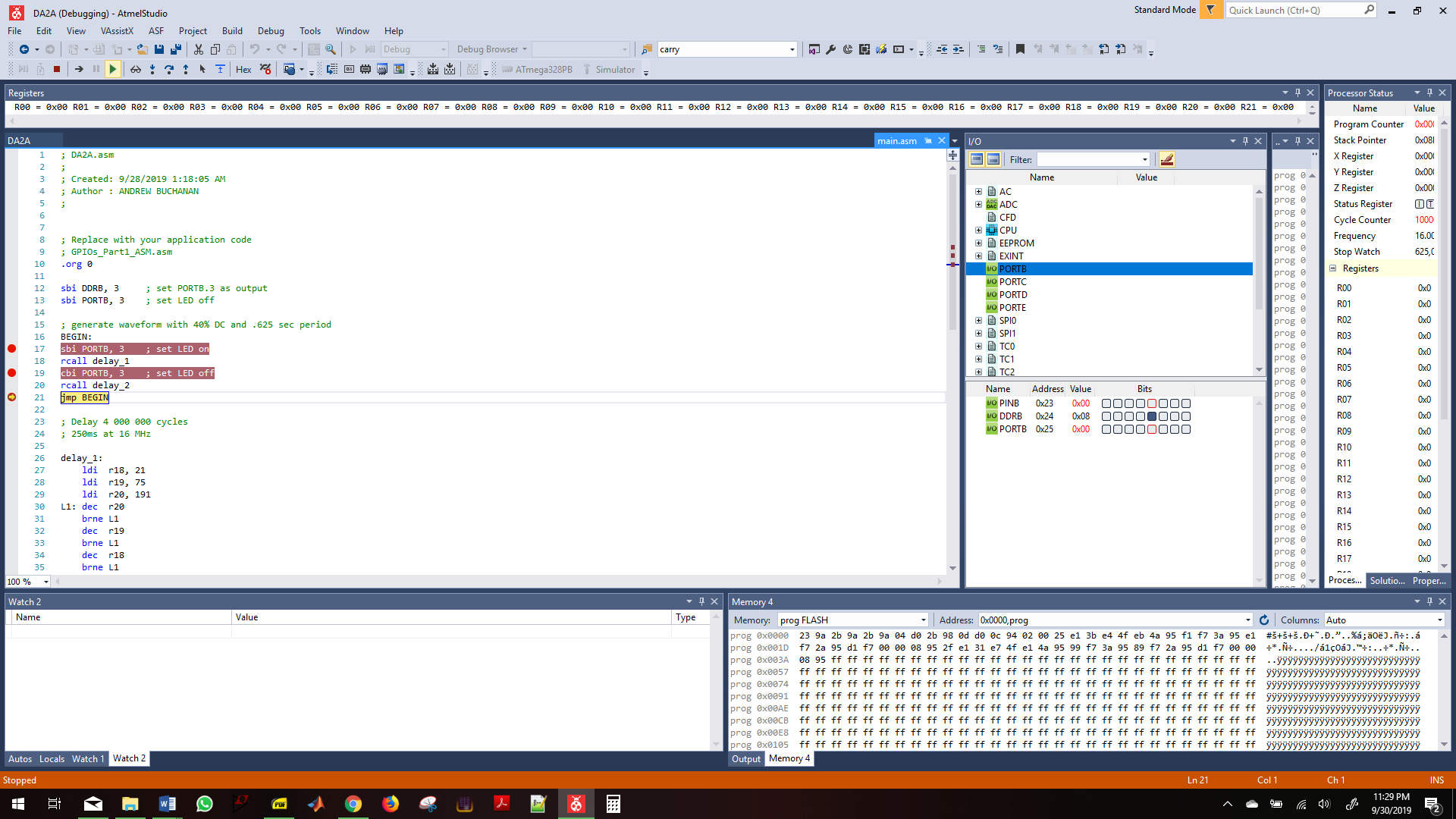
jmp FUNC

1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**
2. **SCHEMATICS**
3. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**

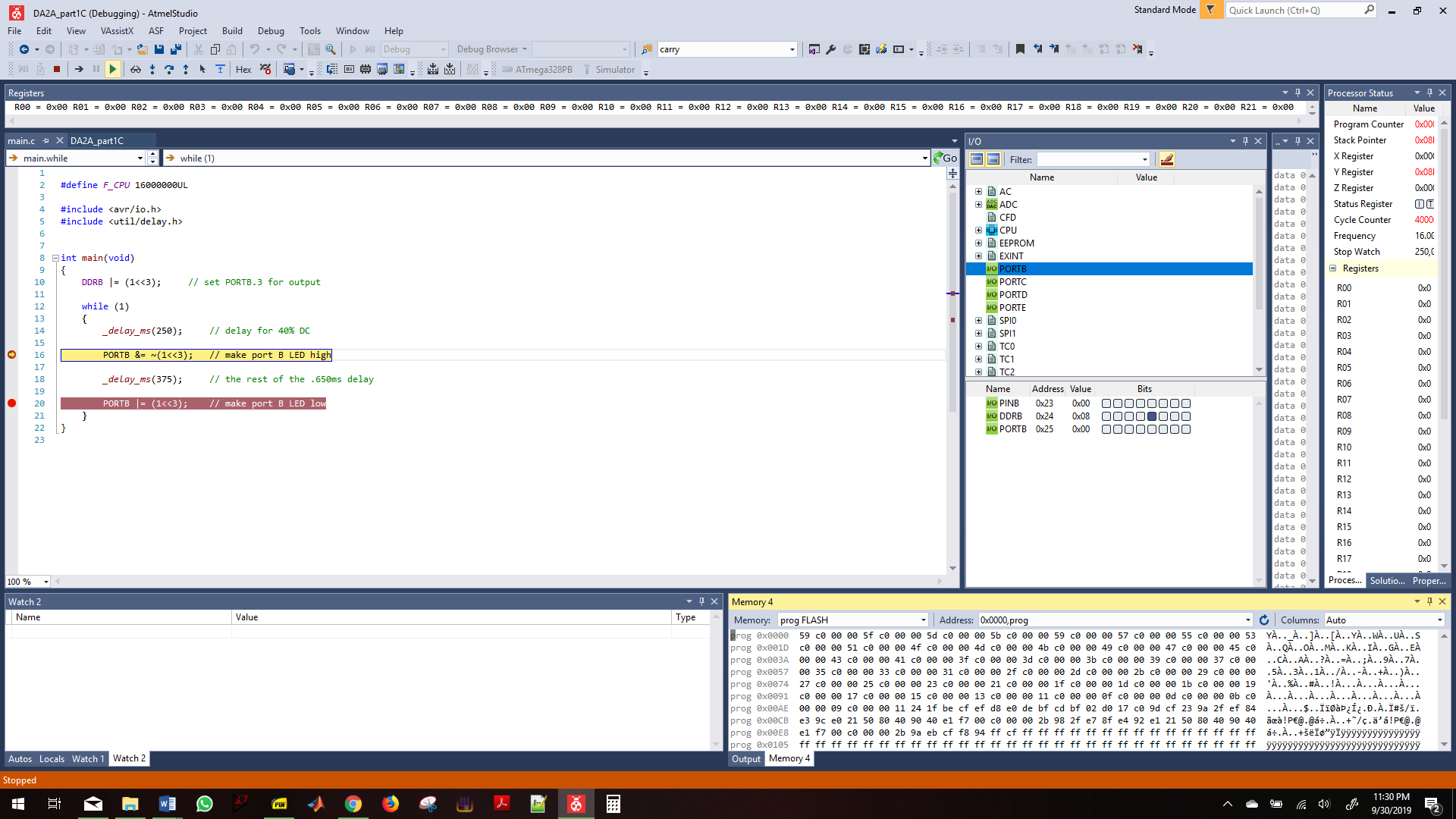


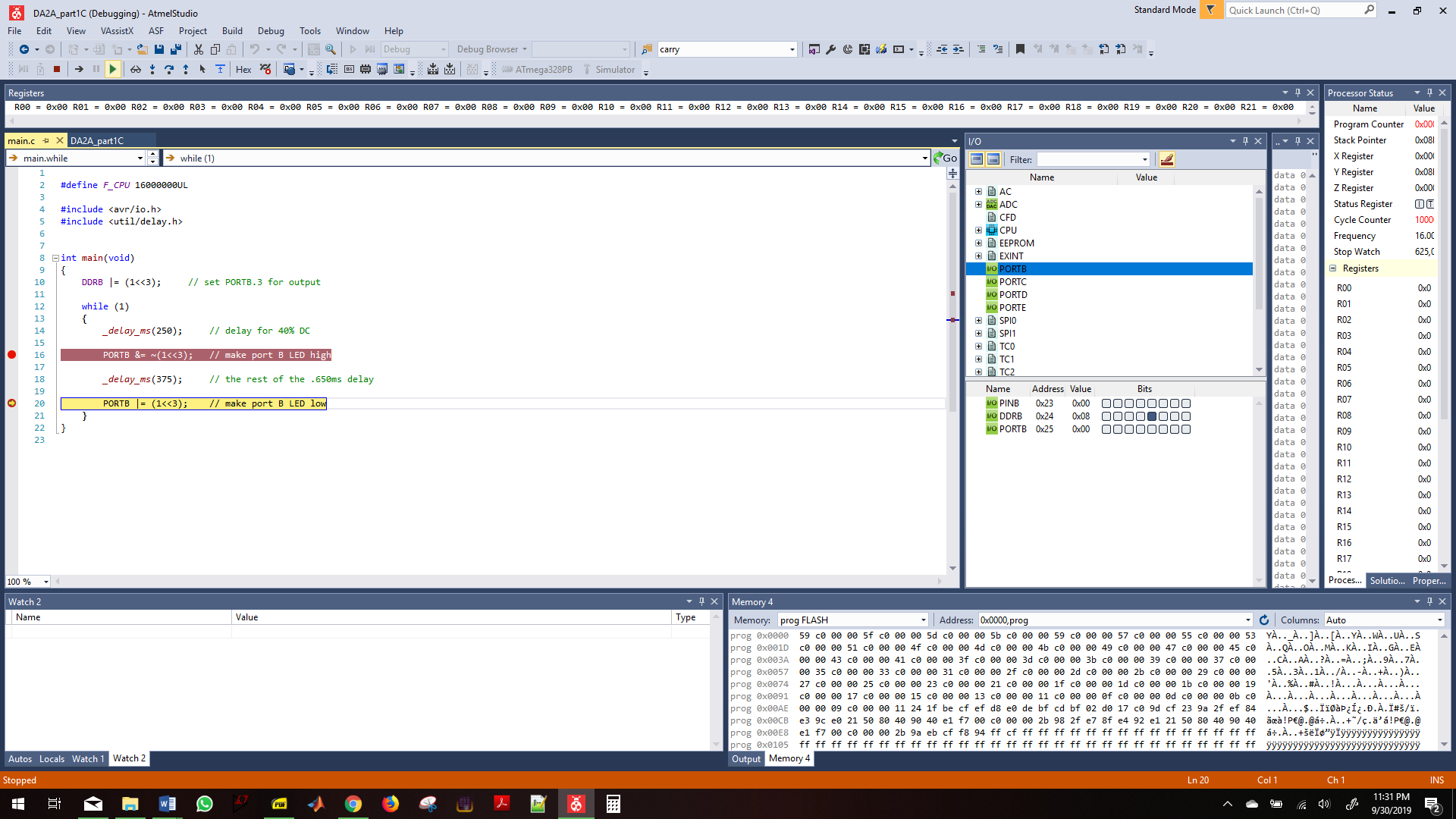




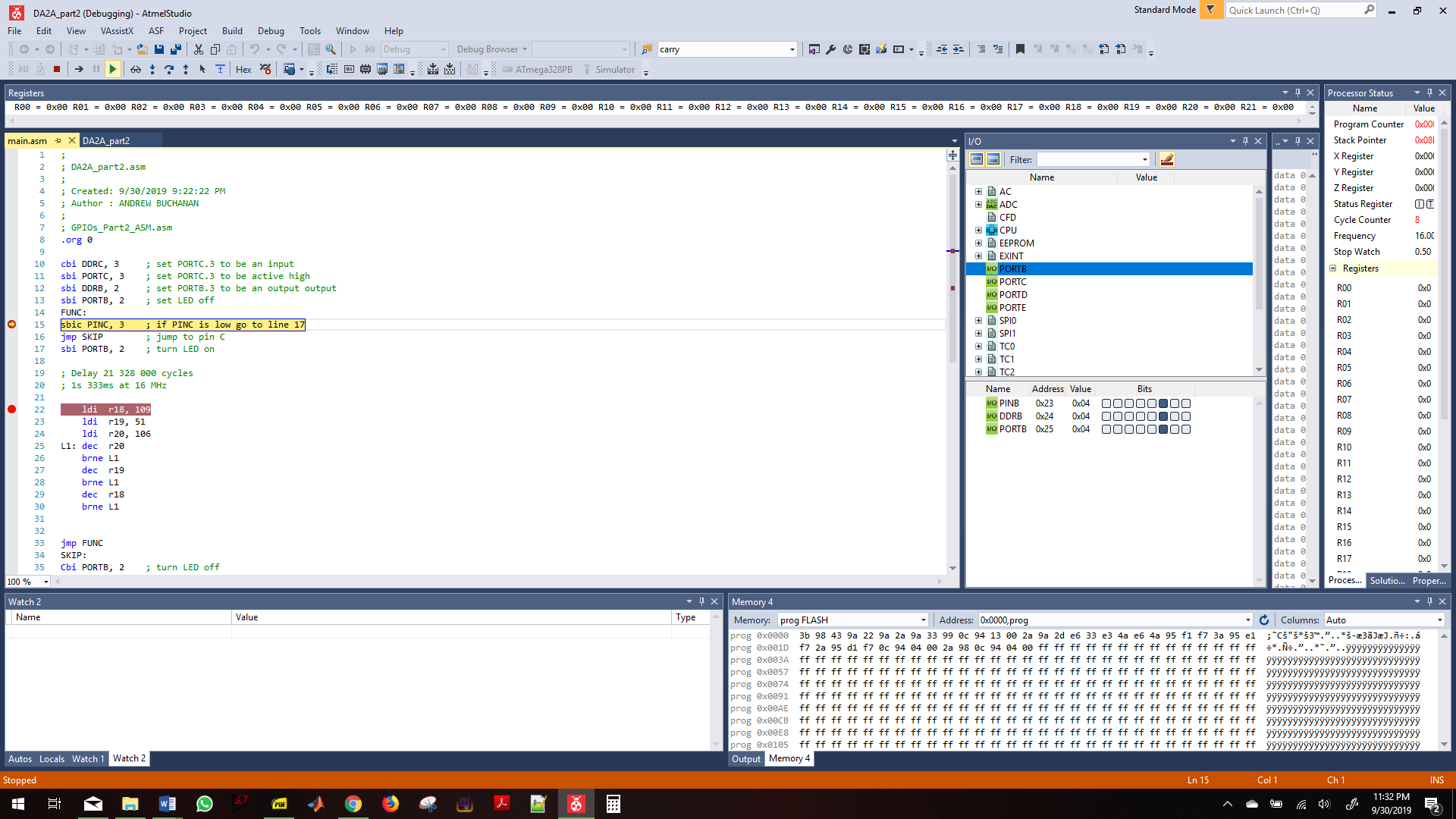


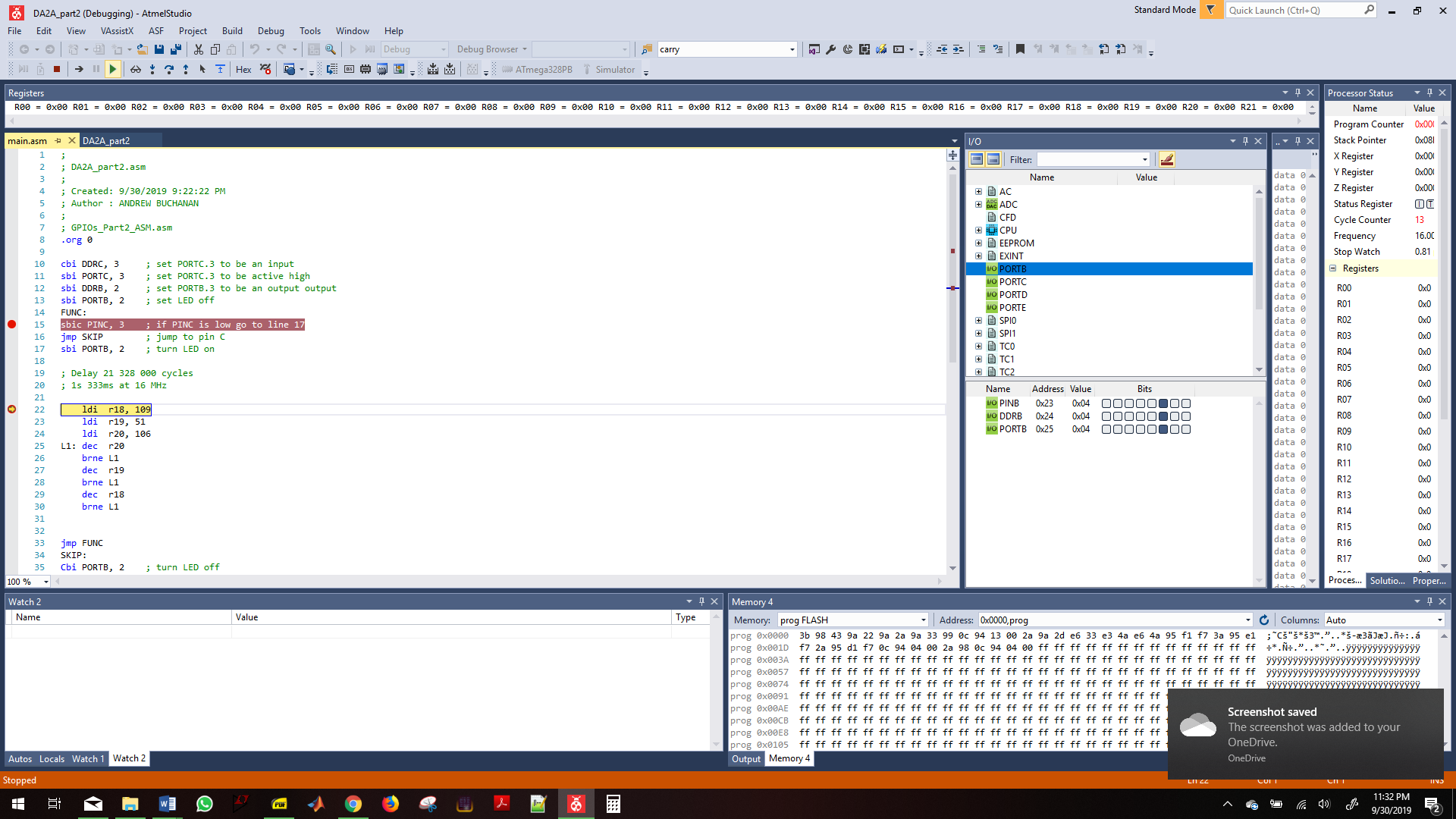
Part 1 C code

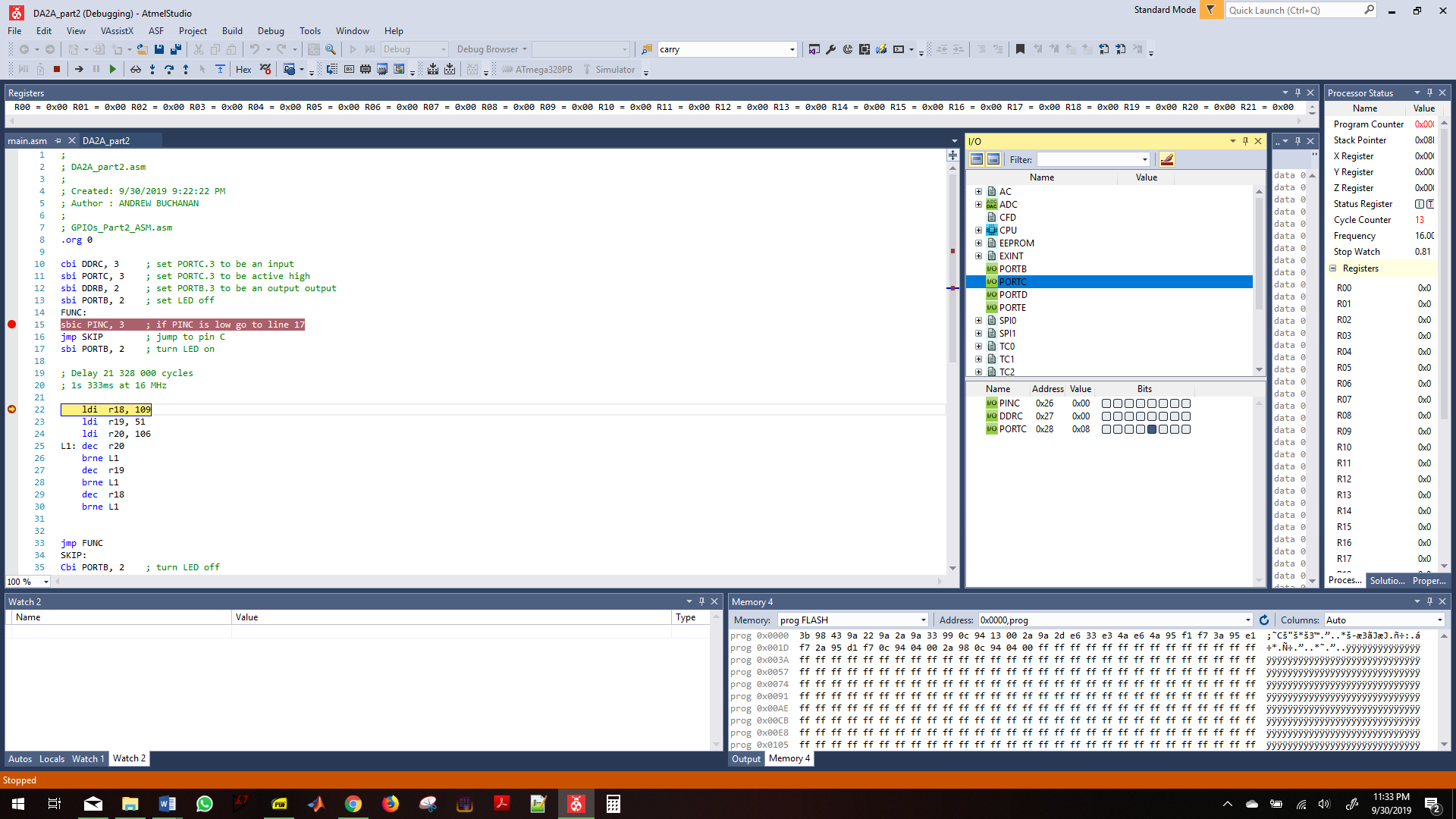




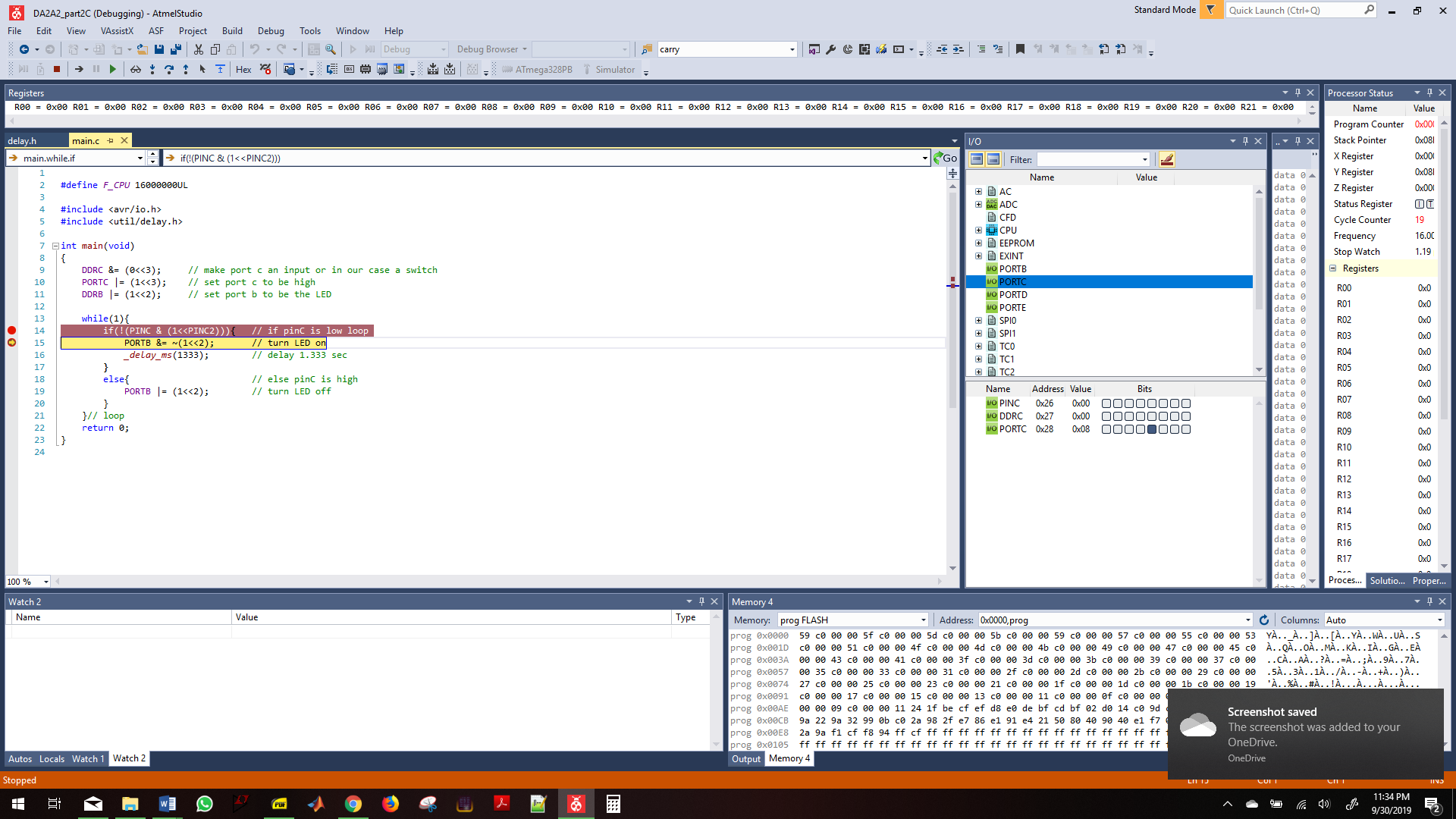
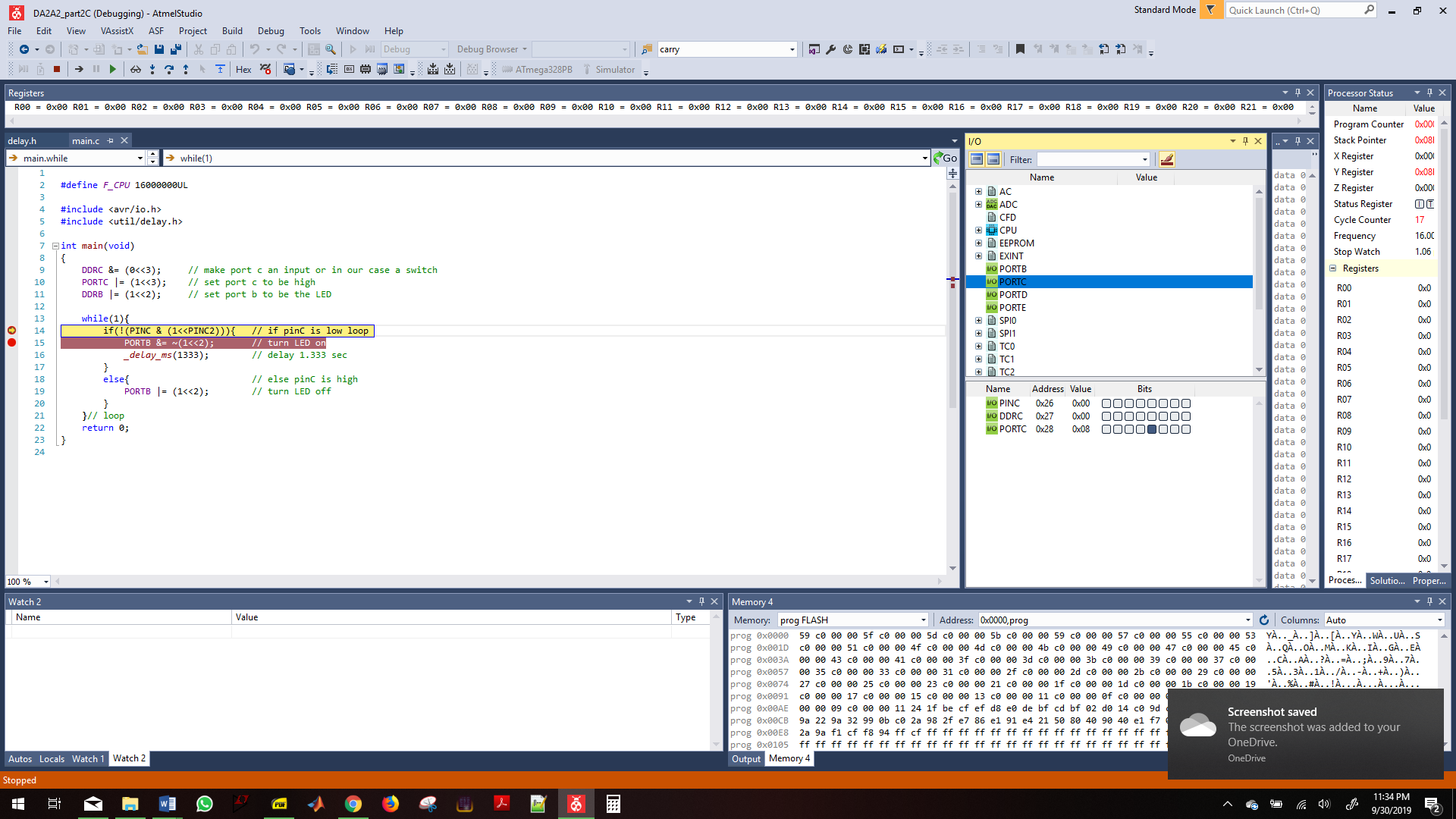
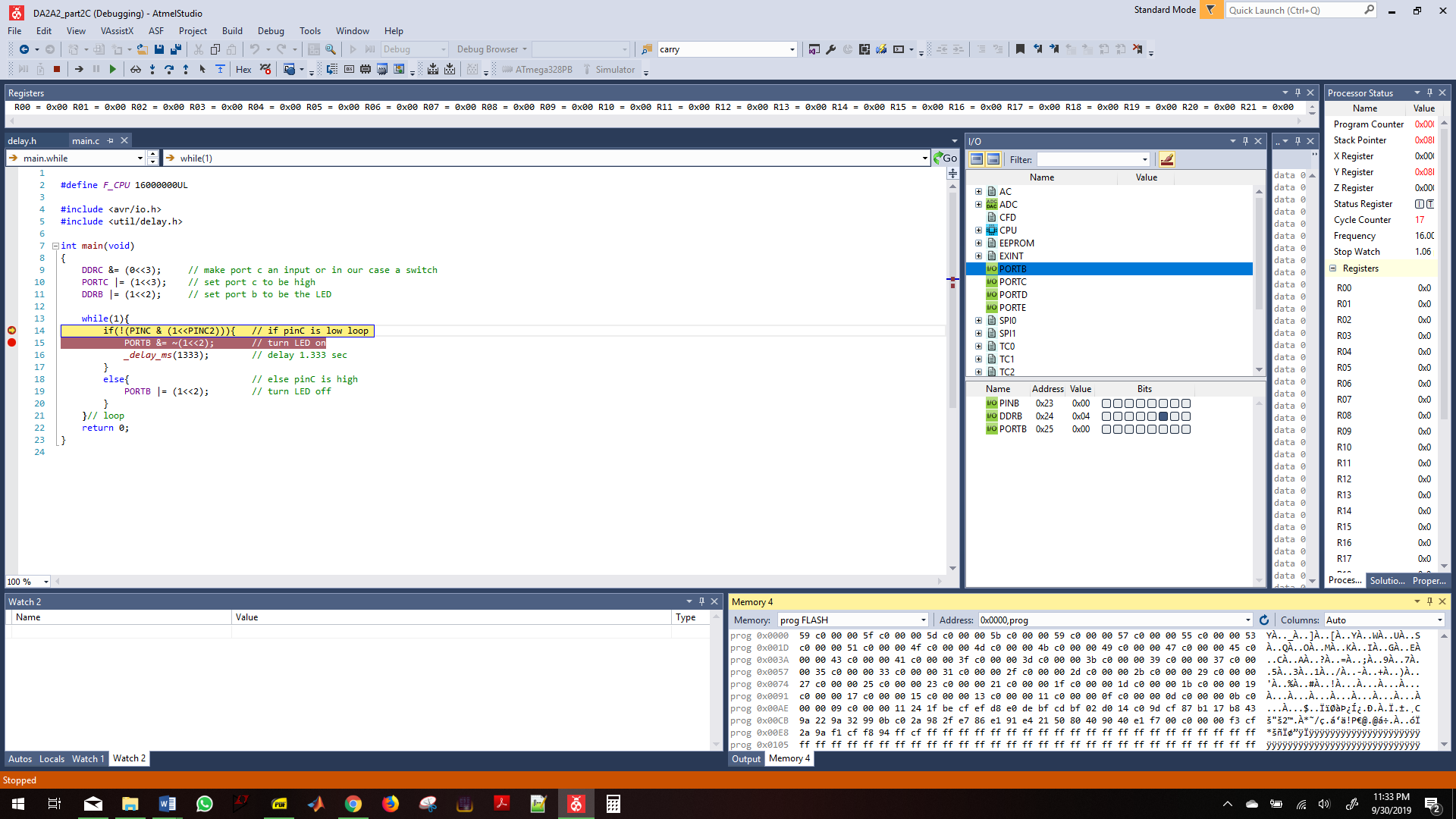
Part 2

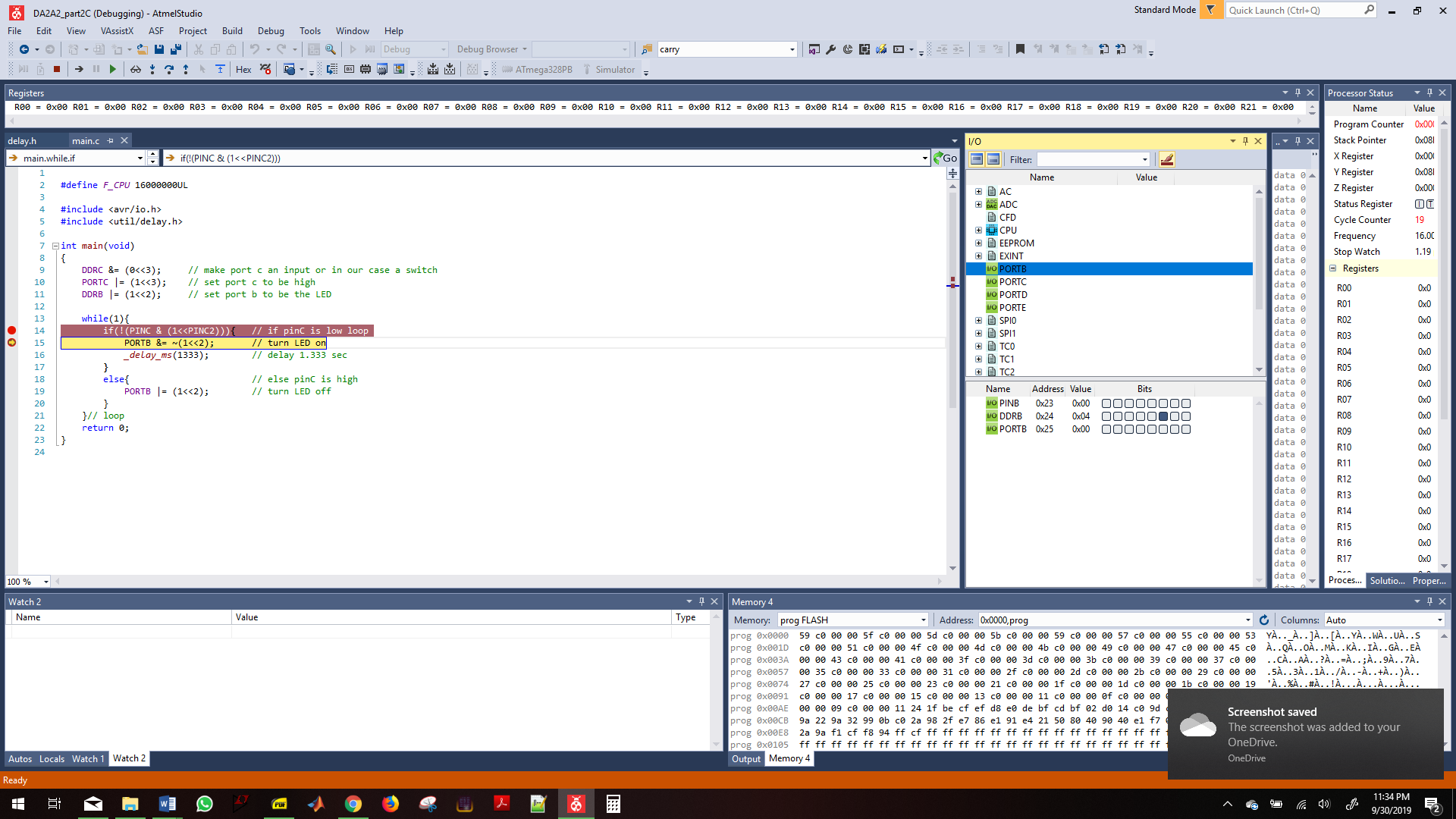






Part2 C code





1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**
2. **VIDEO LINKS OF EACH DEMO**
3. **GITHUB LINK OF THIS DA**

<https://github.com/buchaa2/103EPC/tree/master/DA2A>

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

Andrew Buchanan