VD H-Shaking Issue Report

Issue :

There is H-Shaking problem in this NTSC stream.
(NTSC_070615_1512_201.00M_-32.06_20M_-29.03_NON_FieldSignal)

Root Cause:

This issue is related to H-sync period unstable. Figure 1 is the H-synchronization block diagram. First, RF TV signal down converted by tuner transfers CVBS signal, which is feed through a low-pass filter to remove chrominance and high frequency noise. Then, the data enter the slicer to generate a sliced h-sync. As in Figure2, sliced h-sync is asserted when CVBS data value is changed from high to low across the slice level. The sliced h-sync then enters a phase lock loop (PLL). The phase detect (PD) module gets the difference between sliced h-sync and NCO output, pass the result to loop filter. Then the final value is used to correct the NCO, so that NCO can lock to the input signal and generates a stable HSYNC output.

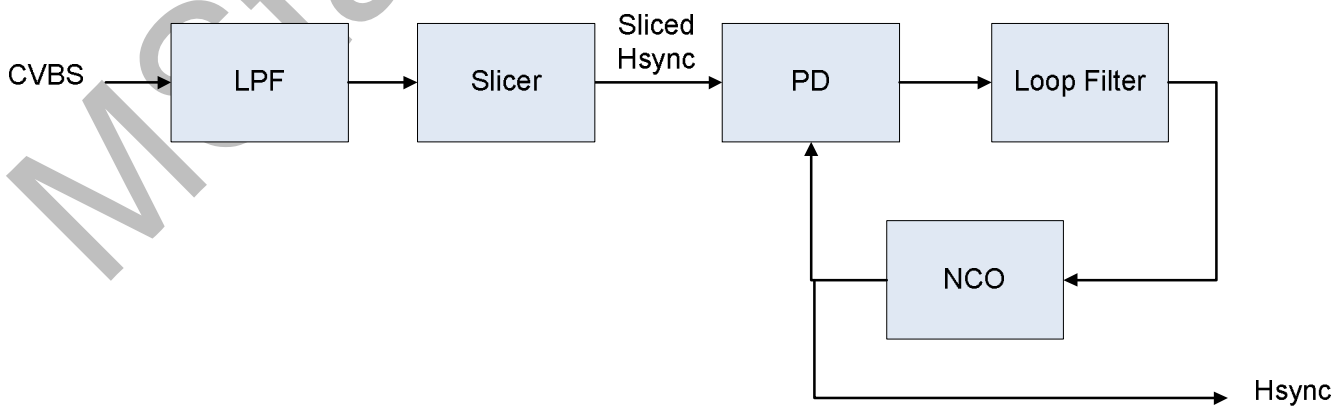


Figure 1

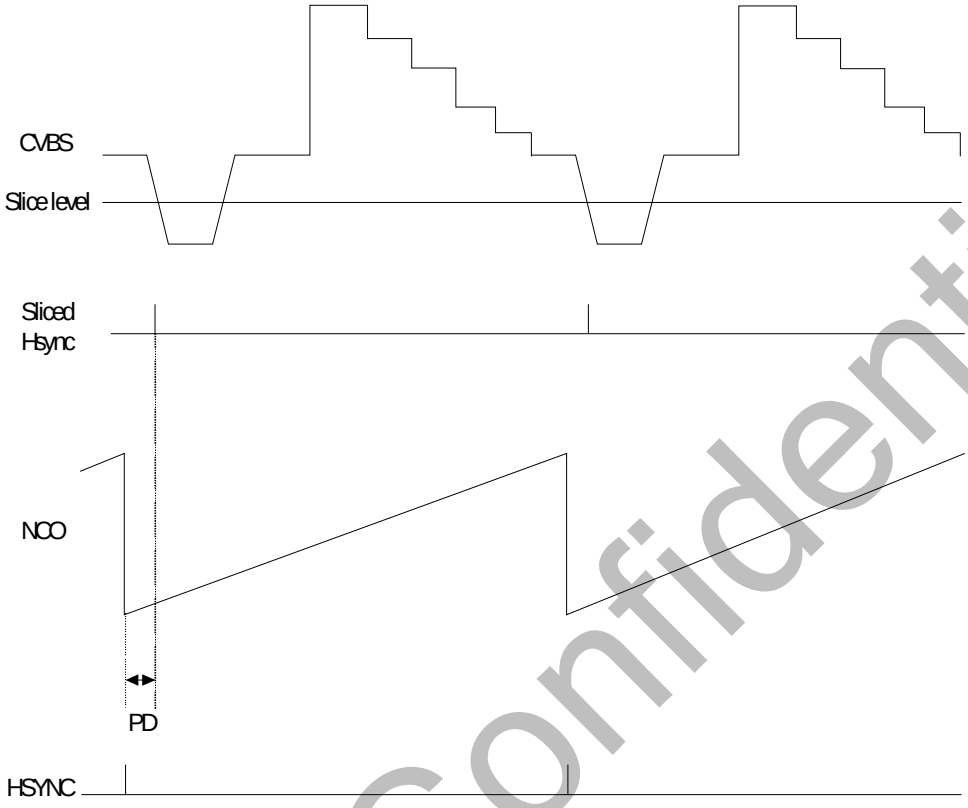


Figure 2

This H-shaking issue is caused by the abnormal H Sync period in this stream, It is like VCR style, shown as Figure 3. The top of image have big H sync phase error, if the display PLL tracking speed is slow, It will happen horizontal shaking at display picture, The Figure 4 is display PLL tracking block diagram. If the accumulation of phase error in phase detector reaches the threshold, the speed of display PLL will accelerate to keep up with h-sync.

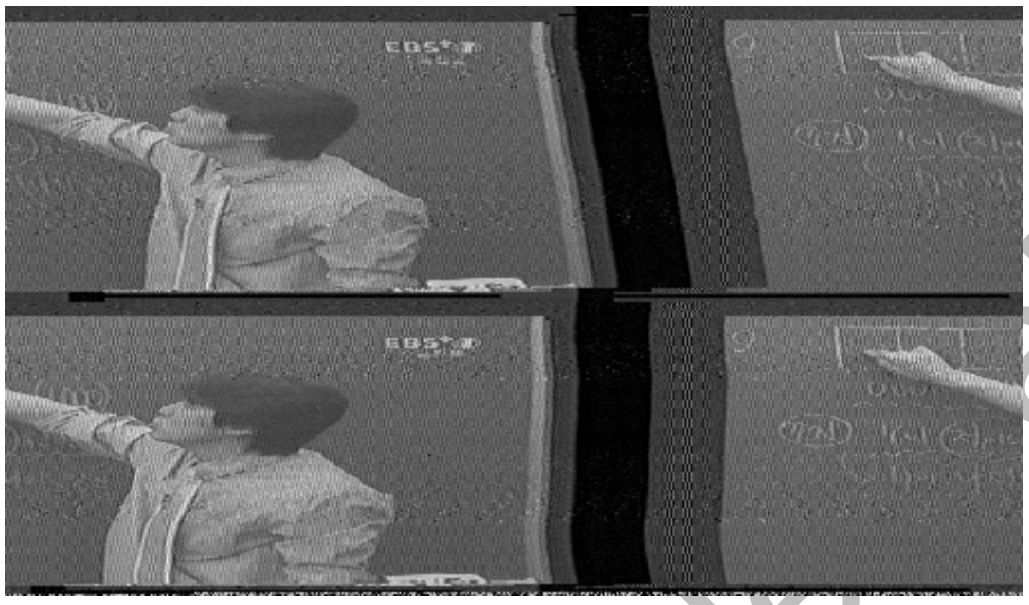
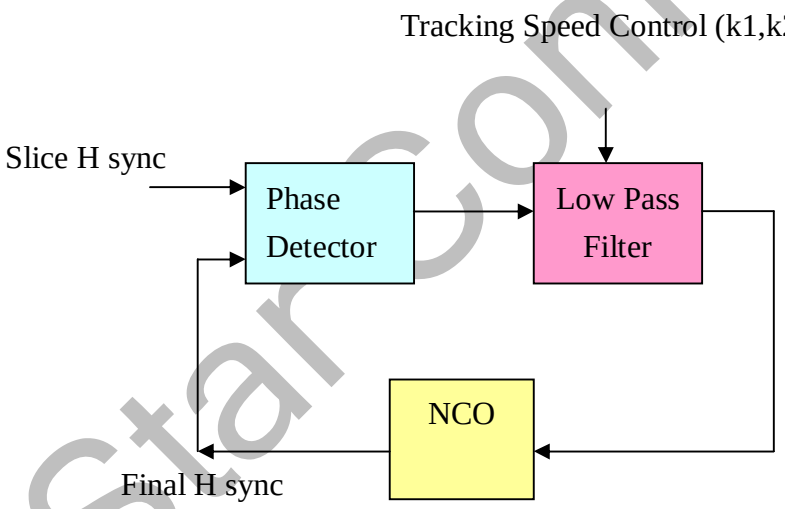


Figure 3



NCO: Numerical Control Oscillator

Figure 4

Solution: Fine-tune the VCR detection threshold to change display PLL tracking speed to improve the stability of H-sync detection.

Discussion:

1. Why does it need to speed up DPL tracking speed gradually?

   Ans: The mechanism of phase detector requires to accumulate enough phase errors to increase higher speed.