Machine Design

Date
Page

Steps

1) Define purpose of machine in simple words. (I/P, O/P, number of flip flops (state)

2) Draw state diagram.

3) Draw state transition table.

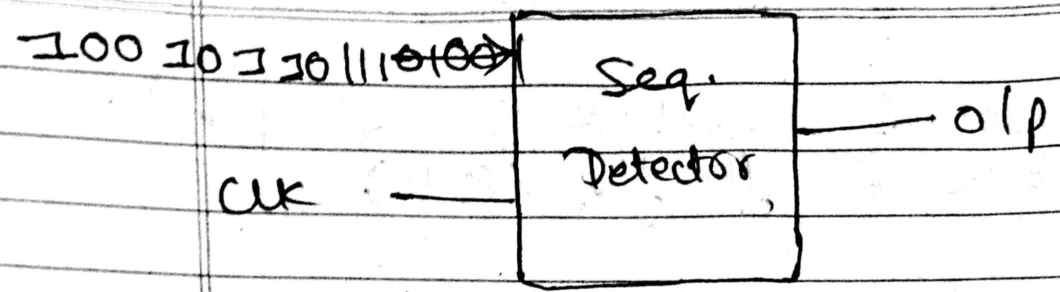
4) Remove redundant states (if any) & assign pure binary.

5) Select flip flop & write excitation table.

6) Find boolean function for each flip flops interms of state variable & inputs. In same manner find o/p boolean function.

7) Draw logic circuit.

1001011011101001



Types → overlapping 2 non-overlapping.

Overlapping

I/p → 1001001001001111011

o/p → 0001001001001000000

non-overlapping

I/p → 1001001001001111011

0001000000100000000

Mealy (overlapping).

1001

78 Bhadra

Step ① → 1-input & 1 output

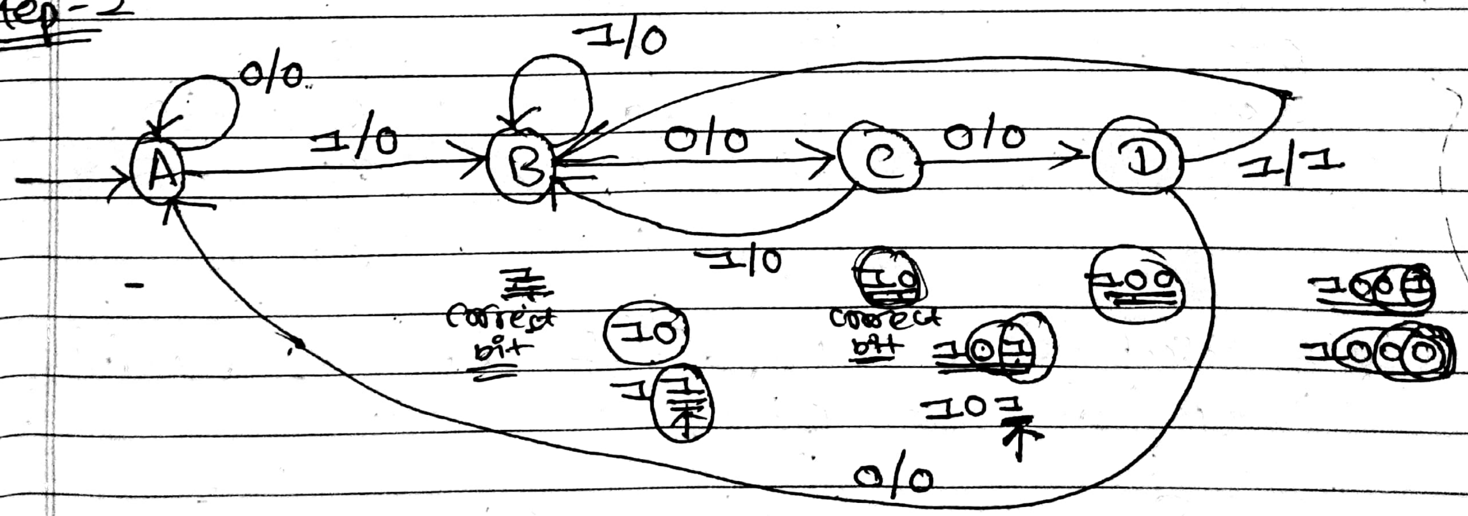
input ⇒ 1001 | o/p ⇒ 0001 } no. of states = 4.

States	Received bits	Remarks
A	–	starting ~~bit~~ state
B	1	1-bit received correctly
C	10	2-bits rec. correctly
D	100	3-bit received correctly

when 4th correct bit in a sequence is received, the o/p of ckt will be 1.

(Number of (states) detector = number of bits in seq.)

Step-2



State diagram

Date
Page

Step-3 Draw Transition table:

Present state	Next state		Output (Y)	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	C	B	0	0
C	D	B	0	0
D	A	B	0	1

Step-4 State reduction & Assignment of pure binary.

Present state ($Q_1 Q_0$)	Next state		Output (Y)	
	X=0	X=1	X=0	X=1
00	00	01	0	0
01	10	01	0	0
10	11	01	0	0
11	00	01	0	1

Step ⑤ Selection of type of FF. & excitation table of same.

Excitation table of D-flip flop.

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(n) $(Q_1 Q_0)$ Present state	Input (X)	(n+1) $(Q_1 Q_0)$ Next state	(Y) output	I/P of FF D_1	D_0
00	0	00	0	0	0
00	1	01	0	0	1
01	0	10	0	1	0
01	1	01	0	0	1
10	0	11	0	1	1
10	1	01	0	0	1
11	0	00	0	0	0
11	1	01	1	0	1

Step (6) Now find Flip flop inputs and outputs interms present state & input.

D_1

Q_1 \ Q_0X	00	01	11	10
0	0	0	0	1
1	1	0	0	0

D_0

Q_1 \ Q_0X	00	01	11	10
0	0	1	1	0
1	1	1	1	0

$D_1 = \overline{Q_1} Q_0 \overline{X} + Q_1 \overline{Q_0}\, \overline{X}$

$D_0 = X + Q_1 \overline{Q_0}$

Y

Q_1 \ Q_0X	00	01	11	10
0	0	0	0	0
1	0	0	1	0

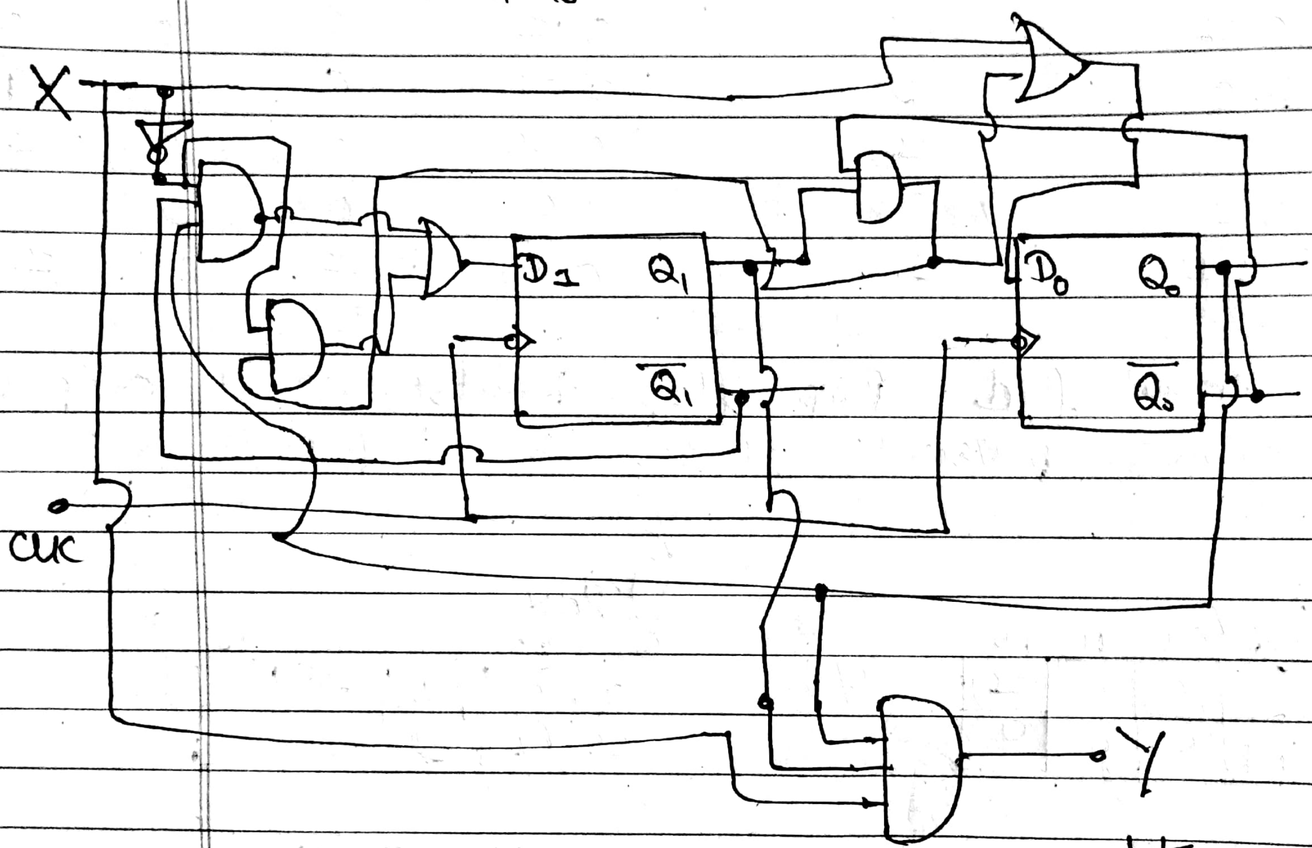
$Y = Q_1 Q_0 X$

Step - 7

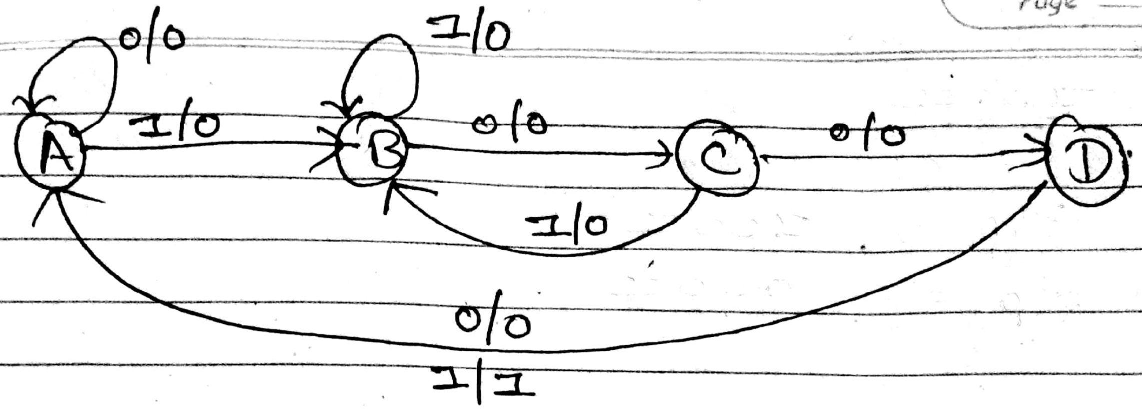
$$D_0 = X + Q_1 \overline{Q_0}$$

$$D_1 = \overline{X}\,\overline{Q_1}\,Q_0 + \overline{X}\,Q_1\,\overline{Q_0}$$

$$Y = X\,Q_1 Q_0.$$



Non-overlapping



Moore (overlapping)

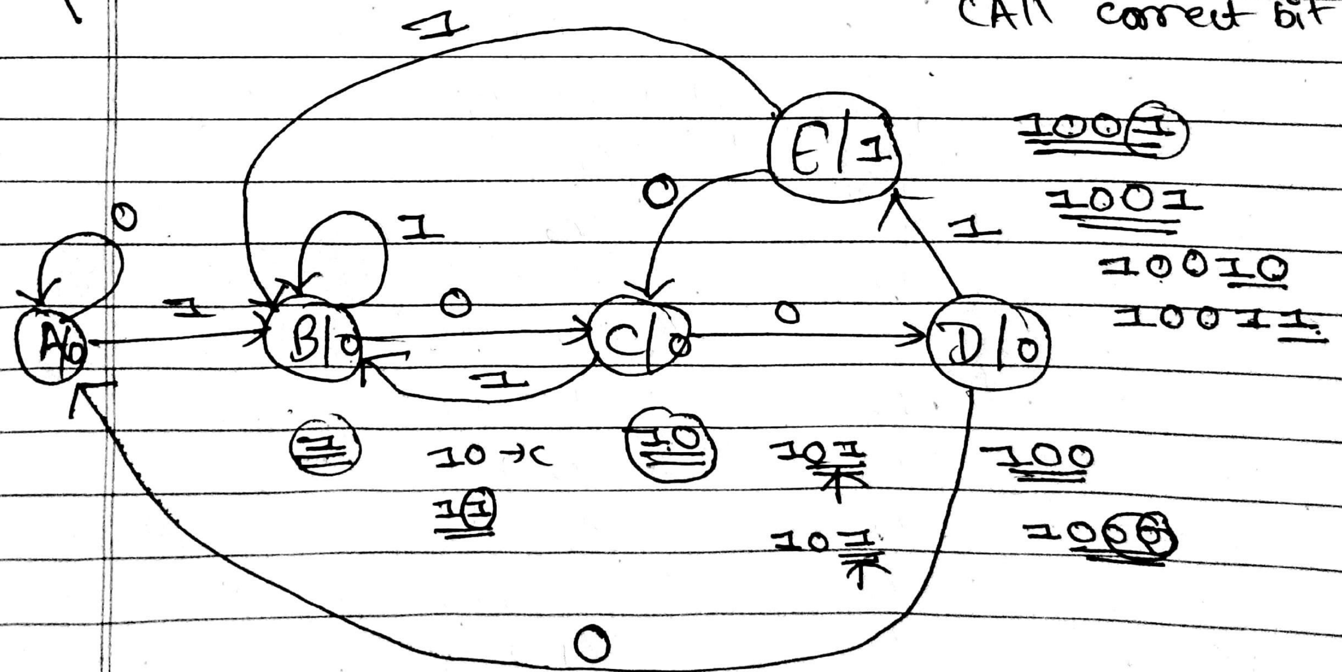
Date
Page

1001

Step ① i/p ⇒ 1001
o/p ⇒ 0001

Step ② Draw state diagram.

State	Received Bits	Remarks
A	—	Starting state
B	1	1st correct bit received
C	10	2nd " " "
D	100	3rd " " "
E	1001	4th " " " (All correct bit rec)



Step ③ Draw transition table:

Present state	Next state $X=0$	Next state $X=1$	output (Y) $X=0$	output (Y) $X=1$
A	A	B	0	0
B	C	B	0	0
C	D	B	0	0
D	A	E	0	0
E	C	B	1	1

(Check for redundancy).

Step ④ State reduction & Assignment of pure binary.
A → 000, B → 001, C = 010, E → 011, D = 100. (101, 110, 111) = DC

Present state ($Q_2 Q_1 Q_0$)	Next state $x=0$ ($Q_2^+ Q_1^+ Q_0^+$)	Next state $x=1$	output (Y) $x=0$	output (Y) $x=1$
000	000	001	0	0
001	010	001	0	0
010	100	001	0	0
100	000	011	0	0
011	010	001	1	1

Step ⑤: Selection of flip flop & excitation table of same:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Date
Page

Step 6

PS ($Q_2 Q_1 Q_0$)	Input (X)	Next state $Q_2^+ Q_1^+ Q_0^+$	O/P (Y)	I/P of FF D_2	D_1	D_0
0 0 0	0	0 0 0	0	0	0	0
0 0 0	1	0 0 1	0	0	0	1
0 0 1	0	0 1 0	0	0	1	0
0 0 1	1	0 0 1	0	0	0	1
0 1 0	0	1 0 0	0	1	0	0
0 1 0	1	0 0 1	0	0	0	1
0 1 1	0	0 0 0	1	0	0	0
0 1 1	1	0 0 1	1	0	0	1
1 0 0	0	0 1 0	0	0	1	0
1 0 0	1	0 0 1	0	0	0	1

PS $Q_2 Q_1 Q_0$	Input X		Next state $Q_2^+ Q_1^+ Q_0^+$	O/P Y	I/P of FF D_2	D_1	D_0
0 0 0	0	0	0 0 0	0	0	0	0
0 0 0	1	1	0 0 1	0	0	0	1
0 0 1	0	2	0 1 0	0	0	1	0
0 0 1	1	3	0 0 1	0	0	0	1
0 1 0	0	4	1 0 0	0	1	0	0
0 1 0	1	5	0 0 1	0	0	0	1
1 0 0	0	8	0 0 0	0	0	0	0
1 0 0	1	9	0 1 1	0	0	1	1
0 1 1	0	6	0 1 0	1	0	1	0
0 1 1	1	7	0 0 1	1	0	0	1

(~~Minterms → M5, M6, M7, M13, M14, M15 are don't care~~)

Date
Page

Step (6) (Using K-Map)

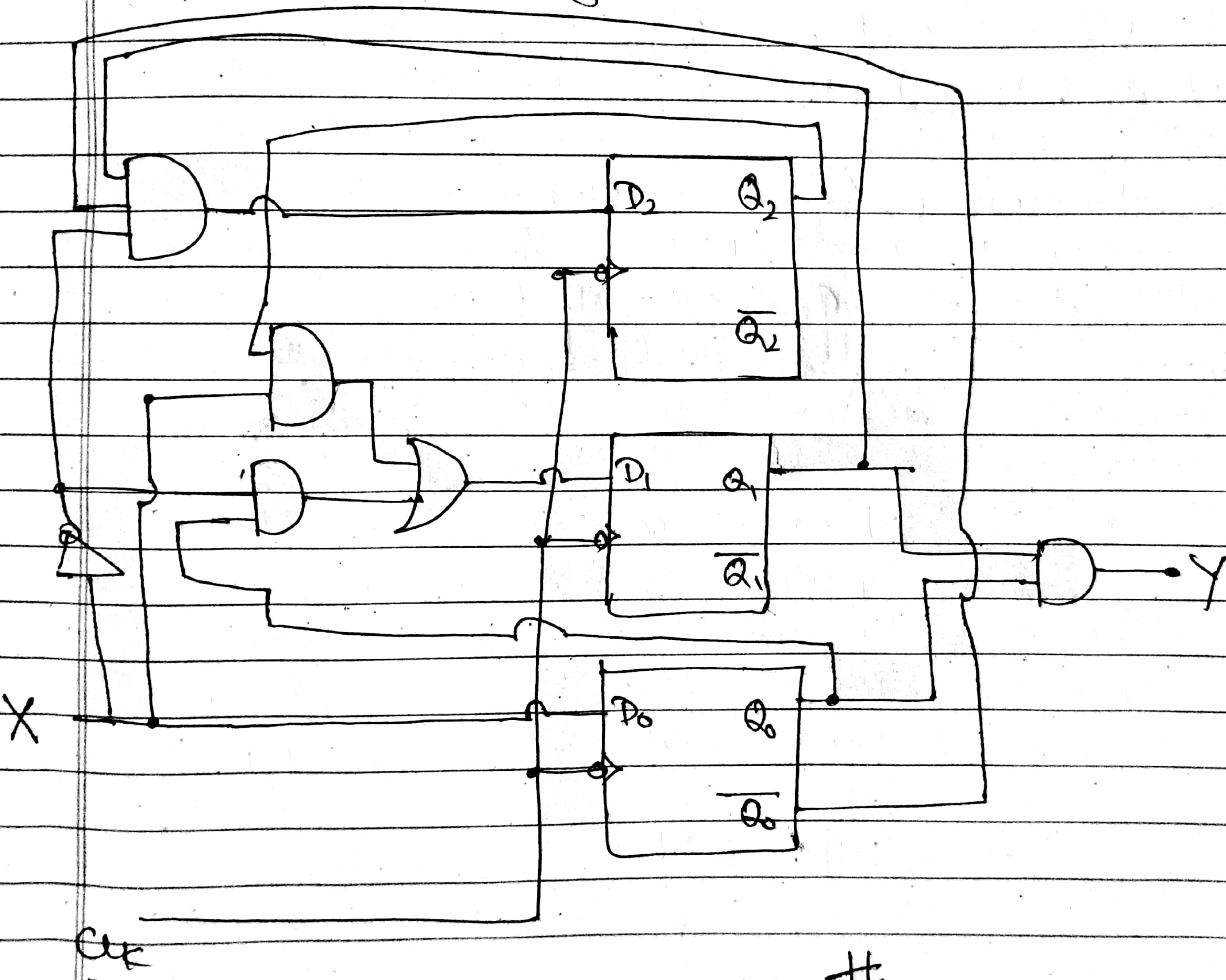
$D_2 = \overline{X}\, Q_1 \overline{Q_0}$

$D_1 = \overline{X}\, Q_0 + X Q_2$

$D_0 = X$

$Y = Q_1 Q_0$

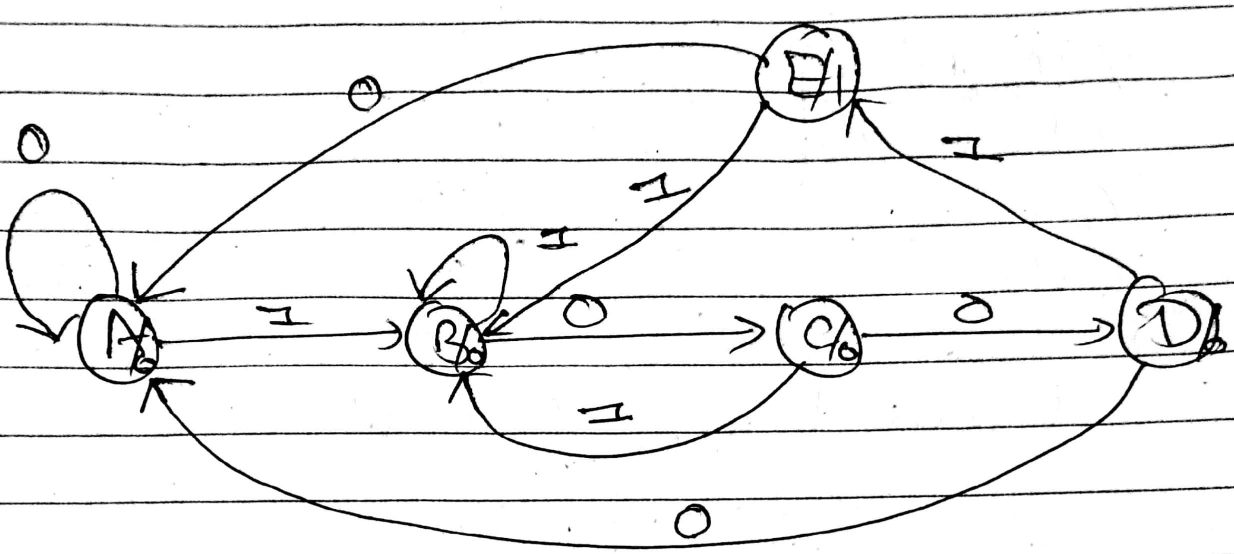
Step (7) Draw Logic Circuit.



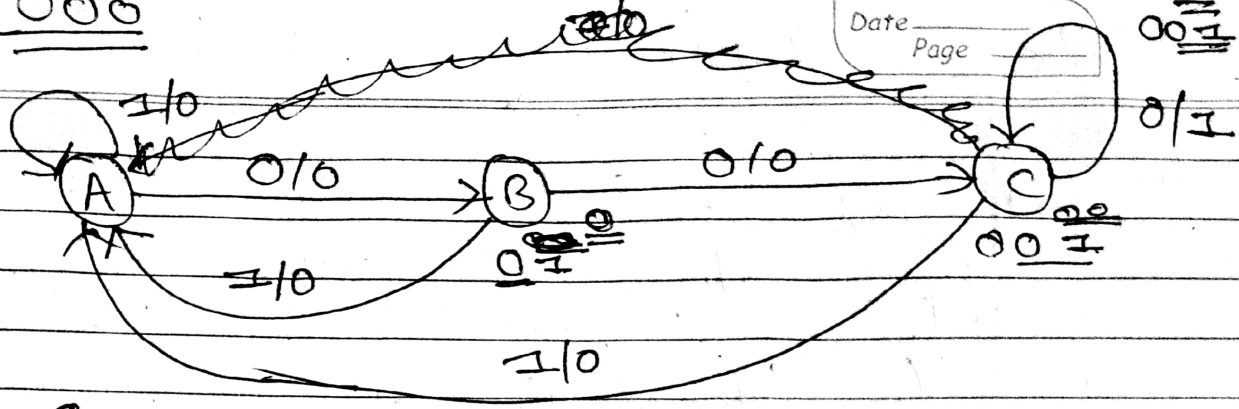
#

Date
Page

For Non-overlapping

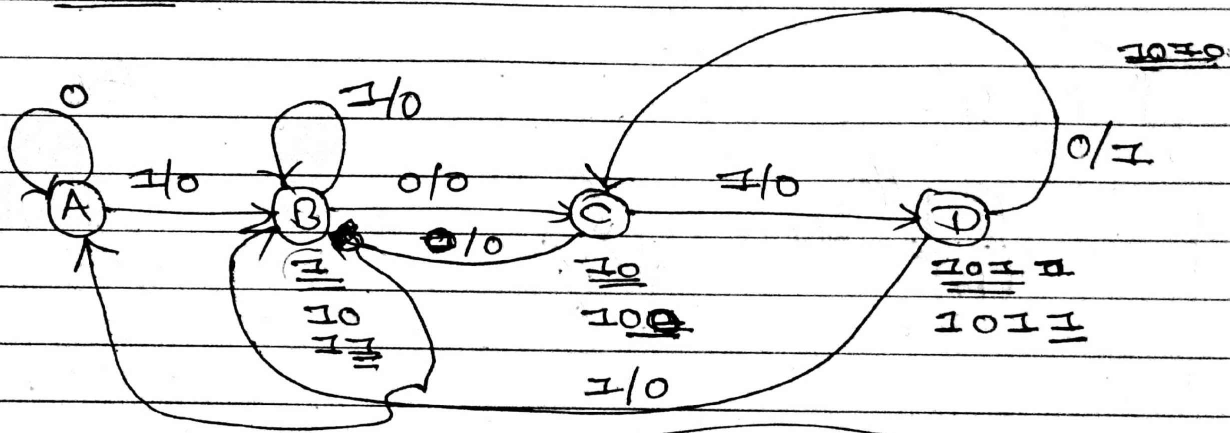


'000'

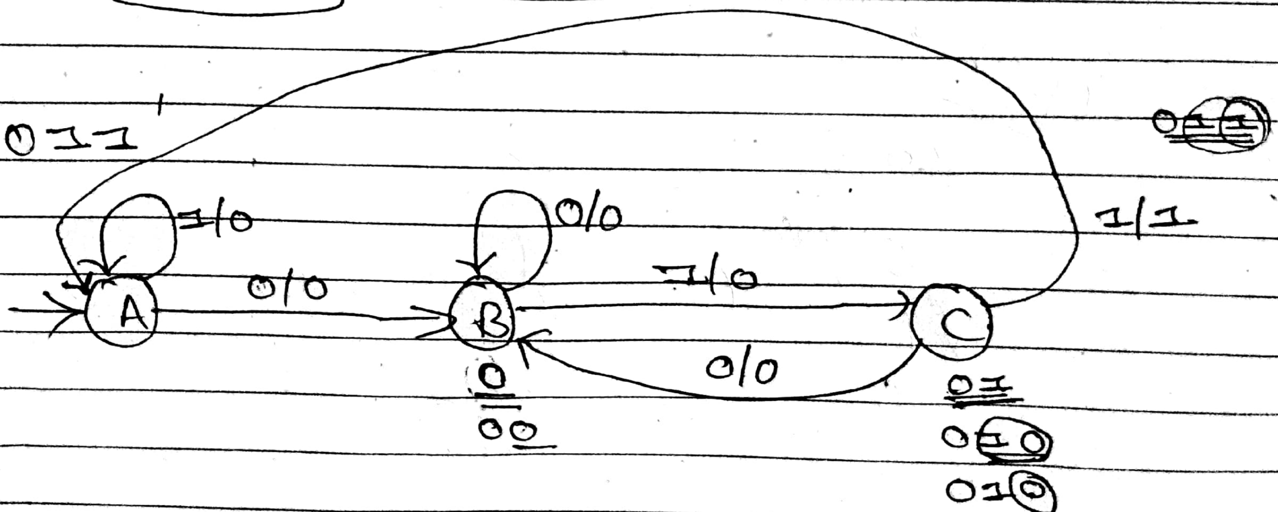


78-Bhadra

1010

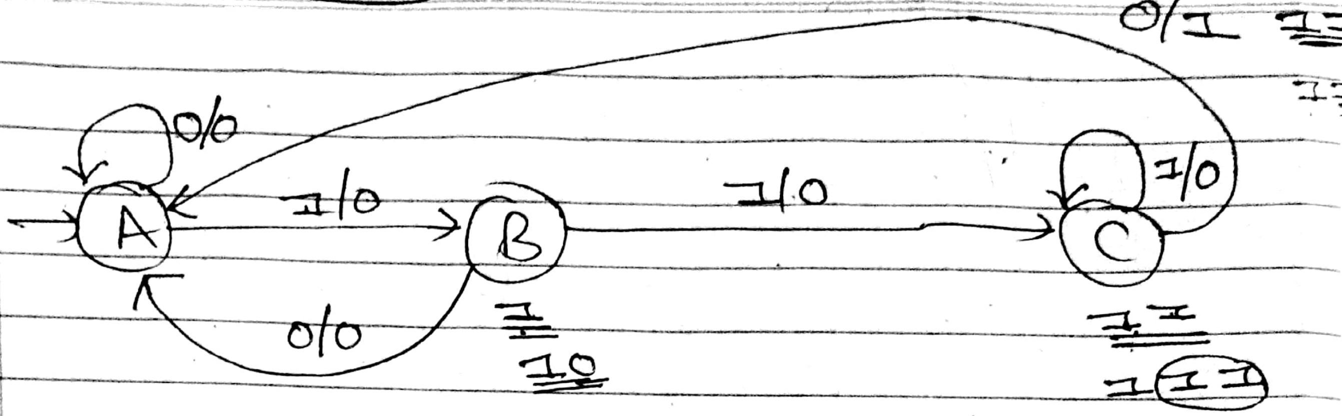


'011'

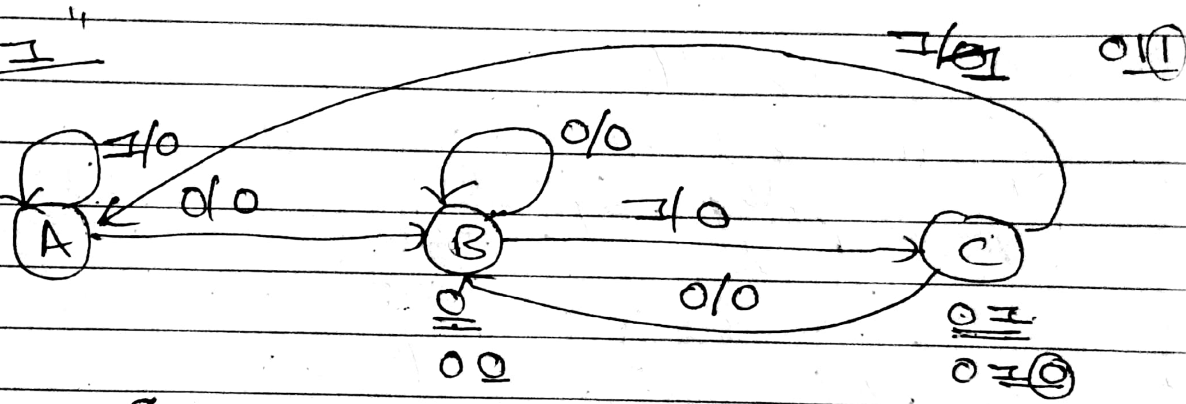


Date
Page

110

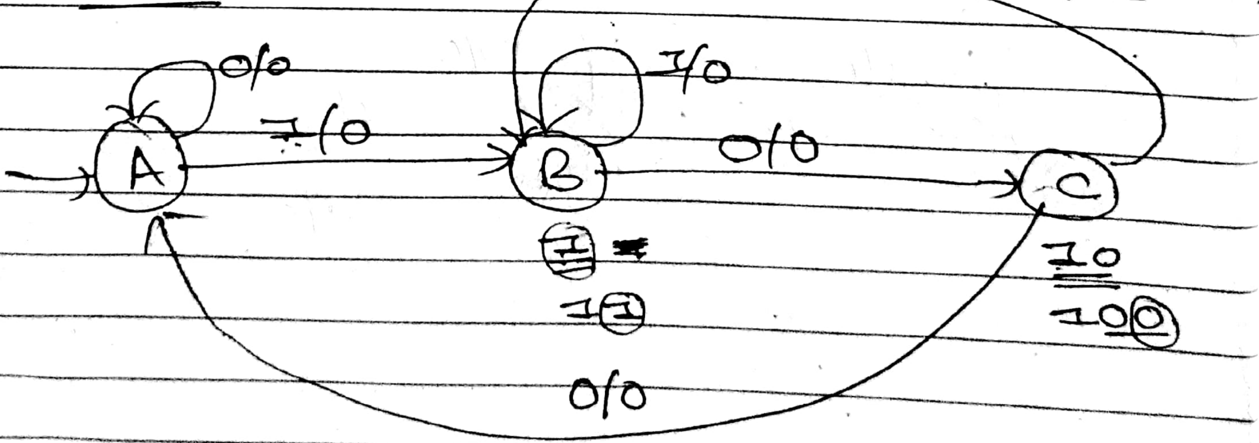


"011"



Tg-Bhadra

101



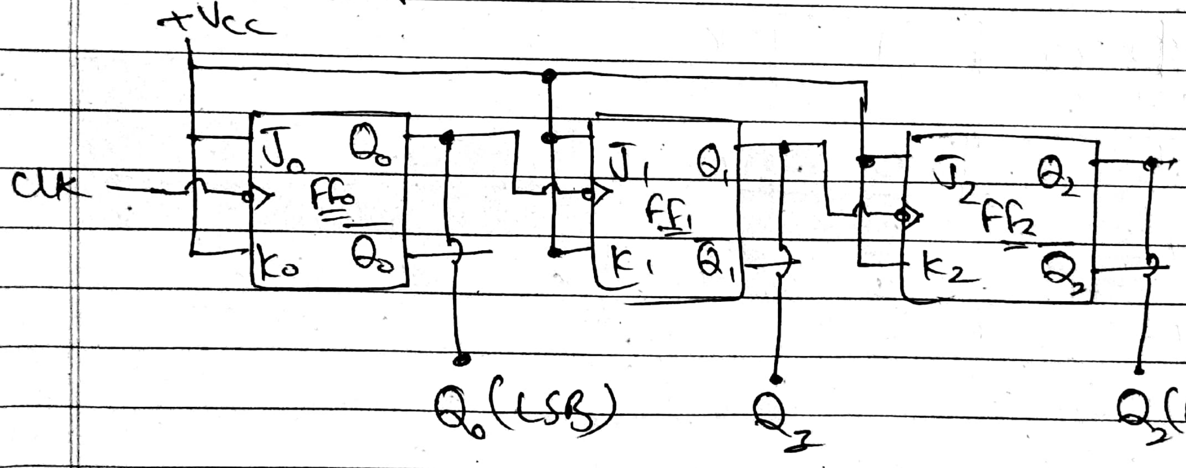
Counters

→ Combination of flip flops that performs counting operation.
→ Seq. ckt that passes through predefined states.

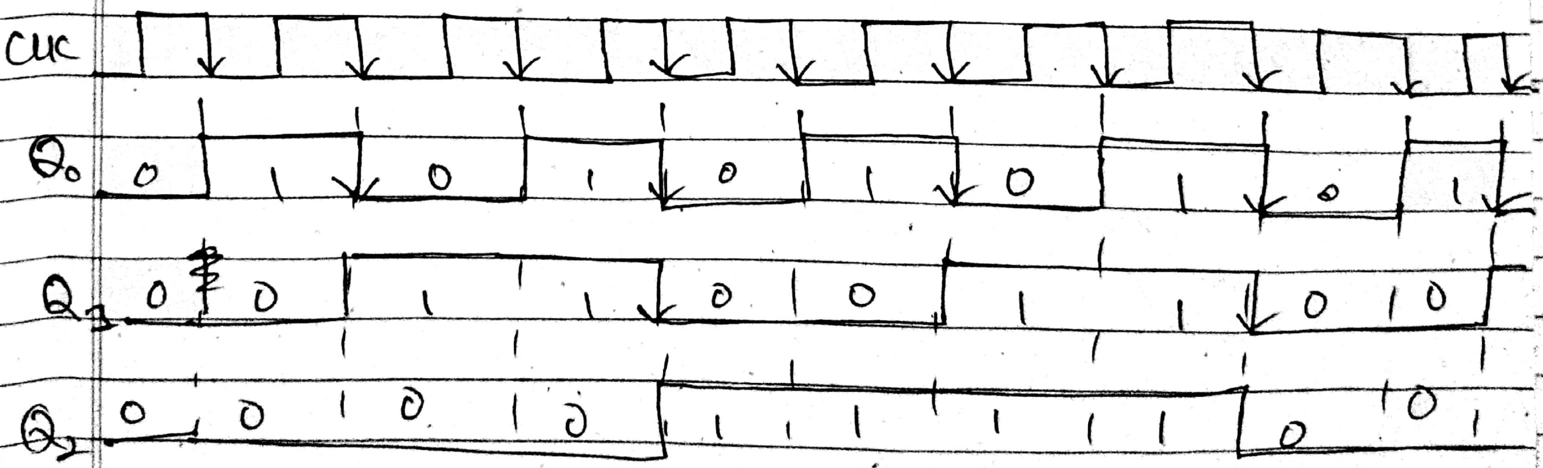
(i) Asynchronous (ripple) counter
(ii) Synchronous counter.

(i) Asynchronous counter.

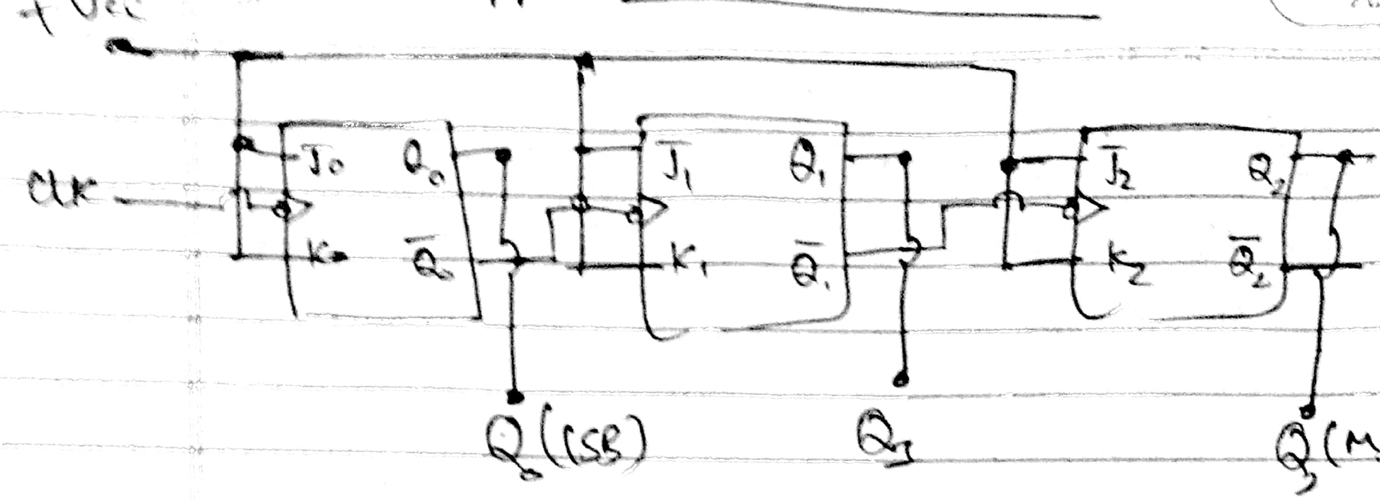
3-bit up-counter.



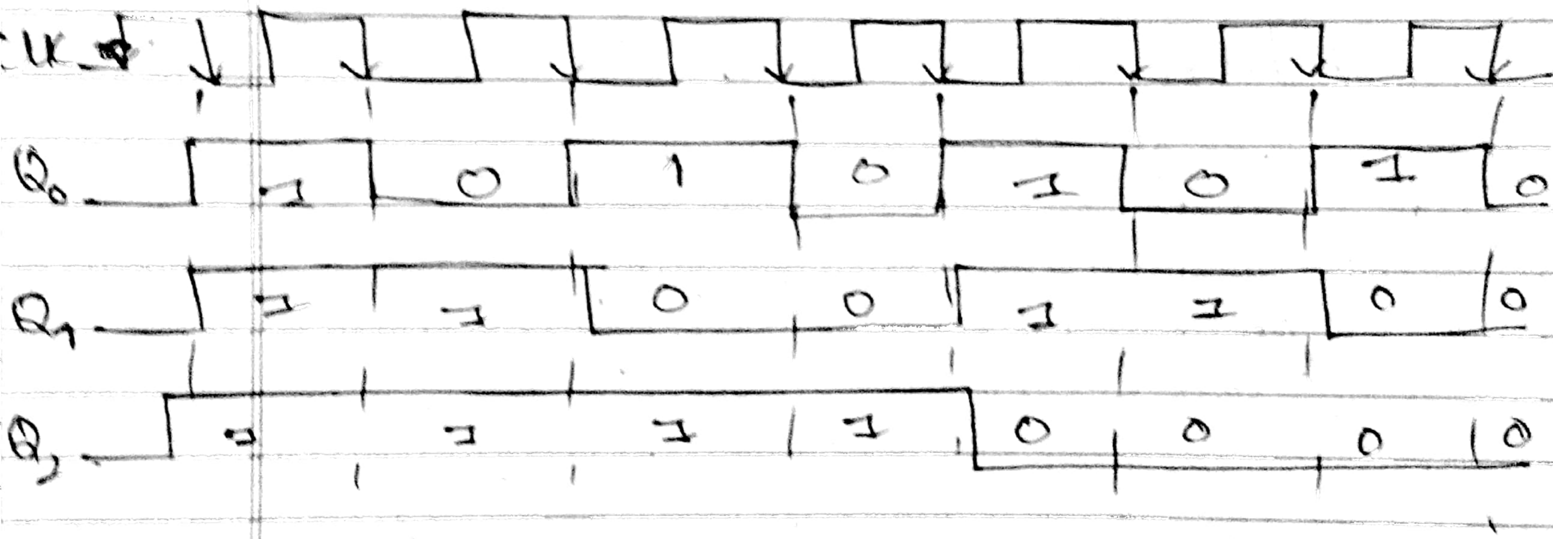
3-bit ripple up-counter.



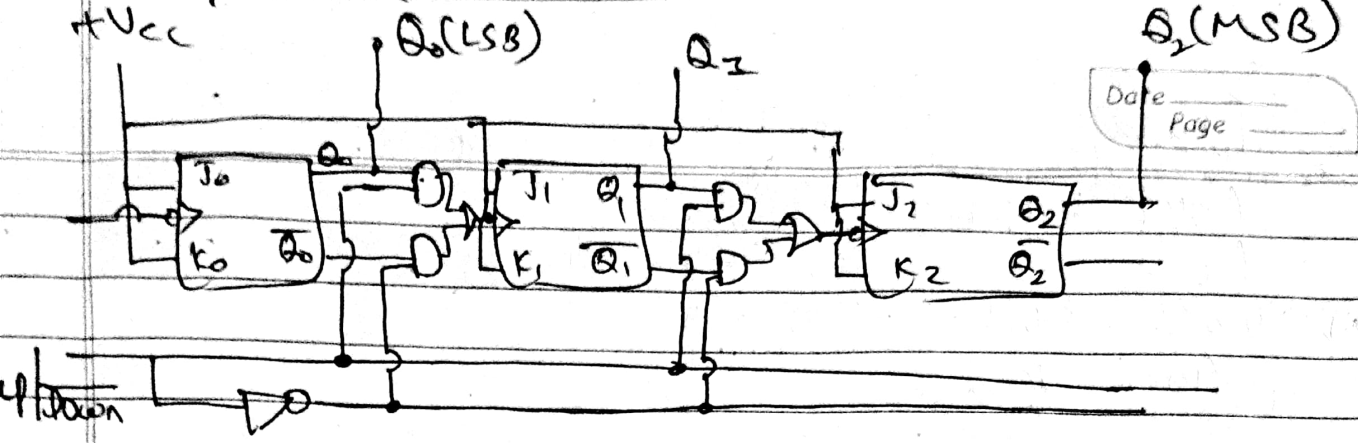
3-bit ripple down counter



3-bit ripple down counter.



up-down Counter



Decoding gates.

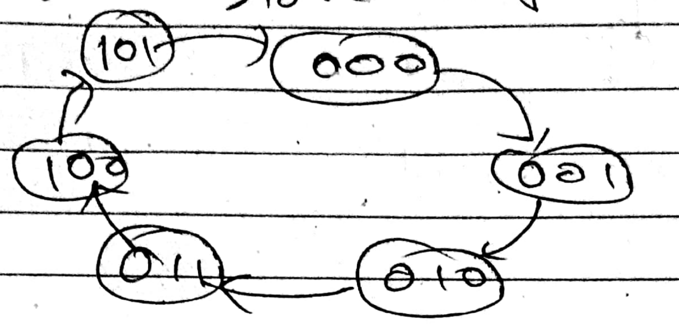
→ Decoding gate can be connected to o/p of counter in such a way that o/p of ~~given~~ gate will be high or low only when ~~counter~~ contents are equals to given state.

eg: decoding gate connected to 3 bit ripple counter in fig will decode state '7' ($Q_2Q_1Q_0$ = 111). The gate will be high when $Q_2 = 1$, $Q_1 = 1$, $Q_0 = 1$ #

Date ______
Page ______

Q. Design a Mod-6 up counter (synchronous)
(i.e 6-state counter)

Step 1: Draw state diagram.



0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

fig state diagram.

Step ② & ③. Next state table & excitⁿ table.

PS.			NS.			FF' excitation.					
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	0	X	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1

110 111

Step-4

J_2

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_2 = Q_1 Q_0$; $K_2 = Q_0$

$J_1 = \overline{Q_2} Q_0$ $K_1 = Q_0$

$J_0 = 1$ $K_0 = 1$

Step-5

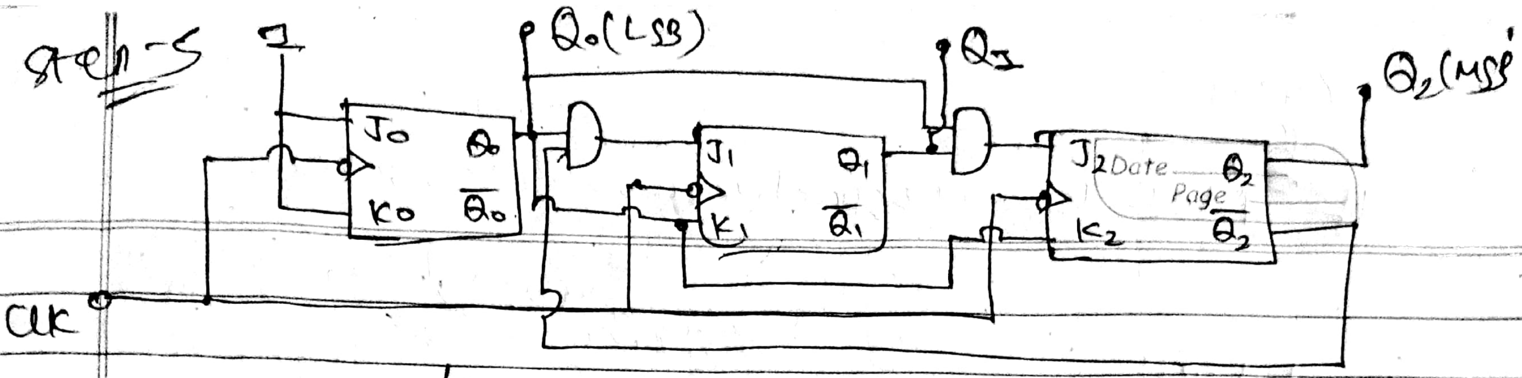
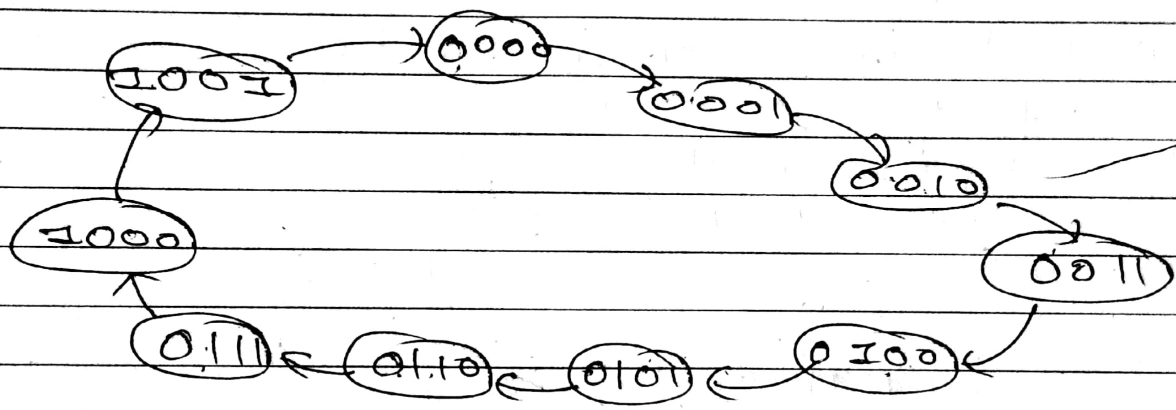


fig: Mod-6 Synchronous up-counter

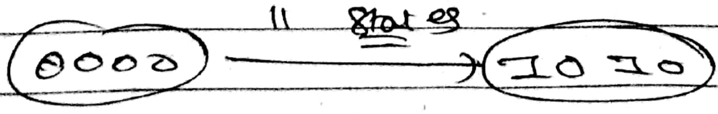
Q. Design synchronous Mod-10 up-counter.



PS NS FF - excitation.

Q. Mod-5 up counter.

Q. Mod 11 counter



Q Mod-12 asynchronous counter

(1, 2, 3, 10, 11) ← 3

\# 6 ← 3 { 3

2074 · Ashwin

Q Design 3-bit synchronous counter which follows gray code sequence.