A Low-Noise Output Capacitorless Low-Dropout Regulator With a Switched-*RC* Bandgap Reference

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***Abstract*—Low-noise linear regulators are critical for power supply regulation of noise-sensitive circuits, such as ADCs, phase-locked loops, and other mixed-signal/RF system-on-a-chip designs. A low-noise low-dropout (LN-LDO) regulator using switched-*RC* bandgap reference and a multiloop, unconditionally stable error amplifier for output capacitorless operation is presented in this paper. A sample-and-hold switched-*RC* filter is developed to reduce the noise of the bandgap reference and drain-side modulated current-mode chopping technique is proposed to reduce the flicker (1/*f*) noise of the error amplifier. A switched capacitor notch filter is utilized to filter out the residual chopping ripple of the error amplifier. Thermal noise of the current reference circuit which is significant at such low noise levels is also reduced by using a low-area penalty passive *RC* filter. These techniques reduce the total integrated output noise of the LDO in the 10 Hz to 100 kHz band from $95.3\ \mu\mathrm{V_{RMS}}$ down to $14.8\ \mu\mathrm{V_{RMS}}$. The LDO delivers a maximum load current of 100 mA with a dropout voltage of 230 mV and a quiescent current consumption of $40\ \mu\mathrm{A}$. It achieves a power supply rejection of 50 dB at 10 kHz for a programmable output voltage range of 1–3.3 V. Fabricated in a $0.25\ \mu\mathrm{m}$ CMOS process, the LDO core occupies an area of 0.18 mm^2.**

***Index Terms*—Bandgap reference, chopping, flicker noise, low dropout (LDO) regulator, low noise (LN), notch filter, power management circuits, switched-*RC*.**

I. Introduction

LOW-DROPOUT (LDO) regulators are widely used in power supply regulation of RF, analog, and mixed-signal applications because of their low noise and high power supply rejection (PSR) capabilities. With the increasing demand for portable battery-operated devices, low quiescent current (I_{Q}) consumption and low dropout voltage specifications are gaining importance for high-efficiency operation of LDOs in state-of-the-art low-supply regime processes. However, decreasing the I_{Q} slows down the response time of the LDO to load current transients and also increases its thermal noise. Several state-of-the-art system-on-a-chip (SOC) designs with embedded high precision analog to digital converters (ADCs), phase-locked loops, and other RF circuits require require low-noise LDOs (LN-LDOs) for their power supply regulation. Design of such LN-LDOs with low I_{Q} and small die area is challenging and demands design innovations to reduce noise while maintaining a competitive transient response, PSR, and efficiency.

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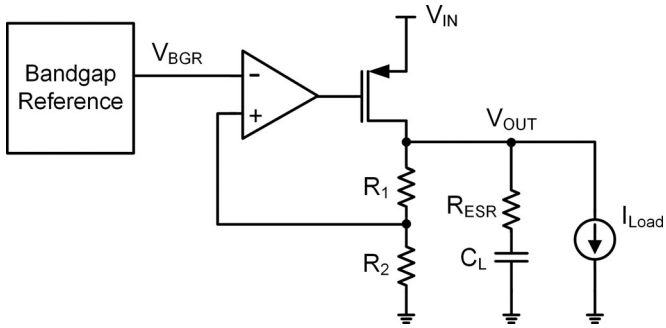

Fig. 1. Block diagram of a conventional LDO.

Fig. 1 shows the block diagram of a conventional LDO consisting of a bandgap reference, an error amplifier, a pass transistor, a resistive feedback network, and an output capacitor. The total output noise power spectral density (PSD) of this LDO, $N_{\mathrm{OUT}}(f)$ is given by

$$N_{\mathrm{OUT}}(f) = \left(N_{\mathrm{BGR}}(f) + N_{\mathrm{EA}}(f)\right)\left(1+\frac{R_1}{R_2}\right)^2 + N_{R2}(f)\left(\frac{R_1}{R_2}\right)^2 + N_{R1}(f) \tag{1}$$

where $N_{\mathrm{BGR}}(f)$ is the output noise PSD of the bandgap reference, $N_{\mathrm{EA}}(f)$ is the input referred noise PSD of the error amplifier, and $N_{R_1}(f), N_{R_2}(f)$ are the noise PSD of resistors R_1 and R_2, respectively. Noise of the regulation FET can be neglected due to its large gate area and high transconductance.

Noise of the bandgap reference which comprises of thermal noise, shot noise, and flicker (1/*f*) noise is typically reduced by low-pole passive *RC* filtering with a cutoff frequency less than 1 Hz, which is often achieved using a large external capacitor, taking up board space and increasing component count. Prior work in LN-LDOs have implemented an *RC* filter using high-density on-chip resistors greater than $100\ \mathrm{M\Omega}$ [1] or a long-channel MOS transistor biased in deep subthreshold region to get a high resistance of $1-100\ \mathrm{G\Omega}$ [2] along with the on-chip capacitor larger than 100 pF, all of which occupy a significant die area. Noise from LDO's output feedback-network resistors was reduced by using a scaling amplifier at the output of bandgap reference and filtering out its noise along with the noise of bandgap reference in [1], [2]. Thermal noise of the error amplifier was reduced by increasing the transconductance $\mathrm{g_m}$ of

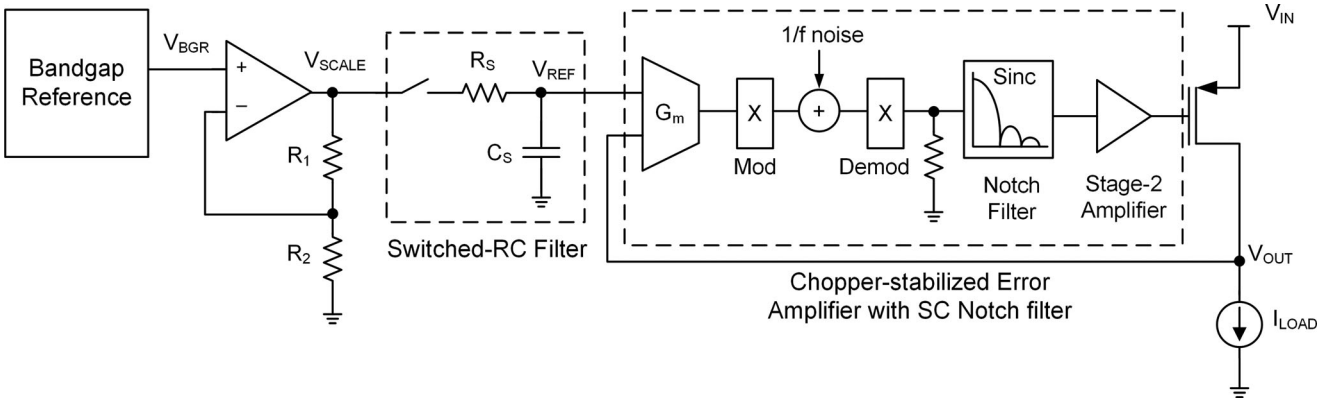

Fig. 2. Block diagram of the proposed low-noise LDO: noise of scaled bandgap reference is reduced using a switched-*RC* filter, whereas chopper-stabilized error amplifier is utilized for lower flicker noise.

the input transistors, whereas flicker noise is reduced by using large-area devices in [3]. A low-flicker noise chopper-stabilized LDO was proposed in [4], but it has high-output ripple at chopping frequency and requires a low noise bandgap reference.

An LN-LDO that reduces noise from all the major contributors, which includes bandgap reference, error amplifier, feedback resistors, and bias circuit is presented in this paper. Output capacitorless LDO regulators are becoming increasingly popular [5]–[11], as they minimize the number of external components and reduce manufacturing cost. In the proposed LN-LDO, a two-stage multiloop, unconditionally stable error amplifier for output capacitor-free stability and fast transient response is presented. Drain-side-modulated current-mode chopping is proposed to reduce the flicker noise of the error amplifier. In chopper-stabilized gain stages, due to mismatches in timing, and dc offsets, a residual ripple is formed at the chopping frequency. In the proposed architecture, the residual ripple due to chopping is reduced by using a switched capacitor (SC) notch filter. Thermal noise of current reference circuit, which is significant at such low-target noise levels, is reduced using a low-area penalty passive *RC* filter. A sample-and-hold (S/H)-based switched-*RC* filter is proposed to reduce the noise associated with the bandgap voltage reference and scaling amplifier. This is the first application of switched-*RC* filter to reduce the overall noise of bandgap reference along with drain-side modulated current-mode chopping for flicker noise reduction of error amplifier and passive filtering of bias circuit thermal noise. Using the proposed techniques, integrated noise in the frequency band of 10 Hz to 100 kHz is reduced from a nominal value of $95.3\ \mu\mathrm{V_{RMS}}$ down to $14.8\,\mu\mathrm{V_{RMS}}$.

The rest of the paper is organized as follows: analysis and design of switched-*RC* bandgap reference, multiloop error amplifier with current-mode chopping and ripple reduction, and bias circuit noise filter is presented in Section II. Silicon measurement results are presented in Section III, and Section IV concludes the paper.

II. Proposed LDO Architecture

A. Switched-RC Bandgap Reference

Fig. 2 shows the block diagram of the proposed LN-LDO, where the error amplifier is used in unity gain configuration. In order to set the regulator output voltage, a bandgap reference voltage $\mathrm{V_{BGR}}$ is scaled prior to error amplifier using a scaling amplifier with a digitally adjustable resistor divider. The noise associated with the bandgap reference, scaling amplifier and its resistor divider is filtered using a S/H-based switched-*RC* filter. This filter emulates a large *RC*-time constant from a small resistor and capacitor by pulse-switching them [12]. If the *RC* low-pass filter as shown in Fig. 2 is switched with a pulse of duty cycle *D*, the effective time constant is given by $\tau_{\mathrm{eff}} = \frac{R_S C_S}{D}$ i.e., the effective filter pole frequency is $f_{\mathrm{LPF}} = \frac{D}{2\pi R_S C_S}$ [13]. The integrated noise at the output of the switched-*RC* filter is given by

$$N_{\mathrm{SWRC}}(f) = (N_{\mathrm{BGR}}(f) + 4kTR)\int_0^\infty \left|\frac{1}{1+s(RC_S/D)}\right| df \quad (2)$$

$$= \frac{N_{\mathrm{BGR}}(f)D}{4RC_S} + \frac{kTD}{C_S} \quad (3)$$

where $N_{\mathrm{BGR}}(f)$ is the combined noise PSD of the bandgap reference and scaling amplifier, duty cycle $D = \frac{T_S}{T_S+T_H}$, $R = R_{O,\mathrm{BGR}} + R_{SW} + R_S$, where $R_{O,\mathrm{BGR}}$ is the output impedance of the scaling amplifier, R_{SW} is the switch resistance, and R_S is the filter resistance. Thus, the output noise is suppressed by a factor of duty cycle *D* and with $C_S = 10\,\mathrm{pF}$, $R_S = 25\ \mathrm{M\Omega}$, and $D = 0.01\%$ (i.e., $T_S = 10\,\mu\mathrm{s}$ and $T_S + T_H = 100\ \mathrm{ms}$), an effective filter pole frequency of $\sim$0.1 Hz can be achieved. This is two decades lower than the noise integration bandwidth (10 Hz–100 kHz) of the proposed LN-LDO, providing a low noice reference voltage. Moreover, such a low cutoff frequency also improves the PSR of the overall LN-LDO by filtering out the power supply-induced ripple from the reference voltage.

Fig. 3 shows the circuit implementation of the switched-*RC* S/H filter along with the control clock timing. In the proposed LN-LDO, a PMOS current-feedback-based bandgap reference is used to generate the reference voltage. To achieve a high-*RC* filtering resistance of 25 MΩ with a low-die area impact, a subthreshold region MOS resistor (M3) biased with a 50 nA current source is used. Since the accuracy of the reference voltage directly determines the accuracy of LN-LDO output voltage, it is important to mitigate the effects of error sources like charge

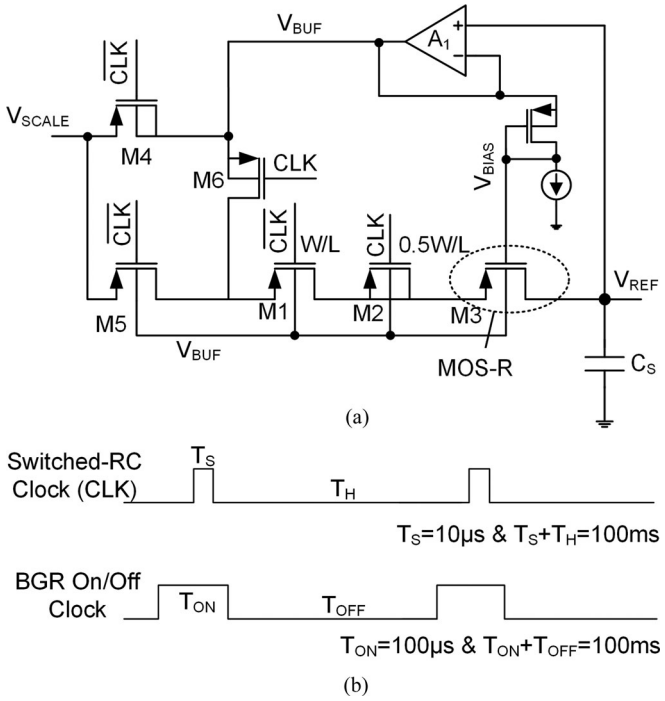

Fig. 3. (a) Proposed switched-*RC* S/H reference voltage circuit. (b) Control clocks for bandgap power cycling and switched-*RC* operation.

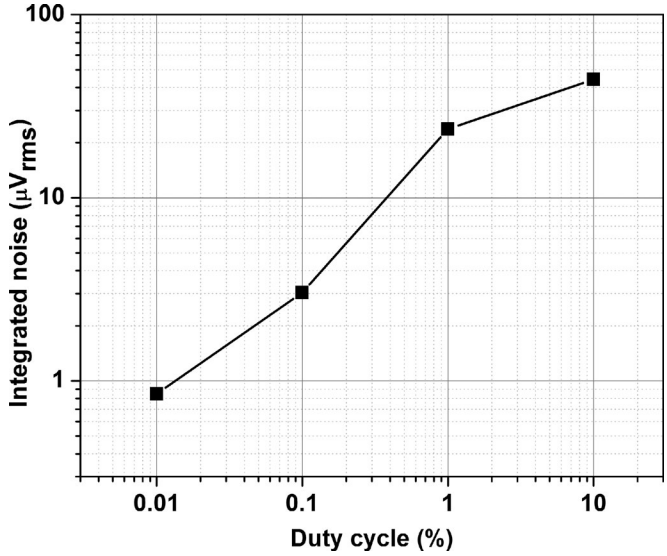

Fig. 4. Integrated noise of switched-*RC* bandgap reference integrated in 10 Hz to 100 kHz band for different duty cycle (*D*).

injection and clock feedthrough on the S/H circuit. A dummy MOS switch M2 with half the size of the actual switch M1 and drain-source shorted, is added in series with M1 to mitigate the channel charge injection effect. It is controlled by a complementary clock compared to that of M1. As M1 turns OFF and M2 turns ON, half of the channel charge from M1 is pushed towards the dummy device M2, where it is completely compensated by the induced channel. However, when M2 turns OFF, since its drain and source are shorted, all of the channel charge in M2 will be injected into the low-impedance scaling amplifier present at the output of the bandgap without affecting the held reference voltage at $\mathrm{C_S}$. Thus, dummy switch M2 cancels the overall charge injection in both clock phases.

Due to the long-hold time $T_{\mathrm{H}} = 100$ ms, charge leakage at $\mathrm{C_S}$ which is dominated by the drain–bulk and drain–source junction leakage of the MOS resistor (M3) and switches (M1, M2), can cause a voltage drop in $\mathrm{V_{REF}}$ which affects the LDO output accuracy during the hold periods. Junction leakage, which is proportional to drain-to-bulk $\mathrm{V_{DB}}$ and drain-to-source $\mathrm{V_{DS}}$ voltages of these transistors, is reduced by using a low-power, low-bandwidth buffer amplifier $\mathrm{A_1}$ to buffer $\mathrm{V_{REF}}$ to bulk and source nodes through M6 in the hold phase as shown in Fig. 3 [14]. This approach limits the $\mathrm{V_{DB}}$ and $\mathrm{V_{DS}}$ of switch M1 to the input offset voltage of $\mathrm{A_1}$. All the switches are implemented using PMOS such that their bulk terminals can be biased to $\mathrm{V_{REF}}$ to reduce the charge leakage at $\mathrm{C_S}$ during hold phase. Fig. 4 shows the simulated noise of the switched-*RC* bandgap reference integrated in $10\,\mathrm{Hz} - 100\,\mathrm{kHz}$ frequency band, which shows a two orders of magnitude noise reduction by reducing the duty cycle (*D*) from 10 to 0.01%.

During hold phase, both the bandgap reference and scaling amplifier are turned OFF to reduce the overall I_{Q}. They are enabled before the sampling phase such that the bandgap reference and scaling amplifier are turned ON and their output $\mathrm{V_{SCALE}}$ is settled before it is sampled. This power cycling reduces the average I_{Q} consumption of the bandgap reference and scaling amplifier to 10 nA. The ON/OFF timing of the bandgap reference and scaling amplifier with respect to the switched-*RC* control clock is shown in Fig. 3. Due to the *RC* charging delay associated with the very low-frequency pole of the switched-*RC* filter, it is bypassed during startup to avoid long startup time.

B. Chopper-Stabilized Error Amplifier

A two-stage unconditionally stable error amplifier as shown in Fig. 5 is designed for output capacitorless operation of the LDO. The high-gain first stage is a folded cascode amplifier with NMOS input pair MN1–MN2, folded cascode MP1–MP4, and MN5–MN8. For output accuracy, this amplifier stage is designed to have a gain higher than 60 dB and a single-pole frequency response for load capacitance $\mathrm{C1}(= 5\ \mathrm{pF})$. Output load regulation is further improved by using a second-stage consisting of two loops: MP5, MP7, and MN11 for pull-up and MP5, MN9, and MN12 for pull-down capability. In a multiloop circuit, a sufficient (although not necessary) condition for stability is the stability of every constituent loop [15]. Since all the loops are ensured to have a single-pole response for any output load capacitor, the overall error amplifier is unconditionally stable. Simulated loop magnitude and phase response plot for this capacitorless LN-LDO for different load currents is shown in Fig. 6. It can be seen that the phase margin is always greater than 75° with a unity gain frequency of ∼20 kHz for all load conditions. Additionally for this multiloop LDO, simulation results for transient response to load step/staircase input with different values of load capacitance is also shown in Fig. 7 to show that

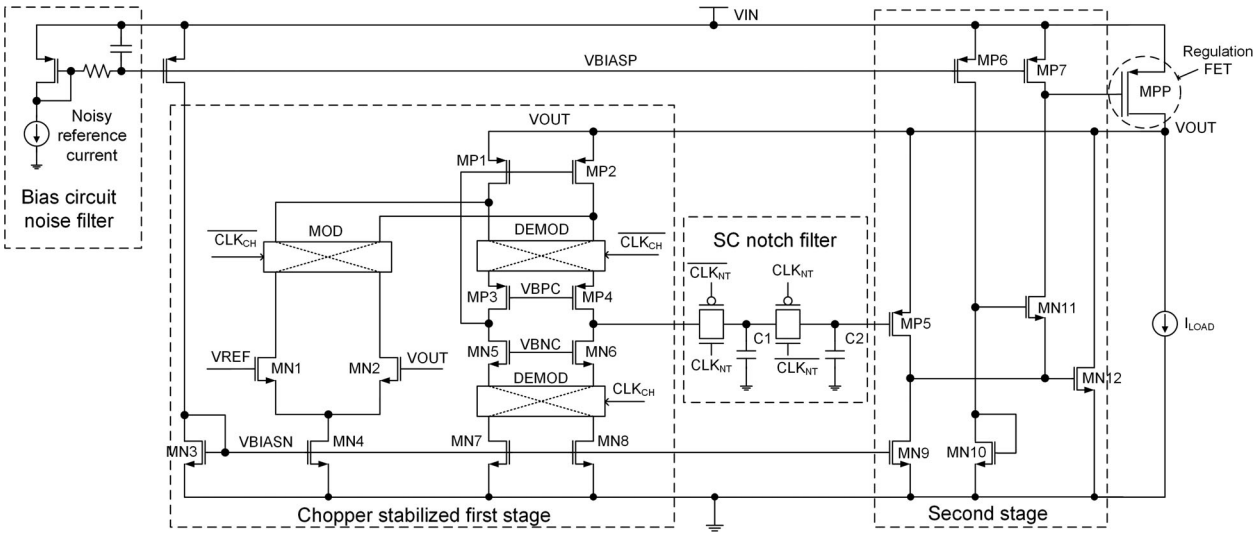

Fig. 5. Low-noise current-mode chopper-stabilized multiloop error amplifier, along with an SC notch filter for ripple reduction and bias circuit noise filter.

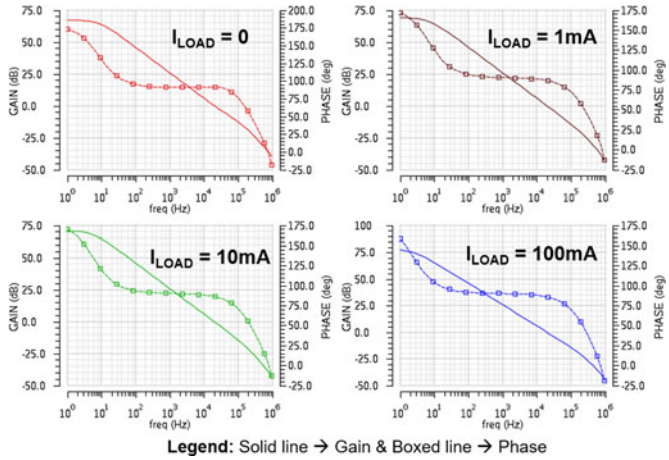

Fig. 6. Simulated loop magnitude and phase response at different load currents for $C_{LOAD} = 0$ obtained using periodic stability simulation.

the overall LDO is unconditionally stable for different load current and capacitor conditions. This error amplifier is powered using the LN-LDO output itself to achieve high PSR at low frequencies. However, this could result in a long-startup time for the LDO due to self-regulation of its supply voltage. To avoid this, a clamp is used to ensure proper gate voltage at the gate of the regulation FET MPP during startup so that the output voltage increases initially until the error amplifier turns ON and starts regulating the LN-LDO output. Moreover, clock buffers driving the chopping switches are also powered by LN-LDO output to reduce the chopping ripple during normal operation.

From noise perspective, the first stage of the error amplifier is the dominant noise contributor and it is important for it to have low noise. Conventionally, the dominant flicker (1/*f*) noise in a folded cascode amplifier is removed using chopping technique with the modulator placed before the gate of the input pair and the demodulator at the folding node [4]. In the proposed LN-LDO, since V_{REF} is held on a storage capacitor C_S for a hold time up to 100 ms, if the chopping modulator is connected to this node it would cause charge leakage and voltage drop in the V_{REF} node. To avoid this, a modified drain-side modulated current-mode chopping technique is proposed where the chopping modulator is placed at the drain of the input pair (MN1 and MN2) modulating in current domain as shown in Fig. 5. The demodulation is also performed in current domain at low-impedance nodes after the PMOS load (MP1 and MP2) and NMOS current sources (MN7 and MN8). This technique modulates the flicker noise due to major contributors MP1, MP2, MN7, and MN8 to chopping frequency. Chopping frequency F_{CHOP} is chosen such that it is at least twice the noise integration bandwidth i.e., $F_{CHOP} \geq 2F_{HIGH}$. It also eliminates the need for degeneration resistance typically used with MP1 and MP2 to reduce their flicker noise and thus increases the available headroom for low-supply voltage design. However, since modulation is performed after the input pair, flicker noise of MN1 and MN2 is not modulated and determines the lower noise limit of this LN-LDO. As mentioned earlier, the chopping clock buffers are powered by LN-LDO output. However, during startup, this results in high resistance for the chopping switches which are driven by low-gate drive voltage and results in long startup time. To avoid this, chopping switches are bypassed during startup.

An undesirable effect of chopping is the residual chopping ripple which can cause periodic inaccuracies in the LDO output. An SC notch filter employed to reduce this ripple is discussed in Section C. Reduction of current bias circuit noise which is significant at such low-target noise levels is discussed in Section D. Overall startup process with clock timing is presented in Section E.

C. Chopping Ripple Reduction Circuit

An SC notch filter placed at the output of the first stage of the error amplifier, immediately after demodulation as shown in Fig. 5 reduces the chopping ripple before transferring the signal to the second stage. It consists of two capacitors (C1 and C2) and

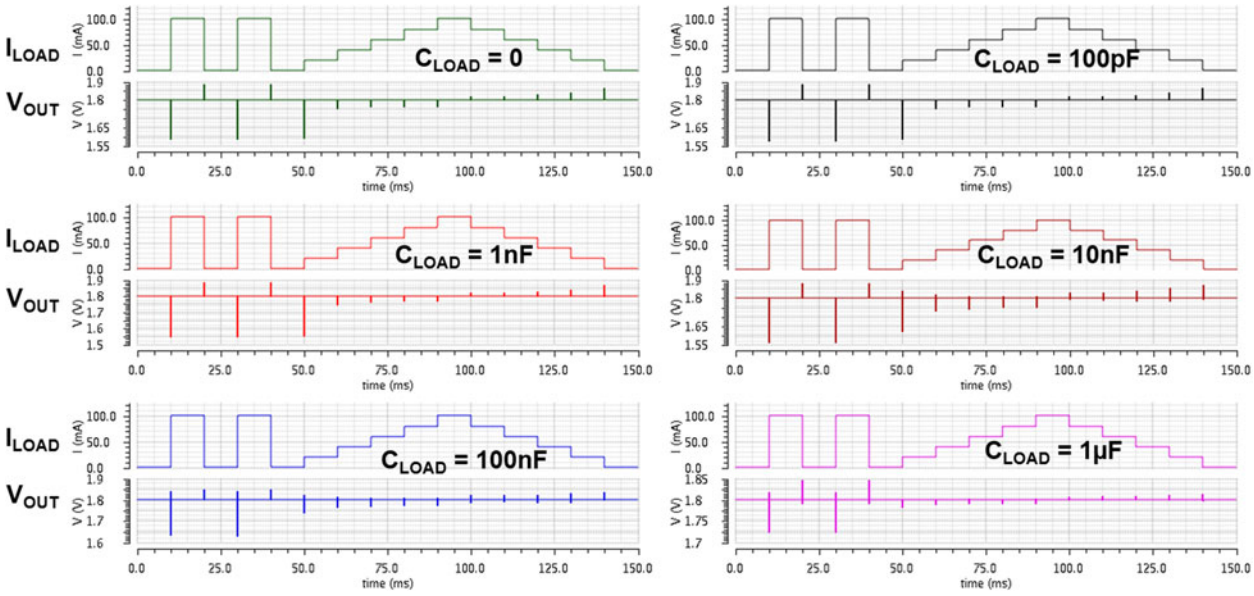

Fig. 7. Transient simulation of LN-LDO for load current step/staircase (slew rate: $100\ \mathrm{mA}/\mu\mathrm{s}$) at different load capacitance values.

two transmission gates (TG1 and TG2). A 90° delayed notch clock ($\mathrm{CLK_{NT}}$) compared to the chopping clock ($\mathrm{CLK_{CH}}$) but with same frequency F_{CHOP}, controls TG1 and TG2. This filter works on the principle of data hold circuit, where the voltage is sampled onto C1 during phase Φ1. This ripple-free sampled voltage is passed onto C2 during phase Φ2 [16].

The time domain response $y(t)$ for an input $x(t)$ for this filter can be given as

$$y(t) = \sum_{k=0}^{\infty} x(kT) * [u(t-kT) - u(t-(k+1)T)] \qquad (4)$$

where $T = \frac{1}{F_{CHOP}}$.

Applying Laplace transform on (3) gives

$$Y(s) = \sum_{k=0}^{\infty} x(kT) \frac{e^{-skT} - e^{-s(k+1)T}}{s}$$
$$Y(s) = \frac{1-e^{-sT}}{s} \sum_{k=0}^{\infty} x(kT) e^{-skT} = \frac{1-e^{-sT}}{s} * X(s). \qquad (5)$$

Re-writing for the transfer function of the filter $H(s)$ from (4), we get

$$H(s) = \frac{Y(s)}{X(s)} = \frac{1-e^{-sT}}{s} \qquad (6)$$

The magnitude response of this filter can be obtained by substituting $s = j\omega$ in (5)

$$|H(j\omega)| = \left| \frac{1-\cos(\omega T) + j\sin(\omega T)}{j\omega} \right| \qquad (7)$$

Thus, $|H(j\omega)| = 0$ for all $\omega = n * \frac{2\pi}{T} = n * 2\pi F_{\mathrm{CHOP}}$, where n is an integer. Transient simulation showing the response of the notch filter along with the control clocks is shown in Fig. 8(a). The input ripple of 2 mV (p–p) is reduced to $6\,\mu$V (p–p). A periodic steady state frequency response of this notch filter is shown in Fig. 8(b) which shows distinct notches at F_{CHOP} and its harmonics. The value of capacitance C2 can be greater than or equal to C1, but was chosen to be twice as that of C1 ($= 5$ pF decided by the error amplifier first stage) to minimize the effects of clock

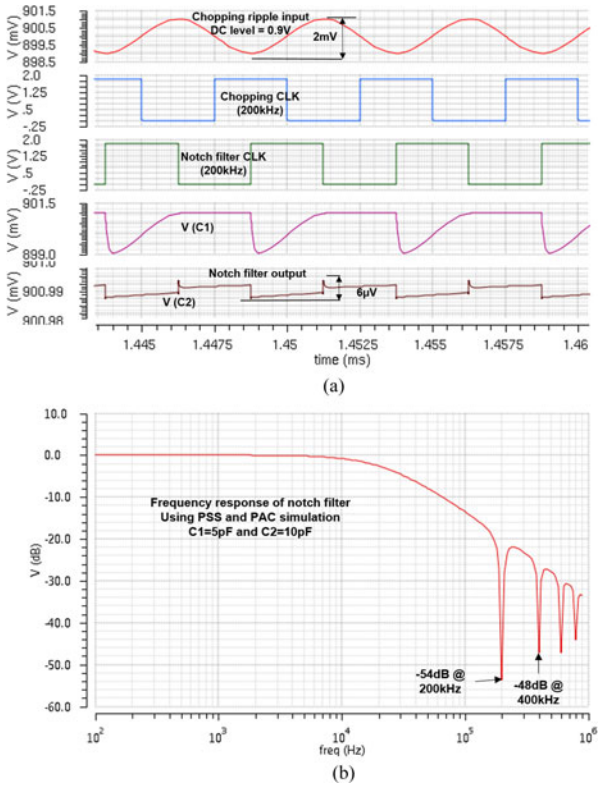

Fig. 8. (a) Simulated transient response of the SC notch filter for input chopping ripple of 2 mV (p–p) along with control clocks. (b) Simulated frequency response of the SC notch filter.

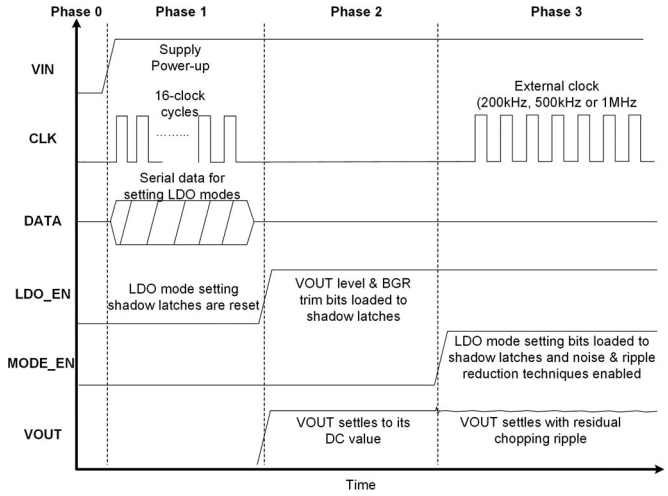

Fig. 9. Startup timing and configuration of noise and ripple reduction modes.

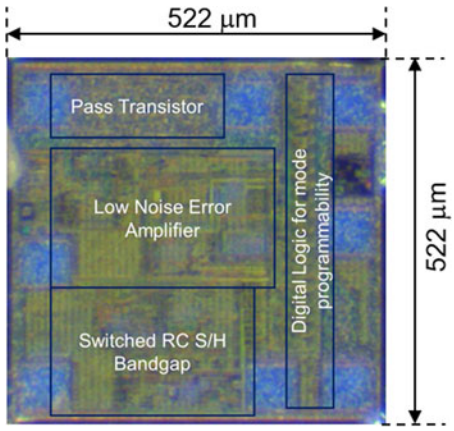

Fig. 10. Die micrograph of LN-LDO regulator.

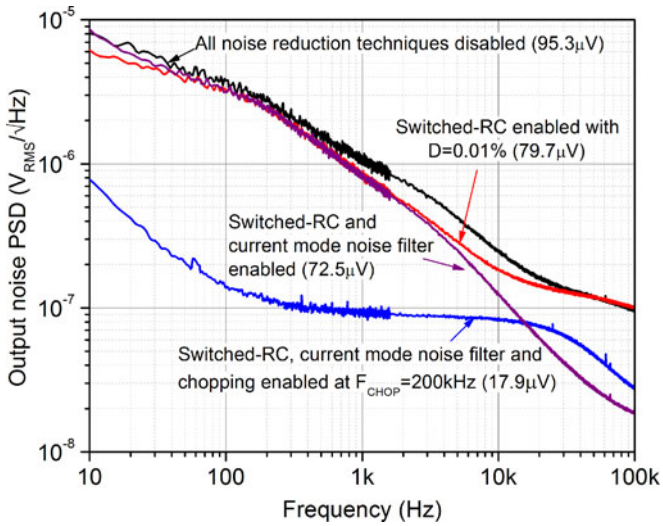

Fig. 11. Measured output noise with different noise reduction techniques enabled.

feedthrough by having a bigger load capacitance C2 ($= 10$ pF). Even though S/H action of the notch filter introduces a delay in the circuit, this delay is very small to raise any stability concerns as the frequency of $\mathrm{CLK_{NT}}$ is much higher than 20 kHz. Chopping clocks and 90° delayed clocks for the SC notch filter are generated from the same external clock. To reduce ripple because of clock feedthrough, these clocks are driven by the output of the LN-LDO ($\mathrm{V_{OUT}}$) which is always at a lower voltage level compared to the input supply voltage.

D. Bias Circuit Noise Filter

The bias current for the error amplifier is typically generated using a constant-gm current reference (or bandgap reference voltage) and appears as a common mode noise for the first stage. Due to the inherent high-dc common mode rejection of the amplifier, this noise is suppressed near dc but as the common mode rejection reduces at frequencies close to F_{HIGH}, this noise contribution to the overall LDO noise increases. A first-order passive *RC* filter with a 5 MΩ polyresistor and 5 pF capacitor placed at the last voltage to current (*V–I*) converter of the bias current mirror, yields a pole location of 6.4 kHz and is implemented to suppress the bias current noise without significant area overhead.

E. Startup Timing

The startup timing of the LN-LDO is shown in Fig. 9. External clock pin (CLK), mode programming pin (DATA), and noise reduction mode enable pin (MODE_EN) are the additional test pins used in the prototype design. After power-ON, the configuration bits are serially transmitted through CLK, DATA pins (Phase-1) and then LDO enable signal (LDO_EN) is asserted using an external switch which loads the bandgap reference trim and scaling amplifier output voltage controls into shadow latches (Phase-2). Asserting LDO_EN starts up the LDO in normal operation with all the noise and ripple reduction techniques disabled. Then MODE_EN is asserted and an external clock as per the required chopping frequency (200 kHz, 500 kHz or 1 MHz) is provided at CLK pin (Phase-3). MODE_EN loads the remaining control bits into shadow latches, thus enabling/disabling the corresponding modes of operation of the LN-LDO. The control clock for the switched-*RC* filter is derived using the same external clock using internal clock dividers.

III. Measurement Results

This LN-LDO is fabricated in a $0.25\,\mu\mathrm{m}$ 1-poly 4-metal CMOS process. Fig. 10 shows the micrograph of the die. The core area is 0.18 $\mathrm{mm^2}$ and the noise reduction techniques occupy 0.02 $\mathrm{mm^2}$ which is around 10% of the overall LDO area. The LN-LDO has a programmable output voltage range of 1V–3.3V with a maximum load current of 100 mA and 230 mV dropout voltage consuming an average I_{Q} of 40μA at no load. An external signal generator is used as a clock source and programmable electronic load or discrete precision resistors are used as load. The noise measurement is done using a dc to 100 kHz dynamic signal analyzer.

Fig. 11 shows the noise PSD of the LN-LDO when switched-*RC* filter with duty cycle $D = 0.01\%$, chopping at $F_{\mathrm{CHOP}} =$

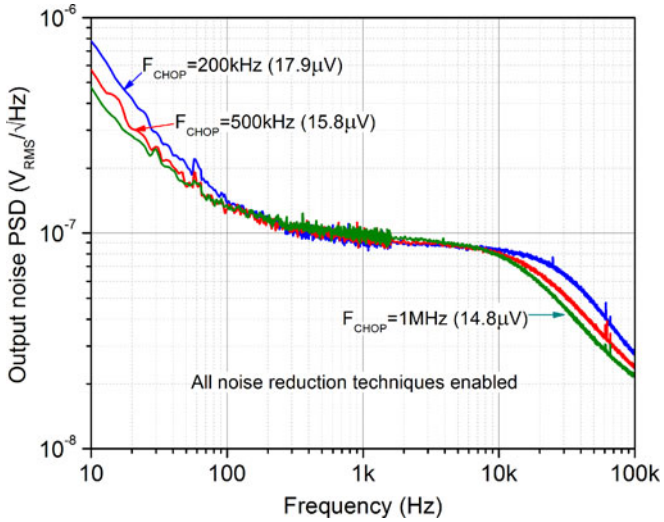

Fig. 12. Measured output noise for different chopping frequencies.

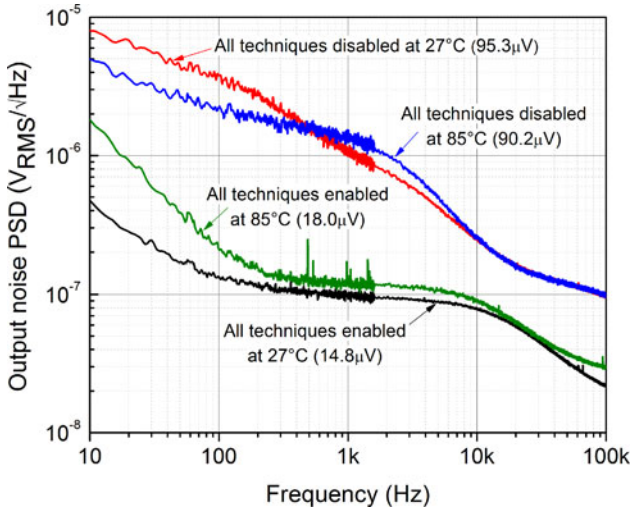

Fig. 13. Measured LDO output noise at room temperature and 85 °C.

200 kHz and bias circuit noise filter are enabled, compared to the baseline noise when the noise reduction techniques are disabled. It can be seen that the switched-*RC* filter reduces thermal and shot noise from bandgap reference circuit and thermal and 1/*f* noise from the scaling amplifier across the entire range of 10 Hz–100 kHz. Current-mode chopping reduces the 1/*f* noise of the error amplifier which is dominant from 10 Hz to about 10 kHz while the bias circuit noise filter reduces the thermal noise mainly beyond 10 kHz. The total noise power reduction achieved by the switched-*RC* filter, current-mode chopping, and bias circuit noise filter are 31%, 55%, and 12%, respectively. Fig. 12 shows the noise PSD of the LN-LDO for different chopping frequencies (F_{CHOP}) at room temperature (27 °C) with all noise reduction techniques enabled. For $F_{\mathrm{CHOP}} = 1$ MHz, the overall integrated noise of LN-LDO in the band of 10 Hz–100 kHz is $14.8\ \mu\mathrm{V_{RMS}}$, which accounts to 98% reduction in noise power when compared to $95.3\ \mu\mathrm{V_{RMS}}$ with noise reduction techniques disabled. A comparison of the measured noise PSD of the proposed LN-LDO at room temperature and 85 °C is given in Fig. 13. The integrated noise of the LN-LDO at 85 °C is $18.0\,\mu\mathrm{V_{RMS}}$, which is higher compared to that at room temperature due to the increased thermal noise at higher temperatures. Nevertheless, the proposed techniques reduce the noise power of the LN-LDO by 97% even at higher temperatures (85 °C). Any leakage current, if present, would result in a voltage drop in the held voltage of the storage capacitor present at the output of switched-*RC* filter and will appear as a low-frequency component in this noise PSD plot. Since there is no such component seen, it shows that leakage current at the output of switched-*RC* filter is limited to pico-Ampere levels even at high temperatures, ensuring that the LDO output does not drop during hold phase.

Effective chopping ripple reduction due to the SC notch filter for the maximum ripple case of $F_{\mathrm{CHOP}} = 200\,\mathrm{kHz}$ is shown in Fig. 14. The ripple at first and third harmonics is reduced from 110 and 6.98 μV to 3 and 0.95 μV, respectively. This confirms that ripple reduction is achieved not only at F_{CHOP} but also

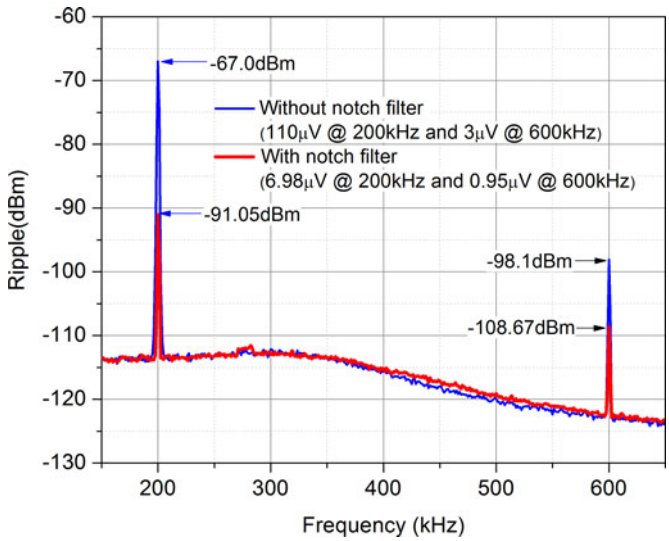

Fig. 14. Measured output ripple at chopping frequency of 200 kHz.

at its harmonics. Fig. 15 shows the load transient response of the LN-LDO for a full-load current change from 0 to 100 mA and Fig. 16 shows the line transient response for a load current of 10 mA for a loading capacitance of 10 pF due to probe capacitance at oscilloscope channel. The LN-LDO has a measured PSR of 50 dB at 10 kHz and 43 dB at 1 MHz as shown in Fig. 17. At frequencies around chopping frequency of 200 kHz, residual chopping ripple exists at the LN-LDO output. It is difficult to isolate only the supply ripple component at the LN-LDO output from the chopping ripple component for frequencies around 200 kHz. This results in an inaccurate, low PSR value around this frequency in spite of no actual degradation in its supply ripple rejection capabilities. Table I summarizes the performance parameters of the proposed LN-LDO and compares it with the previously published LN-LDO and output capacitorless LDO techniques.

TABLE I
PERFORMANCE SUMMARY OF PROPOSED LN-LDO AND COMPARISON TO PRIOR WORK

	[8] 2003	[1] 2005	[3] 2006	[4] 2008	[9] 2010	[10] 2014	[11] 2016	This paper
Process (μm)	0.6	0.35	0.13	0.25	0.35	0.18	0.18	**0.25**
Output voltage (V)	1.5	2.8	2.8	1.5–2	0.8	1.6	1.2–5.4	**1–3.3**
Max. load (mA)	100	100	150	50	66.7	50	150	**100**
Load capacitor (F)	Capless	1μ	0.3μ	50n	Capless	Capless	Capless	Capless
Voltage reference	Internal	External	Internal	Internal	Internal	External	External	Internal
Integrated noise (μV_{RMS})	–	21.2(1 kHz to 100 kHz)		14(1 kHz to 100 kHz)	–	–	40.1(100 Hz to 80 kHz)	**14.8(10 Hz to 100 kHz)**
Noise PSD at 100 Hz($\mu V/\sqrt{Hz}$)	1.8	–	0.34	–	–	–	12	**0.13**
Noise PSD at 100 kHz(nV/$\sqrt{Hz}$)	380	–	100	32	–	250	–	**22**
I_Q (μA)	38	–	100	120	43	55	40	**40**
PSR at 10 kHz (dB)	60	60	67	25	–	60	58	**50**
Area (mm^2)	0.30	0.26	0.166	0.88	0.155	0.14	0.279	**0.21**

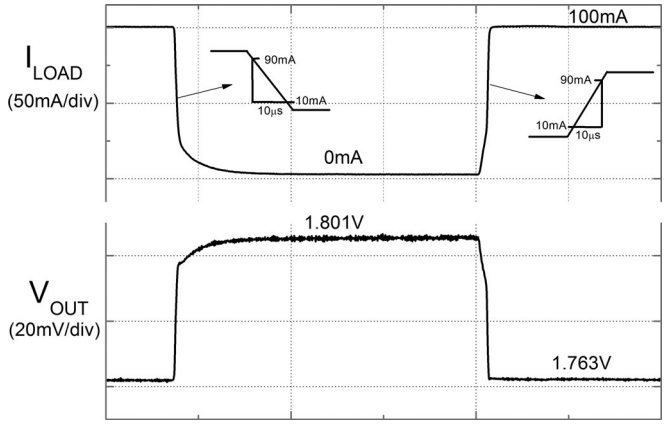

Fig. 15. Measured load regulation for load current step of 0–100 mA for $V_{OUT} = 1.8$ V.

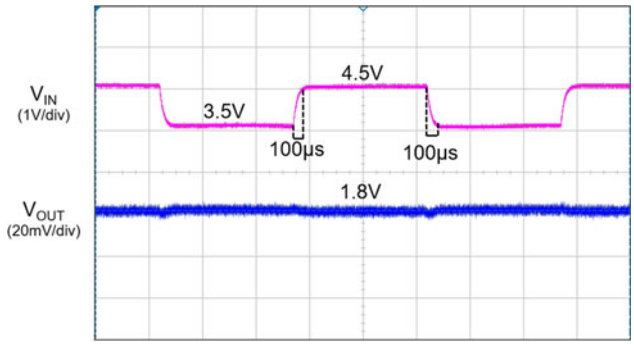

Fig. 16. Measured line regulation for a power supply step of 3.5–4.5 V for $V_{OUT} = 1.8$ V.

IV. CONCLUSION

This paper presents an output capacitorless LN-LDO regulator that achieves an output noise of $14.8\,\mu V_{RMS}$ in the integration band 10 Hz $-$ 100 kHz. The LN-LDO is fabricated in a 0.25μm CMOS process occupying a core area of 0.18 mm^2. It consumes a quiescent current of 40μA and delivers a maximum load current of 100 mA for a programmable output voltage of 1.0–3.3 V. The paper proposes a switched-*RC* filter at the output of the bandgap reference along with drain-side modulated current-mode chopping on an output capacitorless LDO for low noise operation. The proposed techniques reduce noise contributions not only from all major blocks, namely bandgap reference, error amplifier and biasing circuit but also bring down different types of noise including thermal, flicker (1/*f*) and shot noise. These techniques achieve a 98% reduction in noise power with only 10% area overhead, while maintaining high PSR and fast transient response. Furthermore, the chopping ripple, an undesirable by-product of chopping, is also filtered out using an SC notch filter. These techniques can be integrated into any generic wideband LDO, suitable for high-precision mixed signal and RF SOC applications without significant increase in area or power consumption.

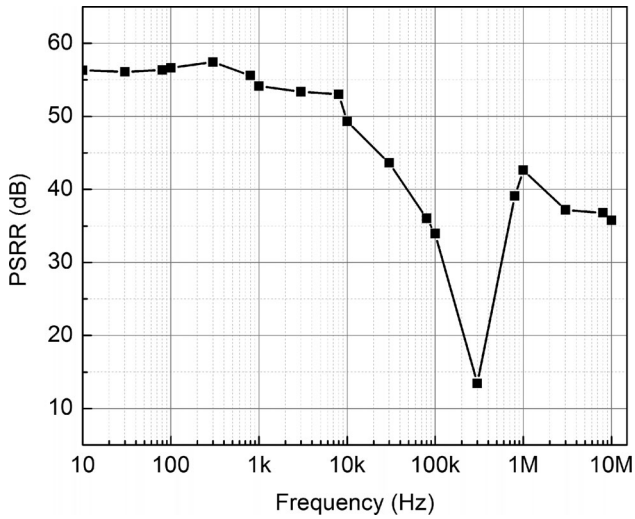

Fig. 17. Measured power supply rejection ratio (PSRR).

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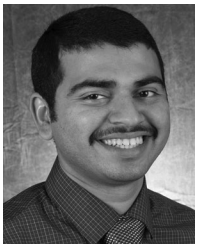

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