# An isolated active balancing and monitoring system for lithium ion battery stacks utilizing a single transformer per cell

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# An Isolated Active Balancing and Monitoring System for Lithium Ion Battery Stacks Utilizing a Single Transformer per Cell.

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***Abstract*—An active battery management system for lithium ion battery stacks is described, that is robust and scalable. The architecture is based on an isolation unit consisting of a small equal turns ratio high isolation transformer with two diodes. One isolation unit is connected to each series connected cell in the battery stack and enables both accurate cell voltage monitoring and active cell balancing.**

**The output of the isolation unit is completely galvanically isolated and thus suitable for high voltage packs with stringent safety requirements such as automotive and industrial electrical vehicles.**

**Detailed measurements results are presented and a complete prototype for a LiFePO4 16s2p 2kWh battery module is constructed and its performance measured.**

***Index Terms*—Battery Management System, Cell Balancing, Cell Isolation, Flyback Transformer, Lithium Ion Battery Stacks.**

## I. Introduction

Battery management systems (BMSs) for Lithium Ion Batteries (LIBs) are a key enabler for their application in a wide variety of products including electric vehicles[1]. For large battery packs in applications such as electric vehicles, two critical functions of the BMS system are 1: individual cell voltage monitoring and 2: individual cell charge balancing. High voltage packs require a large number of cells (typically in the 100's) to be connected in series to achieve the required voltage level. Such a pack thus needs a large number of components in the BMS to monitor and balance each cell individually. Large numbers of components and their required interconnect can potentially result in reduced reliability. This work focuses on the requirement for simplicity and robustness as the key drivers in this BMS design.

A wide variety of battery management architectures have been reported in the literature [2],[3]. A main distinction has been made between *passive* systems which balance cells by removing energy from them, dissipating it as heat and *active* systems which can add energy to a cell, taking it from other cells[4][3], modules[5], the full pack or external sources[6].

The fly-back architecture[7] provides a very convenient method for individual battery balancing as it inherently provides an isolated DC voltage to DC current conversion that can be individually controlled for each cell[8]. The use of transformers in flyback operation is widespread [9], and in this paper, an equal turns transformer is used in a discrete conduction mode. A key principle of the flyback configuration in this mode is that it operates in two discrete phases, the first one being an energy storage phase in which energy is taken from a voltage source through the primary winding and is stored in the magnetic field built up in the transformer core. For the BMS application, the fact that the stored energy only depends on the source voltage and the time it is charged for is advantageous as the cell voltage has no effect on the amount of energy stored. In the second, or discharge phase, that stored energy is released through the secondary winding forcing a current through the battery cell. For the BMS application, the fact that this forced current is only depends on the stored energy and transformer parameters and not the source voltage or cell voltages, allows for a controlled amount of energy into a specific cell, readily enabling individual cell balancing. This controlled energy transfer from a fixed voltage source into a cell is also galvanically isolated, thus providing isolation from the pack voltage. However, accurate cell voltage monitoring with the fly-back structure is potentially less accurate than the transformer technique of [10]. In this paper, a proposed method of accurate cell voltage monitoring within the fly-back structure is developed. The architecture in this paper achieves the dual functions of battery balancing and accurate cell voltage monitoring using a single transformer isolation unit per cell.

This paper is structured with a description of the proposed architecture in section II with the key development of accurate voltage measurement being developed in section II-A. The active cell balancing is described in section II-B. Prototype construction and measurements are presented in section III for both the individual cell interface units in section III-A and a full 16s2p LiFePO4 2 kWh battery module in section III-B. A detailed comparison table with other architectures from the literature is shown in section IV.

## II. Proposed Architecture

Fig. 1 shows the cell interface unit based on a small transformer to be used in a fly-back configuration. The lithium ion cell is connected to the cell port and the diode `D1` is reverse biased ensuring that no current is ever drawn from the cell through the unit.

Balancing is achieved by adding energy to the cell. While the diode forward drop reduces the efficiency of the transfer, the emphasis in this design is on robustness. A Schottky diode

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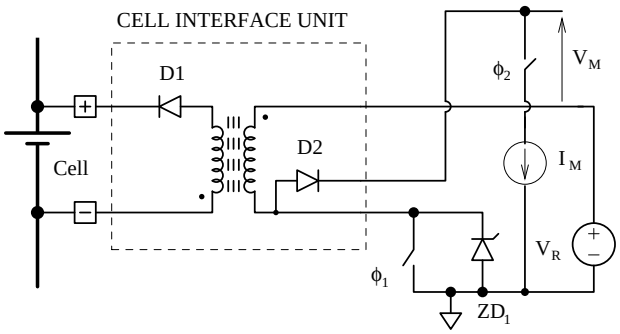


Fig. 1. Cell interface unit with cell and measurement circuitry.

could be used if efficiency is of higher priority, but at the expense of increased reverse biased leakage particularly at higher temperatures. Many designs[7] use MOSFET switches to increase the efficiency of the transfer, but this is avoided here to limit the number of isolation boundaries in the design and prevent any possibility of external signals shorting the cell, either by error or through fault conditions, thus improving the robustness of the design.

The key requirement for any BMS system is accurate monitoring of the cell voltage and for this reason a matching diode `D2`, in close thermal contact with the diode `D1` is included in the cell interface unit. This additional diode allows for the voltage drop of the diode `D1` to be compensated for when operated in the measurement mode, on the basis that the cell interface unit has both diodes at the same temperature. Voltage drop matching also requires that both diodes conduct the same current while voltage sampling and this is arranged as described in section II-A.

Fig. 2 shows the proposed architecture for a BMS utilizing four cell interface units. A common supply line and a voltage sense line is connected to each unit with a separate drive wire to select which one to activate. A 12V auxiliary supply is used for balancing operation but a 3.3V reference supply is used for monitoring to allow interfacing with signal acquisition circuitry. Voltage monitoring is performed in a serial manner. For example, if the select cell 2 MOSFET is turned on, the primary winding for the cell 2 interface unit is energized with 3.3V, while the other 3 transformers for cells 1, 3 and 4 are unconnected. The sense resistor voltage is measured to ensure the correct current level is reached in the cell 2 transformer. When the MOSFET is turned off, the transformer will force current into cell 2 while generating a negative voltage across the primary winding of cell 2 (equal to the cell voltage plus one diode `D1` voltage drop, due to the equal turns transformer ratio). This will forward bias the cell 2 `D2` diode and the bias measurement current $I_M$ will be drawn through the cell 2 diode `D2`. All `D2` diodes for the cells 1,3 and 4 will be reversed biased, thus allowing the voltage monitor ADC to measure the cell 2 voltage level.

For the balancing operation, with the 12V auxiliary supply selected, any combination of the select cell MOSFETs can be turned on together. For example, if the select cell 1 and select cell 3 MOSFETs are turned on, then both respective transformers are energized and store a fixed amount of energy. When both MOSFETs are turned off, the energy stored in each transformer is dumped into its respective cell, thus allowing any combination of cells to be charged up from the 12V auxiliary supply for charge balancing.

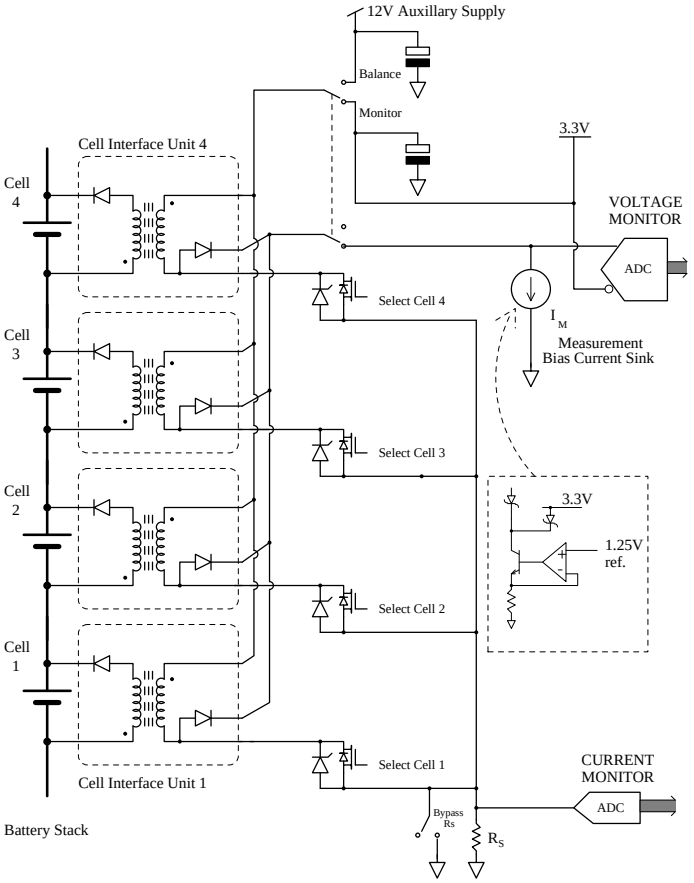


Fig. 2. Proposed BMS architecture.

### A. Cell Voltage Monitoring

Fig. 3 shows an equivalent circuit model for the cell voltage measurement operation. The transformer is represented by its magnetization inductance $L_M$ with primary and secondary leakage inductances $L_P$ and $L_S$. A reference voltage source of value $V_R$ is used to energize the transformer for voltage monitoring operation, and the reflected voltage, $V_M(t)$ in the figure is sampled at a predetermined time to provide the measurement result.

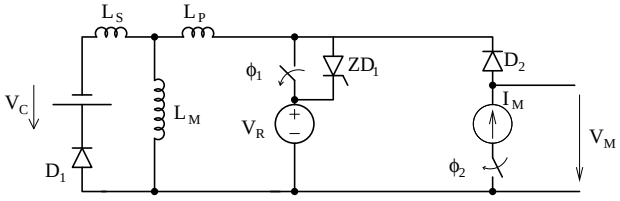


Fig. 3. Circuit model for cell voltage measurement operation.

The measurement of the actual cell voltage $V_C$ is complicated by the presence of the diode `D1` in the secondary

side of the transformer and the circuit configuration for fly-back operation. The diode D1 introduces a current dependent forward drop voltage that is sensitive to temperature. The presence of the diode D2 in the cell interface unit, provides a matched diode which should be at the same temperature as D1. However, their voltage drop will only be equal if they are conducting the same current. Thus during the measurement part of the cell monitoring operation, a bias current sink circuit draws a fixed current, denoted $I_M$, through the transformer primary and diode D2 to cancel the diode D1 voltage drop at the measurement sample instant.

The measurement operation operates by storing energy in the transformer during a first phase, and performing the voltage measurement during a second fly-back phase. There is a short transient phase in-between during which the leakage inductances redistribute currents. Fig. 4 shows the equivalent circuits during this sequence of operations.

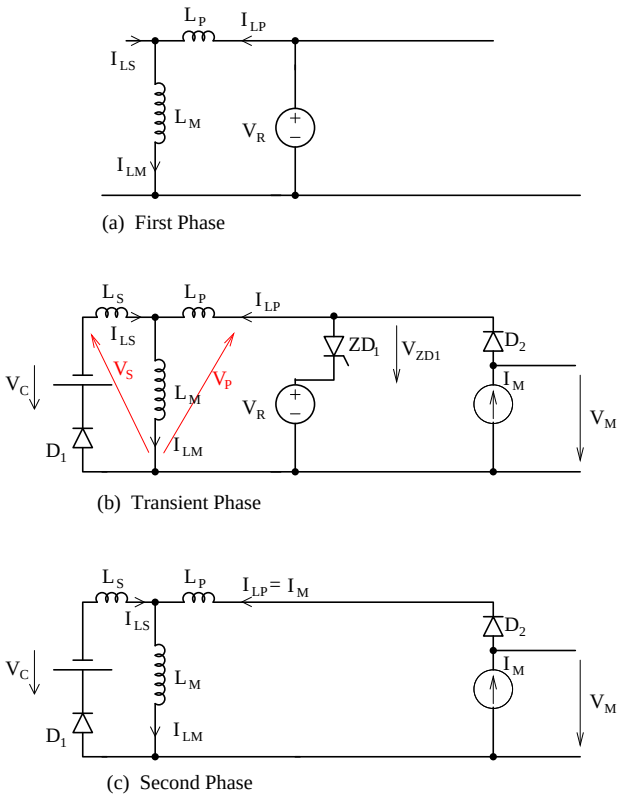


Fig. 4. Sequence of equivalent circuits during voltage measurement operation.

During the first phase, Fig. 4(a), the voltage source $V_R$ is switched across the transformer primary for a period of $T_1$ seconds and both the magnetizing inductance current $I_{LM}$ and primary leakage inductor current $I_{LP}$ rise to the peak transformer current value (denoted $I_0$), with

$$I_0 = \frac{T_1 V_R}{L_M + L_P}. \tag{1}$$

The secondary leakage inductor current, denoted $I_{LS}$, has zero value. The voltage source $V_R$ is switched out of the circuit and the circuit starts with the initial conditions:

$$I_{LS}(0) = 0, \quad I_{LM}(0) = I_0, \quad I_{LP}(0) = I_0 \tag{2}$$

As phase one ends, the circuit enters a transient phase as per Fig. 4(b). The voltage across the secondary of the transformer is $V_S = -V_C - V_{D1}$ and the voltage across the primary of the transformer is $V_P = -V_{ZD1} + V_R$, with $V_{D1}$ being the forward drop voltage of diode D1 and $V_{ZD1}$ being the Zener diode breakdown voltage.

The transient phase ends with the leakage inductance current $I_{LP}$ being equal to the measurement current $I_M$. The second phase then proceeds with the leakage inductance current $I_{LS}$ decaying from approximately $I_0 - I_M$ to zero, and this current flowing through the cell.

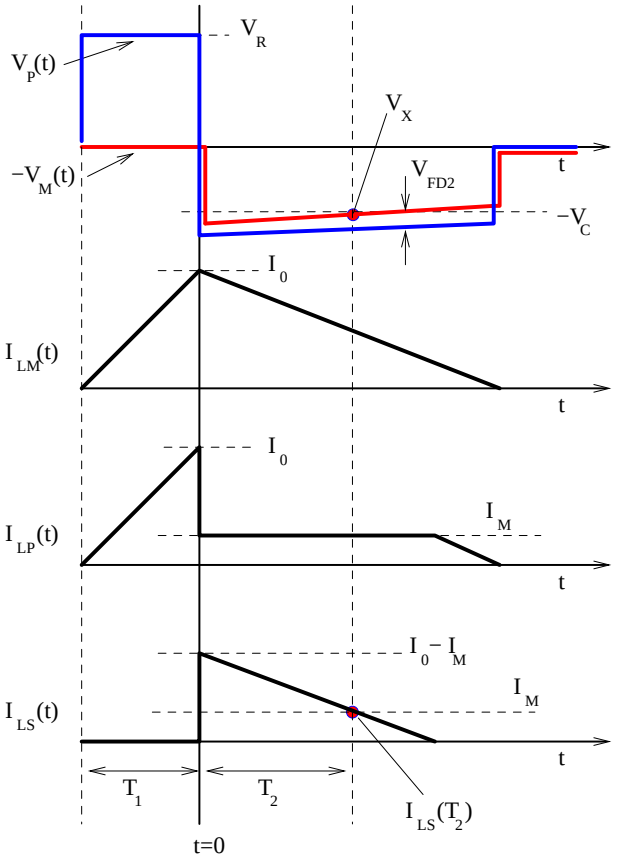


Fig. 5. Ideal waveforms during voltage measurements.

A good quantitative approximation to the operation of the measurement can be achieved by assuming the leakage inductances $L_S$ and $L_P$ are sufficiently small that they can be ignored (and thus the transient phase is sufficiently short, as verified in section III-A). Fig. 5 shows the voltage and current waveforms in this case. The current $I_0$ is approximated as:

$$I_0 \approx \frac{T_1 V_R}{L_M}. \tag{3}$$

Phase 2 begins with the primary current $I_{LP} = I_M$ and the secondary current starting at $I_0 - I_M$ due to the action of the bias current sink. The secondary current ramps down from $I_0 - I_M$ to zero and the key to the circuit operation is to sample the measurement voltage as the secondary current $I_{LS}(t)$ passes through the fixed value $I_M$. At this point, both diodes D1 and D2 have the same current ($I_M$) and thus the same voltage drop which then cancels out.

The secondary voltage is $-V_C - V_{D1}(I_{LS}(t))$ and this phase proceeds for a time denoted $T_2$, at which time the measurement voltage $V_M(t)$ is sampled (denoted $\widehat{V_C} = V_M(T_2)$) to give:

$$\widehat{V_C} = V_C + V_{D1}(I_{LS}(T_2)) - V_{D2}(I_M) \tag{4}$$

where $V_{D1}(I_{LS}(T_2))$ and $V_{D2}(I_M)$ are the diode forward drop voltages of diodes `D1` and `D2`, which are functions of their forward current and temperature. If the time $T_2$ is chosen such that $I_{LS}(T_2) = I_M$ and both diodes are at the same temperature, then the measurement voltage $\widehat{V_C} = V_C$ and the cell voltage is measured without error.

However the ideal sampling time value is a function of the cell voltage and thus the strategy employed in this paper is to choose the time $T_2$ such that the correct cell voltage is measured for the nominal cell voltage, denoted $V_{Cnom}$ and account for the measurement error when the cell voltage differs from the nominal value.

The actual current $I_{LS}(T_2)$ can be calculated as:

$$I_{LS}(T_2) = I_0 - I_M - \frac{1}{L_M}\int_0^{T_2} V_C + V_{D1}(I_{LS}(t))dt \tag{5}$$

Taking $I_{LS}(0) = I_0 - I_M$ , then applying the trapezoidal integration approximation gives

$$\begin{aligned} I_{LS}(T_2) &\approx I_0 - I_M \\ &- \tfrac{T_2}{L_M} \left[V_C + \frac{V_{D1}(I_0 - I_M) + V_{D1}(I_{LS}(T_2))}{2}\right] \end{aligned} \tag{6}$$

and the value of $T_2$ is chosen such that $I_{LS}(T_2) = I_M$ when $V_C = V_{Cnom}$. Hence $T_2$ is chosen as

$$T_2 = \frac{L_M(I_0 - 2I_M)}{V_{Cnom} + \frac{V_{D1}(I_0 - I_M) + V_{D1}(I_M)}{2}}. \tag{7}$$

Eliminating $L_M$ by using eqn 3, and denoting $\frac{1}{2}(V_{D1}(I_0 - I_M) + V_{D1}(I_M)) = \overline{V_{Dn}}$ then

$$T_2 = T_1 \frac{I_0 - 2I_M}{I_0}\left[\frac{V_R}{V_{Cnom} + \overline{V_{Dn}}}\right] \tag{8}$$

With the value of $T_2$ chosen for nominal cell voltage $V_{Cnom}$ and with $\overline{V_{Dn}}$ evaluated at the nominal ambient temperature, the actual measured voltage at cell voltage $V_C$ is then:

$$\widehat{V_C} = V_C + V_{D1}(I_{LS}(T_2)) - V_{D2}(I_M) \tag{9}$$

With the ideal diode equation for a diode current $I_x$, the forward drop voltage is:

$$V_{Dx}(I) = \frac{k\theta_T}{q}\ln\frac{I_x}{I_S} \tag{10}$$

where $k$ is Boltzmann constant, $\theta_T$ is the diode absolute temperature, $q$ is the charge on the electron and $I_S$ is the diode saturation current parameter, then with matched diodes:

$$\widehat{V_C} = V_C + \frac{k\theta_T}{q}\ln\frac{I_{LS}(T_2)}{I_M} \tag{11}$$

and approximating

$$I_{LS}(T_2) \approx I_0 - I_M - \frac{T_2}{L_M}\left[V_C + \overline{V_{Dm}}\right] \tag{12}$$

and with $\frac{1}{2}(V_{D1}(I_0 - I_M) + V_{D1}(I_{LS}(T_2))) = \overline{V_{Dm}}$ , eliminating $L_M$ by using eqn 3 and using eqn 8,

$$\widehat{V_C} = V_C + \frac{k\theta_T}{q}\ln\left(1 + \frac{(I_0 - 2I_M)}{I_M}\left[\frac{\Delta V_C + \overline{\Delta V_D}}{V_{Cnom} + \overline{V_{Dn}}}\right]\right) \tag{13}$$

where $\Delta V_C = V_{Cnom} - V_C$ and $\overline{\Delta V_D} = \overline{V_{Dn}} - \overline{V_{Dm}}$. The right hand term in eqn 13 is an error between the measured voltage and the actual cell voltage. This error is zero at the nominal cell voltage $V_{Cnom}$ under which condition both $\Delta V_C$ and $\overline{\Delta V_D}$ are zero.

Note that selecting the measurement current $I_M$ equal to $I_0/2$ would result in the error term being zero, but would also require the value of $T_2$ to be zero from eqn 8, thus requiring sampling at the end of the transient phase, where some ringing is inevitably expected. In practice a value of $I_M$ of the order $I_0/4$ is used to allow sufficient time for any ringing to settle. However, this leaves the error term non-zero when the cell voltage differs from the nominal value. The error term in eqn. 13 can be numerically evaluated and is plotted in Fig. 6 as a function of the cell voltage and at a range of different temperatures using a nominal voltage of 3.4V. The error varies from -12mV to +15mV, but in a reasonably linear manner. Correcting the error with a gain and offset correction using a two point calibration at 25 deg C, results in an error below $\pm$5mV over voltage and temperature in the figure. Gain and offset correction can also account for other systematic linear errors in the system such as leakage inductance, gains and offsets in the ADC and analogue front end electronics including the bias current sink. Measurements on a prototype design in section III confirm that an error level below $\pm$10mV is feasible in practice.

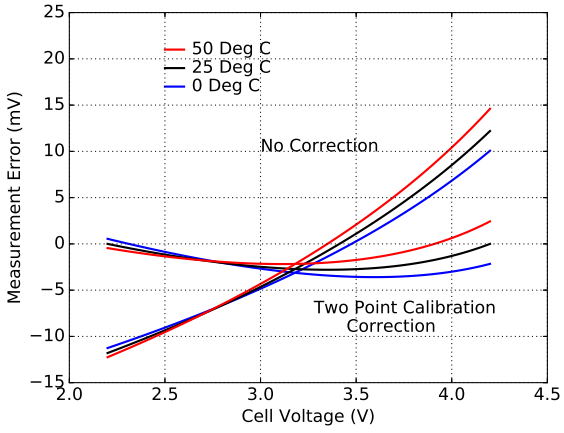


Fig. 6. Theoretical accuracy with and without two point calibration.

### B. Cell Current Balancing

The requirement for cell balancing is addressed in this design by transferring energy into individual cells (i.e. charging them)[7]. The maximum balancing power transfer requirement is determined by the amount of cell mismatch expected and the time available to perform the balancing operation[1].

With the proposed cell interface unit the maximum balancing power transfer is essentially determined by the transformer element. The power transfer during balancing is performed with the fly-back method and the discontinuous conduction mode is the simplest to implement and control with multiple cells being simultaneously balanced. Energy is stored in the transformer core from the auxiliary supply during a first phase, and released to the cell in a second phase. During balancing this is repeated constantly, to effect the desired power transfer level. Control of the balancing current is based on an open loop timing based control. From the voltage monitoring operation, the time taken ($T_1$) to charge the each transformer magnetizing inductance to the current $I_0$ is accurately known for the reference voltage $V_R$. Thus, with the auxiliary voltage $V_{AUX}$ instead of $V_R$, each transformer can be charged to a peak charging current of approximately $I_B$ by turning on the associated transistor for a period $T_C$ calculated as:

$$T_C = \overline{T_1}\frac{I_B}{I_0}\frac{V_R}{V_{AUX}}. \tag{14}$$

where $\overline{T_1}$ is the average value of $T_1$ across the transformers. Thus an energy of $\approx \frac{1}{2}L_M I_B^2$ is stored in each. Knowing, the lowest cell voltage and diode drop, the time to discharge the stored energy into the worst case cell is known. In the prototype during balancing operation, the second phase is enabled for this worst case plus a significant margin, to ensure that all transformers are fully discharged to zero. In this way, a known power level is transferred to each selected cell interface unit in parallel without the need for individual current measurements. Hence, the shunt resistor `RS` in Fig. 2 is bypassed during balancing operations.

A somewhat higher efficiency and higher power level could be achieved if a continuous conduction mode with transformer current measurement and closed loop feedback for each cell interface unit was implemented[8] and this could be feasible if a custom integrated circuit per unit was developed. However, for the prototype system, the open loop method is far simpler to implement and performs well and robustly, with minimum complexity.

Not all the power transferred by the cell interface unit is delivered to the cell. A significant portion is dissipated in the diode `D1` and there are also resistive losses in the transformer winding's. For example, with a diode drop of 0.7V and nominal cell voltage of 3.3V, then the efficiency cannot exceed 82.5%. In this paper, the requirements for the transformer are primarily driven by the requirement for accurate voltage monitoring and balancing efficiency is not the primary consideration[1].

## III. Prototype Design and Verification

### A. Cell Interface Unit

A set of 16 cell interface units are constructed to verify the operation of the proposed techniques and the construction sequence is shown in Fig. 7 with the components used and measured parameters listed in table I. Two jointly wound winding's of insulated 30 AWG wire are wound on a ferrite powder core and the two matched diodes (DO-201 packages) fit within the core in close thermal contact. The diodes were manually matched to within $\pm 1mV$ of each other for the prototypes[1].

Fig. 7. Construction of Prototype Cell Interface Units.

The connections are wired up and the whole unit is molded in an epoxy compound to provide a robust unit that can be directly bolted to the cell terminals.

TABLE I
Prototype Cell Interface Unit Measured Parameters.

| | |
|---|---|
| Magnetic Core | T80-26B ferrite powder |
| Dimensions | 20.5mm OD,12mm ID |
| height | 9.8mm |
| $\mu_R$ | 75 |
| Number Turns | 65T 30 AWG wire |
| Magnetizing Inductance | $290\mu H$ |
| Leakage Inductance | $2.75\mu H$ |
| DC resistance | $0.65\Omega$ per winding |
| Diodes | $2\times$ IN5404 |

The core material is chosen for its low temperature dependence and operated at low current to maintain linear operation during the voltage monitoring operation. Once assembled and wired up with the battery management system electronics, a one time calibration of the monitor current using the sense resistor `Rs` of Fig. 2, is done to set the current level $I_0$ to 100mA. The bias current sink level $I_M$ is set as 25mA for prototype system. Fig 8 shows the measured primary current and measurement voltage waveforms for the prototype system with a cell voltage of 3.35V and shows the transient phase lasting for less than 1uS, allowing for accurate voltage measurements.

The time required for each voltage measurement is approximately 20us for the prototype implementation, thus allowing a module with 16 cells to be measured in about 320uS. All modules operate in parallel and thus a full stack (e.g of 96 cells over $6 \times 16$ cell modules) can also be measured in 320uS. For lower latency systems, the number of cell interface units per voltage monitoring ADC could be reduced with multichannel ADCs and/or multiplexors[10]. Ultimately, a dedicated ADC (or sample and hold circuit) could be used for each cell interface unit to achieve a simultaneously sampling time across the whole pack.

[1]Matched diodes can be supplied by manufacturers, though usually at a higher cost.

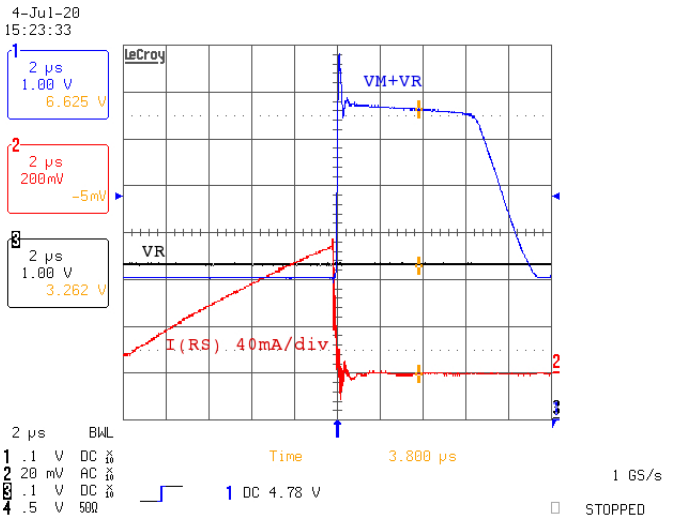


Fig. 8. Transformer primary current *I(RS)* measurement and voltage waveforms for the prototype system.

Adopting a 100 Hz sampling rate in the prototype is readily achievable. A small amount of energy is transferred to the cell during this measurement process, but with a voltage monitoring rate of 100 samples per second, an average charge current of about 25uA per cell is supplied in the prototype system. At low temperatures where cell internal resistance can increase substantially, the measurement current of 25mA can cause an error in the measured cell voltage, however this can be accounted for with BMS systems that track estimates of internal cell resistance. Alternatively a decoupling capacitor across the cell terminals (e.g. 330uF ) can reduce such errors below the mV level as only a short current pulse is required for the voltage measurement[2].

To evaluate the accuracy of the voltage measurements, the 16 prototype cell interface units and prototype system were calibrated at two points (2.2V and 4.2V) at 25 deg C. The BMS system reported voltage was then measured over the input voltage range of 2.2V to 4.2V and with the cell interface units at 0, 25 and 50 deg C. Fig. 9 shows the resulting data with a total measurement error within $\pm 9mV$ over the temperature and voltage range and even better $+9mV/-3mV$ over the LiFePO4 operation window of 2.8V to 3.6V, thus confirming the suitability of the system for individual cell monitoring. The total measurement error in Fig. 9 is defined as the actual measured cell voltage minus the BMS reported cell voltage, thus including calibration, gain, offset, ADC and voltage reference errors. Note that for a different cell chemistry, the design could be centered around a different nominal voltage.

Voltage monitoring ICs have been available for sometime and utilize direct connection to the cell terminals. They can achieve high accuracy voltage measurements such as $\pm 7mV$ [11], $\pm 1.6mV$ [12], $\pm 1mV$ [13], $\pm 0.75mV$ [14]. They typically have a limit on the voltage span supported by a single IC due to process high voltage limits and are not isolated from the battery stack, thus requiring carefully wiring and protection circuits. Reference [10] provides an isolated voltage measurement system with high accuracy of 1mV at 25 deg C for battery voltages of 0V to 2V, and also provides a good comparison of direct voltage measurement techniques, but does not consider balancing techniques.

[2]Injected charge of about 250 nC per measurement event.

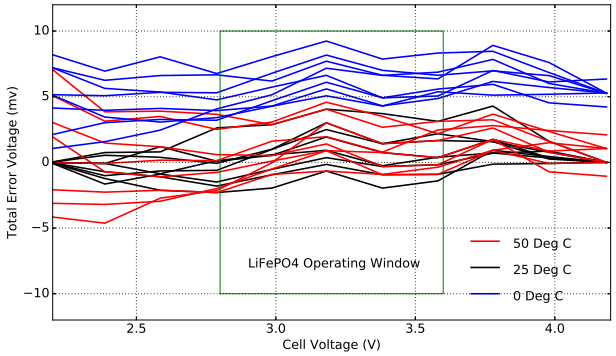


Fig. 9. Voltage Measurement accuracy for 8 units over voltage and temperature (0 deg C to 50 deg C).

The balancing efficiency of the cell interface unit was measured with a 12V auxiliary supply supplying a charge current to a 3.35V reference test load. The resulting efficiency in terms of supplied power to the cell divided by the power drawn from the auxiliary supply is shown in Fig. 10. The measured average cell current was readily variable from 50mA to 500mA and with efficiency dropping from over 60% at low currents towards 40% at 500mA. The efficiency was limited by the forward drop voltage of the silicon diode `D1` and the resistive losses of the transformer winding's. The range of currents supported is sufficient for large (up to 100Ah) battery pack in electric vehicle applications where cells tend to be well matched and regularly balanced[1].

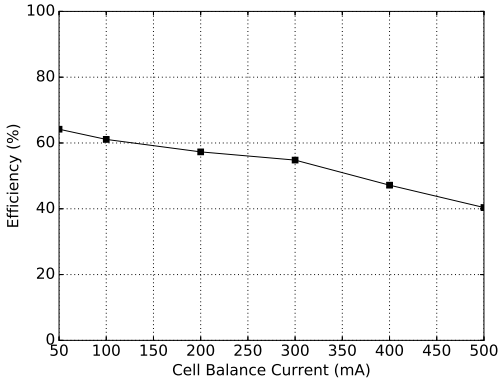


Fig. 10. Measured Efficiency of balancing efficiency versus cell balance current.

## B. Battery Module

To demonstrate the usage of the cell interface unit, a full prototype battery module is constructed. The battery module uses a stack of 16 series connected 2 parallel 20 Ah lithium

iron phosphate (LiFePO4) cells. Fig. 11 shows a photo of the prototype 2 kWh battery module consisting of 32 LiFePO4 20 Ah cells, connected in a 16s2p configuration. Each parallel cell pair has a single cell interface unit mounted directly on its terminals with its wiring brought outside the module enclosure to a BMS circuit board outside. A key advantage of the architecture is that the wiring from each cell interface unit coming outside the enclosure is completely galvanically isolated from the cell voltages. This provides a significant safety advantage and allows the BMS circuit board to be modified or replaced without high voltage precautions. For example, in an automotive application, a faulty BMS circuit board could be replaced by a technician without the need to open the battery module and expose high voltages. The BMS circuit is accessed and controlled through a CAN bus and is supplied with a 12V auxiliary supply. Scaling is supported by adding additional modules in series and connecting the 12V auxiliary supply to each in parallel and adding them to the CAN bus.

Fig. 11. 16s2p $\times$ 20 Ah LiFePO4 cells 2 kWh battery module with 16 cell interface units and proposed battery management system.

The functional operation of the developed BMS with the prototype module is shown in Fig. 12, which shows the BMS reported cell voltages. In this example operation the module was charged from 75% state of charge (SoC) to 100% SoC with a constant current of 2.5A until one cell reached the terminal voltage of 3.45V. At that point, the constant current charger was disconnected and a balancing operation was started. All the other cells were then simultaneously charged with a 250mA current, and as each reached the 3.45V level, its balancing current was turned off. Balancing was completed when no cells were left. The balancing time is thus independent of the number of cells in the stack and only depends on the SOC mismatch between the cell with highest SOC and the cell with the lowest SOC. In the prototype implementation, balancing is activated for 10 sec periods after which a voltage measurement operation is performed. There are no significant transients associated with the transitions between balancing and voltage measurements as the decoupling capacitors for balancing auxiliary supply and the decoupling capacitors for the reference supply $V_R$ to the flyback transformers are connected to the non switched sides as shown in Fig. 2. The magnetizing inductance is discharged to zero after each voltage measurement and as part of the discontinuous mode operation of balancing, thus avoiding losses when switching between each mode. This operation required about 40 minutes to complete and illustrates the correct functioning of the prototype system, including its ability to monitor the cell voltages accurately as well as perform active balancing.

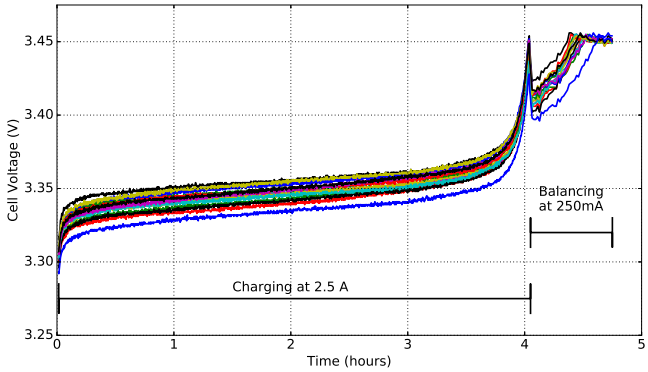


Fig. 12. Cell voltage for 16 parallel pairs of cells when charging from 75% SOC until any cell reaches 3.45V and then performing a module balancing operation to bring all cells to 3.45V.

## IV. Conclusions and Comparison with other Architectures

The proposed architecture is shown to effectively perform the two key per cell functions of voltage monitoring and cell balancing required for a complete BMS. These functions are achieved with a cell interface unit on the cell terminals that provides complete galvanic isolation for the BMS wiring within the battery module enclosure. Table II lists a range of different architectures from the literature under a number of important system headings. The active balancing schemes focus on the balancing and its efficiency and either do not consider the voltage monitoring function or require a separate monitoring system to be implemented. The passive balancing schemes perform both functions, but require wiring directly from the cell terminals to a balancing board making at least part of the board operate at the battery voltage, often requiring fuses per cell for safety, requiring isolation for the circuit board outputs and making assembly, repair or replacement of boards a difficult task, especially in high voltage systems like electric vehicles. Only the proposed scheme achieves both the functions required, while providing full isolation with only low voltage wiring. The robustness of the proposed method is based on the requirement of only a single isolation point, the transformer, for each cell. There is no need for opto-isolators, isolated MOSFET drivers or bootstrapped/floating power supplies. This combined with the structure of a simple passive module bolted to the cell terminals and connected externally by low voltage wiring, has been found by the author to be robust and easy to use in practice. The design is also safe and robust against any break in cell to cell wiring connections.

TABLE II
COMPARISON WITH OTHER BMS'S FROM THE LITERATURE. NOTE: COMPONENTS ARE; T TRANSFORMER, M MOSFET (AND DRIVER), D DIODE, Z ZENER DIODE, R RESISTOR AND C CAPACITOR. WIRING IS: HV BMS WIRING IS AT THE BATTERY STACK POTENTIAL, LV BMS WIRING IS AT THE LOW VOLTAGE ISOLATED SUPPLY POTENTIAL.

| Ref: | Topology | Isolation per Cell | Per Cell Components | Balance Current | Balancing Efficiency | Voltage Monitoring | Voltage Accuracy | Module Wiring |
|---|---|---|---|---|---|---|---|---|
| [7] | Multi-Transformer Parallel Balance | Non Isolated (via ADC) | 1T 1D 2M | 2A | 85% | External ADC | | HV (for ADC) |
| [15] | Switched Capacitor Parallel Balance | Non Isolated | 1C 2M | $\approx 0.5A$ | High | None | | HV |
| [16] | Switch-Matrix Serial Balance | Non Isolated | 2M | 0.2A | 80.4% | External ADC | | HV |
| [5] | Switch-Matrix Modular Balance | Non Isolated | 2M $\frac{1}{12}\times$ LTC6802 | 2A | 82% | LTC6802 | $\pm$8mV | HV |
| [17] | Resistor Passive Balance | Non Isolated | $\frac{1}{18}\times$ LTC6813 1 R | 0.1A | 0% | LTC6813 | $\pm$4.2mV | HV |
| [10] | Multi-Transformer Monitor only | 1 Transformer | 1T 1M 1D | None | | Yes | 1mV | LV |
| *This Work* | Multi-Transformer Monitor AND Balance | 1 Transformer | 1T 2D 1Z 1M | 50mA to 0.5A | 64% to 40% | Yes | $\pm$10mV | LV |

While the proposed method has lower accuracy than other methods in table II, the simplicity of the design and achievement of both balancing and monitoring using a single isolation component per cell, provides an additional option in the design space of battery management systems and should be of interest to designers and engineers in the field.

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