

Data Sheet

VL160

USB Type-C Data Switch with CC Function for USB 3.1 Gen2 (10Gbps)

September 20th, 2016 Revision 0.93





Revision History

Rev	Draft Date	History	
0.50	10/18/2015	Preliminary Release	
0.51	10/16/2015	Add DC Parameter	TH
0.60	02/02/2016	Add Tape and Reel Information	TH
0.9	02/17/2016	Update Electrical Specification	TH
0.91	04/11/2016	Update ordering information	
0.92	05/24/2016	Update Package Mechanical Specification	
0.93	09/20/2016	Add Lead(Pb)-Free and RoHS compliant	TH

深圳市科瑞芯电子有限公司



Contents

Product Feature	4 -
Block Diagram	5 -
Pinout	
Pin List	7 -
Pin Descriptions	
Application Diagram	
Electrical Specification	11 -
Reflow Profile	12 -
Package Mechanical Specifications	
Package Top Side Marking	14 -
Ordering Information	- 14 -
Tape and Reel Information	15 -

List of Figures

Figure 1 - Block Diagram			5 -
Figure 2 - Pin Diagram (QFN-28)			
Figure 3 - Reflow			
Figure 4 - Mechanical Specification			
- ·	a vooroon vooroon v		
Figure 5 - Package Top Side Marking Figure 6 - Tape & Ree Information		17日 人へ	15 -
・ ・ ・ ・ ・	7 1 - 	- 27 YIU	



Product Feature

VL160

USB Type-C Data Switch with CC Function for USB 3.1 Gen2 (10 Gbps)

- 4:2 10Gbps USB Type-C Data Switch
- Support up to 10Gbps
- 2 Differential Channel, 2:1 MUX/DeMUX
- Compatible with 10Gbps USB3.1 Gen2
- Low power consumption with 0.5mA active and 4uW shutdown
- High DC common mode voltage supporting to 2.2V
- 28 pins QFN 3.5 x 4.5mm package
- ESD > 4KV, CDM > 500V
- Lead(Pb)-Free and RoHS compliant
- MUX
- Insertion loss: 1.5dB @ 5GHz typ.
- Return loss: 15dB @ 5GHz typ.
- Crosstalk Isolation: 30dB @ 5GHz typ.
- Off Isolation: 15dB @ 5GHz typ 山市科瑞芯电子有限公司
- Define Role: Device (UFP, default) or Host (DFP)
- Plug Orientation: Flipped or Not, and control Switch SEL
- (UFP) Current Capability Detect: 3.0A, 1.5A, or 0.9A
- (UFP) Rd
- (DFP) Rp (or Ip), Vconn SW if Ra
- (DFP) VBUS_EN to turn on Host VBUS SW

■ Vconn

- 5V, max Power is 1W, max current is 250mA
- Over current protection



Block Diagram

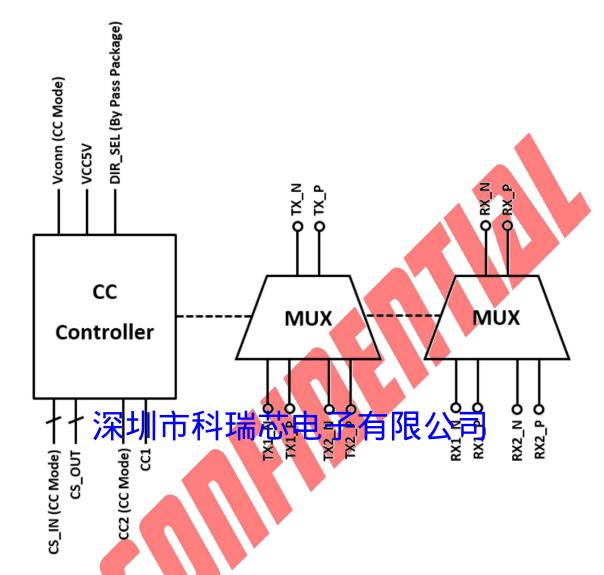


Figure 1 - Block Diagram



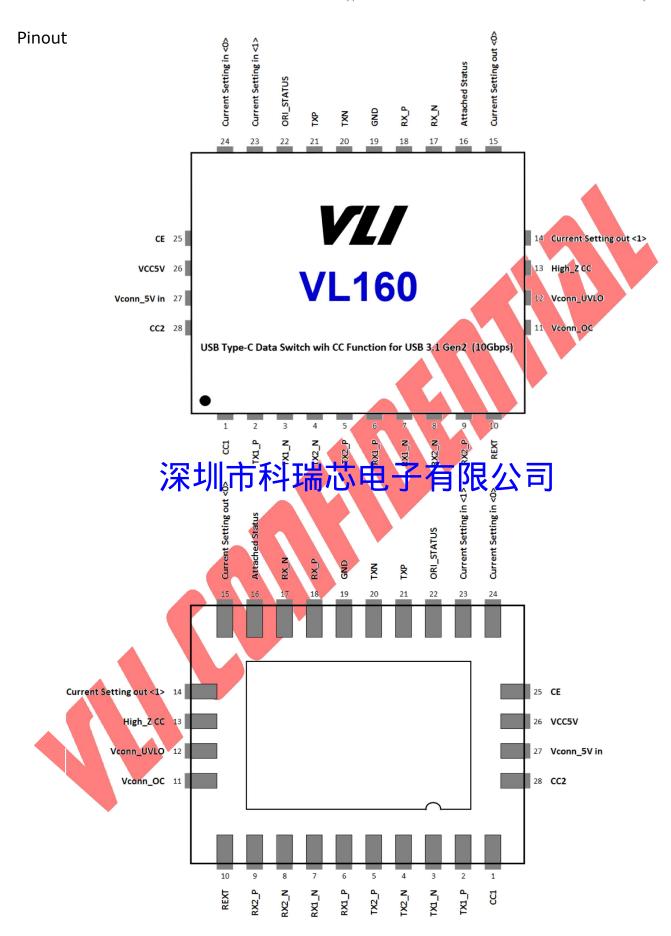


Figure 2 - Pin Diagram (QFN-28)



Pin List

Pin	Pin Name	Pin	Pin Name	
1	CC1	15	Current Setting out <0>	
2	TX1_P	16	Attached_Status	
3	TX1_N	17	RX_N	
4	TX2_N	18	RX_P	
5	TX2_P	19	GND	
6	RX1_P	20	TXN	
7	RX1_N	21	TXP	
8	RX2_N	22	ORI_STATUS	
9	RX2_P	23	Current Setting in <1>	
10	REXT	24	Current Setting in <0>	
11	Vconn_OC	25	CE	
12	Vconn_UVLO	26	VCC5V	
13	High_Z CC	27	Vconn_5V in	
14	Current Setting out <1>	28	CC2	

深圳市科瑞芯电子有限公司



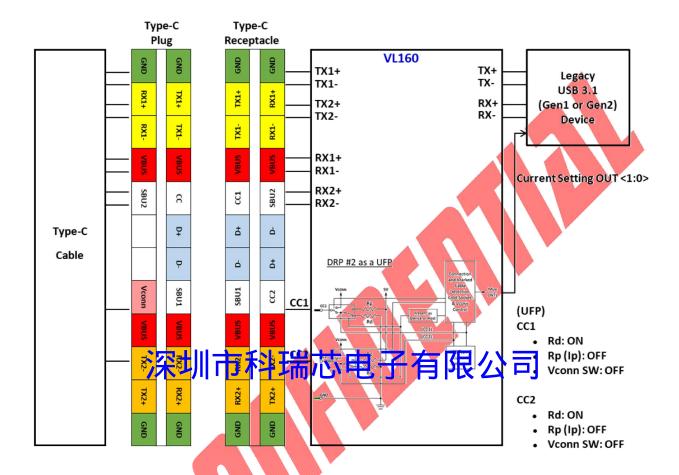
Pin Descriptions

Pin Name	Pin #	I/O	Description
CC1	1	AI/O	0~5V analog input
TX1_P	2	High Crosd I/O	LICE differential rain
TX1_N	3	High Speed I/O	USB differential pair
TX2_N	4	High Coas d I/O	LICE differential ratio
TX2_P	5	High Speed I/O	USB differential pair
RX1_P	6	High Speed I/O	USB differential pair
RX1_N	7	riigii Speed 1/O	OSB differential pair
RX2_N	8	High Speed I/O	USB differential pair
RX2_P	9	riigii Speed 1/O	OSB differential pair
REXT	10		External resister 20.5k 1% connect to GND
Vconn_OC	11	DO	Vconn Over current, 3.3V = Over current
Vconn_UVLO	12	DO	Vconn Under voltage, 3:3V = under voltage
High_Z CC	13	DI	Turn off Rp/Rd on CC1/CC2, 0V = Normal mode, 5V = Hi-Z mode
Current Setting out	14	DO	(3.3V logic) 11: CC Support 3A
<1>	14	50	10: CC Support 1.5A
Current Setting out	深	圳市科:	Reasoning: Easily identify SA vs 1:5A or Legacy/1.5A or Legacy using just
<0>	13		1 pin. If they need to differentiate between 1.5A and 3A, then use 2 pins
Attached_Status	16	DO	Indication for port attached, 3.3V = attached
RX_N	17	High Speed I/O	USB differential pair
RX_P	18	Tilgii Specu 1/0	osb dilicitation pair
GND	19	GND	Ground
TXN	20	High Speed I/O	USB differential pair
TXP	21	riigii Speed 1/0	·
ORI_STATUS	22	DO	Orientation status 0 = TX1/RX1, 3.3V = TX2/RX2
Current Setting in <1>	23	AI	(3.3V logic) Rp/Rd setting input 00: Ip = 80uA
			01: Ip = 180uA 10: Ip = 330uA
Compart Cattings in 10	24		11: $Rd = 5.1k\Omega$
Current Setting in <0>	24	AI	00: Rp = 36kΩ 01: Rp = 12kΩ
			10: $Rp = 4.7k\Omega$ 11: $Rd = 5.1k\Omega$
CE	25	DI	Chip Enable (5V = Enable)
VCC5V	26	PWR	VCC5V for controller
VCONN_5V in	27	PWR	5V input for Vconn
CC2	28	AI/O	0~5V analog input



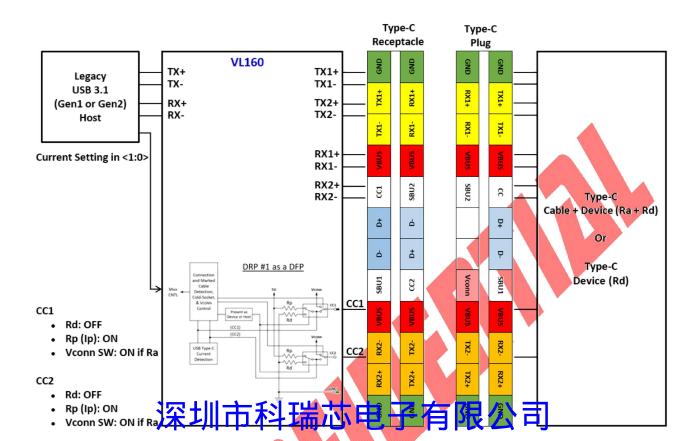
Application Diagram

Application for Cable + Device





Application for Host + Cable or Host only







Electrical Specification

Absolute Maximum Rating

Symbol	Parameter		Min	Max	Unit	Note
T_{STG}	Storage Temperature		-55	125	°C	-
V _{ESD}	Electrostatic Discharge		4KV		V	Human Body Model
0	θ_{jc} Thermal resistance between junction and case —		36.7		00/11	
$\Theta_{ m jc}$			28.1		°C/W	
P _D	Max Power Dissipation		-	8m	W	

Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, Ta is the concerned ambient temperature, and

 $\theta_{ca} = \theta_{ja} - \theta_{jc}$ $T_{J} = \theta_{ja} * P_{D} + T_{a}$ $T_{c} = \theta_{ca} * P_{D} + T_{a}$

Operating Conditions

Symbol	Parameter	Min	Тур.	Max	Unit	Note
VDD	Supply voltage	4.5	5.0	5.5	V	
T _A	Ambient Temperature	-45		85	°C	
T _j	Junction Temperature	0		125	°C	-

深圳市科瑞芯电子有限公司

Static characteristics:

VDD = $5.0V \pm 10\%$; Temp = -40° C to $+85^{\circ}$ C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур.	Max	Unit
IDD	Supply current	Operation mode			500	uA
טטו	Supply current	Shutdown mode			1.5	uA
VIH	High-level input voltage		2.7			V
VIL	Low-level input voltage				0.4	V
Vcom	Input Common mode voltage		0		2.2	V



Reflow Profile

Follow: IPC/JEDEC J-STD-020 D.1

Condition

Average ramp-up rate (217°C to peak): 1~2°C /sec max. Preheat: 150~200°C, 60~120 seconds

Temperature maintained above 217°C: 60~150 seconds

Time (tp)* within 5°C of the specified classification temperature (Tc = (260°C)), (the time above 255°C) \geq 30 sec.

Peak temperature: 260+5/-0°C Ramp-down rate: 3°C /sec. max.

Time 25°C to peak temperature: 8 minutes max.

Cycle interval: 5 minus



Figure 3 - Reflow



Package Mechanical Specifications

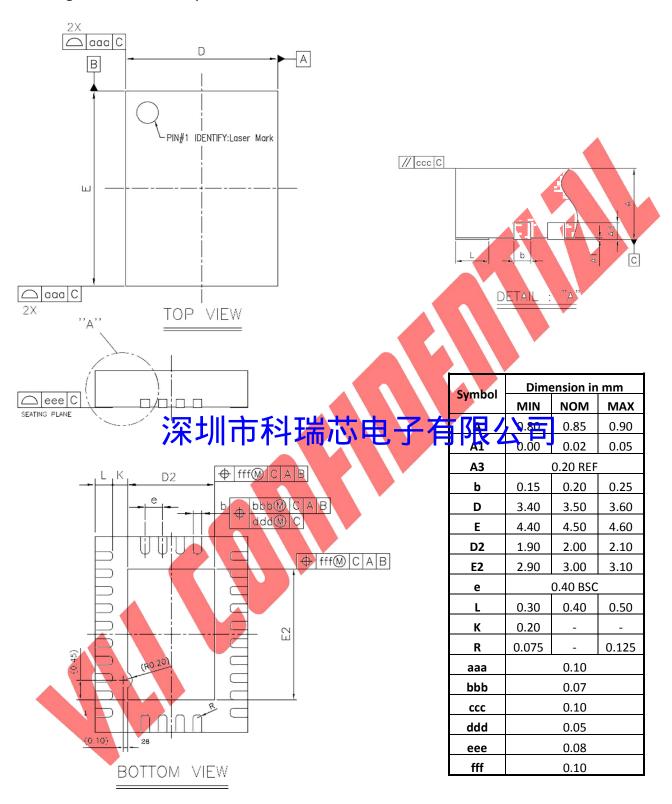


Figure 4 - Mechanical Specification



Package Top Side Marking

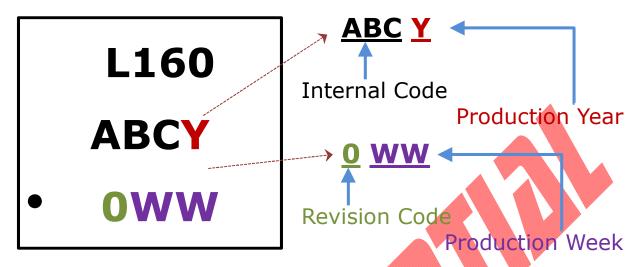


Figure 5 - Package Top Side Marking

Ordering Information

Part Number	Description	Package Type
VL160 (B0)	Tape a reel (3K)	→





Tape and Reel Information

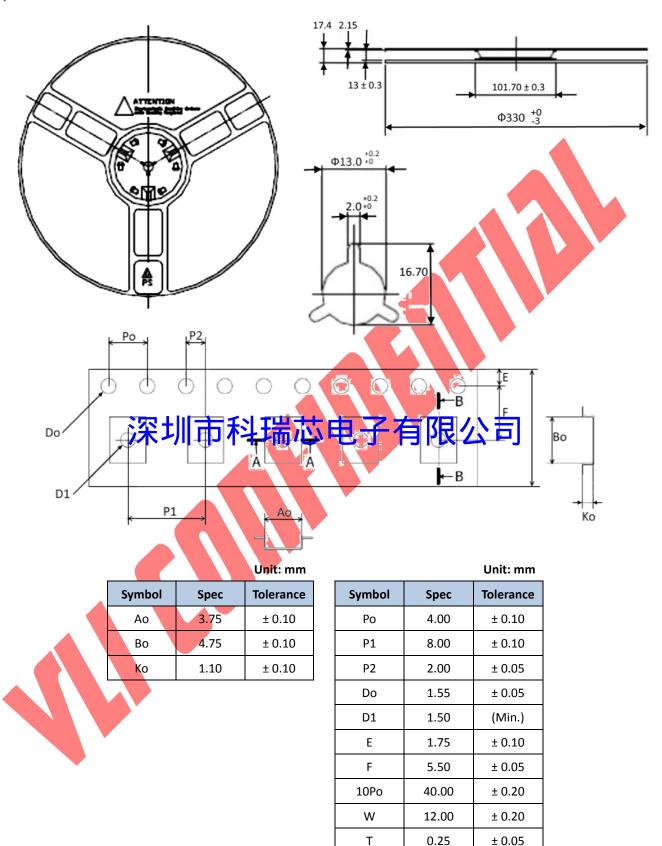


Figure 6 - Tape & Reel Information





VIA Labs, Inc.

www.via-labs.com 7F, 529-1, Zhongzheng Rd.,

Xindian District, New Taipei City 23148 Taiwan

Tel: (886-2) 2218-1838 Fax: (886-2) 2218-2553 Email: sales@via-labs.com.tw

Copyright © 2016 VIA Labs, Inc. All Rights Reserved.

No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise without the prior written permission of VIA Labs, Inc. The material in this document is for information only and is subject to change without notice. VIA Labs, Inc. reserves the right to make changes in the product design without reservation and without notice to its users.

All trademarks are the properties of their respective owners.

No license is granted, implied or otherwise, under any patent or patent rights of VIA Labs, Inc. VIA Labs, Inc. makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided by this document is believed to be accurate and reliable as of the publication date of this document. However, VIA Labs, Inc. assumes no responsibility for any errors in this document. Furthermore, VIA Labs, Inc. assumes no responsibility for the use or misuse of the information in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.