
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32G071RB
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	08/24/2022

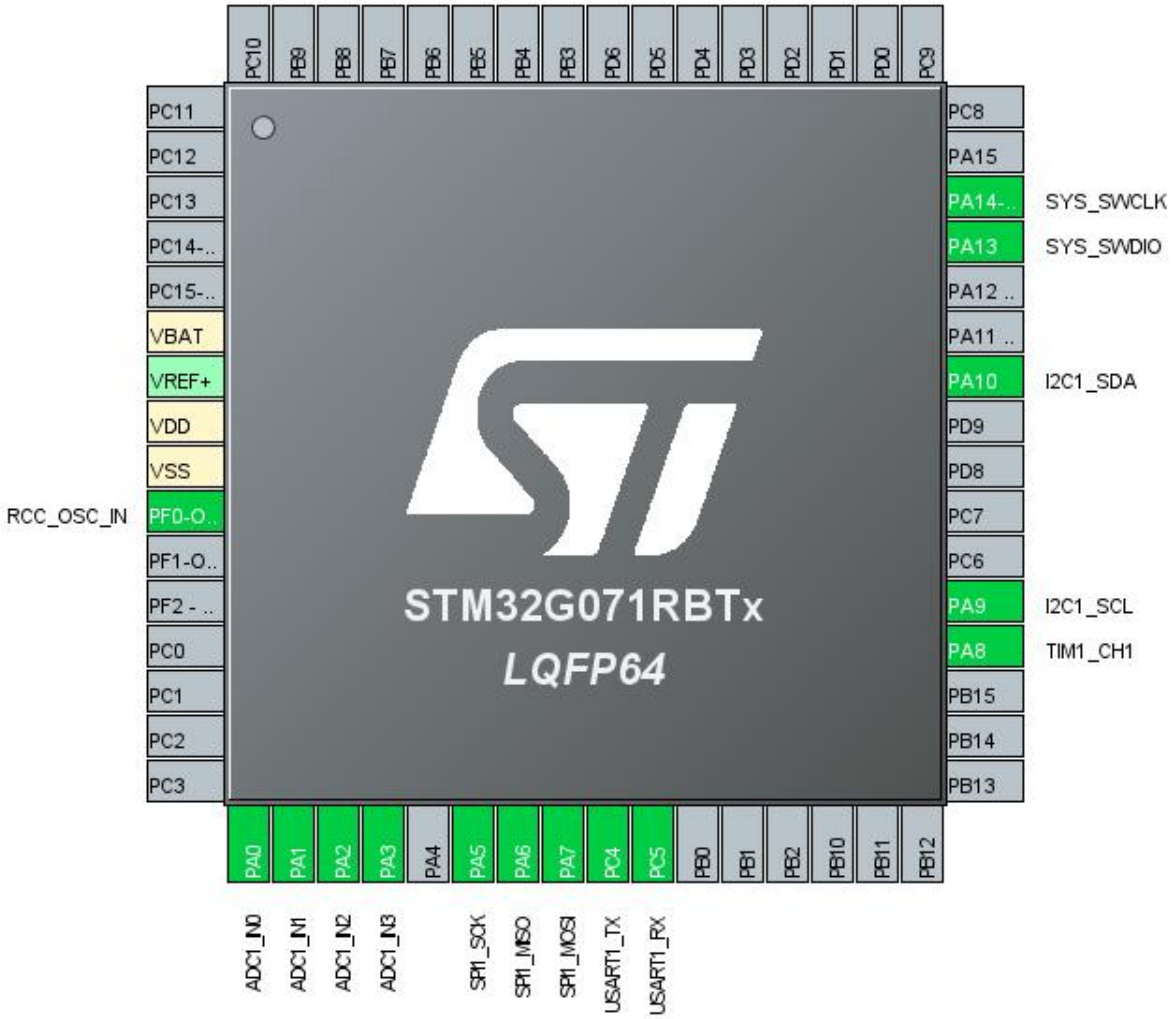
1.2. MCU

MCU Series	STM32G0
MCU Line	STM32G0x1
MCU name	STM32G071RBTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M0+

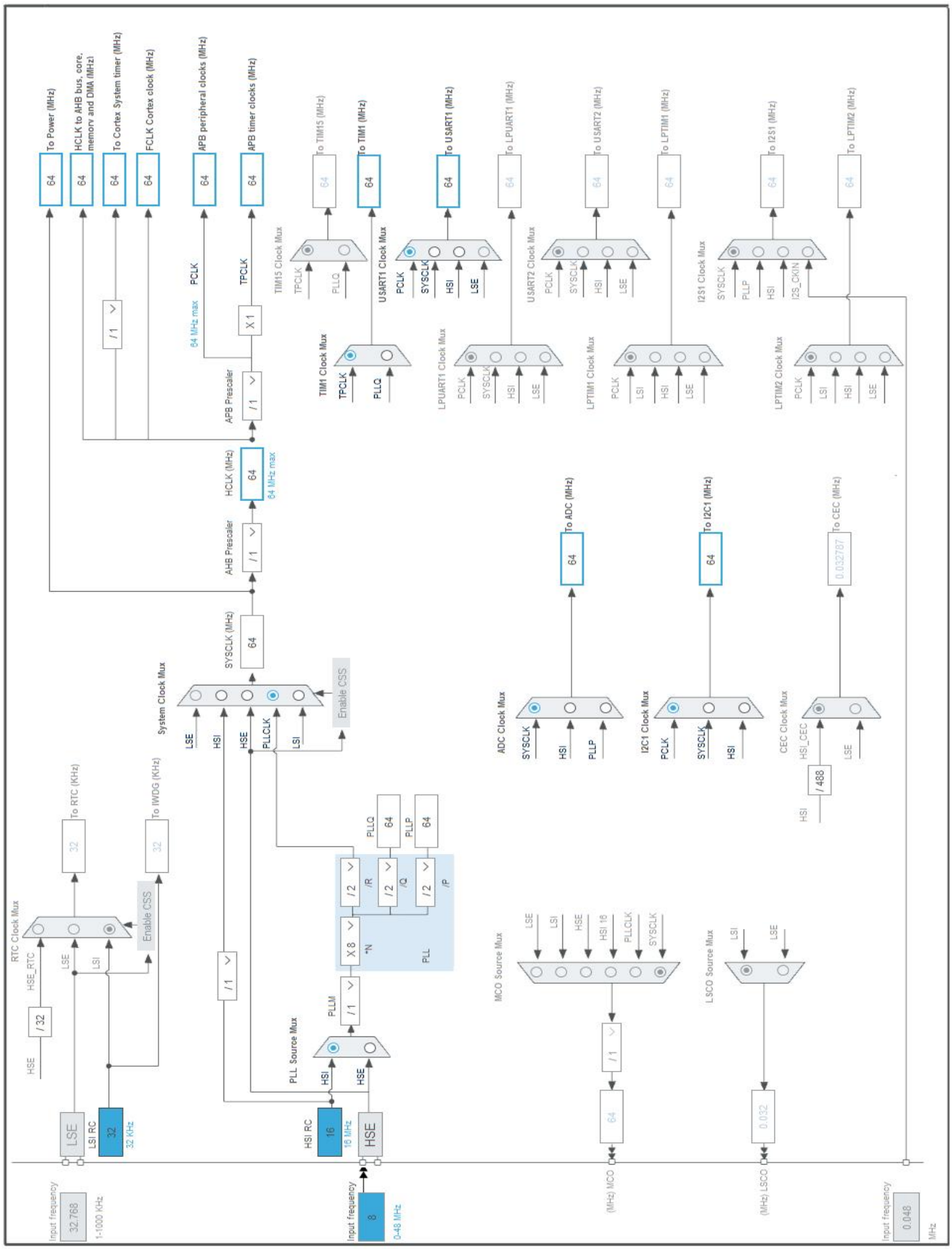
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	VDD	Power		
9	VSS	Power		
10	PF0-OSC_IN (PF0)	I/O	RCC_OSC_IN	
17	PA0	I/O	ADC1_IN0	
18	PA1	I/O	ADC1_IN1	
19	PA2	I/O	ADC1_IN2	
20	PA3	I/O	ADC1_IN3	
22	PA5	I/O	SPI1_SCK	
23	PA6	I/O	SPI1_MISO	
24	PA7	I/O	SPI1_MOSI	
25	PC4	I/O	USART1_TX	
26	PC5	I/O	USART1_RX	
36	PA8	I/O	TIM1_CH1	
37	PA9	I/O	I2C1_SCL	
42	PA10	I/O	I2C1_SDA	
45	PA13	I/O	SYS_SWDIO	
46	PA14-BOOT0	I/O	SYS_SWCLK	

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32G071RB
Project Folder	C:\Users\Lenovo\Desktop\Github\STM32G071RB
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_G0 V1.4.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_I2C1_Init	I2C1
6	MX_SPI1_Init	SPI1
7	MX_TIM1_Init	TIM1
8	MX_TIM3_Init	TIM3
9	MX_USART1_UART_Init	USART1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G0
Line	STM32G0x1
MCU	STM32G071RBTx
Datasheet	DS12232_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1

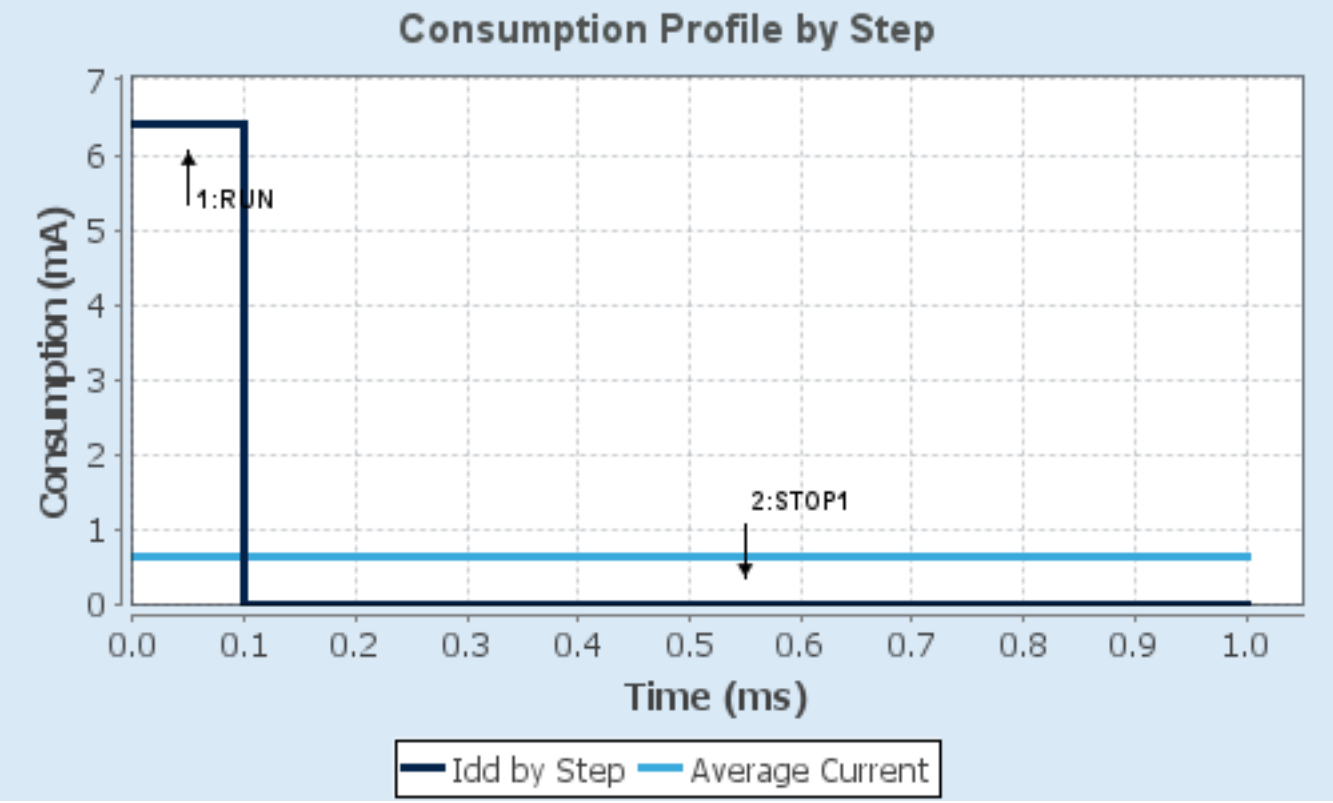
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	Flash-PowerDown
CPU Frequency	64 MHz	16 MHz
Clock Configuration	HSI PLL	HSI
Clock Source Frequency	16 MHz	16 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	6.4 mA	3.4 µA
Duration	0.1 ms	0.9 ms
DMIPS	80.0	0.0
Ta Max	128.75	130
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	643.06 µA
Battery Life	1 month, 14 days, 21 hours	Average DMIPS	80.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
7
6
5
4
3
2
1
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

mode: IN1

mode: IN2

mode: IN3

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 4
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Sequencer	Sequencer set to fully configurable
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled
Auto Off	Disabled
Oversampling Mode	Disabled

ADC_Regular_ConversionMode:

SamplingTime Common 1	1.5 Cycles
SamplingTime Common 2	1.5 Cycles
Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Trigger Frequency	High frequency
Rank	1
Channel	Channel 0
Sampling Time	Sampling time common 1
Rank	**2 ***
Channel	Channel 0
Sampling Time	Sampling time common 1
Rank	**3 ***
Channel	Channel 0
Sampling Time	Sampling time common 1
Rank	**4 ***

Channel	Channel 0
Sampling Time	Sampling time common 1

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00602173 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled

Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.4. SPI1

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**16.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.5. SYS

mode: Debug

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.6. TIM1

Channel1: PWM Generation CH1

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**159 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	**Update Event ***

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.7. TIM3

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1599 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.8. USART1

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PA9	I2C1_SCL	Alternate Function Open Drain	Pull-up	Low	
	PA10	I2C1_SDA	Alternate Function Open Drain	Pull-up	Low	
RCC	PF0-OSC_IN (PF0)	RCC_OSC_IN	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14-BOOT0	SYS_SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PC4	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	**Medium ***

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel 1 interrupt	true	0	0
ADC1, COMP1 and COMP2 interrupts (COMP interrupts through EXTI lines 17 and 18)	true	0	0
TIM1 break, update, trigger and commutation interrupts	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM3 global interrupt	true	0	0
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	true	0	0
SPI1 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel 1 interrupt	false	true	true
ADC1, COMP1 and COMP2 interrupts (COMP interrupts through EXTI lines 17 and 18)	false	true	true
TIM1 break, update, trigger and commutation interrupts	false	true	true
TIM1 capture compare interrupt	false	true	true
TIM3 global interrupt	false	true	true
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	false	true	true

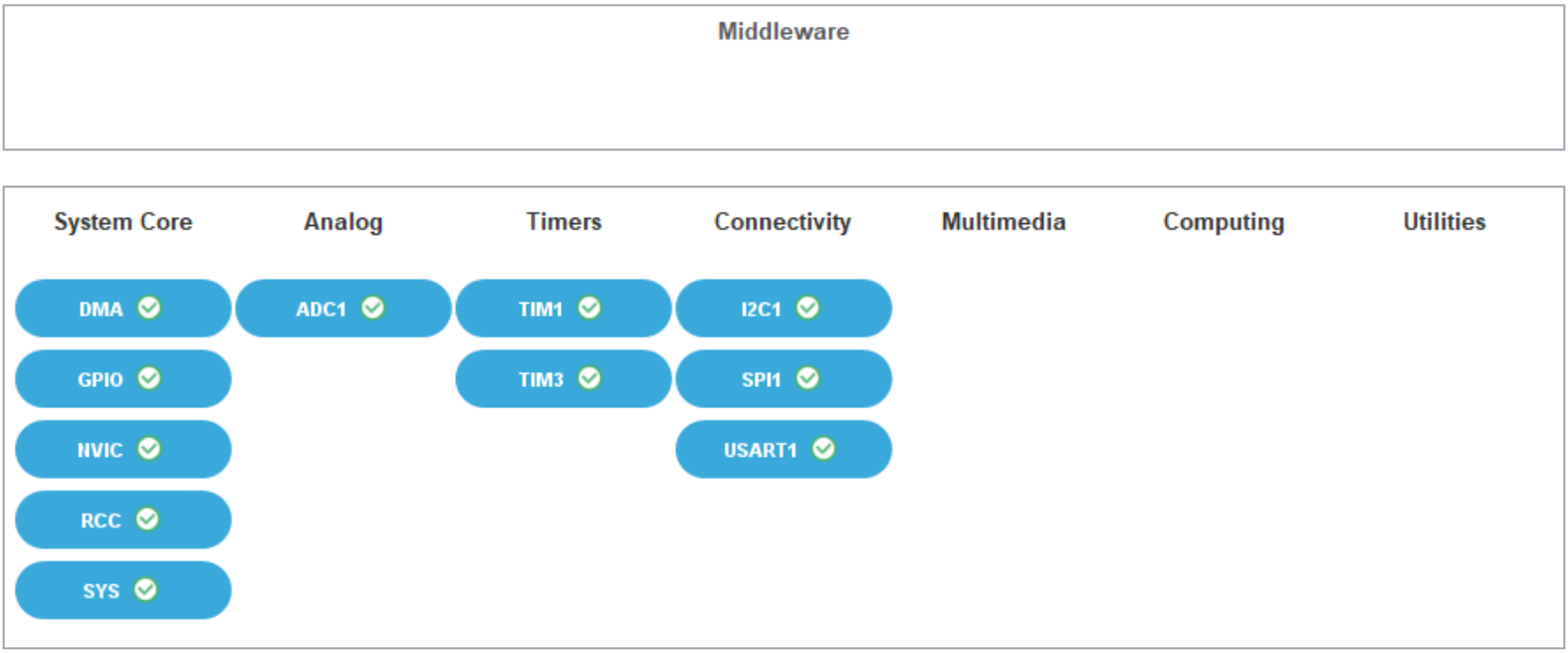
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
SPI1 global interrupt	false	true	true
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00412180.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00371828.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00104451.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00463881.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf