

1. Description

1.1. Project

Project Name	Uart-Adc-Dma-Tim-i2c-Spi
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	08/23/2022

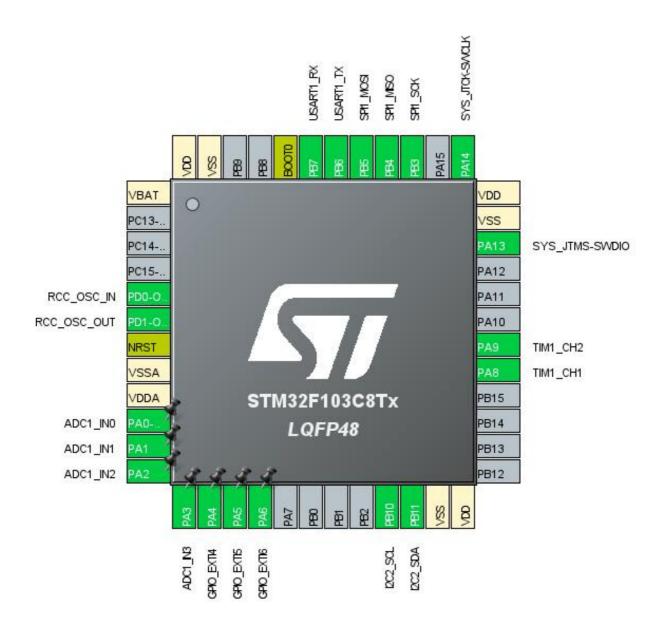
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M3

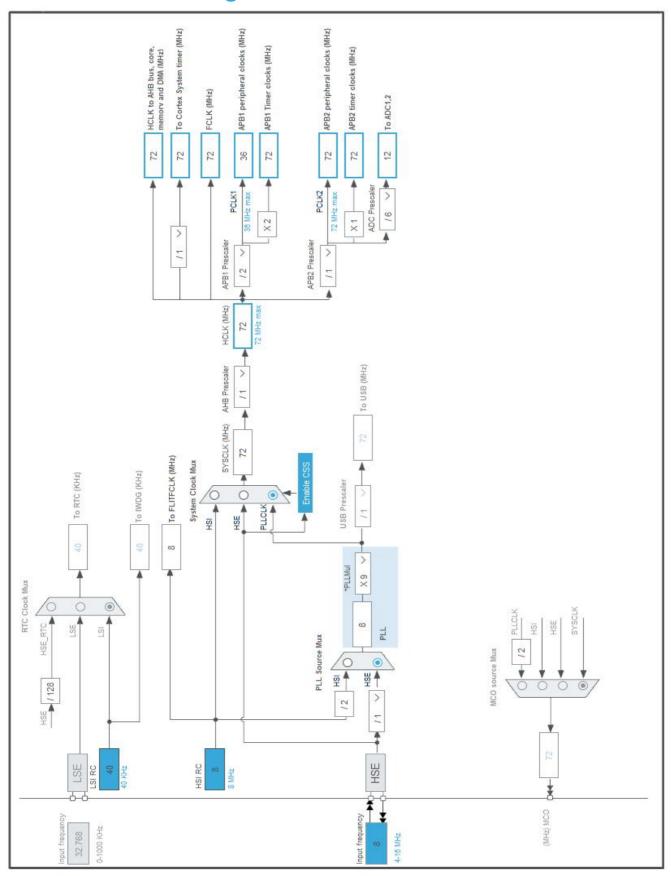
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset	1.00_000_001	
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	
11	PA1	I/O	ADC1_IN1	
12	PA2	I/O	ADC1_IN2	
13	PA3	I/O	ADC1_IN3	
14	PA4	I/O	GPIO_EXTI4	
15	PA5	I/O	GPIO_EXTI5	
16	PA6	I/O	GPIO_EXTI6	
21	PB10	I/O	I2C2_SCL	
22	PB11	I/O	I2C2_SDA	
23	VSS	Power		
24	VDD	Power		
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
39	PB3	I/O	SPI1_SCK	
40	PB4	I/O	SPI1_MISO	
41	PB5	I/O	SPI1_MOSI	
42	PB6	I/O	USART1_TX	
43	PB7	I/O	USART1_RX	
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Uart-Adc-Dma-Tim-i2c-Spi
Project Folder	C:\Users\Lenovo\Desktop\Github\Uart-Adc-Dma-Tim-i2c-Spi
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_I2C2_Init	I2C2
6	MX_SPI1_Init	SPI1
7	MX_TIM1_Init	TIM1
8	MX_TIM3_Init	TIM3
9	MX_USART1_UART_Init	USART1

Uart-Adc-Dma-Tim-i2c-Spi Project
Configuration Report

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
мси	STM32F103C8Tx
Datasheet	DS5319_Rev17

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

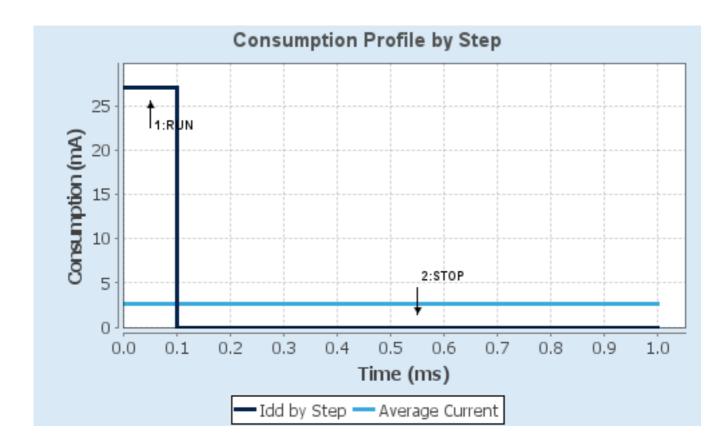
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.1	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days,	Average DMIPS	61.0 DMIPS
	17 hours		

6.6. Chart

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7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN0 mode: IN1 mode: IN2 mode: IN3

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Discontinuous Conversion Mode

Right alignment

Enabled

Enabled

Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Number Of Conversion 4 *

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 0

Sampling Time 55.5 Cycles *

<u>Rank</u> **2** *

Channel 1 *
Sampling Time 55.5 Cycles *

<u>Rank</u> 3 *

Channel 2 *
Sampling Time 55.5 Cycles *

<u>Rank</u> **4** *

Channel 3 *
Sampling Time 55.5 Cycles *

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

WatchDog:

Enable Analog WatchDog Mode false

7.2. I2C2 I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0
General Call address detection Disabled

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

7.4. SPI1

Mode: Full-Duplex Master 7.4.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 8 *

Baud Rate 9.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled NSS Signal Type Software

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. TIM1

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 6000 *

Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 99 *

Internal Clock Division (CKD)

No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Update Event *

Break And Dead Time management - BRK Configuration:

BRK State Disable BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

7.7. TIM3

mode: Clock Source

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

1599 *

Up

No Division

Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

7.8. **USART1**

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate 9600 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	
	PA1	ADC1_IN1	Analog mode	n/a	n/a	
	PA2	ADC1_IN2	Analog mode	n/a	n/a	
	PA3	ADC1_IN3	Analog mode	n/a	n/a	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	n/a	High *	
	PB11	I2C2_SDA	Alternate Function Open Drain	n/a	High *	
RCC	PD0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	n/a	High *	
	PB4	SPI1_MISO	Input mode	No pull-up and no pull-down	n/a	
	PB5	SPI1_MOSI	Alternate Function Push Pull	n/a	High *	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PB7	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
GPIO	PA4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PA5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PA6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Medium *

ADC1: DMA1_Channel1 DMA request Settings:

Mode: Circular *
Peripheral Increment: Disable

Memory Increment: Enable *

Peripheral Data Width: Word *

Memory Data Width: Word *

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	0	0
TIM1 break interrupt	true	0	0
TIM1 update interrupt	true	0	0
TIM1 trigger and commutation interrupts	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM3 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line4 interrupt	unused		
EXTI line[9:5] interrupts	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART1 global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false

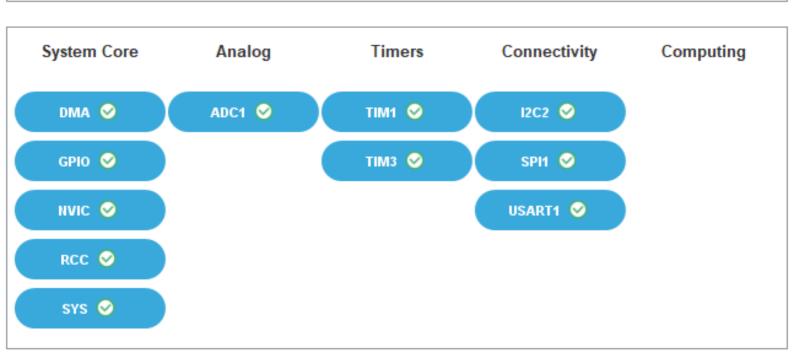
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
TIM1 break interrupt	false	true	true
TIM1 update interrupt	false	true	true
TIM1 trigger and commutation interrupts	false	true	true
TIM1 capture compare interrupt	false	true	true
TIM3 global interrupt	false	true	true
SPI1 global interrupt	false	true	true

^{*} User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current





10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/CD00161566.pdf

Reference http://www.st.com/resource/en/reference_manual/CD00171190.pdf

manual

Programming http://www.st.com/resource/en/programming_manual/CD00228163.pdf

manual

Programming http://www.st.com/resource/en/programming_manual/CD00283419.pdf

manual

Errata sheet http://www.st.com/resource/en/errata_sheet/CD00190234.pdf

Application note http://www.st.com/resource/en/application_note/CD00160362.pdf

Application note http://www.st.com/resource/en/application_note/CD00164185.pdf

Application note http://www.st.com/resource/en/application_note/CD00167326.pdf

Application note http://www.st.com/resource/en/application_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application_note/CD00249778.pdf

Application note http://www.st.com/resource/en/application_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application_note/CD00264321.pdf

Application note http://www.st.com/resource/en/application_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application_note/DM00024853.pdf

Application note http://www.st.com/resource/en/application_note/DM00032987.pdf

Application note http://www.st.com/resource/en/application_note/DM00033267.pdf

Application note http://www.st.com/resource/en/application_note/DM00033344.pdf

Application note http://www.st.com/resource/en/application_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application_note/DM00052530.pdf

Application note http://www.st.com/resource/en/application_note/DM00073742.pdf

Application note http://www.st.com/resource/en/application_note/DM00080497.pdf

Application note http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00160482.pdf http://www.st.com/resource/en/application_note/DM00156964.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00209695.pdf Application note http://www.st.com/resource/en/application_note/DM00220769.pdf http://www.st.com/resource/en/application_note/DM00257177.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00272912.pdf http://www.st.com/resource/en/application note/DM00236305.pdf Application note Application note http://www.st.com/resource/en/application note/DM00296349.pdf Application note http://www.st.com/resource/en/application note/DM00325582.pdf Application note http://www.st.com/resource/en/application note/DM00327191.pdf Application note http://www.st.com/resource/en/application_note/DM00354244.pdf Application note http://www.st.com/resource/en/application_note/DM00315319.pdf Application note http://www.st.com/resource/en/application_note/DM00380469.pdf Application note http://www.st.com/resource/en/application_note/DM00395696.pdf http://www.st.com/resource/en/application_note/DM00493651.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00536349.pdf Application note http://www.st.com/resource/en/application_note/DM00725181.pdf