

Instructions to simulate:

- Set O as the number of elements to be sorted.
- After simulation, from scope add “rg_bank” to simulation and relaunch simulation to view the final results.

The screenshot displays the Xilinx Vivado IDE interface during a simulation. It is divided into three main panels:

- Scope Panel (Left):** Shows a hierarchical list of simulation objects. The 'ms' object under the 'merge_sort' module is selected. A red arrow points from this object to the 'rg_bank' entry in the Objects panel.
- Objects Panel (Middle):** A table listing simulation objects and their current values.

Name	Value	Data T...
op[31:0]	41300000	Array
data_bus[31:0]	408b851f	Array
clk	1	Logic
res	0	Logic
rg_bank[0:6]	c0400000	Array
tempR[511:0]	00000000	Array
state[2:0]	6	Array
count[31:0]	7	Array
ind[31:0]	2	Array
startA[31:0]	0	Array
- Code Editor (Right):** Displays the Verilog source code for 'merge_sort_tv.v'. The code includes several 32-bit data bus assignments and a finish signal. Line 51, containing '#1500 \$finish;', is highlighted in yellow.