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Project Report

On

On-Chip DC/DC Boost Circuits

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1. Abstract:

The boost circuits are used to step-up the input DC voltage level to a higher DC level. These circuits find applications in mobile devices where a single input source is available, for Ex. battery and require multiple voltage levels for various components within the device. Thus the boost or buck circuits in these mobile devices generate the required voltage for different components in the device. In this project two on-chip boost circuits are designed using the boost converter and charge pump. Technology used to design these circuits is 0.5µm AMI process in cadence.

2. Introduction:

In these days portable devices are gaining significance because of their small size and mobility. The portable devices has voltage source with constant voltage supply. Power management is one of the major factor in these devices to increase the life time. All circuits within the devices need either the same voltage or other voltage level. In order to achieve higher or lower voltages, different types of battery charging circuits are used. Battery charging circuits are classified in to two types; Buck and Boost circuits. Buck circuits generate voltages less than the input voltage and boost circuits generate voltages greater than the input voltage.

Most of the battery charging circuits is designed for high voltage power applications. Thus the size of those circuits in such applications does not matter. In portable device applications the size is an issue, the battery charging circuits should be small in order to build these devices portable. Thus there is a need for designing the on-chip battery charging circuits. Two different types of on-chip boost circuits are designed to boost 1.2V of DC input to a higher voltage level.

3.Plan:

The DC/DC converter designed in [1] used United Microelectronics Corp. (UMC) 180-nm low-threshold CMOS process. The threshold voltage of MOSFET in this process is less than 100mV. A. Richelli et. al used 0.2V as the input and generated an output of 1.2V. In AMI 0.5µm process, the threshold voltage of MOSFET is 0.75V. Thus a DC/DC converter with an input

voltage of 0.2V cannot be implemented in this process. In order to implement this DC/DC boost converter we designed our circuits with different input voltages: 0.5V, 0.6V and 1.2V.

3.1 DC/DC converter with 0.5V input:

Fig.1 Block diagram of dc/dc converter

The basic building blocks of a DC/DC boost circuit are shown in Fig. 1. This includes ring oscillator, step-up converter and a boost converter.

The first step in our project is to generate a 50% duty cycle clock signal with $0.5V_{pp}$. This was generated using a ring oscillator. The second stage is a step up converter that shifts the voltage level from 0-0.5V to 0.5-1V in order to switch the transistor in boost converter. The final stage in this DC/DC converter is a boost converter that boosts the voltage to 2 - 2.5V.

Sub-blocks:

3.1.1 Ring oscillator:

A Ring oscillator is a circuit that generates a square wave with power supply rail as input. The ring oscillator is a chain of odd number of inverters that oscillates periodically from high voltage to low voltage or vice-versa. The feedback for the oscillator is designed by connecting the output of last stage to the input of first stage. The width of MOSFETS in each inverter stage is made 10 times the dimension of a simple inverter.

The ring oscillator is given preference in our design over the other oscillators as its design is simple occupies low silicon area when integrated on a chip. Moreover, a ring oscillator generates a superior square wave when compared with other oscillators. In our project we designed a ring-oscillator with a optimum number of stages 9 to obtain a square wave with

maximum frequency for 0.5V of supply. As the number of stages was increased the frequency was reduced. When the number of inverter stages was reduced below the optimum number, the output of the ring oscillator was triangular due to the low delay in switching. Fig. 2 shows schematic of the ring oscillator.

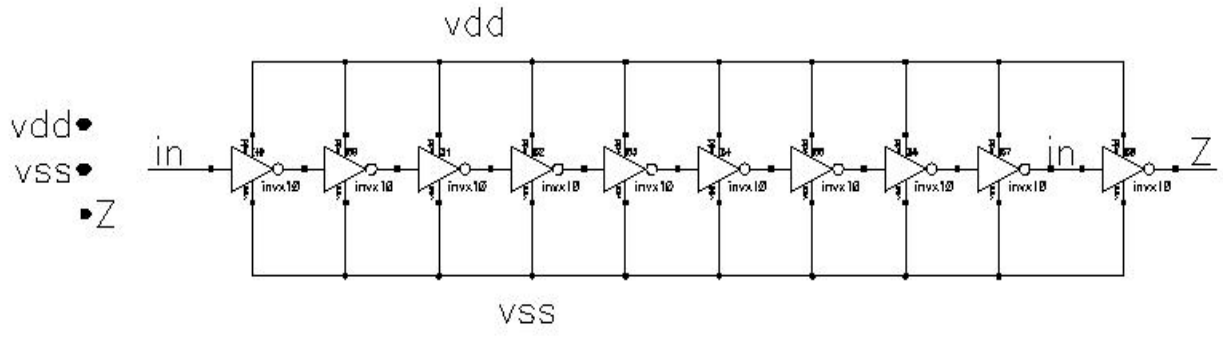

Fig.2 Ring oscillator schematic

The dimensions of NMOS and PMOS in inverter are 18µm/0.6µm and 54µm/0.6µm respectively. In 0.5µm AMI process technology, the threshold voltage of N-MOS is 0.75V and P-MOS is 0.95V. Even though the threshold voltages are higher than supply voltage, the ring oscillator was capable of generating a clock signal of 0.5V peak to peak with a frequency of 1.2K Hz.

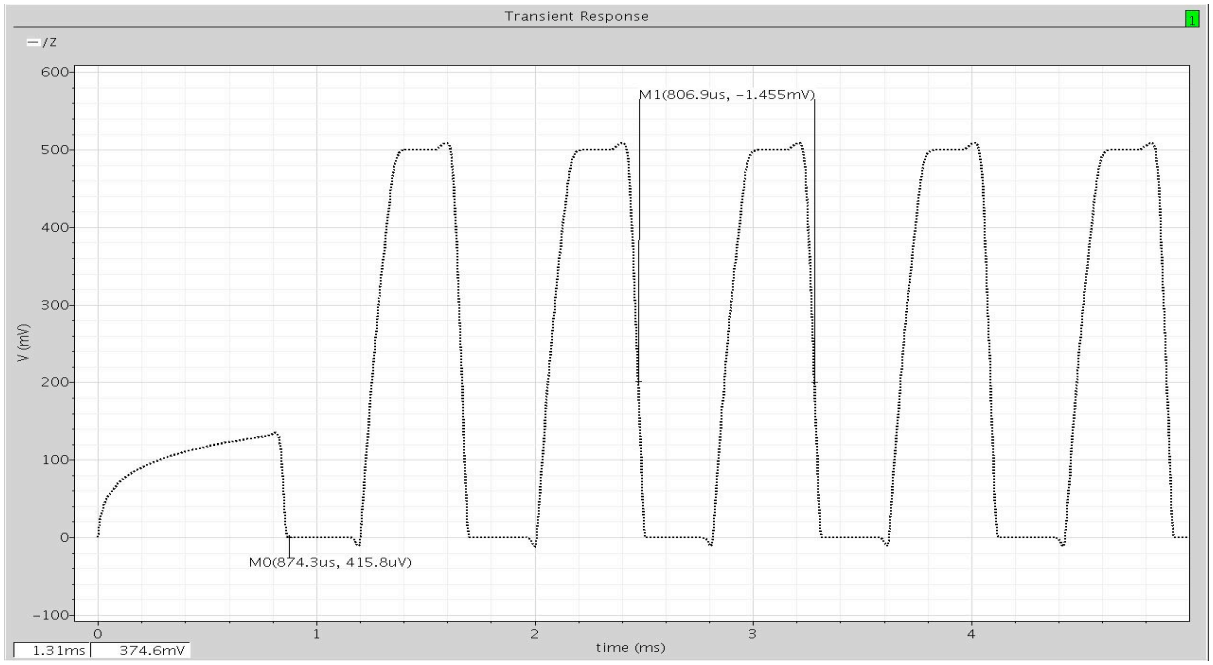

Fig 3. Simulation result of Ring Oscillator

Fig. 3 shows the simulation result of the ring oscillator. The result shows a delay of 874µs before the actual oscillation starts. This delay is the first cycle and the ring oscillator starts working from the second cycle. Furthermore, the duty cycle of the ring oscillator can be varied by obtaining the output at various stages and performing an OR operation on it.

3.1.2 Step-up converter:

The circuit for the step-up converter shown in [1] cannot be implemented in the AMI 0.5µm process. Thus we designed a new step-up converter using an inverter, N-MOS transistor and a capacitor.

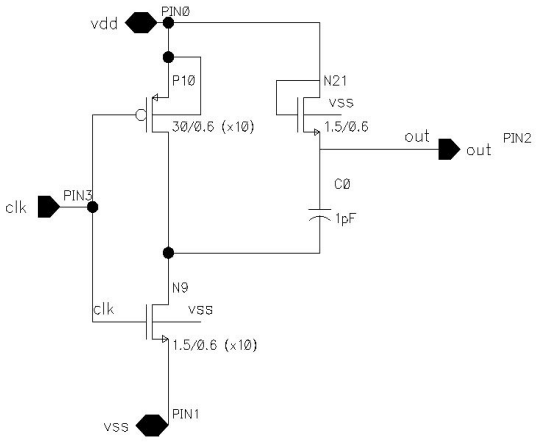

Fig 4. Step-up converter with N-MOS as diode connected transistor

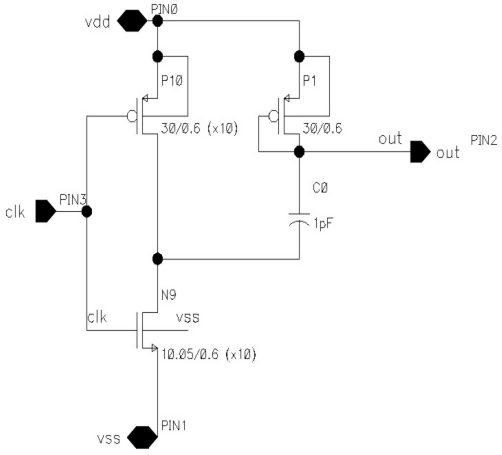

Fig 5. Step–up converter with P-MOS as diode connected transistor

In this circuit the N-MOS transistor is designed as a diode connected transistor. A capacitor is connected to the source of the diode-connected transistor and the other end is connected to inverter output as shown in fig.4. The output of the ring oscillator is given to the input of a inverter of step-up converter. This circuit could not shift the voltage to the required level of threshold value (0.75V) as shown in fig.6. Thus, we changed the design by altering the N-MOS diode connected transistor with a P-MOS diode connected transistor as shown in fig.5. Though the circuit could shift the voltage to a superior level than the previous circuit, but it could not reach the desired level as shown in fig.7. The simulation results Fig. 6 and 7 show that the maximum output voltage was around 0.7V.

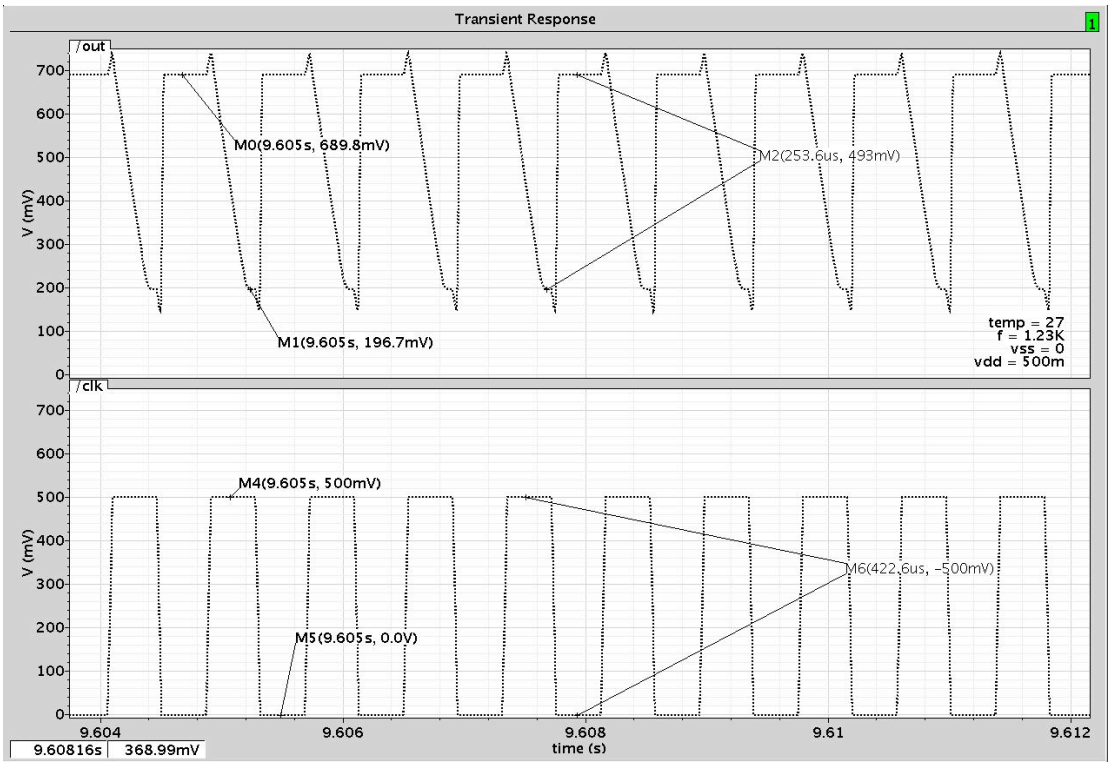

Fig 6. Simulation result of step-up converter of fig.4

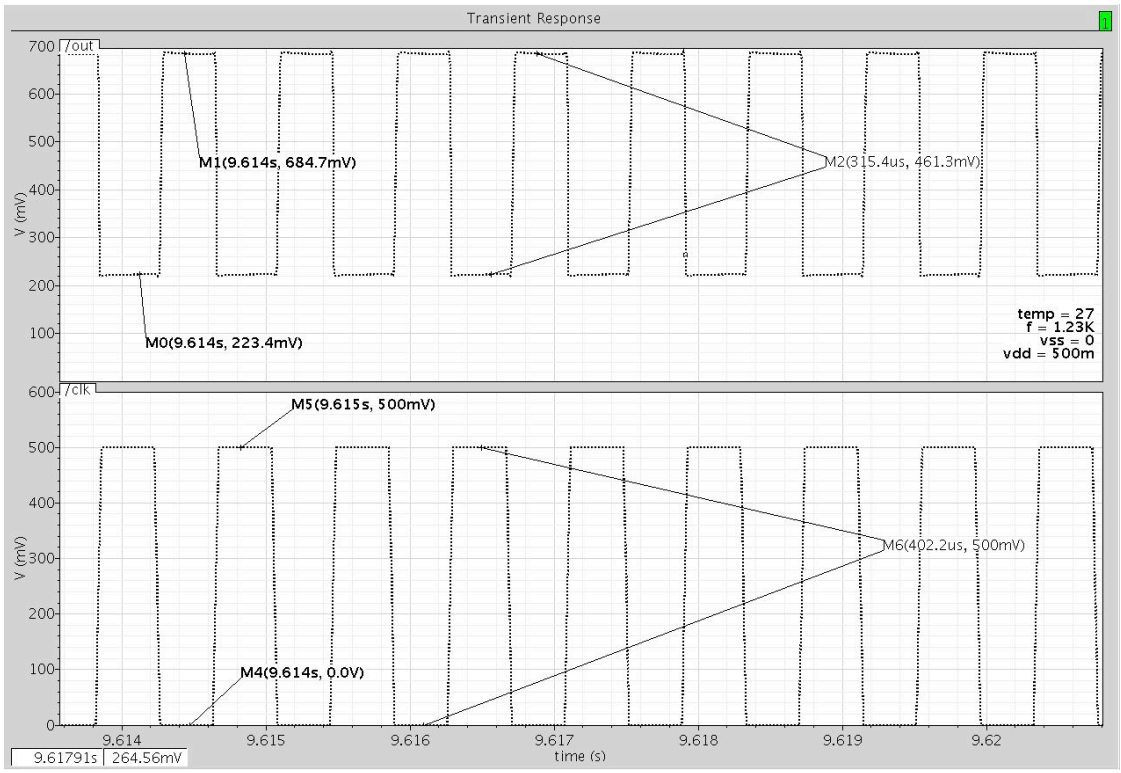

Fig 7. Simulation result of step-up converter of fig.5

In order to enhance the voltage to the desired level silicon diode was employed, as it has lower bias voltage. The PMOS silicon diode is connected as shown in fig. 8. As the drop across the silicon diode is less, it shifted the voltage to the required level (0.5V-1V).

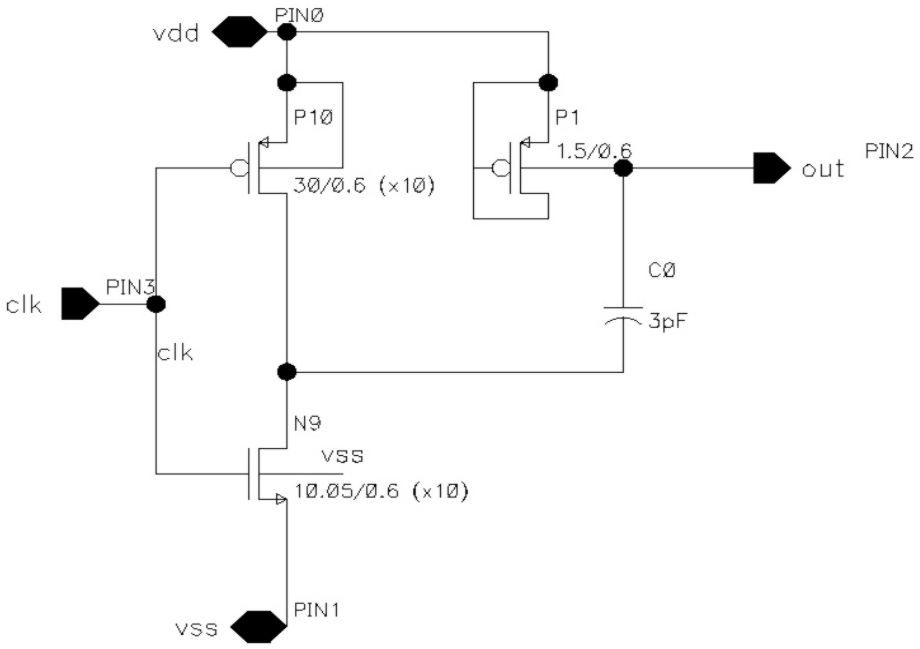

Fig 8. Step-up converter with silicon diode

How Silicon Diode works:

The transistor P1 in fig. 8 is a PMOS silicon diode whose gate, source and drain are connected together and are given a voltage of vdd (0.5V). As the gate and source are at the same potential there exists no channel between source and drain for the current to flow. The bulk of the PMOS is a N-well and the output is attained from it. As the source and drain of the PMOS are P type material and N-well is a N type material, two parasitic PN junction diodes are created in the PMOS transistor. Thus the transistor acts as a diode. The circuit in fig. 8 is simulated and the results obtained are plotted as shown in fig. 9. The output of the step-up is given to the charge pump

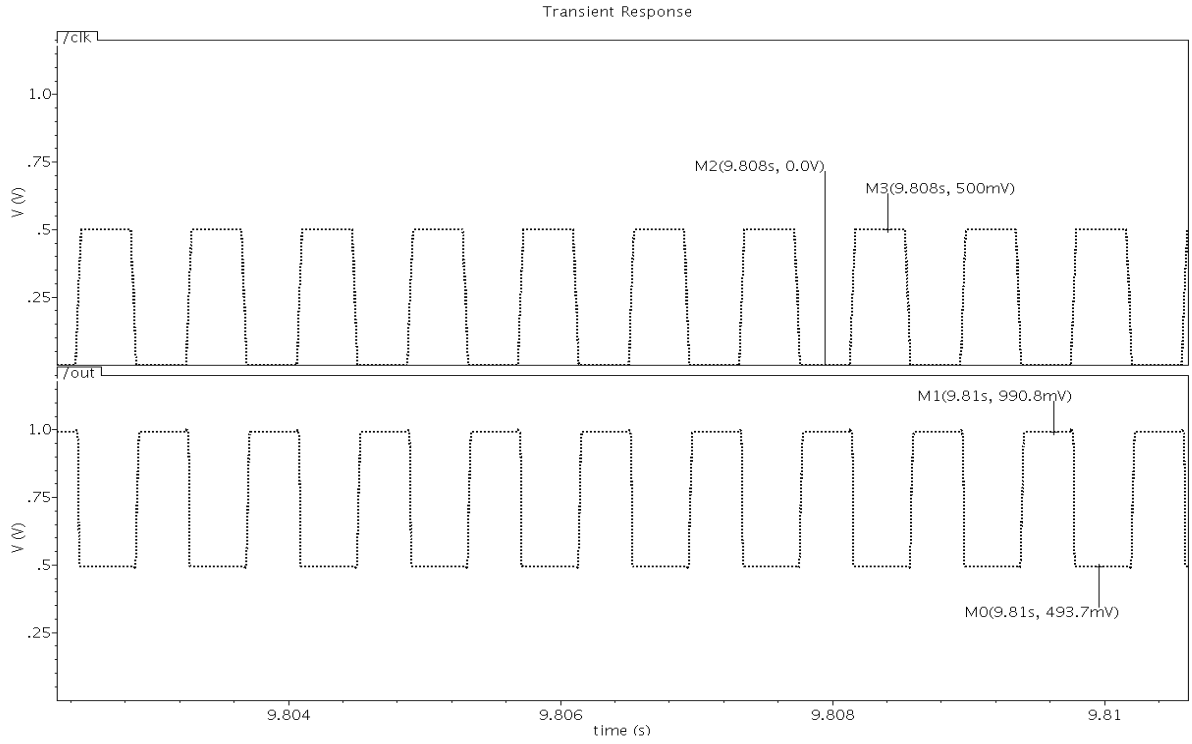

Fig. 9. Plots of step-up converter simulated with capacitor load of 10fF.

3.1.3 Charge Pump:

A charge pump was used in [1] to boost the output voltage. Following is analysis of the charge pump circuit proposed in [1], shown in fig.10.

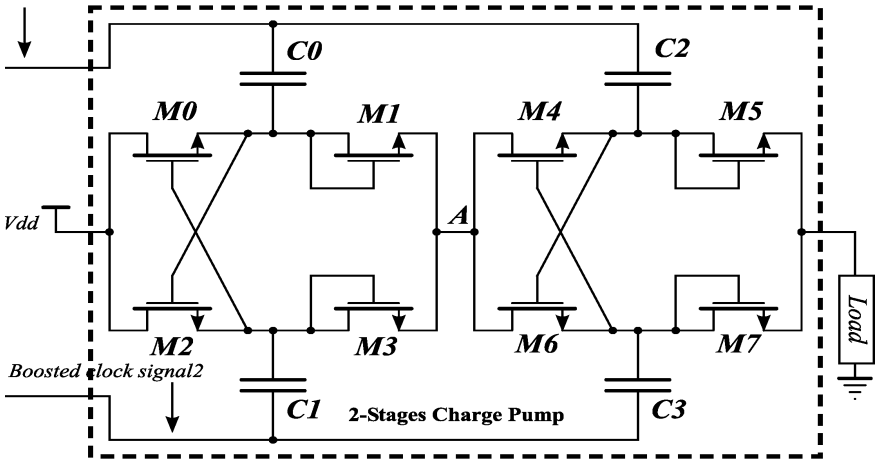

Fig 10. Charge pump circuit proposed in [1]

Two non-overlapping clock signals are given as inputs to the two-stage charge pump circuit. When clock signal1 is high, the capacitor C0 and C2 will charge up to high voltage of clock (0.8V in [1]). The diode connected transistors M1 and M5 will turn ON passing the voltage with a threshold drop to node A and output node respectively. The voltage at capacitor C0 and C2 will turn ON the pass transistors M2 and M6 charging the capacitor C1 and C3 to vdd and voltage at node A respectively with a threshold drop. Since the voltage at C1 and C3 is less than the voltages at nodes A and the output respectively, the diode connected transistors M3 and M7 will act as reverse biased diodes and thus are OFF. Therefore, the output voltage is equal to voltage at capacitor C2 with a threshold drop.

As the clock signal1 goes to a low voltage the capacitors C0 and C2 are discharged to 0V. When the clock signal2 is high, the capacitors C1 and C3 will charge up to a voltage equivalent to the sum of the clock signal voltage and the previously accumulated charge at the capacitors C1 and C3, turning ON the transistors M0 and M4. This again charges the capacitors C0 and C2 to a voltage of vdd and a voltage A respectively with a threshold voltage drop. The diode connected transistors M3 and M7 are ON generating a voltage at the output node equivalent to the voltage at the capacitor C3 with a threshold drop.

As the process continuous, the output remains at a constant voltage 1.2V as mentioned in [1]. Moreover, in [1] the input voltage is 0.2V and the threshold voltage of the transistor is less than 100mV. Therefore, Richelli et. al could generate a clock signal with peak to peak voltage of 0.8V. In 0.5 AMI process technologies this cannot be implemented and the voltage drop at each charge pump stage increases with stages and reduces the strength of the output signal. This was observed when the charge pump circuit was designed and simulated. Fig.11 shows the simulated results at the first and second stage of charge pump circuit. In order to acquire the desired voltage of 2-2.5V at the output, we designed another boost circuit.

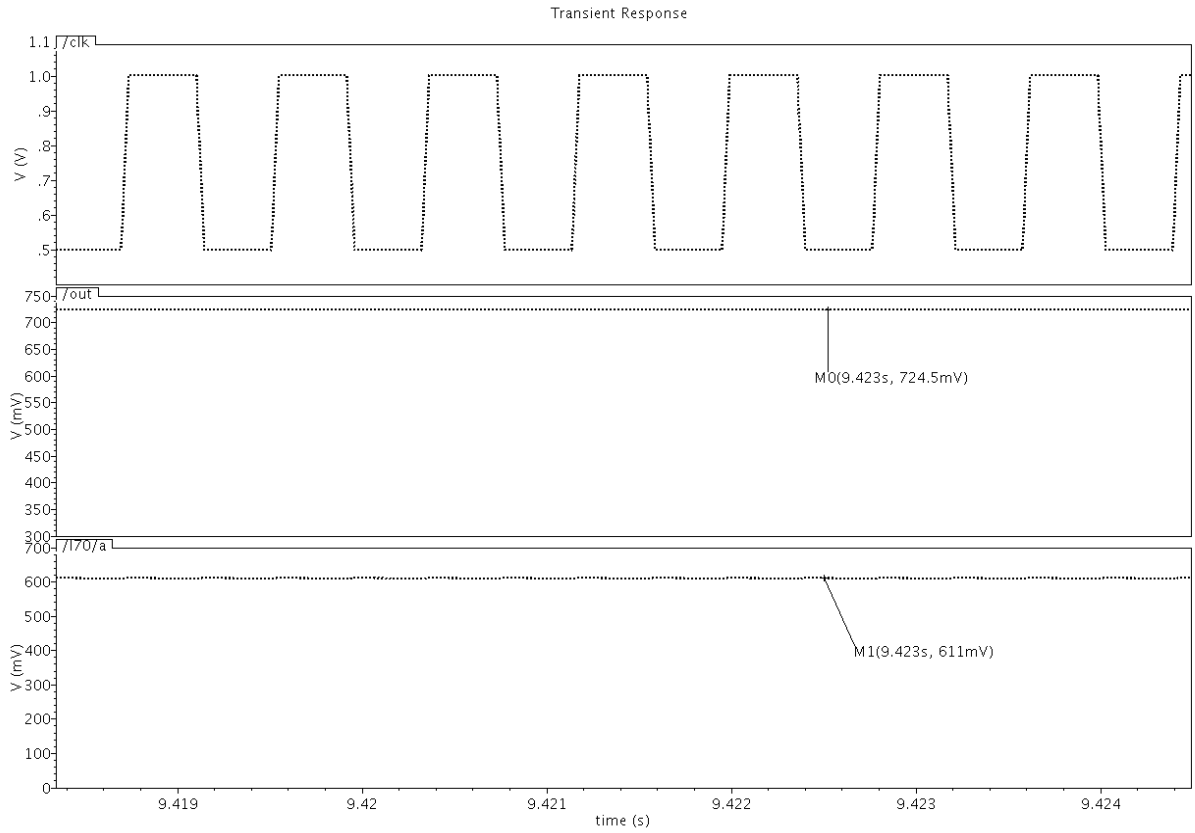

Fig. 11. Outputs of the 1-stage (a) and 2-stage (out) charge pumps.

3.1.4 Boost Converter:

The schematic of the boost circuit is shown in fig.12. The components in the boost circuit are inductor, MOSFET as switch, diode connected transistor, capacitor and resistor. The value of inductor is selected as 2.5H as it draws a current of 100uA for 0.5V input. As the size of the inductor is reduced the change in current is increased which is not desired for the MOSFET. In order to handle large currents the size of the MOSFET is increased as shown in fig.12.

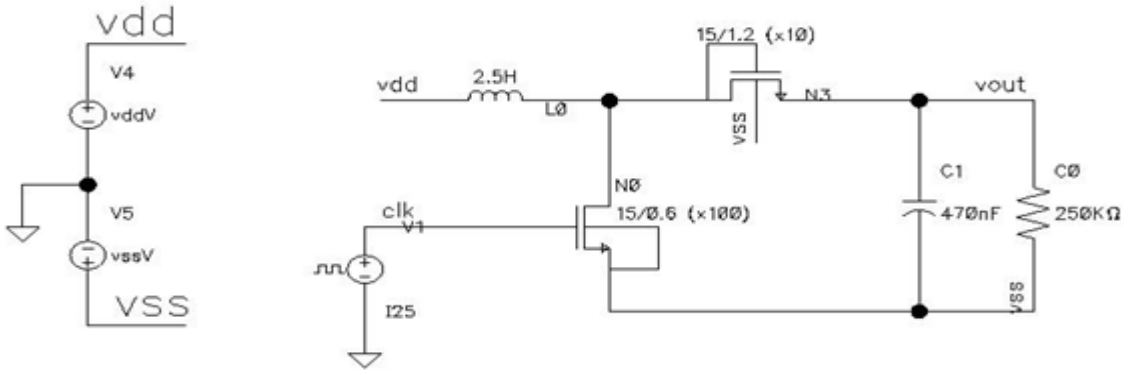

Fig. 12. Schematic of the boost converter

The simulation failed when all the blocks are connected and simulated. The output of the step-up converter should switch the switching transistor ON and OFF. When simulating the step-up converter for more than 10sec it was observed that the current was increasing as shown in fig.13. This is due to the current flowing through the PNP transistor formed by the drain/source, n-well and the p-substrate. This process is known as latch-up and it is not desire in MOSFET. The output started to decrease as shown in fig. 13.

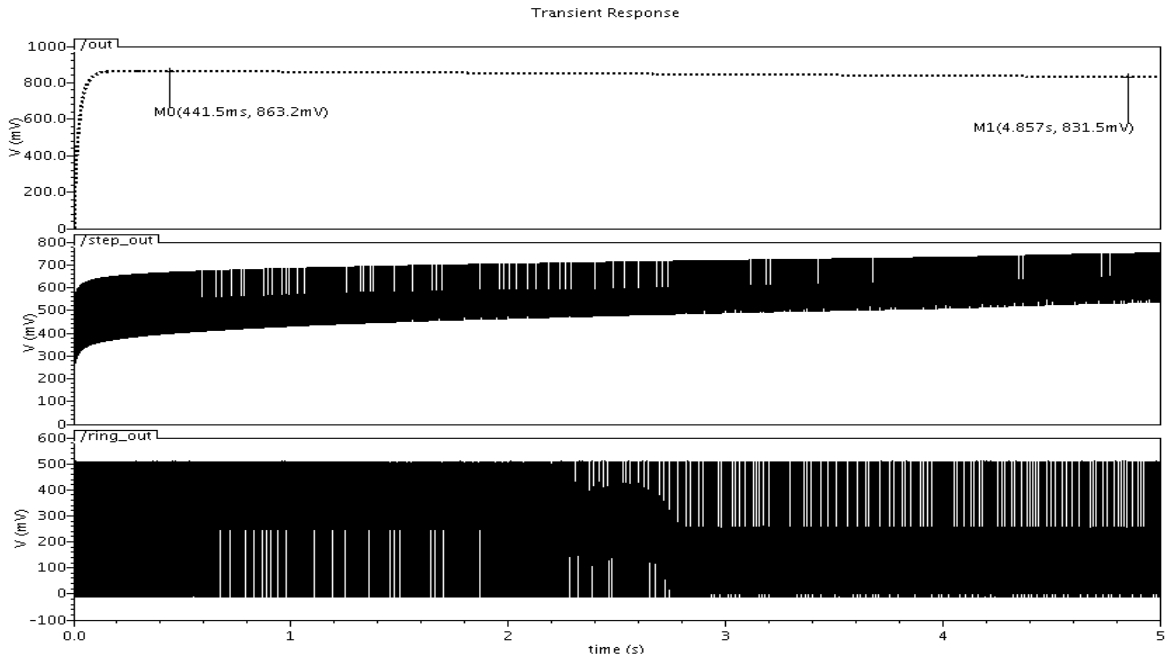

Fig. 13. Outputs when the step-up is simulated with boost converter as the load.

In order to overcome this drawback we designed the step-up converter as shown in fig. 14. The silicon diode of fig. 8 is replaced with the diode-connected transistor that was designed previously as shown in fig. 4. The dimensions of this diode-connected transistor are increased in order to block the reverse leakage current.

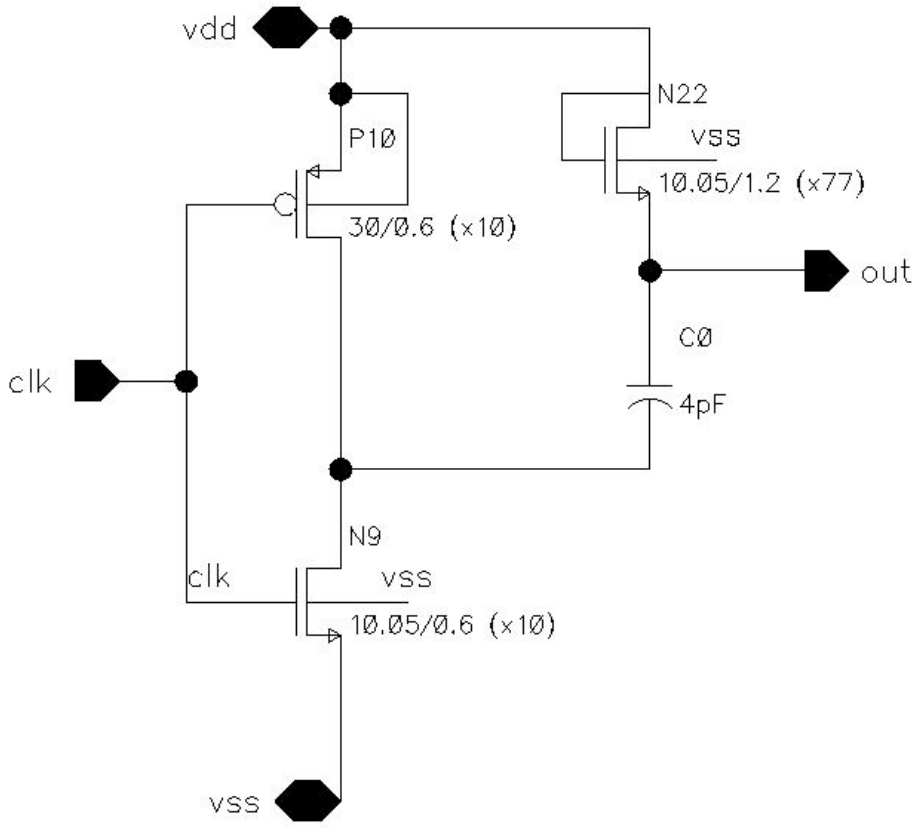

Fig. 14. Schematic of the modified Step-up converter.

The entire design is simulated with the modified step-up converter and the results are plotted as shown in fig.15 & 16. It was observed that the output for 50% duty cycle was 1.12V for 0.5V input. The load capacitance is 470 nF and resistance is 250 KΩ.

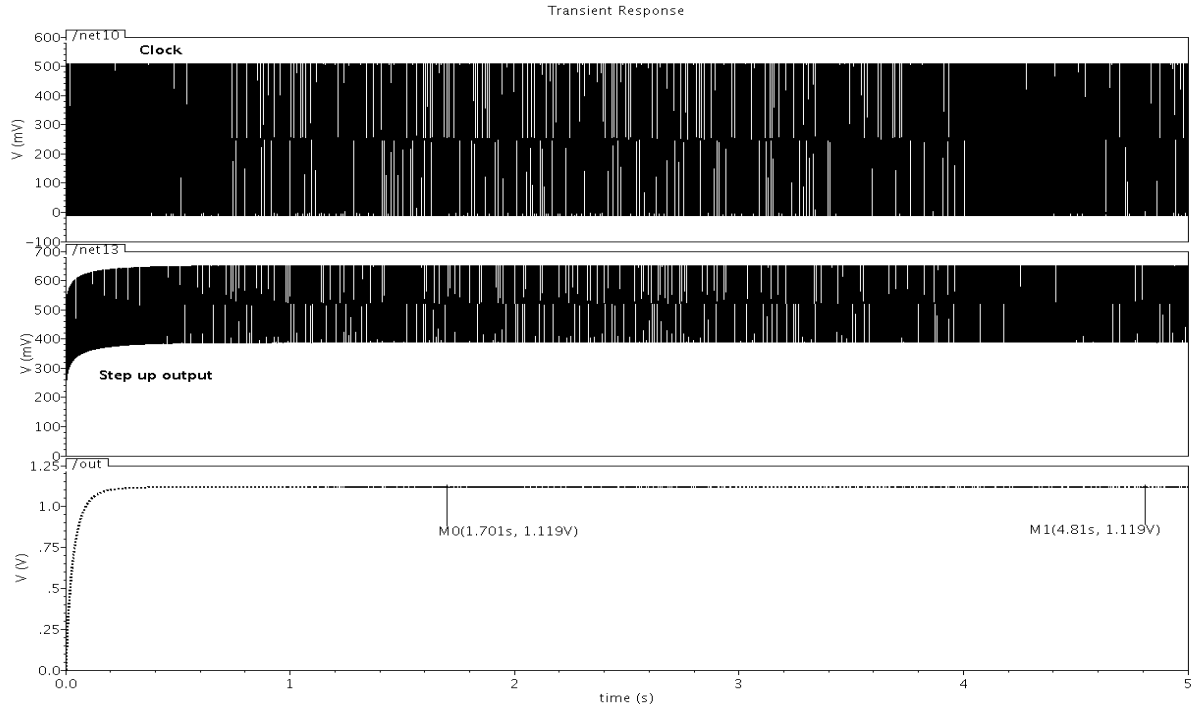

Fig. 15. Boost converter output simulated for 5 sec.

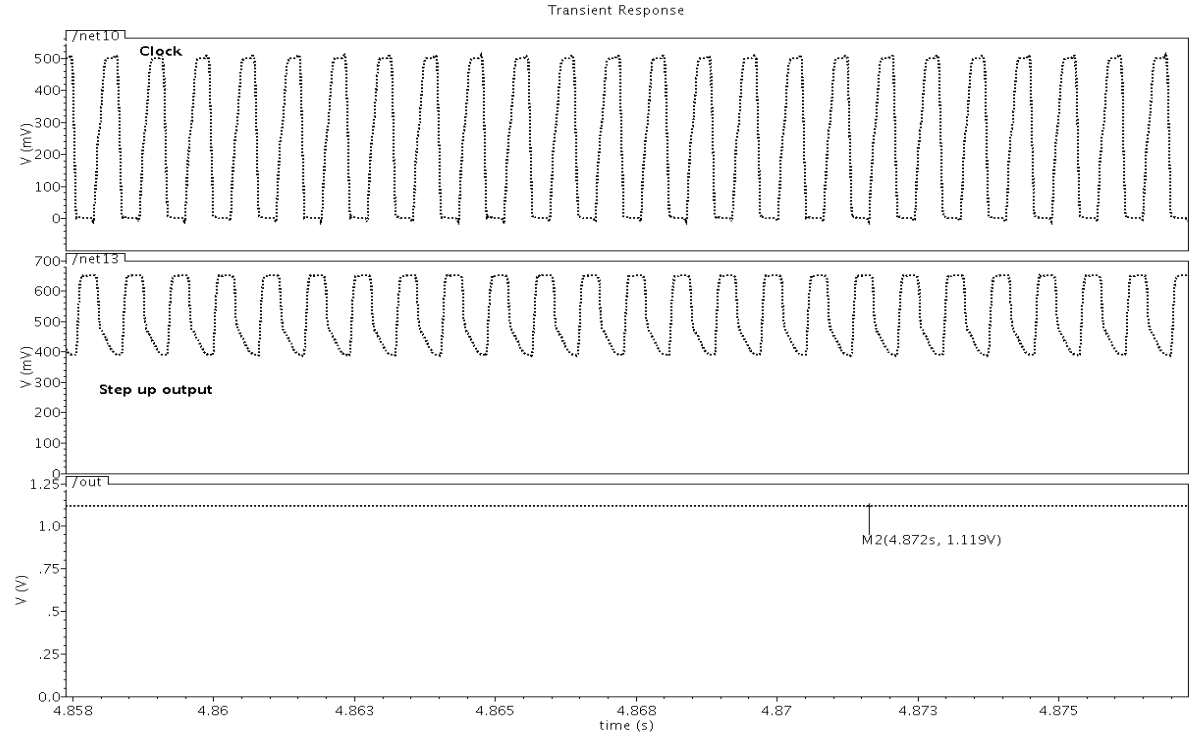

Fig. 16. Boost converter zoomed output.

As the inductor value is very large (2.5H), we had to optimize the design parameters. The inductor value is constrained by the frequency of the ring oscillator. Thus increasing the input voltage level increased the frequency of ring oscillator.

3.2 DC/DC Converter with 0.6V input:

We simulated the boost converter as shown in fig. 17 with an input voltage of 0.6V that gives an output frequency of 10 KHz from the ring oscillator. The change in frequency and the input voltage the inductor value was reduced to 300 mH. This gave us the boosted output of 1.3 V for a duty cycle of 50% as shown in fig. 19.

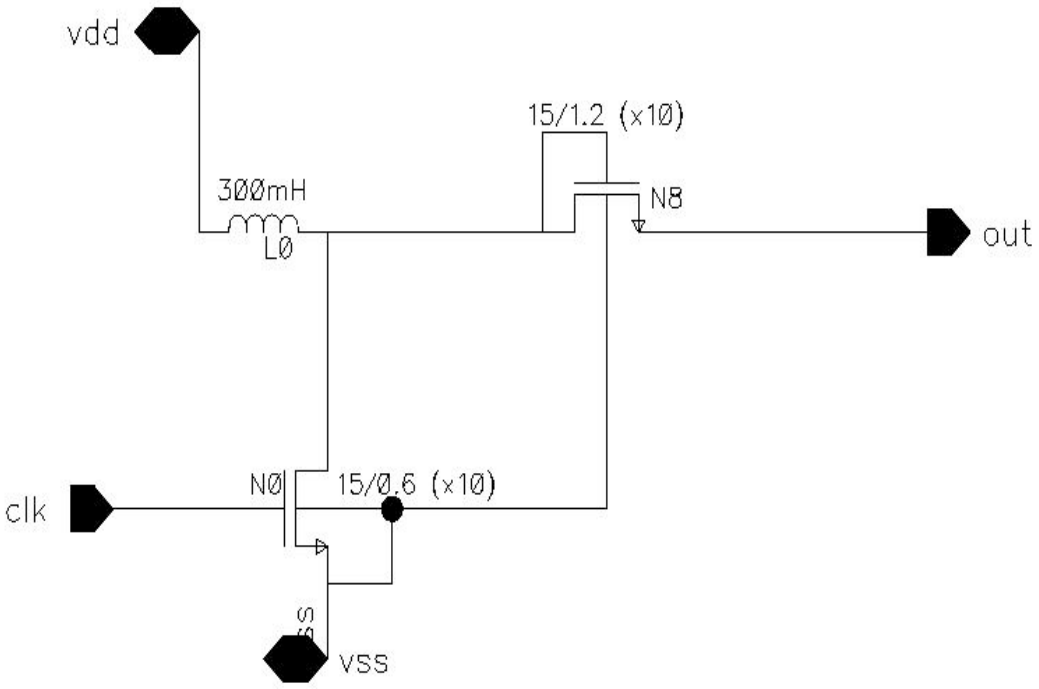

Fig. 17. Schematic of boost converter.

Fig. 18 shows the test bench for the complete design. The capacitor and resistor are the connected externally for the boost circuit.

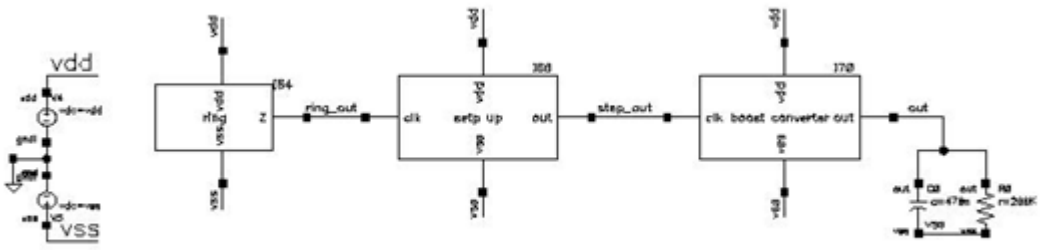

Fig. 18. Test Bench for the boost converter.

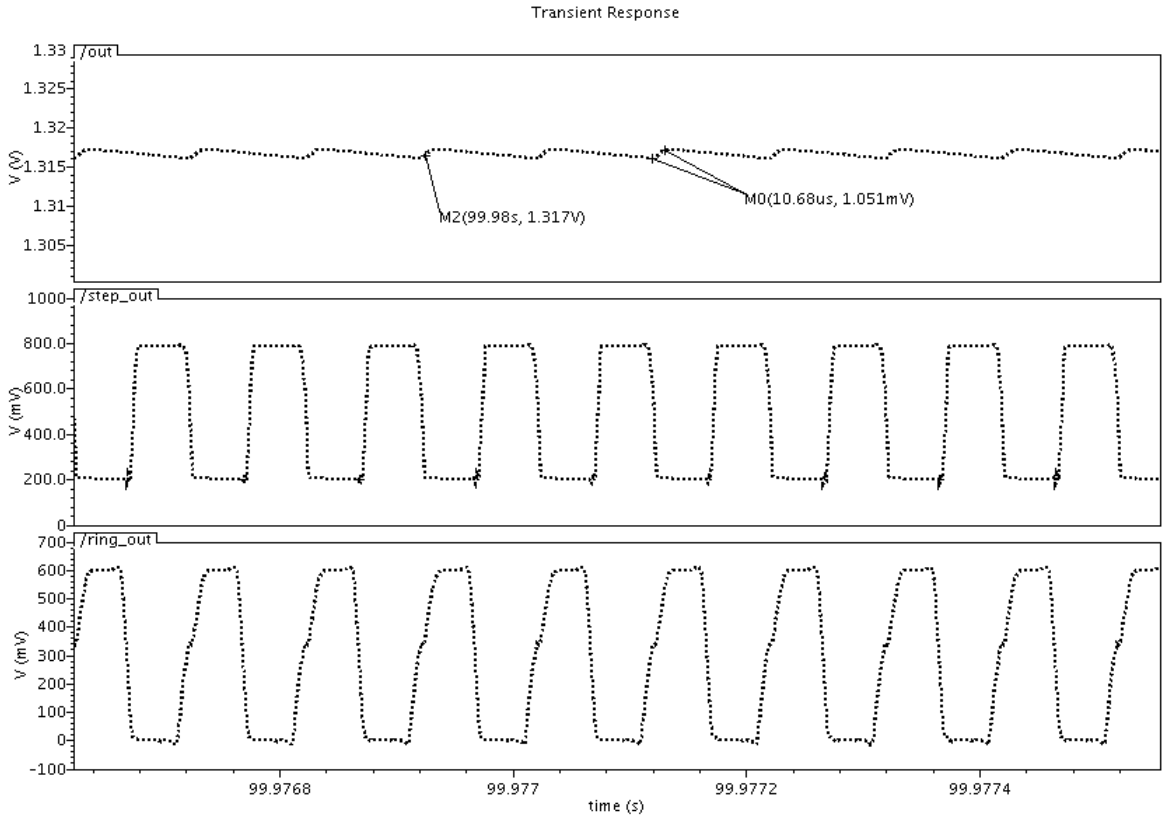

Fig. 19. Simulation results for the boost converter with input of 0.6 V.

As 300mH inductor was considered still a large value, we have stepped-up our input voltage level to 1.2 V (energy band-gap reference voltage).

3.3 DC/DC converter with 1.2V input:

The frequency of the ring oscillator was increased to 18MHz with the increase in input voltage and the number of stages to 17. Moreover, it reduced the inductance value to 1mH. Load Capacitance and resistance of the boost converter were changed to 2 pF and 2 MΩ. The design for 1.2V input does not require a step-up converter to switch the transistor in boost circuit. Thus the circuit with ring oscillator and boost converter was simulated. The output of boost converter was 2.75V for 50% duty cycle clock as shown in fig. 20

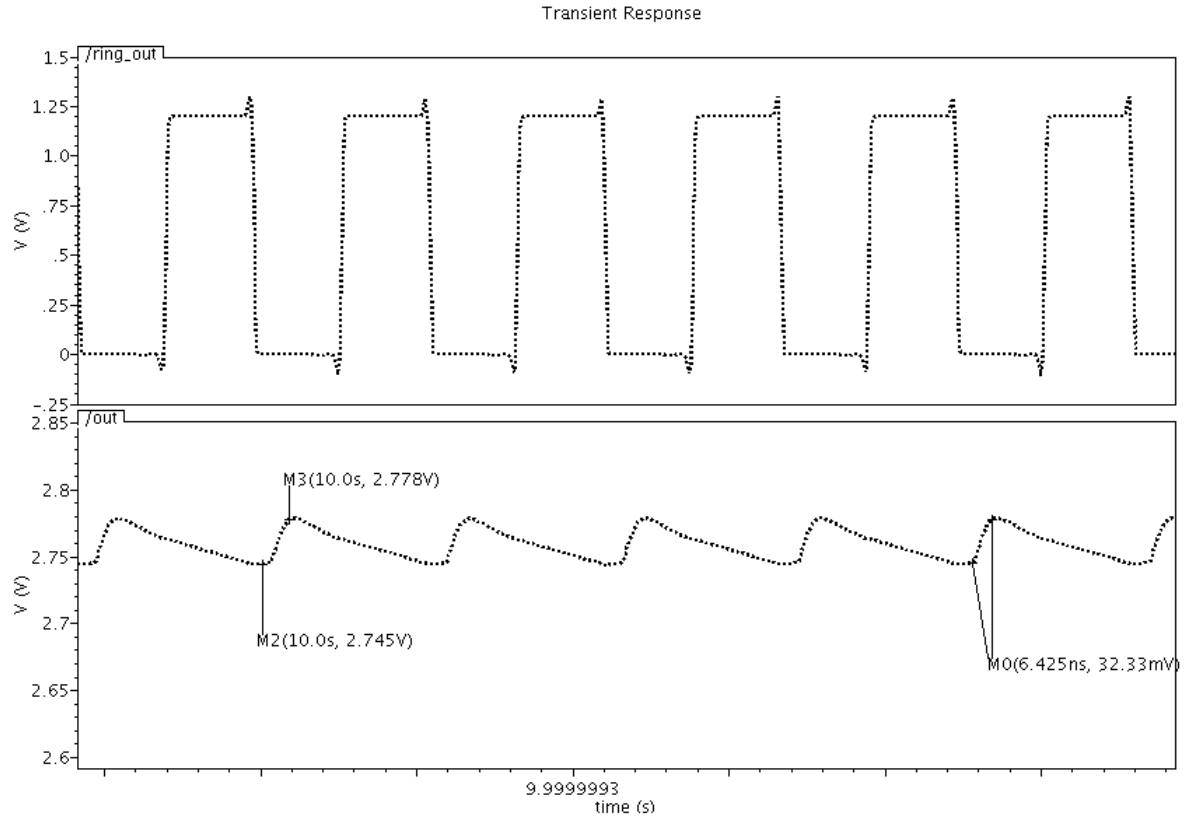

Fig. 20. Simulation result of the boosted output for 50% duty cycle.

In order to obtain desired voltage of 4V-4.5V at the output, the duty cycle of the clock signal was increased to 70%. The simulated results for 70% duty cycle are shown in fig. 21.

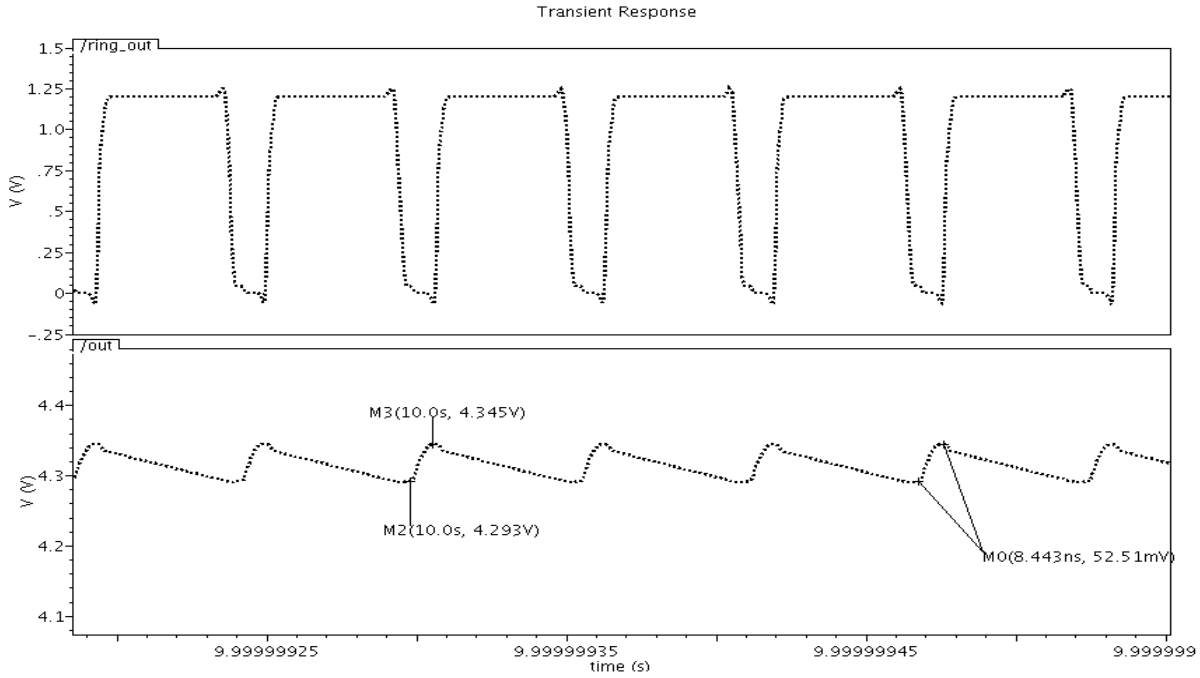

Fig. 21. Boost converter output for a duty cycle of 70%.

In order to design the entire circuit On-Chip we implemented charge pump circuit.

3.4 Charge pump for an input voltage of 1.2 V:

The charge pump can be designed On-chip as it has no inductor present in the circuit. A two-stage charge pump is shown in Fig. 22. The output from the ring oscillator is given to the charge pump and the circuit was simulated. The results obtained are shown in fig. 24. The output of the two-stage charge pump is 2.6V. The ripple at the output was almost negligible. In order to increase the output voltage to a higher level, initially the duty cycle was varied. This had no effect on the output. Thus to increase the output voltage the number of stages of the charge pump were increased to three as shown in fig. 25. This resulted in an output of 3.3V with a ripple of 86.99mV as shown in fig. 26.

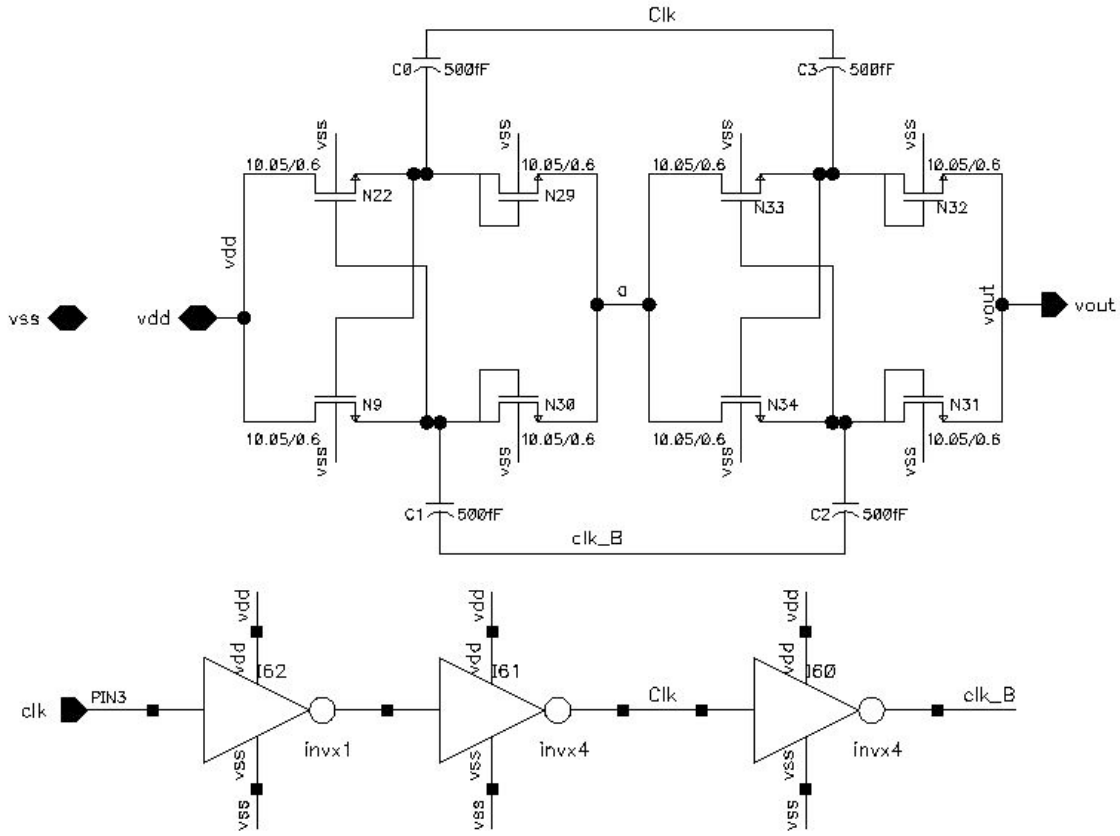

Fig. 22. Schematic of a 2-stage charge pump.

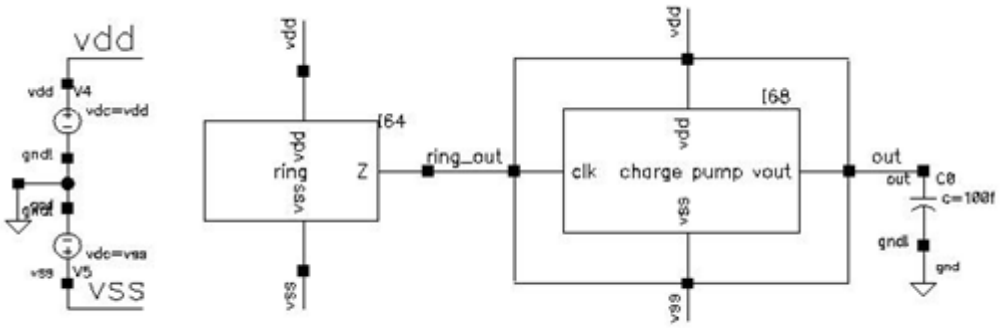

Fig. 23. Test Bench for 2-stage charge pump.

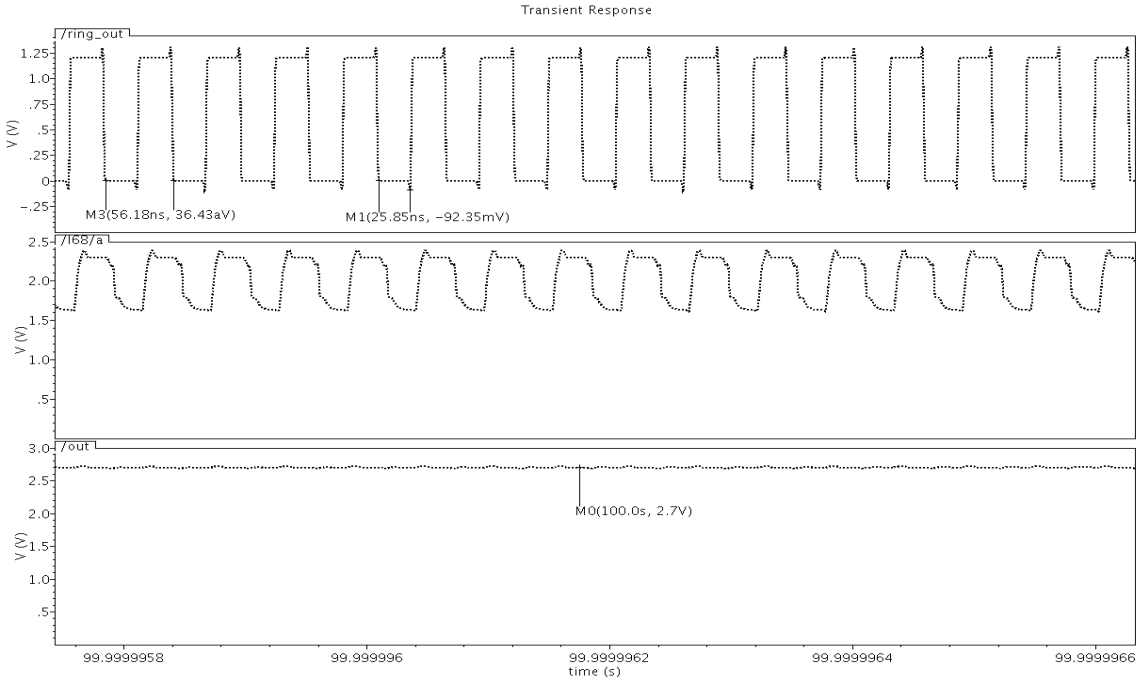

Fig. 24. Simulation results for 2-stage charge pump

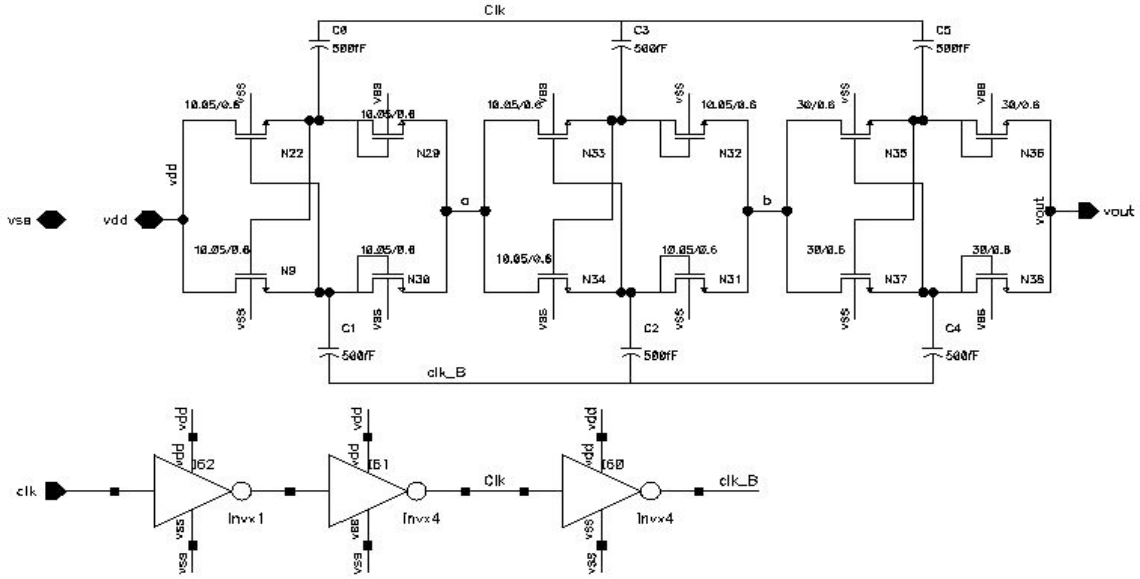

Fig. 25. Schematic of a 3-stage charge pump.

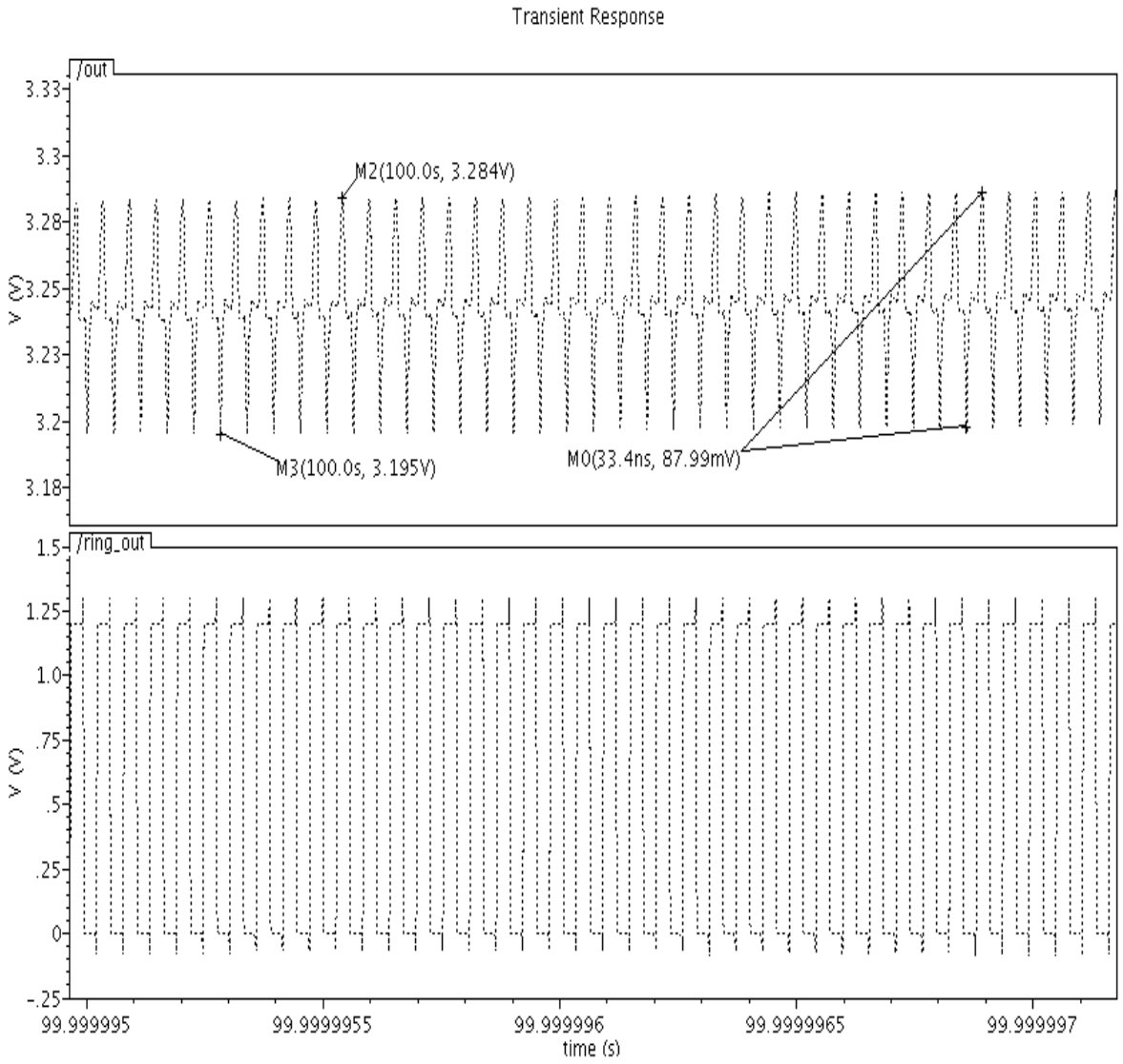

Fig. 26. Simulation results for 3-stage charge pump

In the charge pumps the output voltage do not change with the duty cycle. One of the ways to increase the output voltage is to increase the number of stages for the charge pump at the expense of Silicon area. Using a variable resistor at the switching transistor and varying it can also vary the output voltage.

4 Conclusion:

Two different boost circuits are designed in this project, charge pump and boost converter. The charge pump is implemented with three stages to obtain an output voltage of 3.3V with an expense of large silicon area. The boost circuit was designed with smaller dimensions for the MOSFETS and inductor value. The output of the boost converter is 4V. Furthermore, changing the duty cycle of the ring oscillator output, the output of the boost converter can be programmed.

References:

[1] A. Richelli, L. Colalongo, S.Tonoli and Z. M. Kovacs-Vajna, "A 0.2−1.2 V DC/DC Boost Converter for Power Harvesting Applications", *IEEE Transactions on Power Electronics*, vol. 2, no. 6, pp. 1541-1546, Jun. 2003.