

SGPC Programmer's Manual

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Contents

Contents	i
About This Manual	iv
Related Documentation	iv
Organization	iv
Conventions	iv
Acronyms and Abbreviations	iv
1 Overview	1
1.1 SGPC Architecture Overview	1
1.2 Registers	1
User-accessible Registers	1
Internal Registers	1
1.3 Instruction Conventions	1
Instruction Layout	1
Addressing Modes	1
1.4 Instruction Set	1
1.5 Interrupt Model	1
1.6 Memory Management Model	1
2 Register Set	2
2.1 Foreground Registers	2
General-Purpose Registers (GPRs)	2
Stack Pointer Register (SP)	3
Program Counter Register (PC)	3
2.2 Background Registers	3
Backup Registers	3
Interrupt Registers	3
2.3 Indirect Registers	3
Flags Register	3
Section Registers	3
2.4 Output Registers	3
3 Operand Conventions and Addressing Modes	4
3.1 Operand Conventions	4
Bit and Byte Ordering	4
Aligned and Misaligned Memory Access	4
3.2 Addressing Modes	4
Not From Memory	4

From Memory	4
4 Instruction Set Summary	5
4.1 Instruction Types	5
Move Instructions	5
Arithimic Instructions	5
Control Instructions	5
Reserved Instructions	5
Artifact Instructions	5
4.2 Instruction Format	5
exceptions	5
5 Memory Management	6
5.1 Segments	6
Base	6
Limit	6
5.2 Code Segment (CS)	6
5.3 Data Segment (DS)	6
5.4 Segment Switching	6
5.5 Changing Segments	6
6 Interrupts	7
6.1 Interrupt Enabling/Disabling	7
Interrupt Enabled Flag	7
Internal Interrupt Mask	7
Programmable Interrupt Controller (PIC)	7
6.2 State Preservation	7
Backup	7
Full Restore	7
Partial Restore	7
6.3 Interrupt Service Routine (ISR)	7
Interrupt Far Jump	7
Return to Context	7
Switch Context	7
7 I/O Conventions	8
7.1 Reading Input	8
7.2 Writing Output	8
Problem with Interrupts	8
8 Instruction Set	9
A Instruction Set Listings	10
B Simplified Mnemonics	12
C Common Procedures	13
D Standard Peripherals	14
D.1 Programmable Interrupt Controller (PIC)	14
D.2 Keyboard	14

D.3	Programmable Interrupt Timer (PIT)	14
D.4	Sound Card	14
D.5	Graphical Card	14
D.6	Memory Control Hub (MCH)	14
D.7	Segements and Out Of Bounds Exception	14

About This Manual

Related Documentation

Organization

Conventions

Acronyms and Abbreviations

Chapter 1

Overview

1.1 SGPC Architecture Overview

1.2 Registers

User-accessible Registers

Internal Registers

1.3 Instruction Conventions

Instruction Layout

Addressing Modes

1.4 Instruction Set

1.5 Interrupt Model

1.6 Memory Management Model

Chapter 2

Register Set

This chapter describes the registers separated in four groups based on accessibility. However, the internal registers are omitted from this chapter since these are implementation specific.

2.1 Foreground Registers

The foreground registers are the registers all regular instructions can read from and write to. There are eight 8-bit and eight 16-bit foreground registers. These registers are preserved in interrupts.

General-Purpose Registers (GPRs)

These registers are meant for normal computational storage.

Table 2.1: List of Foreground Registers

ID	Mnemonic	Descriptive Name	Length in bits
0x0	al	The lower byte of ax	8
0x1	ah	The higher byte of ax	8
0x2	bl	The lower byte of bx	8
0x3	bh	The higher byte of bx	8
0x4	cl	The lower byte of cx	8
0x5	ch	The higher byte of cx	8
0x6	dl	The lower byte of dx	8
0x7	dh	The higher byte of dx	8
0x8	ax	The first GPR	16
0x9	bx	The second GPR	16
0xA	cx	The third GPR	16
0xB	dx	The fourth GPR	16
0xC	ex	The fifth GPR	16
0xD	tm	Temporary data	16
0xE	sp	Stack pointer	16
0xF	pc	Program counter	16

Stack Pointer Register (SP)

Program Counter Register (PC)

2.2 Background Registers

Backup Registers

Interrupt Registers

2.3 Indirect Registers

Flags Register

Section Registers

2.4 Output Registers

Chapter 3

Operand Conventions and Addressing Modes

3.1 Operand Conventions

Bit and Byte Ordering

Aligned and Misaligned Memory Access

3.2 Addressing Modes

Not From Memory

Register Direct

Absolute

Register with displacement

From Memory

Direct

Base Plus Displacement

Chapter 4

Instruction Set Summary

4.1 Instruction Types

Move Instructions

Arithmetic Instructions

Control Instructions

Reserved Instructions

Artifact Instructions

4.2 Instruction Format

exceptions

Chapter 5

Memory Management

5.1 Segments

Base

Limit

5.2 Code Segment (CS)

5.3 Data Segment (DS)

5.4 Segment Switching

5.5 Changing Segments

Chapter 6

Interrupts

6.1 Interrupt Enabling/Disabling

Interrupt Enabled Flag

Internal Interrupt Mask

Programmable Interrupt Controller (PIC)

6.2 State Preservation

Backup

Full Restore

Partial Restore

6.3 Interrupt Service Routine (ISR)

Interrupt Far Jump

Return to Context

Switch Context

Chapter 7

I/O Conventions

7.1 Reading Input

7.2 Writing Output

Problem with Interrupts

Chapter 8

Instruction Set

0x00: MOVZ

0x01: MOVNZ

0x02: MOVS

0x03: MOVNS

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Appendix A

Instruction Set Listings

Table A.1: List of instructions sorted by opcode

Opcode			Memmonic	Operand A	Operand B
Decimal	Hex	Binary			
0	0x00	000000	MOV	W?	R?
1	0x01	000001	MOV	W?	R?
2	0x02	000010	MOV	W?	R?
3	0x03	000011	MOV	W?	R?
4	0x04	000100	MOV	W?	R?
5	0x05	000101	MOV	W?	R?
6	0x06	000110	MOV	W?	R?
7	0x07	000111	MOV	W?	R?
8	0x08	001000	MOV	W?	R?
9	0x09	001001	MOV	W?	R?
10	0x0A	001010	MOV	W?	R?
11	0x0B	001011	MOV	W?	R?
12	0x0C	001100	MOV	W?	R?
13	0x0D	001101	MOV	W?	R?
14	0x0E	001110	MOV	W?	R?
15	0x0F	001111	MOV	W?	R?
16	0x10	010000	MOV	W	R
17	0x11	010001	N/A	N/A	N/A
18	0x12	010010	WRI	-	R
19	0x13	010011	N/A	N/A	N/A
20	0x14	010100	ISTR	O	R
21	0x15	010101	ILD	W	O
22	0x16	010110	OUT	O	R
23	0x17	010111	IN	W	O
24	0x18	011000	BACK	-	-
25	0x19	011001	FRET	-	-
26	0x1A	011010	PRET	-	-
27	0x1B	011011	FJMP	-	-
28	0x1C	011100	HLT	-	-
29	0x1D	011101	NOP	-	-
30	0x1E	011110	CMP	R	R

Table A.1: List of instructions sorted by opcode

Decimal	Opcode		Memmonic	Operand A	Operand B
	Hex	Binary			
31	0x1F	011111	TEST	R	R
32	0x20	100000	OR	R&W	R
33	0x21	100001	OR	!R&W	R
34	0x22	100010	OR	R&W	!R
35	0x23	100011	OR	!R&W	!R
36	0x24	100100	AND	R&W	R
37	0x25	100101	AND	!R&W	R
38	0x26	100110	AND	R&W	!R
39	0x27	100111	AND	!R&W	!R
40	0x28	101000	XOR	R&W	R
41	0x29	101001	XOR	!R&W	R
42	0x2A	101010	XOR	R&W	!R
43	0x2B	101011	XOR	!R&W	!R
44	0x2C	101100	ADD	R&W	R
45	0x2D	101101	ADD	!R&W	R
46	0x2E	101110	ADD	R&W	!R
47	0x2F	101111	ADD	!R&W	!R
48	0x30	110000	ADD1	R&W	R
49	0x31	110001	ADD1	!R&W	R
50	0x32	110010	ADD1	R&W	!R
51	0x33	110011	ADD1	!R&W	!R
52	0x34	110100	ADDC	R&W	R
53	0x35	110101	ADDC	!R&W	R
54	0x36	110110	ADDC	R&W	!R
55	0x37	110111	ADDC	!R&W	!R
56	0x38	111000	SHL	W	R
57	0x39	111001	SHL1	W	R
58	0x3A	111010	RCL	W	R
59	0x3B	111011	ROL	W	R
60	0x3C	111100	SHR	W	R
61	0x3D	111101	SHR1	W	R
62	0x3E	111110	RCR	W	R
63	0x3F	111111	ROR	W	R

Appendix B

Simplified Mnemonics

Appendix C

Common Procedures

Appendix D

Standard Peripherals

D.1 Programmable Interrupt Controller (PIC)

D.2 Keyboard

D.3 Programmable Interrupt Timer (PIT)

D.4 Sound Card

D.5 Graphical Card

D.6 Memory Control Hub (MCH)

D.7 Segements and Out Of Bounds Exception