ANALOG DESIGN AND IMPLEMENTATION OF A 6T-SRAM CELL

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Declaration

We, the undersigned members of Group 5, hereby declare the following regarding our final project titled " ***Analog design and implementation of a 6T-SRAM celll****":*

- This project is the product of collaborative effort from all group members, with each contributing to the research, design, implementation, and documentation.
- All information, data, and findings in this project are accurate and obtained through ethical research practices.
- Proper citations and references have been provided for all external sources, ensuring full credit is given where due.
- We uphold the highest standards of academic honesty and are committed to the responsible conduct of research.

By signing below, we affirm our commitment to these principles and the integrity of our work.

Date:[08/2024]

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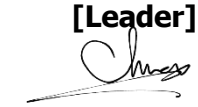
This project would not have been possible without the encouragement and assistance of everyone involved.

[Leader]



Do Minh Chuong

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Abstract

The Bitcell circuit, also known as the memory unit cell in SRAM (Static Random-Access Memory), plays a crucial role in storing and retrieving information in microchip systems. The 6T (6 Transistors) bitcell is the most common type, utilizing six transistors (4 NMOS and 2 PMOS) to form a flip-flop that allows for stable storage of one bit of data. The 6T bitcell is favored for its compact size, fast access speed, and low power consumption, making it the preferred choice in designing integrated memories on modern microchips.

As microchip technology becomes increasingly complex and demands higher performance, the design and optimization of the bitcell circuit have become critically important. The analog design process for bitcell circuits involves several steps, from schematic design, simulation, to layout creation, DRC/LVS checks, and finally, post-layout simulation. Each step in this process plays a vital role in ensuring the circuit operates correctly and meets technical requirements.

Keywords: Bitcell, SRAM, 6T Bitcell, NMOS, PMOS, Data Storage, Low Power Consumption, Analog Design Process

1. INTRODUCTION

1.1 Objectives

The objective of this report is to detail the design process of a 6T bitcell circuit using Synopsys Custom Designer, covering steps from schematic design to simulation, layout creation, DRC/LVS checks, and post-layout simulation. The report will analyze the results obtained at each stage, evaluate the circuit's performance, and propose optimization directions if necessary. The specific objectives include:

Schematic Design: Create an accurate schematic for the 6T bitcell circuit.

Pre-layout Simulation: Evaluate the circuit's functionality through initial simulations.

Layout Design: Develop the circuit layout adhering to strict design rules.

DRC and LVS: Ensure that the layout complies with design rules and accurately reflects the schematic.

1.2 Design Requirements

In the design of the *6T Bitcell* circuit, selecting the W/L ratio of the transistors is crucial to ensure speed, stability, and overall performance. Specifically, the read/write speed of the *6T bitcell* must be fast enough to meet the system's speed requirements. The circuit must remain stable, especially when using small sizes in advanced semiconductor technology.

For the Access Transistor (NMOS), its function is to connect the storage nodes to the bitlines (BL and BLB) during read or write operations.

The Inverter Transistors (PMOS and NMOS) store logic values (Q and QB) by creating a stable state. They must be strong enough to maintain the stored state without being disturbed or flipped during operation.

Regarding W/L design, for the NMOS Inverter Transistor, the length (L) should be chosen as small as possible to reduce area and increase speed. The width (W) typically has a W/L ratio of **2:1** to provide sufficient current for stable operation. For the PMOS Inverter Transistor, the length (L) should be as small as possible, similar to the NMOS length. The width (W) usually needs to be larger to balance with the NMOS due to the weaker current characteristics of PMOS.

2. LITERATURE REVIEW

Deepak Mittal and V.K. Tomar compared 6T SRAM cells with 7T, 8T, and 9T SRAM cells, focusing on read/write delays, power consumption, and static noise margins (RSNM and WSNM) using Cadence Spectre. Another study by Ms. Isma Rizvi and colleagues examined the impact of noise on a 6T SRAM cell, analyzing write margin, write time, and static noise margin with 180nm CMOS technology. C. Premalatha and team addressed power dissipation in SRAM cells by applying dual threshold voltage to 6T, 7T, 8T, and 9T SRAMs, assessing delay and power dissipation using Cadence Virtuoso and Spectre in a 90nm process.

3. SRAM BIT-CELL OPERATION

SRAM memory cells operate primarily in three states: Standby (Hold), Data Read, and Data Write.

In the Standby Operation (Hold), the word line (WL) is connected to the ground (WL=0), turning off the access transistors M5 and M6, which disconnects the cell from the bit lines (BL and BLB). This leaves transistors M1, M2, M3, and M4, forming two cross-coupled inverters that continue to reinforce each other as long as they remain disconnected from external influences, with the current flowing in this state known as standby current.

In the Data Read Operation, the bit lines BL and BLB are precharged to VDD, and the word line is connected to VDD, turning on the access transistors M5 and M6. If the stored data is Q='0' and Qb='1', transistors M2 and M3 are off, and M4 and M1 are on, allowing current to flow through BL-M5-M1, discharging BL while BLB remains the same, creating a voltage difference that is detected by the sense amplifier to complete the read '0' operation. Conversely, if Q='1' and Qb='0', transistors M1 and M4 are off, and M2 and M3 are on, causing current to flow through BLB-M6-M2, discharging BLB while BL remains the same, thus performing the read '1' operation.

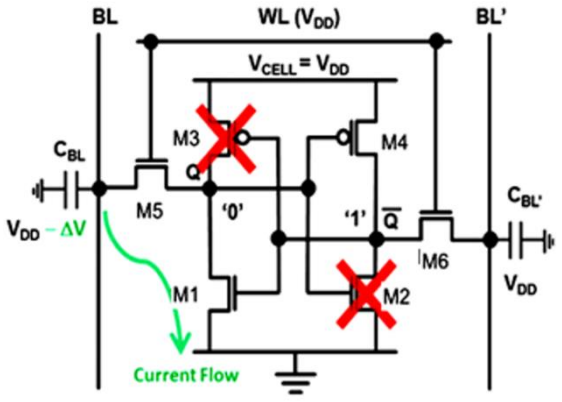

Figure 1. Current flow and the voltage level at each node during the read operation. The initial data stored in the SRAM cell is '0' (i.e., Q = 0).

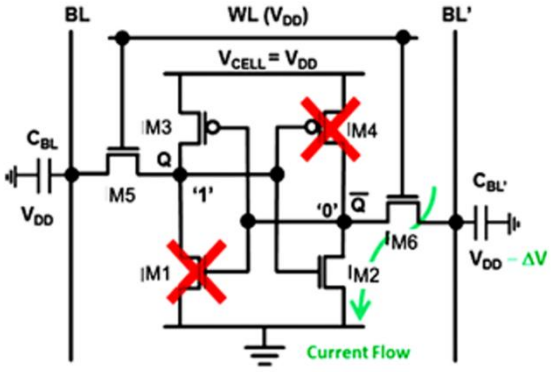

Figure 2. Current flow and the voltage level at each node during the read operation. The initial data stored in SRAM cell is '1' (i.e., Q = 1).

Data Write Operation: In the Write Operation BL and BLB are complementary to each other as BL='0' and BLB= '1'.
Write operation has been divided into 4 cases:

a. When '0' is stored and writing '0' is requested.
b. When '0' is stored and writing '1' is requested.
c. When '1' is stored and writing '0' is requested.
d. When '1' is stored and writing '1' is requested.

Case (a) and (d) are the insignificant cases in which same data write over the previously stored data so we cannot see any variation in these cases.

Now in case (b): When '0' is stored and writing '1' is requested. bit lines BL will be precharged and BLB will be driven from VDD to GND. And the Word Line should be high after then access transistor M5 and M6 are ON and as the memory stores previous information i.e. Q= '0' and $\bar{Q}$='1' then the transistor M2 and M3 will be turned off and M4 and M1 will be turned on and now the current will flow through BL-M5-M1 and M4-M6-BLB thus precharged BL will be discharged and BLB remains same. The voltage at node $\bar{Q}$ drops and the voltage at Q increases until the voltage level of $\bar{Q}$ will be low enough to turn on the transistor M3 and turn off M1 or the voltage level at node Q will be high enough to turn on transistor M2 and turn off the transistor M4. After then the voltage level of Q and $\bar{Q}$ will be flipped to VDD and GND respectively.

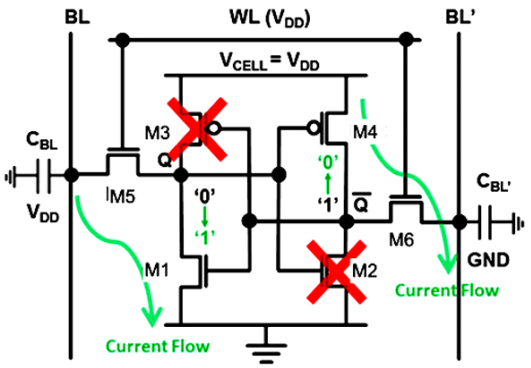

Figure 3. Current flow and the voltage level at each data storage node (i.e., Q and $\bar{Q}$) when writing '1' at the node Q are required. The initial data stored at the node Q was '0'.

Now in case (c): When '1' is stored and writing '0' is requested. Bit lines BLB will be precharged and BL will be driven from VDD to GND. And the word line should be high after then access transistor M5 and M6 are ON and as the memory stores previous information i.e. Q= '1' and $\bar{Q}$='0' then the transistor M1 and M4 will be turned off and M2 and M3 will be turned on and now the current will flow through M3-M5-BL and BLB-M6-M2 thus precharged BLB will be discharged and BL remains same. The voltage at node Q drops and the voltage at $\bar{Q}$ increases until the voltage level of Q will be low enough to turn on the transistor M4 and turn off M2 or the voltage level at node $\bar{Q}$ will be high enough to turn on transistor M3 and turn off the transistor M1. After then the voltage level of $\bar{Q}$ and Q will be flipped to VDD and GND respectively.

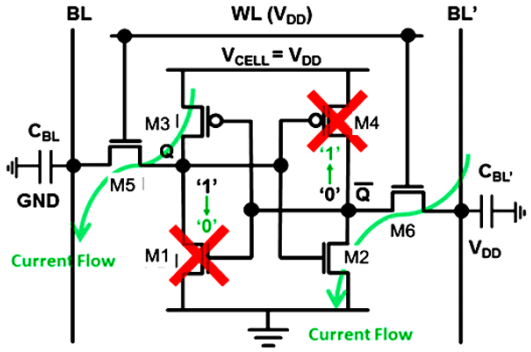

Figure 4. Current flow and the voltage level at each data storage node (i.e., Q and Qb) when writing '0' at the node Q are required. The initial data stored at the node Q was '1'.

4. SRAM WORKING

The SRAM generally works in three modes of operation, namely hold mode, read mode and write mode. When SRAM is in standby mode or Hold mode the Word Line is connected to ground.

SRAM retains the data without flip-ping the data. Data is retained in the SRAM till power is applied. When the SRAM is in Read mode, bit-line is pre-charged to VDD and the word-line is set. To read a '0' or'1' the bit-line is generally discharged through the access transistor. Discharging Current is equated through M1 and M5 and is specified in equation 1. The cell ratio is defined as the ratio of the drive transistor and the load transistor. The SNM depend on the Cell Ratio. Therefore it is verified that as the CR increases SNM of the memory cell increases resulting in increase of current in a memory cell .

$$\beta_{n,M5}\left\{(V_{DD}-V_{QB}-V_{tn})V_{DSATn}-\frac{V_{SATn}^2}{2}\right\}=\beta_{n,M1}\left\{(V_{DD}-V_{tn})V_{QB}-\frac{V_{QB}^2}{2}\right\} \quad (1)$$

The equation 1 is simplified to equation 2

$$V_{QB}=\left\{V_{SSATn}+CR(V_{DD}-V_{tn})-\sqrt{V_{DSATn}^2(1+CR)+CR^2(V_{DD}-V_{tn})^2}\right\}\div CR \quad (2)$$

Where CR is called the CR or β ratio and is represented in equation 3

$$Cell\ Ratio\ (CR)=\frac{W_1/L_1}{W_5/L_5} \quad (3)$$

If the SRAM is working write mode, the bit-lines in the SRAM are always complementary and to store '0' or '1'discharging through the access transistor is necessary. The PR is defined as the ratio of the load transistor and the access transistor. Therefore it is verified that as the PR increases SNM of the memory cell increases. Current passing through M4 and M6 are equated in equation 4 to ensure that write is success.

$$\beta_{n,mn6}\left\{(V_{DD}-V_{tn})V_Q-\frac{V_Q^2}{2}\right\}=\beta_{p,M4}\left\{(V_{DD}-V_{tp})V_{DSATp}-\frac{V_{DSATp}^2}{2}\right\} \quad (4)$$

This equation 4 is simplified to equation 5 as

$$V_Q=V_{DD}-V_{tn}-\sqrt{(V_{DD}-V_{tp})^2 2\frac{\mu_p}{\mu_n}PR\left\{(V_{DD}-V_{tp})V_{dsatp}-\frac{V_{DSATp}^2}{2}\right\}} \quad (5)$$

Where PR or α Ratio and is represented in equation 6 is

$$Pullup\ Ratio\ (PR)=\frac{W_4/L_4}{W_6/L_6} \quad (6)$$

5. SCHEMATIC DESIGN

5.1 Schematic

General Function Description: The 6T bitcell circuit is designed to store one bit of data in SRAM (Static Random-Access Memory). The circuit consists of NMOS and PMOS transistors, with key components such as the access transistors (M1 and M5), which connect the storage nodes Q and QB to the bit lines (BL) and bit line bar (BLB) during read and write operations, and the inverter transistors (M2, M4 for NMOS and M3, M6 for PMOS), which create a stable state at the Q and QB nodes, maintaining the logic value of the stored bit. The word line (WL) controls the access transistors to perform read and write operations.

Transistor Functions: The access transistors (M1 and M5) are used to control access to the bitcell circuit, allowing data to be read or written to the Q and QB nodes via the BL and BLB lines. The inverter transistors (M_2, M_3, M_4, M_6) maintain the stored state by creating two opposing stable states at Q and QB. These transistors must be designed to ensure stability and prevent state flipping during operation.

Operating Principle: During a write operation, the access transistors are activated by the word line (WL) signal, allowing the bit line (BL) or bit line bar (BLB) to change the state of the storage nodes Q and QB. During a read operation, the WL signal also activates the access transistors, and the data is retrieved from the Q or QB node through the BL or BLB lines.

3.2. Parameter Calculations

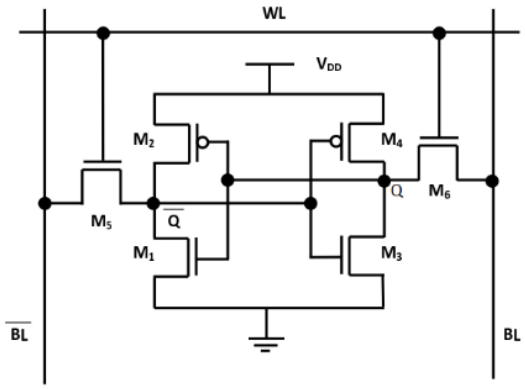

Figure 5. SRAM Schematic.

Cell Ratio (CR):

$$CR = \frac{W_1/L_1}{W_5/L_5} = \frac{W_4/L_4}{W_6/L_6} \quad (3)$$

CR typically controls the strength of the driver transistors M_1 and M_4 compared to the access transistors M_5 and M_6

Pull-up Ratio (PR):

$$PR = \frac{W_3/L_3}{W_2/L_2} = \frac{W_6/L_6}{W_5/L_5} \quad (6)$$

PR controls the strength of the pull-up transistors M_2 and M_3 compared to the access transistors M_5 and M_6

Set the values for W_5 and W_6:

W_5=0.25µm

W_6=0.25µm

L_1=L_2=L_3=L_4=L_5=L_6=0.1µm

These values were calculated using a CR of 0.8, meaning the driver transistors M1 and M4 are slightly smaller than the access transistors M5 and M6. This sizing is often used to ensure sufficient read stability while minimizing power consumption.

These values were calculated using a PR of 2.0, meaning the pull-up transistors M_2 and M_3 are twice as large as the access transistors M_5 and M_6. This larger size for the pull-up transistors ensures a stronger ability to pull the bitlines up during a write operation, providing a good write margin.

Calculate W_1 and W_4 using the (CR):

Assuming a typical Cell Ratio CR=0.8

W_1=C_R×W_5=0.8×0.25µm=0.2µm

W_4=C_R×W_6=0.8×0.25µm=0.2µm

Calculate W_2 and W_3 using the (PR):

Assuming a typical Pull-up Ratio PR=2.0

W_2=P_R×W_6=2.0×0.25µm=0.5µm

W_3=P_R×W_5=2.0×0.25µm=0.5µm

Summary of Calculated Widths:

- W_1=0.2µm
- W_2=0.5µm

- W_3=0.2µm
- W_4=0.5µm
- W_5=0.25µm
- W_6=0.25µm

6. METHODOLOGY

A 6T SRAM is implemented in Custom Designer using 90nm technology, as illustrated. In this design, the sizes of the NMOS and PMOS transistors are carefully selected to ensure optimal performance, with the length of the NMOS and PMOS transistors set at 100nm.

To determine the **Cell Ratio (CR)**, transistor NM2 is considered as the driver transistor, and NM3 is considered as the load transistor. In this design, the ratio of the driver transistor to the load transistor is set at 0.8, ensuring that the Read Margin (RM) is directly proportional to the CR, thereby providing stability during the read operation.

To determine the **Pull-up Ratio (PR)**, transistor PM1 is considered as the load transistor, and NM4 is considered as the access transistor. The ratio of the load transistor to the access transistor is set at 2, ensuring that the Write Margin (WM) is directly proportional to the PR, thus improving the performance during the write operation.

Additionally, the **Static Noise Margin (SNM)** and **Data Retention Voltage (DRV)** are both directly proportional to the threshold voltage Vth.

For 90nm technology, the threshold voltage Vth is set at 200mV, ensuring that the circuit operates reliably under typical operating conditions.

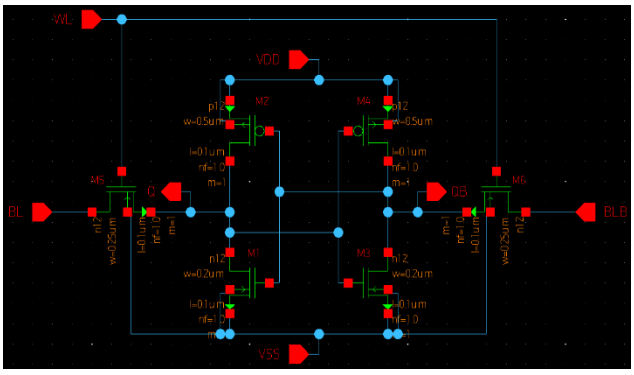

Figure 6. Schematic diagram of SRAM cell.

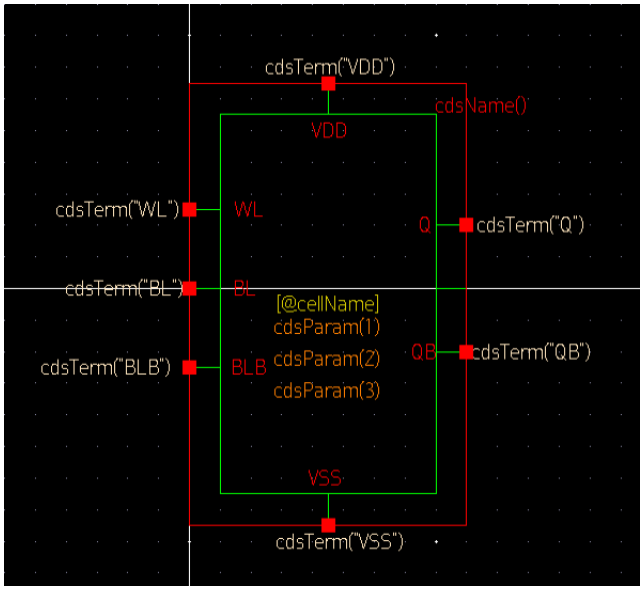

Figure 7. Symbol of design of SRAM cell.

7. SIMULATION RESULTS

7.1 Setup Simulation

PrimeWave in Custom Designer is a simulation environment that integrates various analysis tools for verifying and optimizing analog and mixed-signal designs. It allows designers to perform simulations such as transient, AC, DC, and noise analysis, providing a comprehensive platform to test and validate circuit behavior before fabrication.

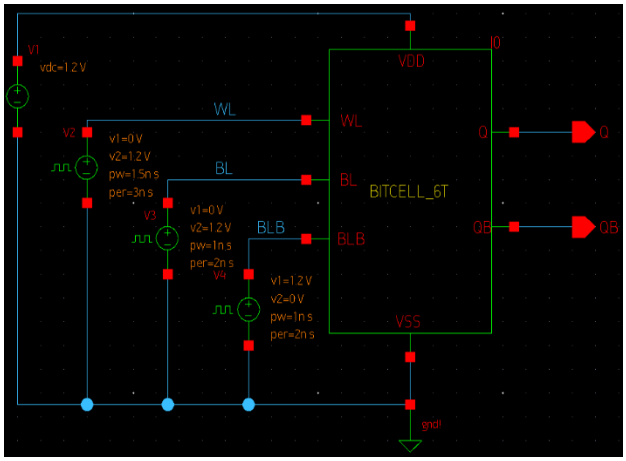

Figure 8. Setup Simulation for BitCell6T.

Simulation Configuration

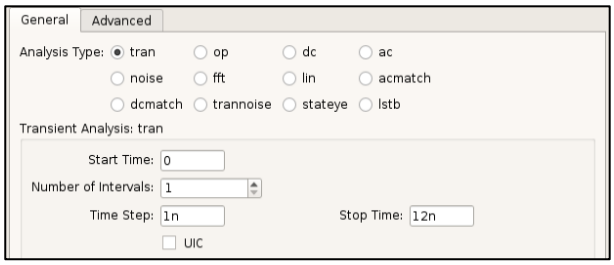

Figure 9. Transient for BitCell6T.

Analysis Type: Transient (tran)
Start Time: 0 ns
Stop Time: 12 ns
Time Step: 1 ns
Number of Intervals: 1

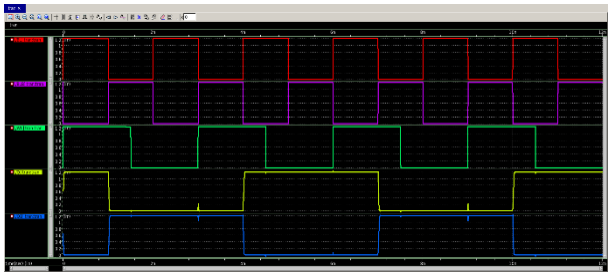

Figure 10. Wave transient for BitCell6T.

BL and BLB (Red and Purple): Bit lines used for reading and writing data. They alternate between high and low states.

- These signals represent the bit lines used to read and write data into the bitcell. The waveform shows the behavior of these bit lines as they alternate between high (logic 1) and low (logic 0) states during read and write operations.
- When one bit line is high, the other is typically low, which is characteristic of differential signaling in SRAM cells.

WL (Green): Word line that enables access to the bitcell during read/write operations.

Q and QB (Yellow and Blue): Internal node states of the SRAM cell, showing complementary.

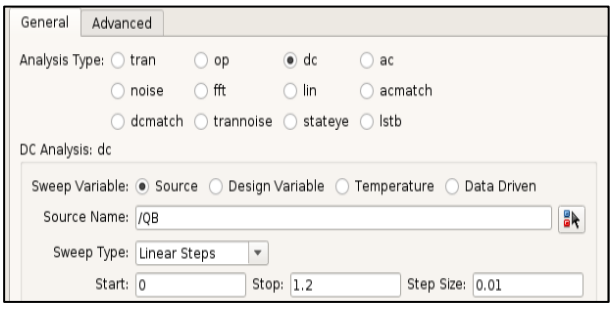

Figure 11. Dc (Direct Current) for BitCell6T.

This configuration sets up a DC sweep analysis where the voltage at the /QB node is incrementally increased from 0V to 1.2V in steps of 0.01V. This type of analysis is typically used to observe how the circuit responds to changes in the DC operating point, particularly at the /QB node.

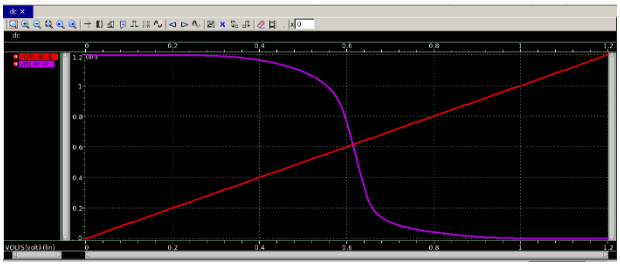

Figure 12. Wave Dc (Direct Current) for BitCell6T.

Interpretation:

- **Voltage Transfer Characteristics:** The graph demonstrates the bistable nature of the 6T SRAM cell, where **/Q** and **/QB** hold opposite logic levels. As **/QB** is swept from 0V to 1.2V, **/Q** transitions from 1.2V to 0V, indicating the flip-flop behavior of the SRAM bitcell.
- **Switching Thresholds:** The point where the two curves cross (around 0.6V) represents the threshold voltage at which the cell switches states. This is crucial for determining the stability and noise margins of the SRAM cell.

Conclusion:

This analysis confirms that the SRAM cell is functioning correctly, showing clear bistable behavior with well-defined switching thresholds.

The complementary nature of **/Q** and **/QB** is evident from the waveforms, with one node holding high while the other is low, and vice versa.

The steepness of the transition regions provides insights into the cell's noise margins and stability under varying conditions.

8. LAYOUT

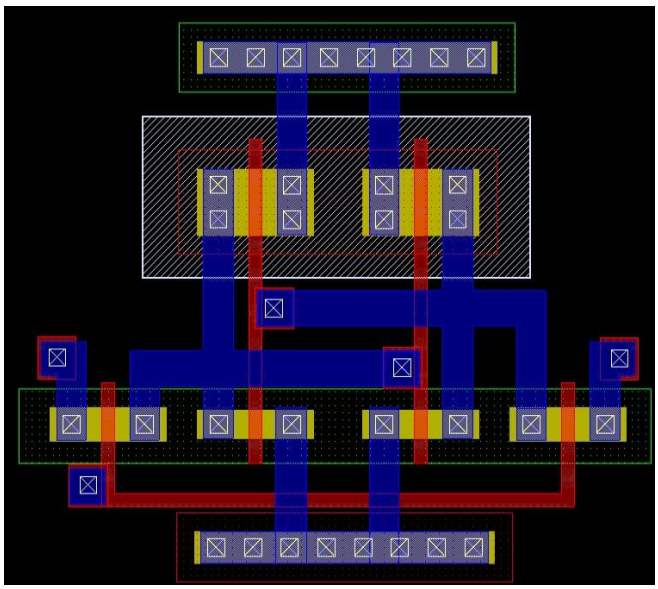

Figure 13. Layout of BitCell6T.

Check DRC

DRC (Design Rule Check) in Custom Designer is a verification process used to ensure that a semiconductor layout adheres to the manufacturing design rules specified by the foundry. It checks for issues such as spacing, width, and layer overlap to ensure that the design can be manufactured reliably without defects.

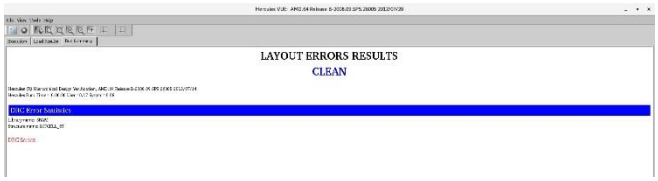

Figure 14. Check DRC of BitCell6T.

Check LVS

LVS (Layout vs. Schematic) in Custom Designer is a verification process that compares the physical layout of a circuit to its corresponding schematic to ensure they match. This check ensures that the circuit layout will function as intended by verifying that the connections and components in the layout are consistent with the schematic design.

7. CONCLUSION

This thesis has presented the design, simulation, and analysis of a 6T SRAM bitcell implemented using 90nm technology. The primary focus was on optimizing the cell for stability, performance, and reliability by carefully selecting the appropriate transistor sizes and ensuring that critical ratios, such as the Cell Ratio (CR) and Pull-up Ratio (PR), were maintained within the desired ranges.

The design process included detailed calculations and simulations, particularly focusing on the behavior of the SRAM cell during read and write operations. The Cell Ratio (CR) was set to **0.8**, which provided a stable Read Margin (RM) by ensuring that the driver transistors had adequate strength compared to the load transistors. The Pull-up Ratio (PR) was chosen as **2**, optimizing the Write Margin (WM) to ensure reliable data writing under various operating conditions.

In conclusion, the designed 6T SRAM bitcell meets the necessary criteria for stability, performance, and reliability. The successful implementation of this design in a 90nm technology process demonstrates its viability for use in memory arrays where low power consumption and high performance are required. The methods and analysis presented in this thesis can serve as a foundation for further research and optimization in SRAM design, particularly in advanced technology nodes.

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