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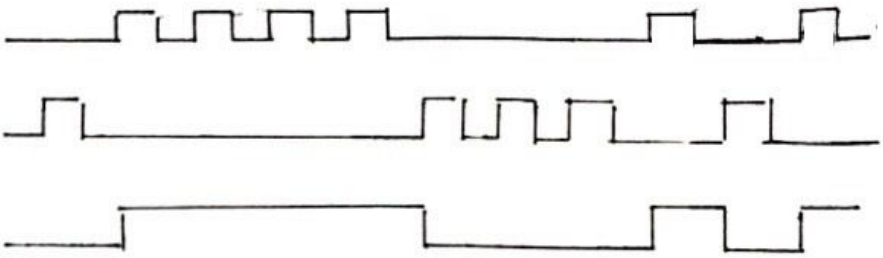
EIE2050 Assignment 6

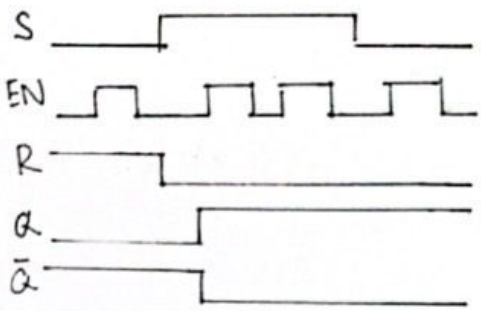
1. Truth table for an active-LOW input $\bar{S}$-$\bar{R}$ latch

Inputs		Outputs		comments
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
1	1	NC	NC	No change
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
0	0	1	1	Invalid



2. Truth table for a gated S-R latch

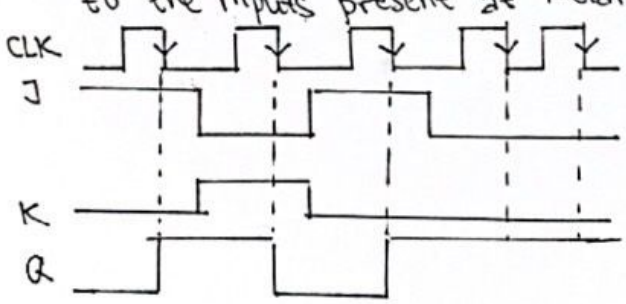
EN	Inputs		Outputs		comments
	S	R	Q	$\bar{Q}$	
0	X	X	NC	NC	No change
1	0	0	NC	NC	No change
1	0	1	0	1	Latch SET
1	1	0	1	0	Latch RESET
1	1	1	1	1	Invalid



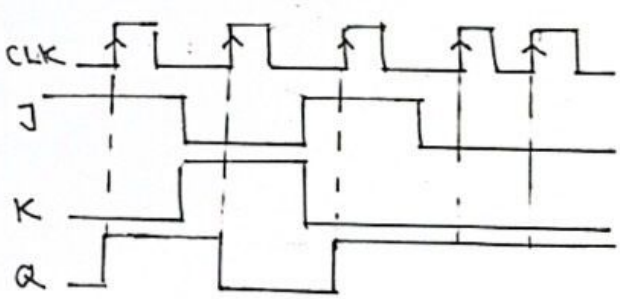
3. Truth table for a positive edge-triggered S-R flip flop:

Inputs			Outputs	comments
S	R	CLK	Q	
0	0	X	Q_0	No change
0	1	↑	0	Latch RESET
1	0	↑	1	Latch SET
1	1	↑	1	Invalid

(a) since the clock circuit applied is a negative edge-triggered clock, the output changes on the negative edge of the clock pulse according to the inputs present at instant

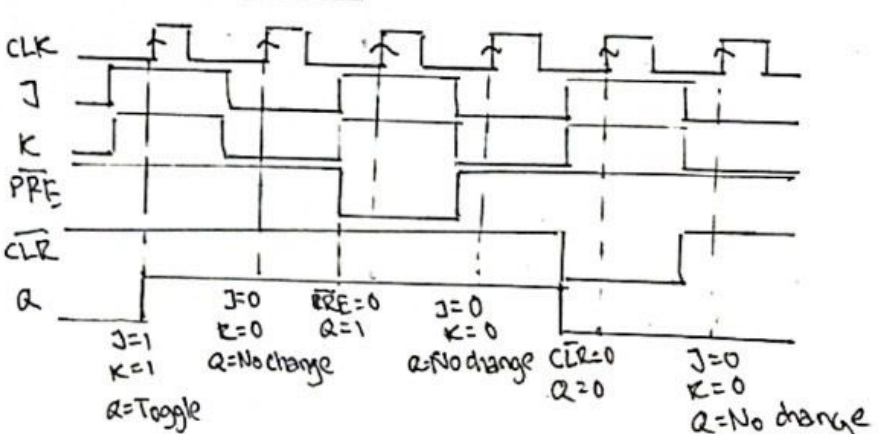


(b) Since the clock circuit applied is a positive edge-triggered clock, the output changes on the positive edge of the clock pulse according to the inputs present at instant



4. Truth table for the J-K flip flop

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	C	J	K	Q	$\bar{Q}$
0	0	X	X	X	1	1
0	1	X	X	X	1	0
1	0	X	X	X	0	1
1	1	↑	0	0	No change	
1	1	↑	0	1	0	1
1	1	↑	1	0	1	0
1	1	↑	1	1	Toggle	
1	1	0	X	X	No change	



5. since the counter is synchronized,

$$T_{CLK} \geq t_{pdFF} + t_{su}$$

$$\Rightarrow T_{CLK} \geq 6\,ns + 3ns = 9ns$$

$$\Rightarrow f_{CLK} \leq \frac{1}{9 \cdot 10^{-9}}\ Hz$$

$$\Rightarrow f_{CLK_{max}} = 111.11\ MHz$$

6. given $t_w = 3\,\mu s$ & $C_{EXT} = 50000\,pF$

for 74LS122 one-shot,

$$t_w = 0.32\, R\, C_{EXT}\left(1 + \frac{0.7}{R}\right)$$

$$= 0.32\, R_{EXT} C_{EXT} + 0.7 \cdot \frac{0.32\, R_{EXT} C_{EXT}}{R_{EXT}}$$

$$= 0.32\, R_{EXT} C_{EXT} + (0.7)(0.32) C_{EXT}$$

$$\Rightarrow R_{EXT} = \frac{t_w - (0.7)(0.32) C_{EXT}}{0.32\, C_{EXT}} = 186.8\ \Omega$$

7. since it is given astable multivibrator,

$$T = 0.69(R_1 + 2R_2) C$$

$$\Rightarrow f = \frac{1.45}{(R_1 + 2R_2) C}$$

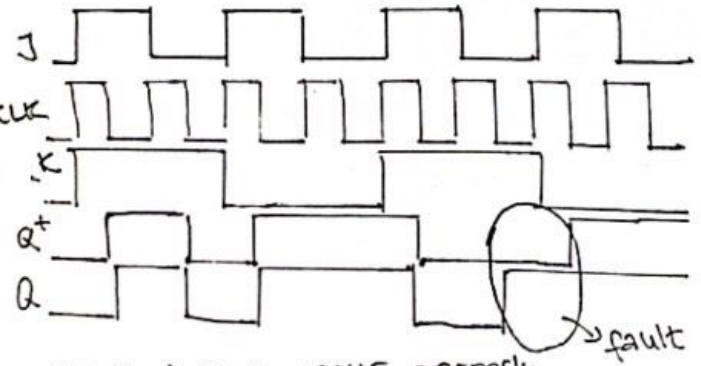
$$= \frac{1.45}{(2.0 + 2 \times 4.3) 10^3 \cdot 0.01 \cdot 10^{-6}}\ Hz$$

$$= 13.679 \cdot 10^3\ Hz$$

$$= 13.679\ kHz$$

8. Truth table for a -ve edge triggered flip flop:

inputs		outputs
J	K	Q^+
1	1	$\bar{Q}$
0	1	0
1	0	1
0	0	Q



as it doesn't occur properly, it is probably caused by static Hazards

9. since the clock is applied asynchronously, the change in Q_a is not reflected simultaneously in Q_b, implying a mismatch between inputs to gates

- since there are practical gates used, there exist some delays in giving output to the desired inputs

we should use quality gates with the least value of propagation delay. we have to be careful with ECL, TTL, etc and choose it wisely

- inputs to gates arrive at different times and caused ambiguity in output gate

we should carefully ensure that the inputs to both terminals of gates traversing the same length (in wiring circuit)

- flip-flops are formed by gates only; therefore, the same precautions also hold true