

1. the shift register is a 10-bit shift register, which shows that it has 10 stages

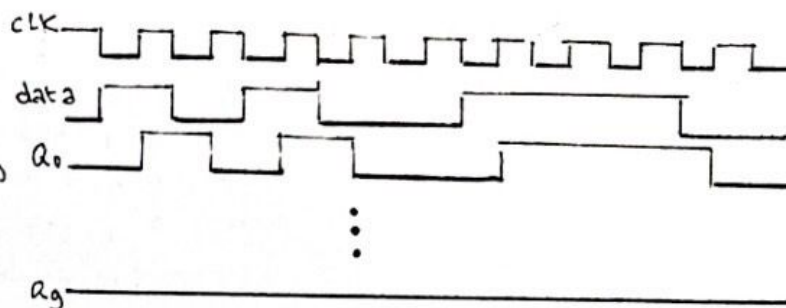
initial stage: 0000000000

input sequence; 01010011100100110110

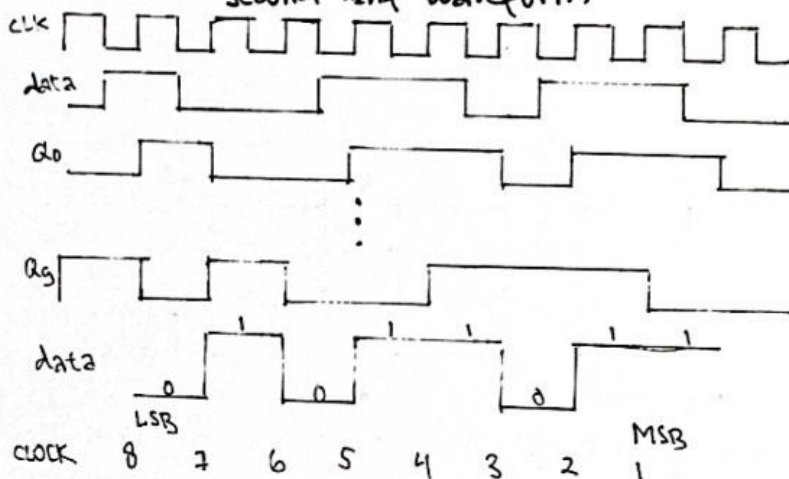
CLOCK	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Q <sub>5</sub>	Q <sub>6</sub>	Q <sub>7</sub>	Q <sub>8</sub>	Q <sub>9</sub>	Q <sub>10</sub>
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	0	0	0
3	0	1	0	0	0	0	0	0	0	0
4	1	0	1	0	0	0	0	0	0	0
5	0	1	0	1	0	0	0	0	0	0

17	0	1	1	0	0	1	0	0	1	1
18	1	0	1	1	0	0	1	0	0	1
19	1	1	0	1	1	0	0	1	0	0
20	0	1	1	0	1	1	0	0	1	0

first half waveform



second half waveform



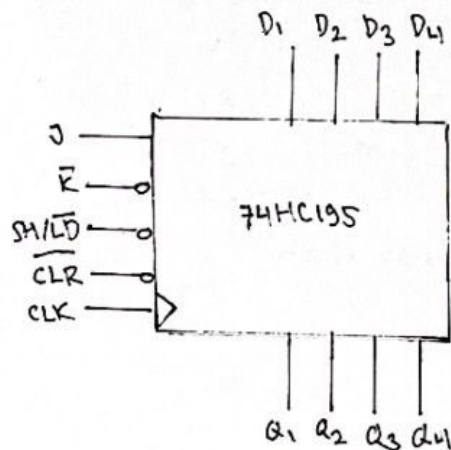
2. → For leading-edge clocked serial-in / serial-out shift register, one-bit data shifts every time when clock signal goes from 0 to 1

- First bit comes out is MSB
- Last bit comes out is LSB

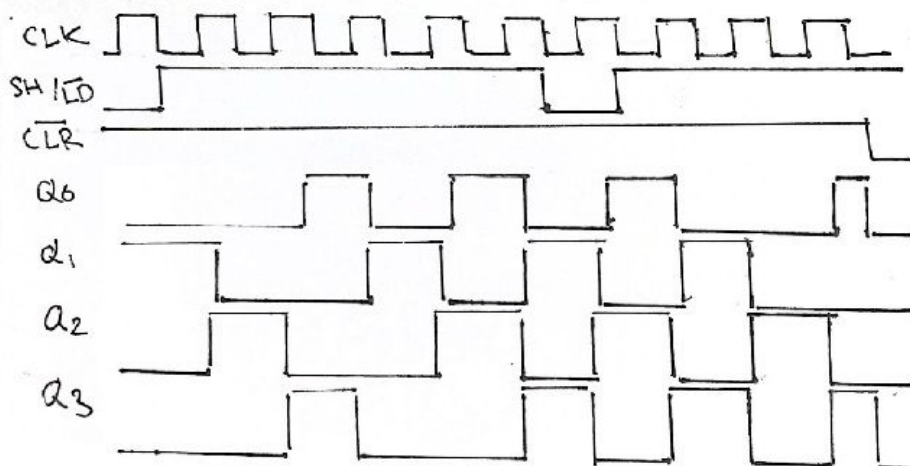
⇒ so, the binary number stored as

1	1	0	1	1	0	1	0
MSB							LSB

3.



- Q<sub>3</sub> is used as a serial out pin
- J & K inputs are used to input data serially
- SH/LD is used to load the parallel data and to allow shift operations on the clock transition
- CLR input is used to clear the register asynchronously



4. CLOCK  $Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7 Q_8 Q_9$

0	0	0	0	0	1	0	0	0	1	0
1	0	0	0	0	0	1	0	0	0	1
2	1	0	0	0	0	0	1	0	0	0
3	0	1	0	0	0	0	0	1	0	0
4	0	0	1	0	0	0	0	0	1	0
5	0	0	0	1	0	0	0	0	0	1

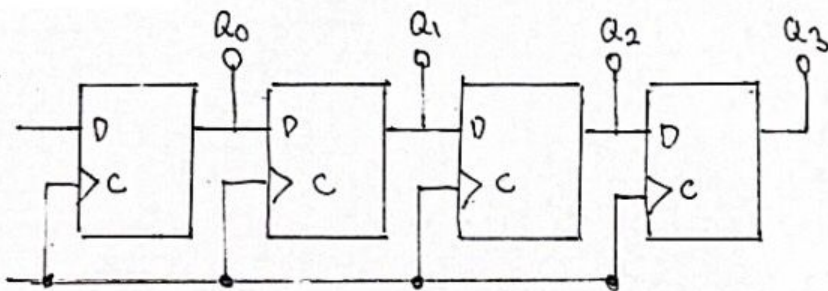
⋮

12	1	0	0	0	1	0	0	0	0	0
13	0	1	0	0	0	1	0	0	0	0
14	0	0	1	0	0	0	1	0	0	0
15	0	0	0	1	0	0	0	1	0	0

preset value of the ring counter

is 0000100010

5.



the given register is a 4-bit serial in parallel out shift register  
 each stage output of the register is referred as  $Q_0, Q_1, Q_2$ , and  $Q_3$   
 the given waveform shows that the 4 flip-flops were initially RESET  
 with the first clock pulse, the first flip-flop stores 1 as the input data  
 waveform and  $Q_0$  shows 1. with this way, the register shifts 1 bit every  
 clock and store one serial input data bit into first flip-flop. However,  
 since the  $Q_3$  waveform is not in proper way. Starting from the first  
 clock pulse, it switched into SET stat, which remains in this state.  
 Therefore, it can be concluded that the third D flip-flop is the  
 most likely problem, that is, it is faulty.