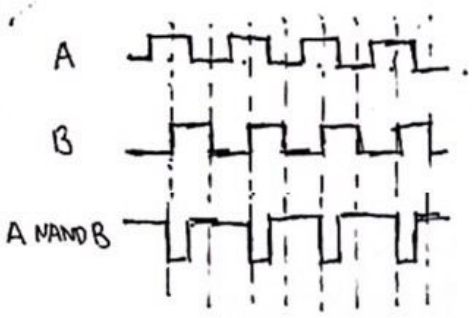
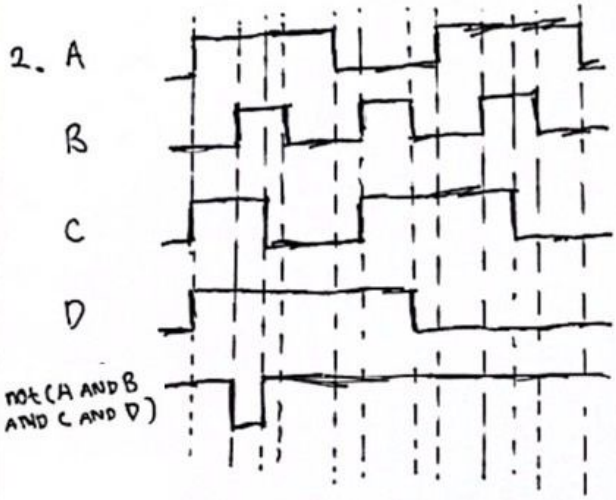
Yohandi (1200400025)
E1E2050 - Assignment 2

1.



2.



3. Gate A, the shorter the propagation delay, the higher the frequency at which it can operate

4. $P_D = V_{cc}\left(\frac{I_{CCH} + I_{CCL}}{2}\right)$

consider one of the gates when the output is HIGH:

$P_D' = V_{CC} \times I_{CCH}$

in figure 3-66,

$V_{CC\,max} = 5.25\ V$

$I_{CCH} = 1.6\ mA$

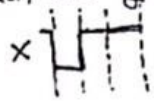
$\Rightarrow P_D' = 8.4mW$

$P_D = 4 \times P_D'$

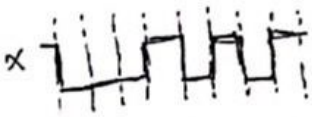
$= 4 \times 8.4\ mW$

$= 33.6mW$ (maximal)

5 (a) this gate is faulty, X should be:



(b) this gate is faulty, X should be:



(c) this gate is not faulty

(d) this gate is faulty, X should be: