

Electrical Sub-Block

8.

8.1 Electrical Specification Introduction

Key attributes of the Electrical Specification include:

- Support for 2.5, 5.0, 8.0, 16.0, and 32.0 GT/s data rates
- Support for common and separate independent reference clock architectures
- Support for Spread Spectrum clocking
- Reduced swing mode for lower power Link operation
- In-band receiver detection and electrical idle detection
- Channel compliance methodology
- Adaptive transmitter equalization and reference receiver equalization allowing closed eye channel support at 8.0, 16.0, and 32.0 GT/s
- Lane margining
- AC coupled channel

The 4.0 version of the PCI Express electrical specification is organized into separate sections for the Transmitter, Receiver, the channel, and the Refclk. In this version most parameters have been regularized such that a common set of parameters is used to define compliance at all data rates.

8.2 Interoperability Criteria

8.2.1 Data Rates

A device must support 2.5 GT/s and is not permitted to skip support for any data rates between 2.5 GT/s and the highest supported rate.

8.2.2 Refclk Architectures

PCIe supports two Refclk data architectures: Common Refclk, and Independent Refclk. These are described in detail in Section 8.6. A PCIe device may support one or more of these architectures.

8.3 Transmitter Specification

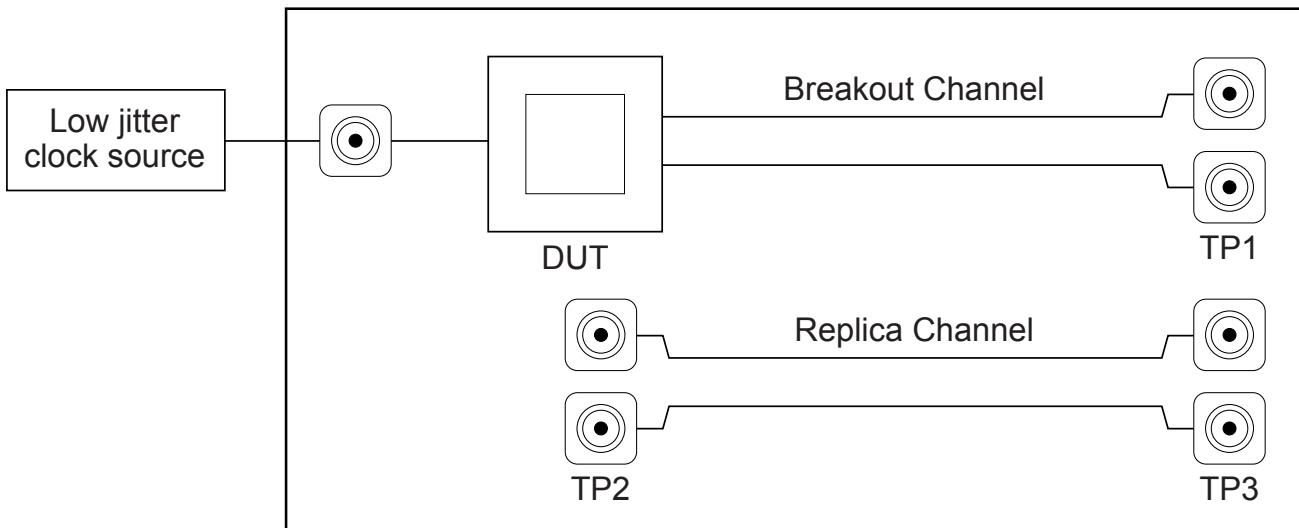
8.3.1 Measurement Setup for Characterizing Transmitters

The PCI Express electrical specification references all measurements to the device's pin. However, the pin of a device under test (DUT) is not generally accessible, and the closest accessible point is usually a pair of microwave-type coaxial

connectors separated from the DUT pins by several inches of PCB trace, called the breakout channel on a silicon test board. On a test board with many Lanes the minimum breakout channel length is constrained by the need to route to a large number of coaxial connectors. Typically, this limitation holds true for both the Tx and the Rx pins. [Figure 8-2](#) illustrates a typical test connection to a DUT, showing a single Tx Lane breakout.

A low jitter Refclk source is used when the silicon supports using an external reference clock in order that the jitter measurements for the DUT include only contributions from the Transmitter.

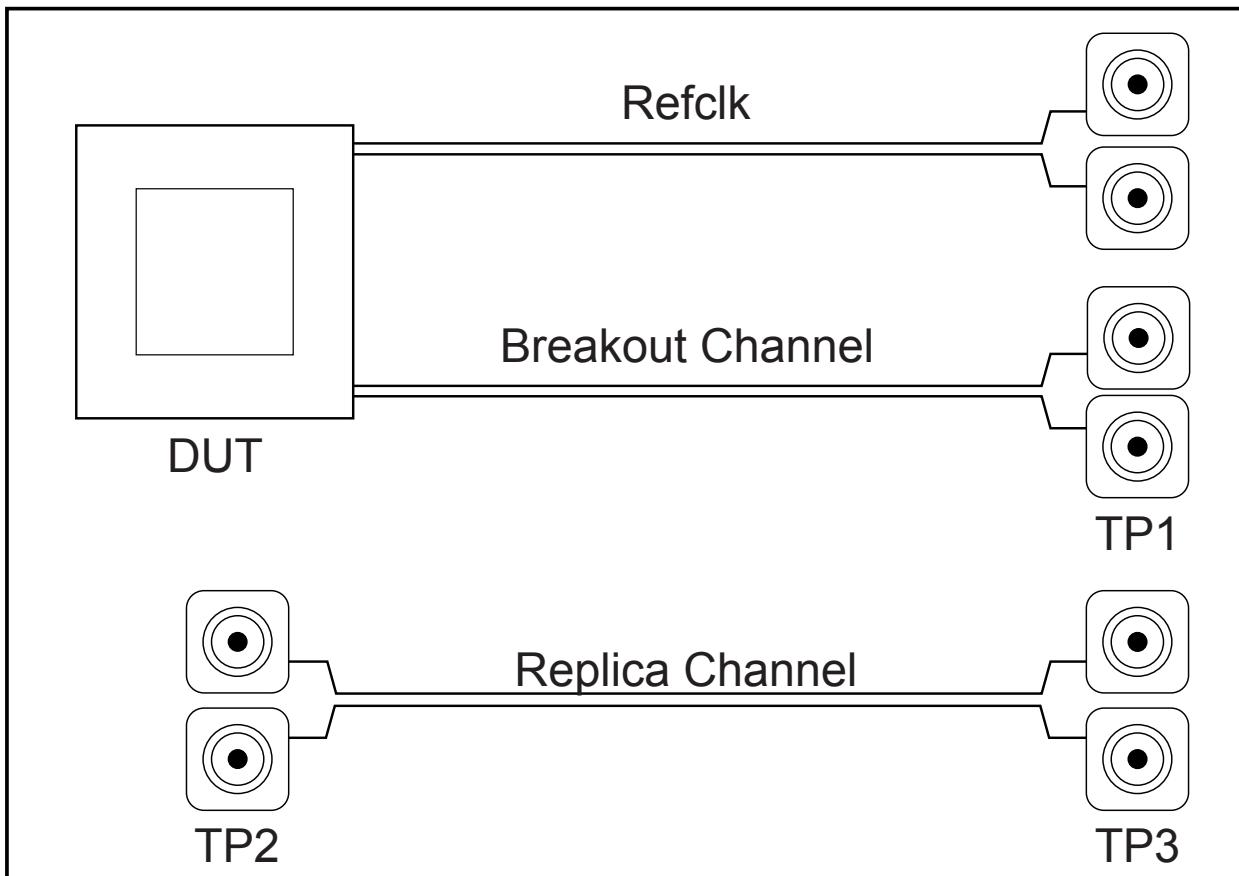
When testing a Transmitter it is desirable to have as many other PCI Express Lanes sending or receiving the compliance pattern as is feasible. Similarly, if the device supports other I/O it should also be sending or receiving on these interfaces. The goal is to have the Tx test environment replicate that found in a real system as closely as possible.



A-0811

Figure 8-1 Tx Test Board for Non-Embedded Refclk

The 4.0 version of the Tx specification also includes explicit support for Transmitters utilizing embedded Refclks. In this case the Tx under test is not driven with a low jitter clock source, and both the Tx data and Tx Refclk out must be sampled simultaneously by means of a 2-port measurement. For more details consult [Section 8.3.5.3](#). When an implementation is tested that is configured for the independent reference clock architecture only the data is sampled for both the Non-Embedded and Embedded reference clock cases.



A-0811-Embedded

Figure 8-2 Tx Test board for Embedded Refclk

8.3.1.1 Breakout and Replica Channels

In order to specify a Transmitter with a uniform set of Tx parameters it is necessary to establish a one-to-one correspondence between what is measurable at TP1 and the corresponding Tx voltage or jitter at the pin. This may be achieved by means of a breakout channel and a replica channel. The replica channel reproduces the electrical characteristics of the breakout channel as closely as possible, matching its length, layer transitions, etc, making it possible to de-embed Tx measurements to the pin of the DUT. All voltage parameters are de-embedded to the pins unless otherwise specified. While the specification does not define precise electrical characteristics for the replica and breakout channels, it is advisable to adhere to the following guidelines:

- Breakout channels should be the same length for each Lane and routed on as few layers as possible, thereby reducing the number of replica channels that need to be built and measured.
- Each routing layer on a test board should have a separate breakout channel where the via and pad structures of the breakout and replica channels on respective layers match as closely as possible.
- Break-out and replica channels should be designed to have an insertion loss of less than 2 dB at the nyquist frequency for the signaling rate (4 dB at nyquist if the maximum signaling rate is 16.0 GT/s or 32.0 GT/s) and a return loss of greater than 15 dB to nyquist when measured from either TP2 or TP3, which may require use of low loss dielectric, wide signal traces and back-drilling of break-out vias or use of micro-via technology.

- The impedance targets for the breakout channel are $100\ \Omega$ differential and $50\ \Omega$ single-ended. For best accuracy the actual breakout channel impedance should be within $\pm 5\%$ of these values. For larger deviations a more complex de-embedding technique may be required.

8.3.2 Voltage Level Definitions

A differential voltage is defined by taking the voltage difference between two conductors. In this specification, a differential signal or differential pair is comprised of a voltage on a positive conductor, V_{D+} , and a negative conductor, V_{D-} . The differential voltage (V_{DIFF}) is defined as the difference of the positive conductor voltage and the negative conductor voltage ($V_{DIFF} = V_{D+} - V_{D-}$). The Common Mode Voltage (V_{CM}) is defined as the average or mean voltage present on the same differential pair ($V_{CM} = [V_{D+} + V_{D-}] / 2$). This document's electrical specifications often refer to common mode peak-to-peak measurements or peak measurements, which are defined by the following equations.

$$V_{DIFFp-p} = (2 * \max |V_{D+} - V_{D-}|) \text{ (This applies to a symmetric differential swing)}$$

Equation 8-1 $V_{DIFFp-p}$

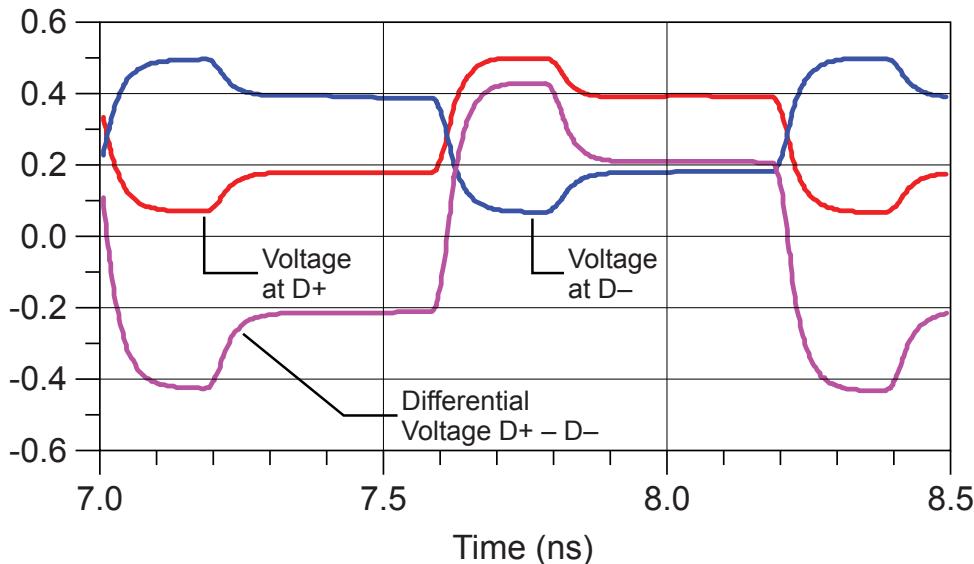
$$V_{TX-AC-CM-PP} = \max(V_{D+} + V_{D-})/2 - \min(V_{D+} + V_{D-})/2$$

Equation 8-2 $V_{TX-AC-CM-PP}$

Note: The maximum value is calculated on a per unit interval evaluation with unit interval boundaries determined by the behavioral CDR. The maximum function as described is implicit for all peak-to-peak and peak common mode equations throughout the rest of this chapter.

In this section, DC is defined as all frequency components below $F_{DC} = 30\ \text{kHz}$. AC is defined as all frequency components at or above $F_{DC} = 30\ \text{kHz}$. These definitions pertain to all voltage and current specifications.

An example waveform is shown in Figure 8-3. In this waveform the differential voltage (defined as $D+ - D-$) is approximately 800 mVPP, and the single-ended voltage for both $D+$ and $D-$ is approximately 400 mVPP for each. Note that while the center crossing point for both $D+$ and $D-$ is nominally at 200 mV, the corresponding crossover point for the differential voltage is at 0.0 V.



A-0547

Figure 8-3 Single-ended and Differential Levels

8.3.3 Tx Voltage Parameters

Tx voltage parameters include equalization coefficients, equalization presets, and min/max voltage swings.

8.3.3.1 2.5 and 5.0 GT/s Transmitter Equalization

Tx equalization at 2.5 and 5.0 GT/s is only de-emphasis. Tx equalization de-emphasis values at 2.5 and 5.0 GT/s are measured using the average ratio of transition to non-transition average eye amplitude at the 0.5 UI location using 500 repetitions of the compliance pattern.

8.3.3.2 8.0, 16.0, and 32.0 GT/s Transmitter Equalization

Tx voltage swing and equalization presets at 8.0, 16.0 and 32.0 GT/s are measured by means of a low frequency pattern within the compliance pattern. Consisting of a sequence of 64 zeroes followed by 64 ones, this pattern permits an accurate measurement of voltage since ISI effects will have decayed and the signal will have approached a steady state. 8.0, 16.0, and 32.0 GT/s transmitters must implement a coefficient-based equalization mode in order to support fine grained control over Tx equalization resolution. Additionally, a Transmitter must support a specified number of presets that give a coarser control over Tx equalization resolution. Both coefficient space and preset space are controllable via messaging from the Receiver via an equalization procedure. The equalization procedure operates on the same physical path as normal signaling and is implemented via extensions to the existing protocol Link layer.

All 8.0, 16.0, and 32.0 GT/s Transmitters must implement support for the equalization procedure, whereas 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s Receivers may optionally make use of requests for the Transmitter on the Link partner to update Transmitter equalization. Details of the equalization procedure may be found in the Physical Layer Logical Block chapter.

Tx equalization coefficients are based on the following FIR filter relationship as shown in Figure 8-4. Equalization coefficients are subject to constraints limiting their max swing to \pm unity with c_{-1} and c_{+1} being zero or negative. The

inclusion of the unity condition means that only two of the three coefficients need to be specified to fully define v_{out_n} . In this specification the two coefficients so specified are c_{-1} and c_{+1} , where c_0 is implied. Note that the coefficient magnitude is not the same as the Tx voltage swing magnitude.

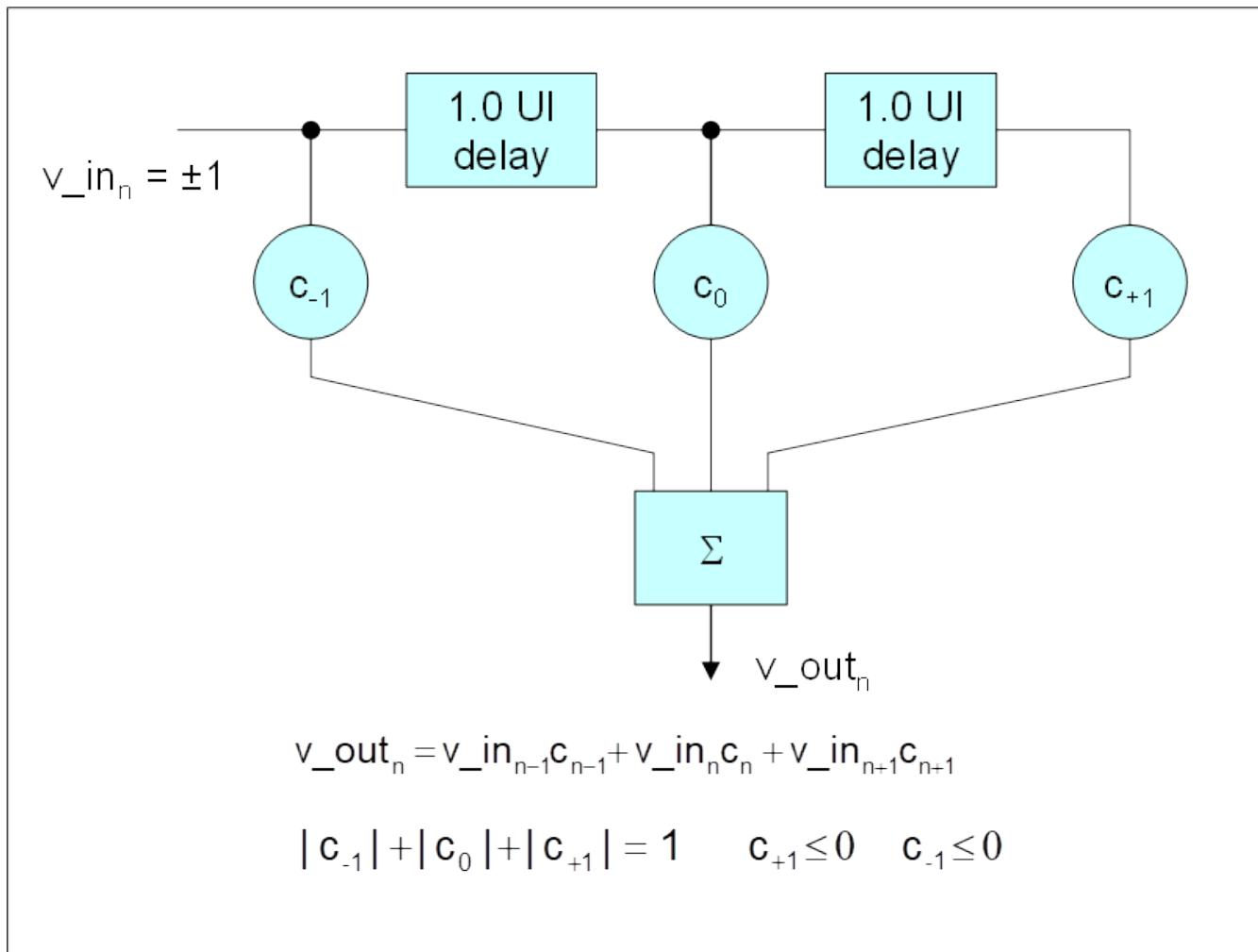
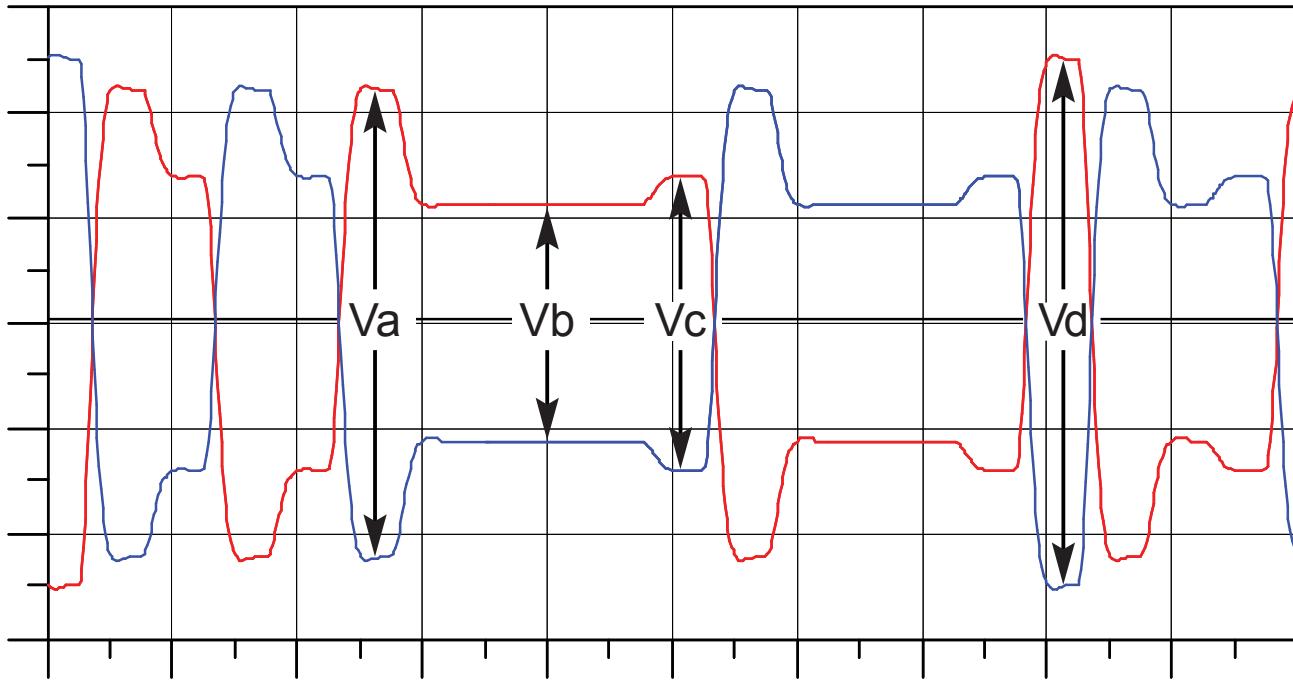


Figure 8-4 Tx Equalization FIR Representation

8.3.3.3 Tx Equalization Presets

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1. Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (V_c) is referred to as pre-shoot, while the post-cursor (V_b) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows pre-shoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, V_d , is also shown to illustrate that, when both c_{+1} and c_{-1} are non-zero, the swing of V_a does not reach the maximum as defined by V_d . Figure 8-5 is shown as an example of transmitter equalization, but it is not intended to represent the signal as it would appear for measurement purposes. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms, as shown in Figure 8-6 and Figure 8-7.

The presets defined in Table 8-1 and Table 8-2 are numbered to match the designations in Table 4-4.



$$\text{De-emphasis} = 20 \log_{10} V_b/V_a$$

$$\text{Preshoot} = 20 \log_{10} V_c/V_b$$

$$\text{Boost} = 20 \log_{10} V_d/V_b$$

A-0813

Figure 8-5 Definition of Tx Voltage Levels and Equalization Ratios

Table 8-1 lists the values for presets; at 8.0 GT/s, 16.0 GT/s and 32.0 GT/s all preset values must be supported for full swing signaling.

Table 8-1 Tx Preset Ratios and Corresponding Coefficient Values

Preset #	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000

Preset #	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	V _a /V _d	V _b /V _d	V _c /V _d
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	Note 2.	0.000	Note 2.	1.000	Note 2.	Note 2.

Notes:

1. Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

8.3.3.4 Measuring Tx Equalization for 2.5 GT/s and 5.0 GT/s

Tx equalization de-emphasis values at 2.5 and 5.0 GT/s are measured using the average ratio of transition to non-transition eye heights at the 0.5 UI location using 500 repetitions of the compliance pattern.

8.3.3.5 Measuring Presets at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s

Figure 8-6 and Figure 8-7 illustrate the waveforms observed when measuring presets using the 64-zeroes/64-ones sequence that is part of the compliance pattern. Depending on whether the preset implements de-emphasis, preshoot, or both, the corresponding waveshape will differ. The two cases illustrated below show preshoot and de-emphasis as can be observed by noting whether the equalization occurs before or after an edge transition. For the case where both de-emphasis and preshoot are present, boost occurs both before and after each edge transition. In all cases the voltage of interest occurs during the flat portion (at V_b) of the waveform, where it can be accurately measured independent of high frequency effects. Measurements of V_b are made using the average voltage from UI 57 to 62 in all the 64 zeroes and 64 ones sequences over 500 repetitions of the compliance pattern.

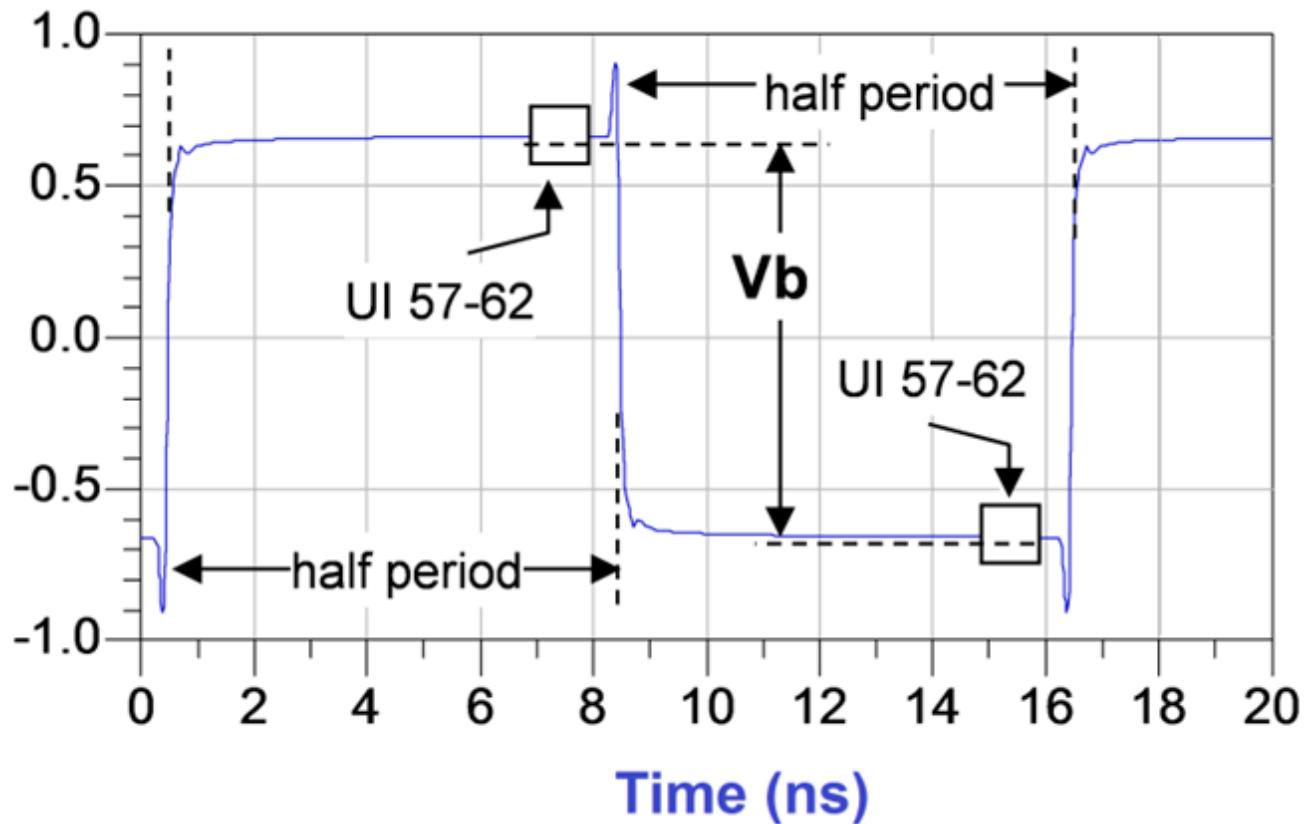


Figure 8-6 Waveform Measurement Points for Pre-shoot

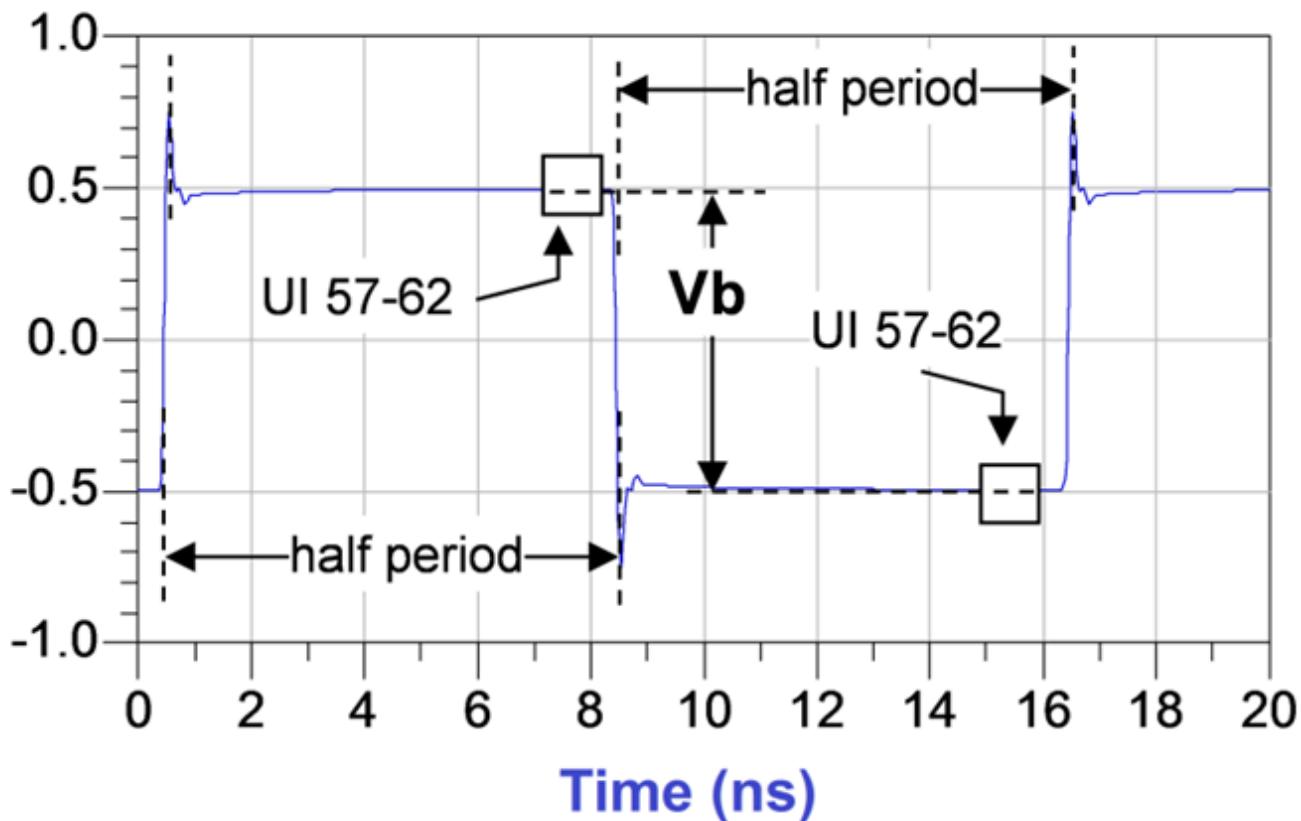


Figure 8-7 Waveform Measurement Points for De-emphasis

With the exception of P4 (for which both pre-shoot and de-emphasis are 0.0 dB) it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are 1 UI wide and therefore subject to attenuation by the package and the breakout channel. Instead the Va and Vc values are obtained by setting the DUT to a different preset value where the former's Va or Vc voltage occurs during the latter's Vb interval. Table 8-2 lists the preset values required to measure each of the Va and Vc values from which their preshoot or de-emphasis values may be derived from the ratio of Vb values for the indicated presets.

Table 8-2 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20 \log_{10} (Vb(i)/Vb(j))$	Preshoot (dB) $20 \log_{10} (Vb(i)/Vb(j))$
P4	N/A	N/A
P1	P1 / P4	N/A
P0	P0 / P4	N/A
P9	N/A	P4 / P9
P8	P8 / P6	P3 / P8
P7	P7 / P5	P2 / P7
P5	N/A	P4 / P5

Preset Number	De-emphasis (dB) $20 \log_{10} (V_b(i)/V_b(j))$	Preshoot (dB) $20 \log_{10} (V_b(i)/V_b(j))$
<u>P6</u>	N/A	<u>P4 / P6</u>
<u>P3</u>	<u>P3 / P4</u>	N/A
<u>P2</u>	<u>P2 / P4</u>	N/A
<u>P10</u>	<u>P10 / P4</u>	N/A

8.3.3.6 Method for Measuring $V_{TX-DIFF-PP}$ at 2.5 GT/s and 5.0 GT/s

$V_{TX-DIFF-PP}$ ($V_{TX-DIFF-PP-LOW}$ for reduced swing) at 2.5 GTs and 5.0 GT/s are measured using the average transition eye amplitude at the 0.5 UI location using 500 repetitions of the compliance pattern.

8.3.3.7 Method for Measuring $V_{TX-DIFF-PP}$ at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s

The range for a Transmitter's output voltage swing, (specified by V_d) with no equalization is defined by $V_{TX-DIFF-PP}$ ($V_{TX-DIFF-PP-LOW}$ for reduced swing), and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 8-8 . High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern.

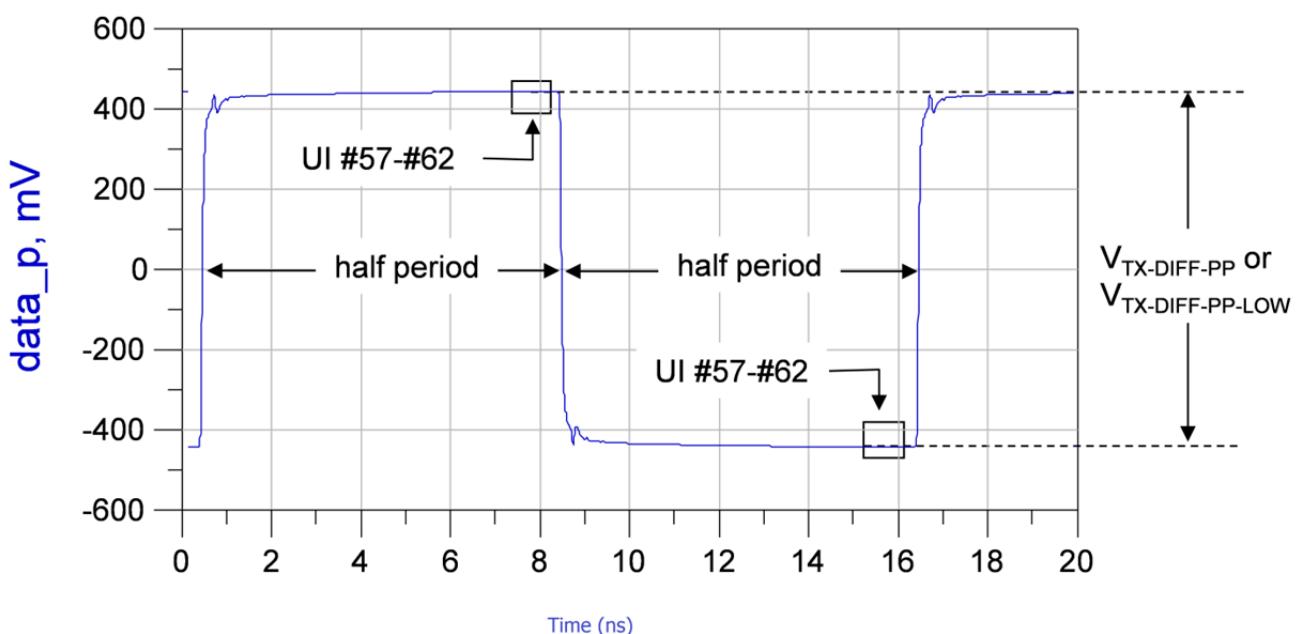


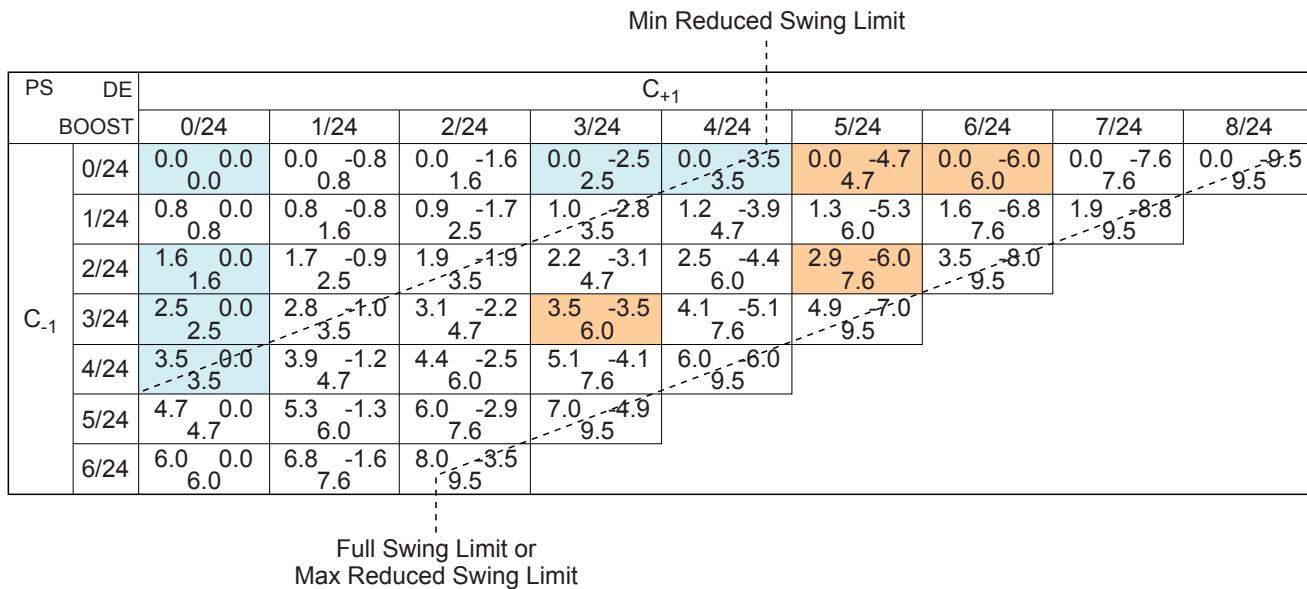
Figure 8-8 $V_{TX-DIFF-PP}$ and $V_{TX-DIFF-PP-LOW}$ Measurement

8.3.3.8 Coefficient Range and Tolerance

8.0 GT/s, 16.0 GT/s, and 32.0 GT/s Transmitters are required to inform the Receiver of their coefficient range and tolerance. Coefficient range and tolerance are constrained by the following requirements.

- Coefficients must support all eleven presets and their respective tolerances as defined in Table 8-2
- All Transmitters must meet the full swing signaling $V_{TX-EIEOS-FS}$ limits.
- Transmitters may optionally support reduced swing, and if they do, they must meet the $V_{TX-EIEOS-RS}$ limits.
- The coefficients must meet the boost and resolution ($V_{TX-BOOST-FS}$, $V_{TX-BOOST-RS}$ and $EQ_{TX-COEFF-RES}$) limits defined in Table 8-6.

When the above constraints are applied the resulting coefficient space may be mapped onto a triangular matrix, an example of which is shown in Figure 8-9. The matrix may be interpreted as follows: Pre-shoot and de-emphasis coefficients are mapped onto the Y-axis and X-axes, respectively. In both cases the maximum granularity of 1/24 is assumed. Each matrix cell, corresponding to a valid combination of preshoot and de-emphasis coefficients, has three entries corresponding to preshoot (PS), de-emphasis (DE), and boost (as shown in the upper left hand corner). Diagonal elements are defined by the maximum boost ratio. Those cells highlighted in blue are presets required for reduced swing, while cells in either blue or orange represent presets required for full swing signaling. Note that this figure is informative only and is not intended to imply any particular Tx implementation or to alter requirements for nominal preset equalization values and allowed ranges.



A-0816

Figure 8-9 Transmit Equalization Coefficient Space Triangular Matrix Example

8.3.3.9 EIEOS and $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ Limits

EIEOS signaling is defined for 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s only. At 5.0 GT/s the K28.7 Symbol is used. $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured using the EIEOS sequence contained within the compliance pattern for 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s. At 8.0 GT/s the EIEOS pattern consists of eight consecutive ones followed by the same

number of consecutive zeroes, where the pattern is repeated for a total of 128 UI. At 16.0 GT/s the EIEOS pattern consists of 16 consecutive ones followed by the same number of consecutive zeroes, where the pattern is repeated for a total of 128 UI. At 32.0 GT/s the EIEOS pattern consists of 32 consecutive ones followed by the same number of consecutive zeroes, where the pattern is repeated for a total of 128 UI. At 32.0 GT/s the pattern is repeated for two consecutive blocks.

A transmitter sends an EIEOS to cause an exit of Electrical Idle at the Receiver. This pattern guarantees the Receiver will properly detect the EI Exit condition with its squelch exit detect circuit, something not otherwise guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ± 1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with preset P1.

A Transmitter is not always permitted to generate the maximum boost level noted above. In particular, a Transmitter that cannot drive significantly more than 800 mVPP is limited by the need to meet $V_{TX-EIEOS-FS}$. The Tx must reject any adjustments to its presets or coefficients that would violate the $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ limits. The EIEOS voltage limits are imposed to guarantee the EIEOS threshold of 175 mVPP at the Rx pin.

Figure 8-10 illustrates the de-emphasis peak as observed at the pin of a Tx for $V_{TX-EIEOS-FS}$. At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI at 8.0 GT/s, UI number 5-14 at 16.0 GT/s, and UI number 9-28 at 32.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform over 500 repetitions of the compliance pattern. $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

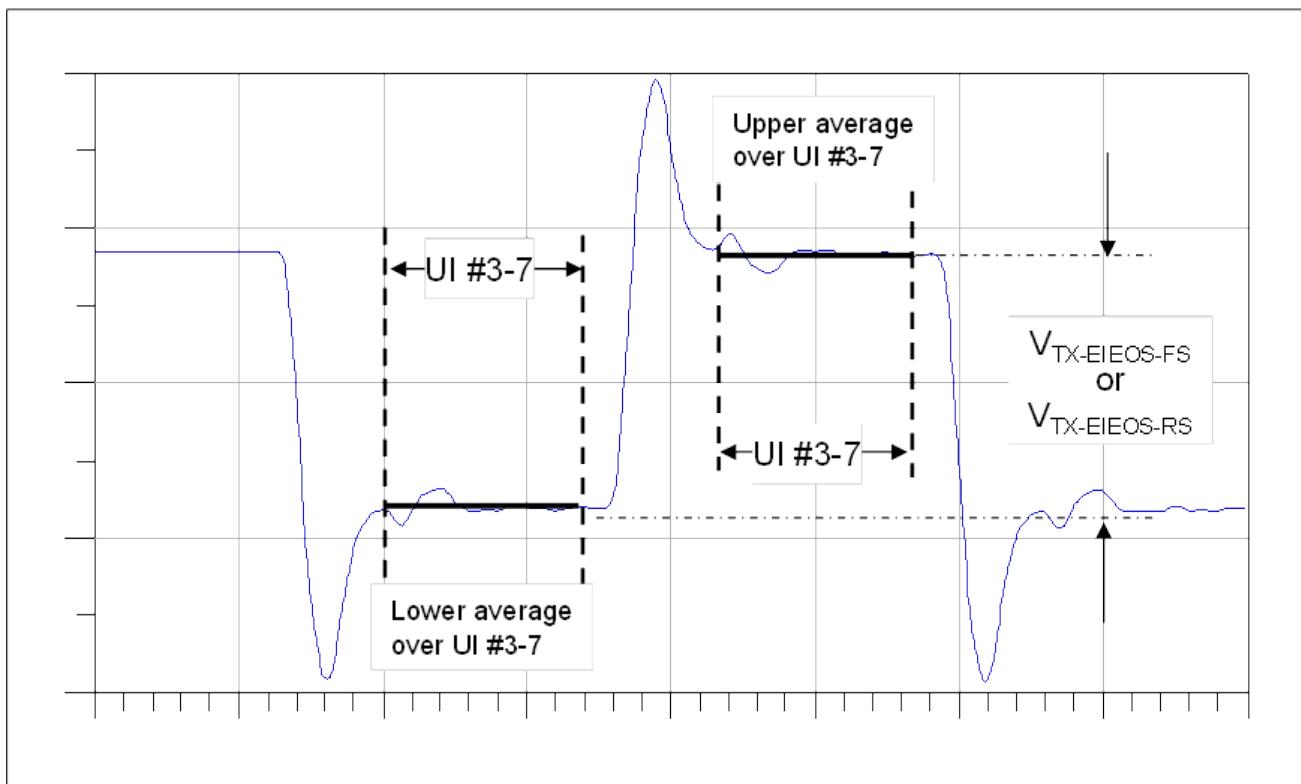


Figure 8-10 Measuring $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ at 8.0 GT/s

8.3.3.10 Reduced Swing Signaling

PCI Express Transmitters may optionally support a reduced swing signaling. It is left as an implementation option to define the maximum reduced swing voltage value for $V_{TX-DIFF-PP-LOW}$ anywhere up to the maximum full swing voltage. The minimum for $V_{TX-DIFF-PP-LOW}$ is captured indirectly by the constraint imposed by $V_{TX-EIEOS-RS}$, so there is no need to define a separate minimum limit for $V_{TX-DIFF-PP-LOW}$. Reduced swing limits the range of presets and the maximum boost. The boost for reduced swing must be in the region shown in Figure 8-9 between the Max reduced swing limit and minimum reduced swing boost limit.

Form factors are permitted to disallow, optionally allow, or require Reduced Swing Signaling, depending on the channel requirements for the form factor. When Reduced Swing Signaling is allowed or required it is required that form factor specifications provide any additional details necessary to support interoperability.

8.3.3.11 Effective Tx Package Loss at 8.0 GT/s, 16.0 GT/s and 32.0 GT/s

Package loss (including silicon driver bandwidth) is represented by the $ps21_{TX}$ parameter. Since both package IL and driver bandwidth affect the signal as observed at the Tx pin, the $ps21_{TX}$ parameter has the advantage of representing both of these effects, while permitting the measurement to be made at a point (TP1) that can easily be probed. It is necessary to include a package loss parameter in the Tx specification, since the voltage swing parameters ($V_{TX-DIFF-PP}$ and $V_{TX-DIFF-PP-LOW}$) are defined at an equivalent pulse frequency of 1/128 UI and purposely do not capture high frequency driver or package loss effects.

At 16.0 GT/s and 32.0 GT/s, separate ps21_{TX} parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

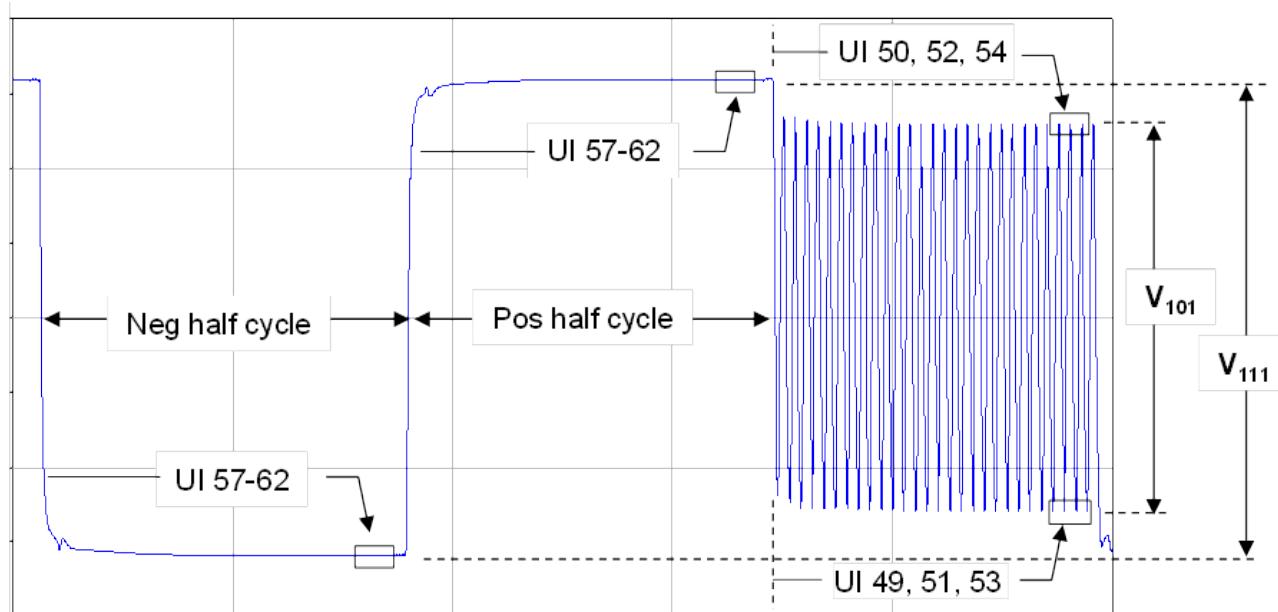
The ps21_{TX} parameter is informative for 16.0 GT/s Root Package devices and for Non-Root Package devices that only support PCI Express standard form factors (i.e., CEM, M.2, etc.). The ps21_{TX} parameter is normative for all 8.0 GT/s and 32.0 GT/s devices and for 16.0 GT/s Non-Root Package devices that support captive channels. (See [Table 8-3](#) below).

Table 8-3 Cases that the Reference Packages and ps21_{TX} Parameter are Normative

	8.0 GT/s and 32.0 GT/s		16.0 GT/s	
	Root Package Device	Non-Root Package Device	Root Package Device	Non-Root Package Device
Device supports captive channels	Normative	Normative	Informative	Normative
Device does not support captive channels	Normative	Normative	Informative	Informative

All implementations of PCI Express standard form factors must still meet form factor requirements. Devices for which the ps21_{TX} parameter is informative, as defined above must provide a package model for use in channel compliance if they do not meet the informative ps21_{TX} parameter.

Package loss is measured by comparing the 64-zeroes/64-ones voltage swing (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. Measurements shall be made averaging over 500 repetitions of the compliance pattern.



$$\text{ps21}_{\text{TX}} = 20 \log_{10} (V_{101}/V_{111})$$

Figure 8-11 Compliance Pattern and Resulting Package Loss Test Waveform

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the average voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over 500 repetitions of the compliance pattern.

At 32.0 GT/s only the ps21_{TX} parameter is calculated by filtering the captured voltage waveforms normally used for ps21_{TX} measurements as follows:

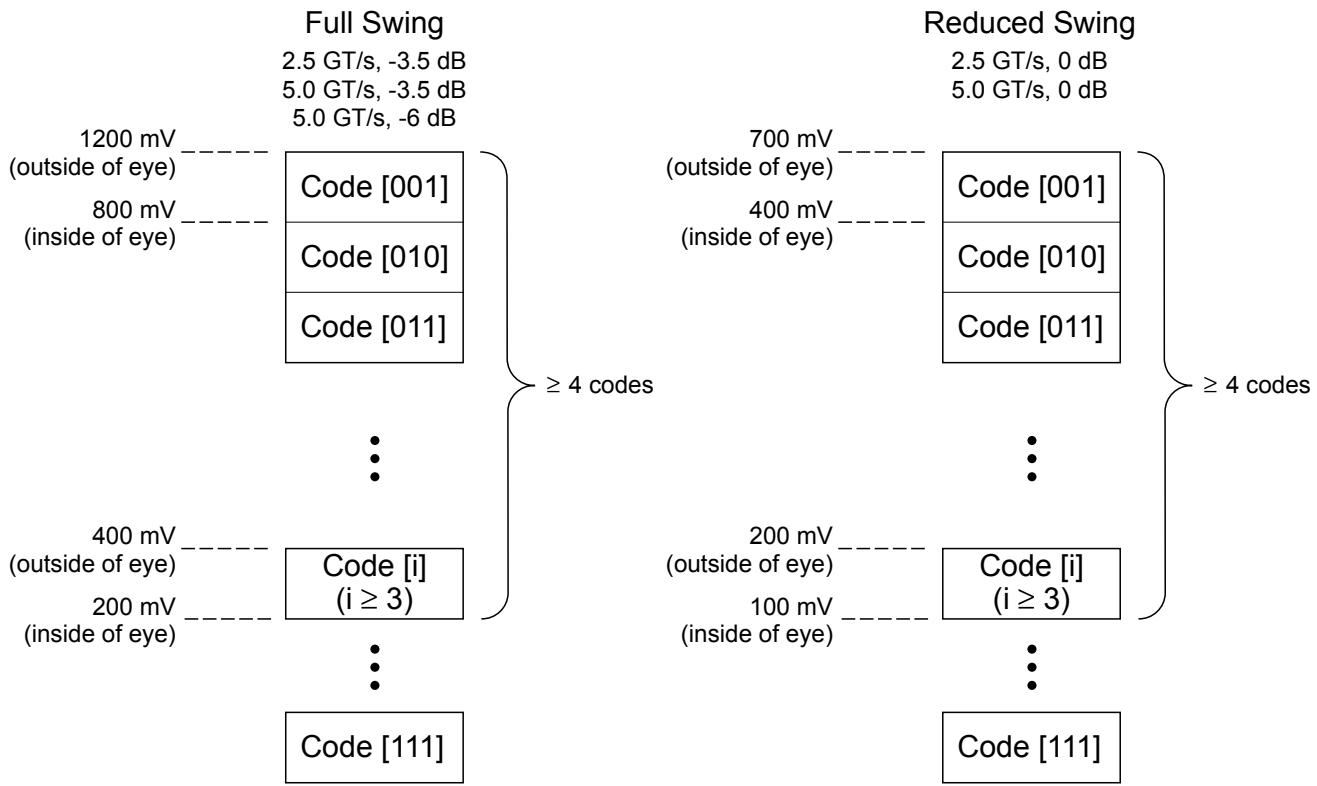
- V_{111} is measured from a filtered voltage waveform with a first order (20 dB/decade) low pass filter with a -3 dB corner frequency at 1 GHz applied.
- V_{101} is measured from a filtered voltage waveform with a first order (20 dB/decade) high pass filter with a -3 dB corner frequency at 7 GHz applied.

8.3.4 Transmitter Margining

Transmitters shall implement a margining procedure that allows the Tx launch voltage to be adjusted. Margining is enabled by programming a register set. Due to the larger range of Transmitter equalization, 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s Tx margining is subject to additional constraints: Tx margining at these speeds shall not require any coefficient or preset resolution finer than can be generated with 1/24 coefficient resolution defined for normal operation, and shall not require more Tx accuracy or capability than is required to support normal operation. It is acceptable that V_b fall below the limit set by $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$, although proper end to-end operation is no longer guaranteed.

Transmitter equalization accuracy requirements do not need to be met during margining. A Transmitter is not required to change the FS/LF values it sends in TS1 Ordered Sets during margining from the values used in normal operation.

There are 8 encoded values for transmit margin from 000b to 111b. Encoding 000b represents the normal operating range. For all supported data rates and Tx signalling mode (full swing or reduced swing), encoding 001b must produce a $V_{TX-DIFF-PP}$ compliant with the specification limits. At least three additional encodings with monotonically decreasing values for $V_{TX-DIFF-PP}$ must be supported for each data rate and Tx swing mode. For full swing signalling there must be at least one encoding with index 100b or higher that produces a $V_{TX-DIFF-PP}$ between 200 and 400 mV. For reduced swing signalling there must be at least one encoding with value 100b or higher that produces a $V_{TX-DIFF-PP}$ between 100 and 200 mV.



A-0574A

Figure 8-12 2.5 and 5.0 GT/s Transmitter Margining Voltage Levels and Codes

8.3.5 Tx Jitter Parameters

Jitter limits are defined identically for all data rates, although their respective values will vary with data rate. Jitter is measured at the zero crossing point at full speed using the Compliance Pattern. When measuring a particular Tx Lane it is necessary to ensure that all other PCI Express Lanes are transmitting Compliance Pattern in order to capture Tx die and package crosstalk effects. When measuring Tx jitter it is required for the DUT to drive as many of its outputs as would occur during normal operation in a system environment. When measuring jitter, the preset yielding the lowest jitter value should be selected.

8.3.5.1 Post Processing Steps to Extract Jitter

Measured Tx jitter is referenced to the Tx pin, and depending on what type of jitter is being measured and what reference clock architecture is being tested, is subsequently referenced to a recovered data clock, an embedded reference clock captured simultaneously with the data, or to a data edge. Data captured at TP1 requires post processing in order to remove the effects of the breakout channel and to regenerate a data clock (when an embedded reference clock is not captured simultaneously with the data).

8.3.5.2 Applying CTLE or De-embedding

Direct probing at a Transmitter's pins is not generally feasible, so data is instead measured at TP1 of the breakout channel. By means of the replica channel it is possible to determine the loss vs. frequency characteristics of the breakout

channel and de-embed this channel, resulting in measurements that are effectively referenced to the DUT's pins. Note that since de-embedding amplifies HF noise there is a practical frequency cutoff limit to de-embedding. As de-embedding amplifies HF channel and measurement noise, an HF cutoff limit must be applied to de-embedding, depending on data rate as shown in Table 8-4.

Table 8-4 Recommended De-embedding Cutoff Frequency

Data Rate	HF Cutoff limit for de-embedding
8.0 GT/s	8 GHz - 12 GHz
16.0 GT/s	20 GHz
32.0 GT/s	33 GHz

Jitter is decomposed into data dependent and uncorrelated terms. This separation process effectively separates the jitter caused by package effects from that caused by signal integrity effects. As a result the uncorrelated jitter terms define jitter as it would appear at the die pad.

As an alternative to de-embedding at 16.0 GT/s the -12 dB CTLE in the reference equalizer can be applied to the data measured at TP1 for measuring all uncorrelated jitter parameters (not DDJ).

It is recommended that s-parameters for de-embedding are measured to at least 3 times the Nyquist frequency.

As an alternative to de-embedding at 32.0 GT/s any CTLE curve in the reference equalizer can be applied to the data measured at TP1 for measuring all uncorrelated jitter parameters (not DDJ). The CTLE curve that gives the lowest result for $T_{TX-UPW-TJ}$ is used.

If both de-embedding and CTLE approaches are used and given different answers only the lower values for the uncorrelated jitter parameters are used.

8.3.5.3 Independent Refclk Measurement and Post Processing

A Transmitter may operate in the Independent Refclk (IR) mode, in which case the Transmitter may not provide a Refclk output. In this case a single-port jitter measurement is required. The post processing algorithm must employ the appropriate model CDR for the reference clock architecture being tested.

8.3.5.4 Embedded and Non Embedded Refclk Measurement and Post Processing

When the transmitting PCIe device is driven from an external source to its Refclk pin it permits the Tx under test to be driven with a clean Refclk as shown in Figure 8-1.

The specification now explicitly supports the complete matrix of Refclk options, including where the Refclk is embedded, where the reference clock is external, where the reference clock is available at the DUT's pins, and where the reference clock is not available at the DUT's pins. Table 8-5 lists the post processing requirements for each of the four possible combinations. Embedded Refclk with Refclk available at the DUT's pin represents a special case where any jitter common to both the Refclk and the data must be removed via a two-port measurement.

If the DUT supports multiple Refclk modes, as described in Table 8-5 then the Tx needs to be tested in each of the Refclk modes it supports.

Table 8-5 Tx Measurement and Post Processing For Different Refclks

	Embedded Refclk	Non-Embedded Refclk
Refclk available at DUT pin and not testing SRIS mode	2-port measurement, CC CDR, PLL ¹ and 10 ns transport delay ²	1-port measurement, CC CDR, clean external Refclk
Refclk not available at DUT pin or testing SRIS mode	1-port measurement, SRIS CDR	1-port measurement, CC CDR, clean external Refclk

Notes:

1. PLL characteristics are defined in Refclk section for each data rate.
2. Refer to [Section 8.6.6](#) for a discussion of the transport delay

8.3.5.5 Behavioral CDR Characteristics

A behavioral CDR filter is applied to reject low frequency jitter that would normally be tracked by the CDR in a Receiver. As such, the behavioral CDR represents a bounding function for actual CDR implementations. Rolloff characteristics of the behavioral CDR are dependent on whether the corresponding DUT supports an embedded vs. non-embedded Refclk, is operating in CC or IR mode, and whether the Refclk pin is available for probing (see [Table 8-5](#)). In all cases the behavioral CDR represents a highpass filter function where the corner frequency depends on the Tx data rate. [Figure 8-13](#) shows the CC first-order CDR transfer functions for an f_{3dB} of 1.5 MHz, 5.0 MHz, and 10 MHz that corresponds to 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s, respectively. The 10 MHz behavioral CDR is also used for CC Transmitter and CC Reference Clock testing for 16.0 GT/s and, optionally, for Receiver Stressed Eye calibration when 32.0 GT/s is not supported.

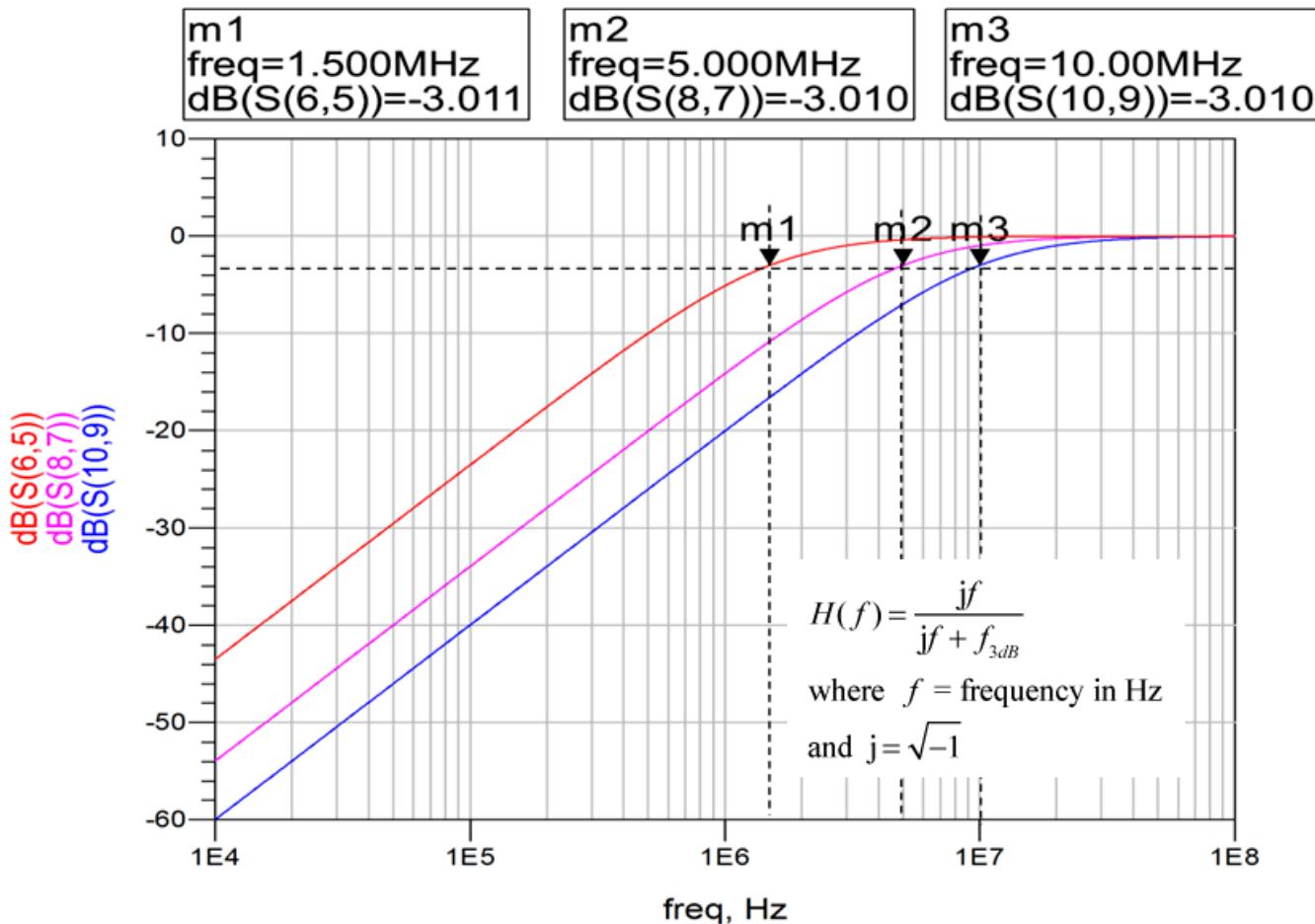


Figure 8-13 First Order CC Behavioral CDR Transfer Functions

Figure 8-14 illustrates second order CDR transfer functions corresponding to 2.5 GT/s and 5.0 GT/s. These functions are defined by a ζ of 0.707 and an f_{3dB} of 1.5 MHz and 5.0 MHz, respectively. Behavioral transfer functions for 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s approximate the piecewise linear sinusoidal jitter (S_j) masks shown in Section 8.4.2.2.1. SRIS capable Transmitters must be evaluated using these behavioral transfer functions.

Note: The common clock (CC) and independent reference clock (IR) architectures are not interoperable - although it is possible to design a single Receiver that meets both sets of electrical requirements.

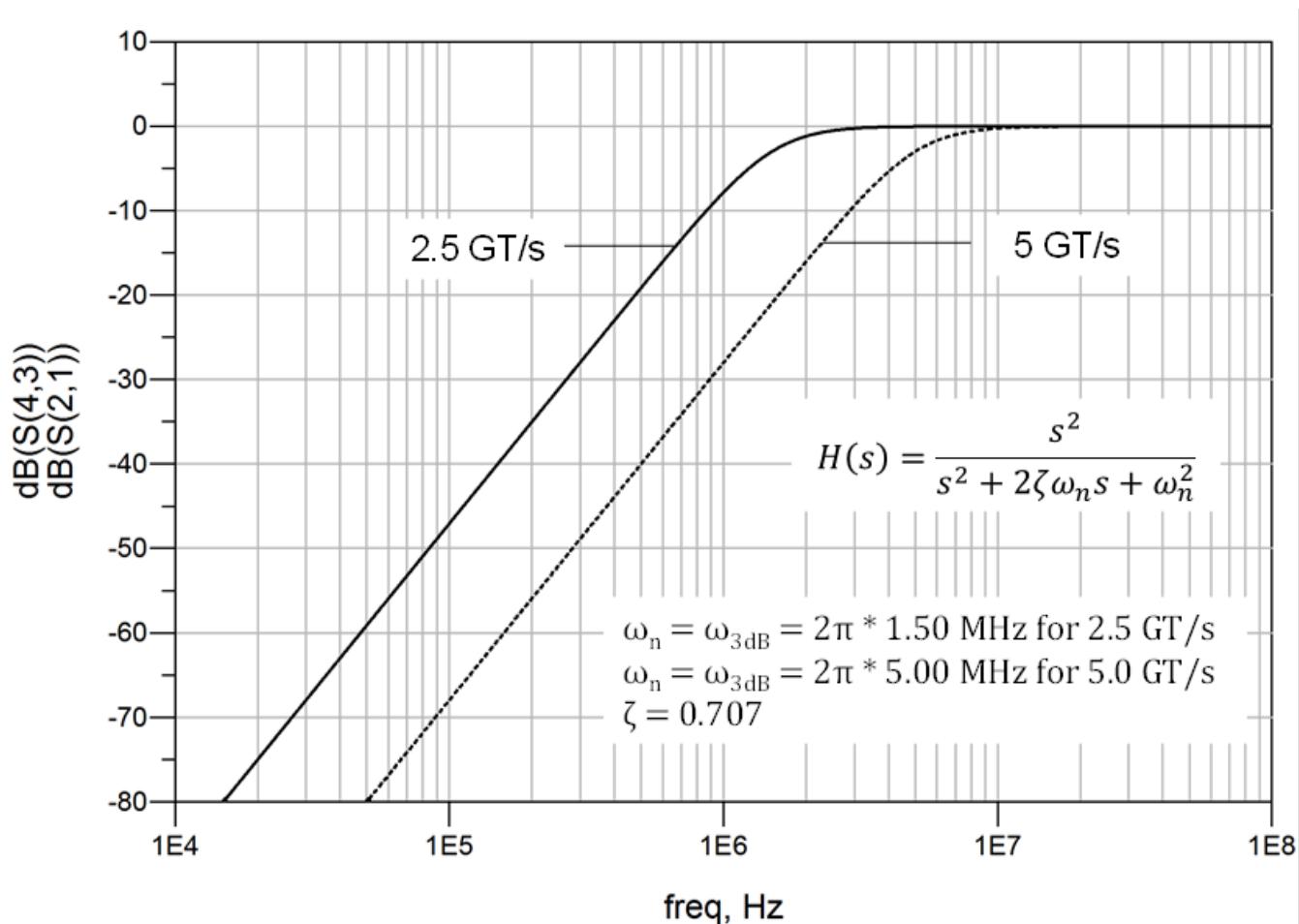


Figure 8-14 2nd Order Behavioral SRIS CDR Transfer Functions for 2.5 GT/s and 5.0 GT/s

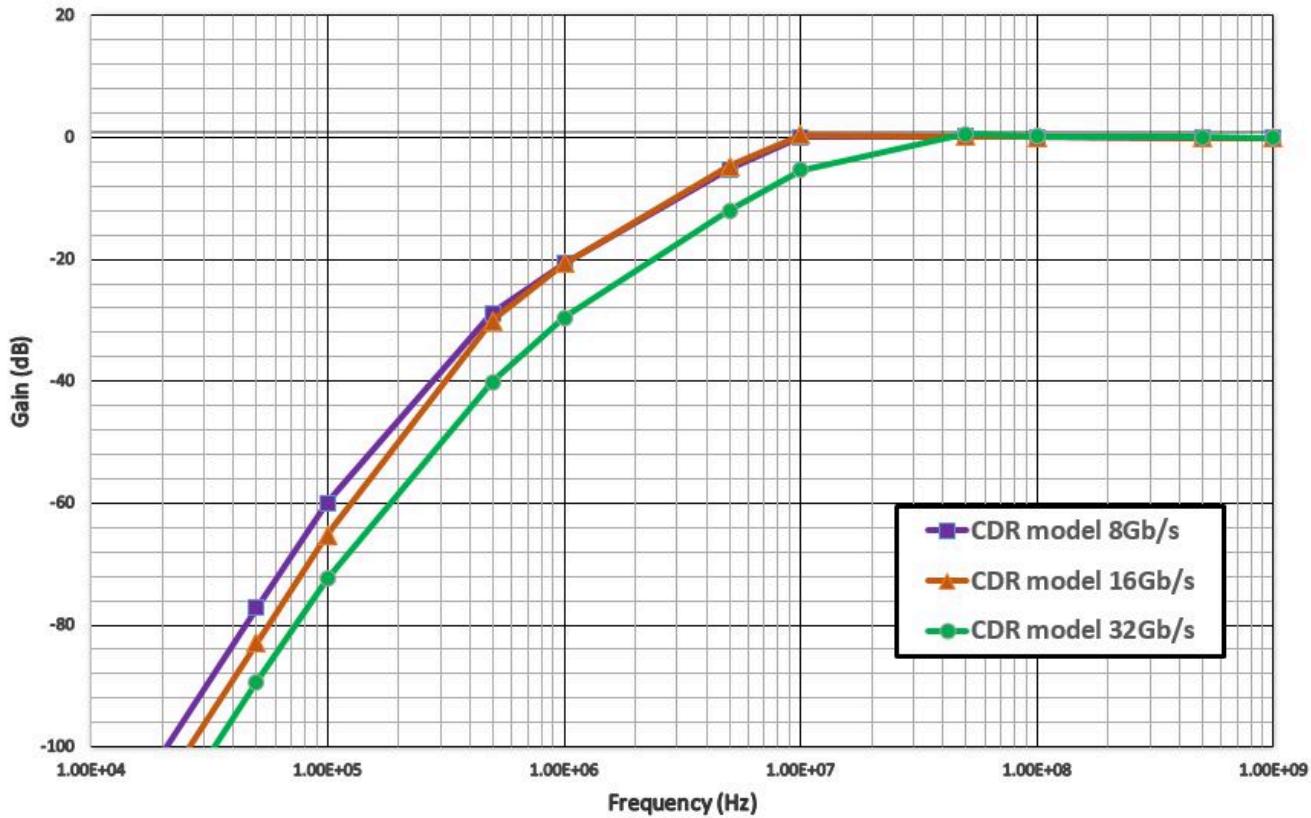


Figure 8-15 Behavioral SRIS CDR Function for 8.0 GT/s and SRIS and CC CDR for 16.0 GT/s

$$H(s) = \frac{s^2}{s^2 + sA + B} \times \frac{s^2 + 2\zeta_2\omega_0s + \omega_0^2}{s^2 + 2\zeta_1\omega_0s + \omega_0^2} \times \frac{s}{s + \omega_1}$$

$$\zeta_1 = \frac{1}{\sqrt{2}}$$

$$\zeta_2 = 1$$

$$\omega_0 = 10^7 \times 2\pi$$

$$\omega_1 = 4 \times 10^5 \times 2\pi$$

Equation 8-3 Behavioral SRIS CDR at 8.0 GT/s and SRIS and CC Behavioral CDR at 16.0 GT/s

$$A = 10^7 \times 2\pi$$

$$B = 2.2 \times 10^{12} \times (2\pi)^2$$

Equation 8-4 SRIS Behavioral CDR Parameters at 8.0 GT/s

$$A = 9.5 \times 10^6 \times 2\pi$$

$$B = 4.36 \times 10^{12} \times (2\pi)^2$$

Equation 8-5 SRIS and CC Behavioral CDR Parameters at 16.0 GT/s

$$H(s) = \frac{s^2}{(s + \omega_0) \times (s + \omega_1)} \times \frac{s^2 + 2\zeta_2\omega_0 s + \omega_0^2}{s^2 + 2\zeta_1\omega_0 s + \omega_0^2} \times \frac{s}{s + \omega_{LF}}$$

$$\zeta_1 = \frac{1}{\sqrt{2}}$$

$$\zeta_2 = 1$$

$$\omega_0 = 20 \times 10^6 \times 2\pi$$

$$\omega_1 = 1.1 \times 10^6 \times 2\pi$$

$$\omega_{LF} = 160 \times 10^3 \times 2\pi$$

Equation 8-6 SRIS and CC Behavioral CDR Parameters at 32.0 GT/s

8.3.5.6 Data Dependent and Uncorrelated Jitter

Measured at TP1 and de-embedded back to the pin, a Transmitter's jitter contains both data dependent and uncorrelated components. The data dependent components occur principally due to package loss and reflection. Uncorrelated jitter sources include PLL jitter, power supply noise, and crosstalk. The specification separates jitter into uncorrelated and data dependent bins, because such a separation matches well with the Tx and Rx equalization capabilities. Uncorrelated jitter is not mitigated by Tx or Rx equalization and represents timing margin that cannot be recovered via equalization. It is important that margin recoverable by means of equalization (data dependent) is not budgeted as non-recoverable jitter.

Once data dependent jitter has been removed from the Tx measurement it becomes possible to resolve the remaining jitter into T_j and deterministic jitter (Dual Dirac Model) (DJDD) components. High frequency jitter (which is subject to jitter amplification in the channel) is accounted for by separate $T_{TX-UPW-DJDD}$ and $T_{TX-UPW-TJ}$ parameters.

8.3.5.7 Data Dependent Jitter

While DDJ is not explicitly defined as a parameter in the specification, it is necessary to separate DDJ in order to eliminate package loss effects and reference the jitter parameters of interest to the Tx die pad. Separation of jitter into data dependent and uncorrelated components may be achieved by averaging techniques; for example, by having the Tx repeatedly drive the compliance test pattern which is a repeating pattern.

Figure 8-16 illustrates the relation between Tx data, recovered clock, and the data's PDF. Data dependent jitter is defined as the time delta between the PDF's mean for each zero crossing point and the corresponding recovered clock edge. A sufficient number of repeated patterns must be accumulated to yield stable mean values and PDF profiles for each transition. These PDFs are then utilized to extract uncorrelated jitter parameters.

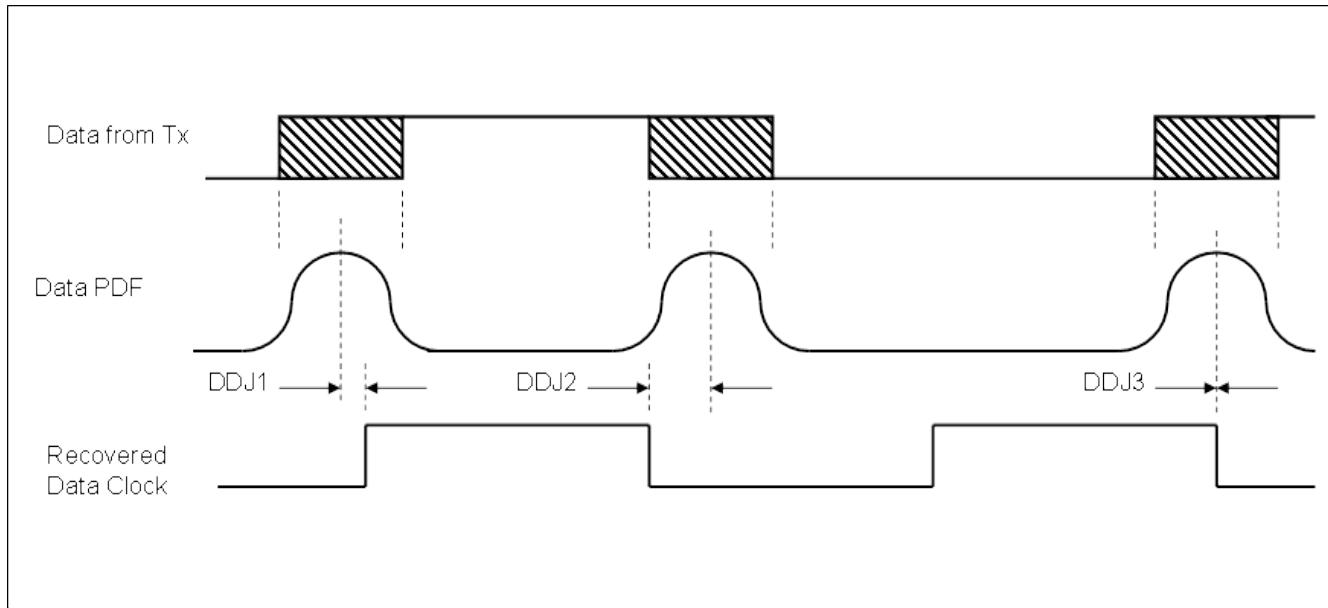
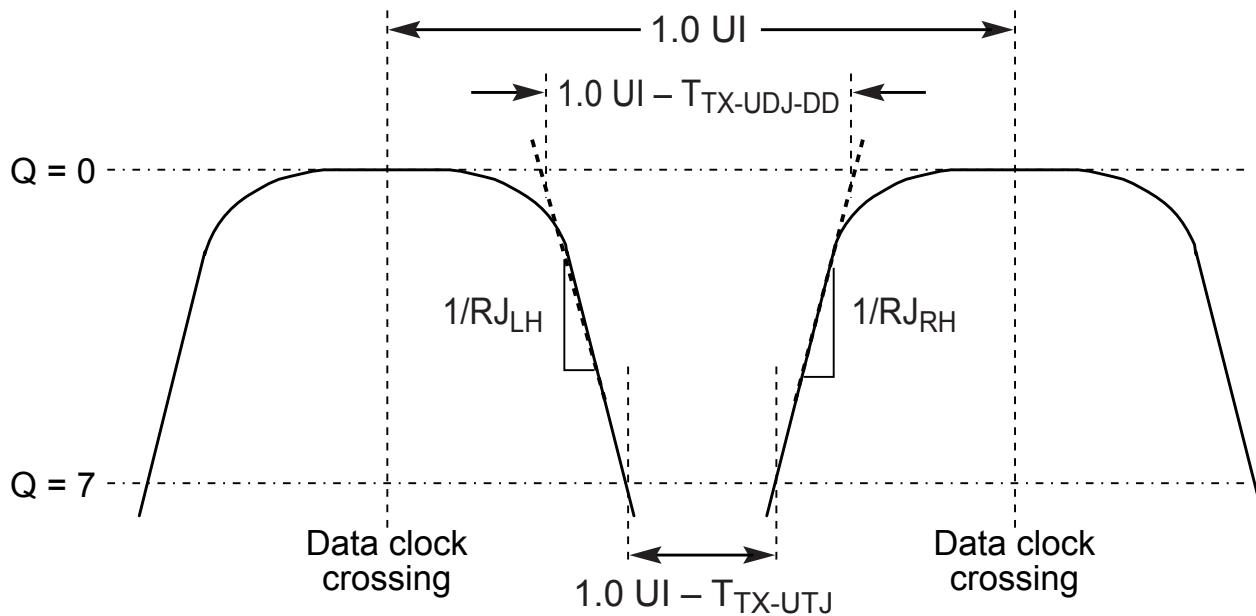


Figure 8-16 Relation Between Data Edge PDFs and Recovered Data Clock

8.3.5.8 Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$)

Uncorrelated Total Jitter (UTJ) and uncorrelated deterministic jitter (Dual Dirac model) (UDJDD) are referenced to a recovered data clock generated by means of a CDR tracking function. Uncorrelated jitter may be derived after removing the DDJ component from each PDF and combining the PDFs for all edges in the pattern. By appropriately converting the PDF to a Q-scale it is possible to obtain the graphical relation shown in Figure 8-17, from which T_{TX-UTJ} and $T_{TX-UDJDD}$ may be derived. In Figure 8-17 note that the two PDF curves are identical but that the fitted slopes, defined by $1/RJ_{LH}$ and $1/RJ_{RH}$, may differ.



A-0821A

Figure 8-17 Derivation of T_{TX-UTJ} and $T_{TX-UDJDD}$

8.3.5.9 Random Jitter (T_{TX-RJ}) (informative)

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJDD}$ from T_{TX-UTJ} and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

8.3.5.10 Uncorrelated Total and Deterministic PWJ ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$)

Pulse width jitter is defined as an edge to edge phenomenon on consecutive edges nominally 1.0 UI apart. Figure 8-18 illustrates how PWJ is defined, showing that it is typically present on both data edges of consecutive UI. To accurately quantify PWJ it is first necessary to remove the ISI contributions to PWJ. The shaded areas on either side of the unjittered edges represent the maximum amount of jitter about that edge. Note the jitter for one edge is assumed to be independent from the other.

An equivalent description of PWJ may be obtained by referencing to a fixed leading edge and having jitter contributions from both edges appear at the trailing edge. This approach yields a single PDF as shown below. Each 1 UI wide pulse in the pattern will have a different median for this PDF which is caused by ISI and F/2 jitter. The average of the medians for 1 UI wide pulses at odd and even UI numbers within the pattern are calculated, and the odd and even PDF's are normalized to the appropriate average of medians and summed to form an odd UI PDF and an even UI PDF. The final PDF is calculated from the sum of the summed odd and even UI PDFs. The key idea here is that the final PDF for uncorrelated PWJ should include F/2 or odd/even UI jitter

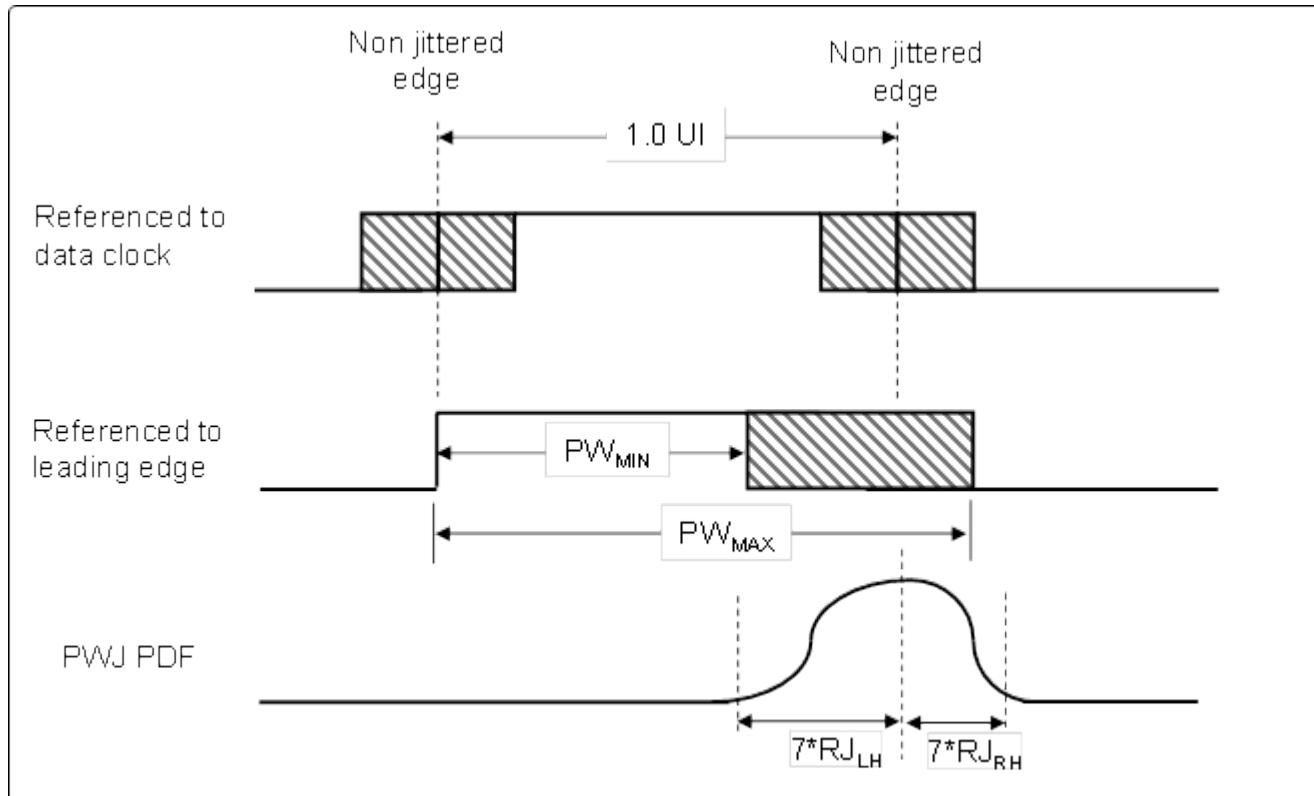


Figure 8-18 PWJ Relative to Consecutive Edges 1 UI Apart

The PDF of jitter around each non-jittered edge may be converted into the Q-scale (see Figure 8-19) from which $T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$ may be derived in a manner analogous to T_{TX-UTJ} and $T_{TX-UDJDD}$. Note that the PDF may not be symmetric, and the tail of interest is RJ_{LH} , since it represents pulse compression.

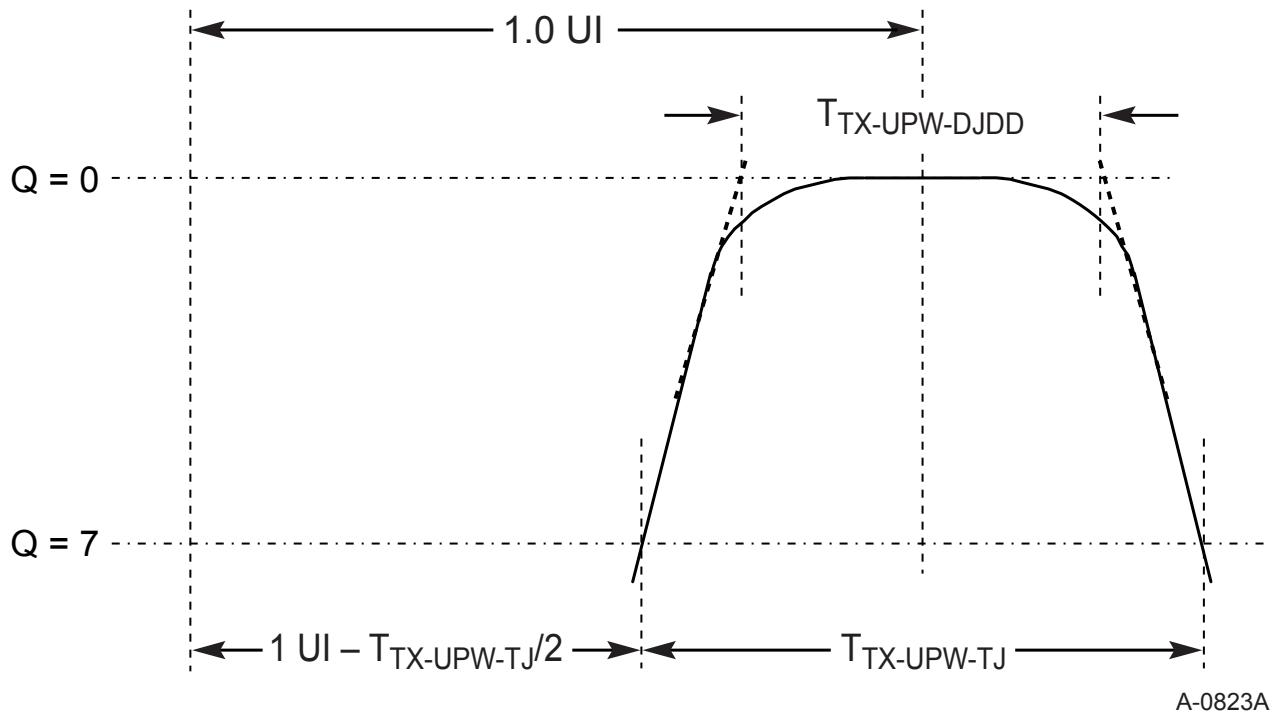


Figure 8-19 Definition of $T_{TX-UPW-DJDD}$ and $T_{TX-UPW-TJ}$ Data Rate Dependent Transmitter Parameters

8.3.6 Data Rate Dependent Parameters

Note: the jitter margins for 2.5 GT/s and 5.0 GT/s were previously defined at the device's pins. For 2.5 GT/s the jitter was defined via a single parameter that lumped DDJ, UDJDD, UTJ, PWJ-DDJ and PWJ-TJ into a single quantity. Consequently, it is necessary to first remove the DDj jitter component. Since there was no previous UDJ-UTj separation T_{TX-UTj} and $T_{TX-UDJDD}$ are set equal to each other. Similarly, there was no UTj-PWj separation, so it is necessary to assume that the entirety of the uncorrelated jitter is PWJ that occurs oppositely on consecutive edges of a 1 UI wide pulse.

For 5.0 GT/s a similar removal of DDj must be performed to obtain UTj. However, [PCIe-3.0] for 5.0 GT/s did specify Rj, so a distinct value for $T_{TX-UDJDD}$ can be obtained. Similarly, [PCIe-3.0] for 5.0 GT/s defined a minimum pulse width, assumed to be 100% Dj, from which $T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$ may be derived.

Table 8-6 Data Rate Dependent Transmitter Parameters

Symbol	Parameter description	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Notes
UI (Tx)	Unit Interval	(min) 399.88 (max) 400.12 (300 PPM)	(min) 199.94 (max) 200.06 (300 PPM)	(min) 124.9625 (max) 125.0375 (300 PPM)	(min) 62.48125 (max) 62.51875 (300 PPM)	(min) 31.246875 (max) 31.253125 (100 PPM)	ps	Does not include SSC variations
BW_{TX-PKG-PLL1}	Tx PLL bandwidth corresponding to $P_{PKG-TX-PLL1}$	(min) 1.5 (max) 22.0	(min) 8.0 (max) 16.0	(min) 0.5 (max) 4.0	(min) 0.5 (max) 4.0	(min) 0.5 (max) 1.8	MHz	Second order PLL jitter transfer bounding function. Notes 1, 2, 9.

Symbol	Parameter description	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Notes
$BW_{TX-PKG-PLL2}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL2}$	N/A	(min) 5.0 (max) 16.0	(min) 0.5 (max) 5.0	(min) 0.5 (max) 5.0	N/A	MHz	2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter. Notes 1, 2, 9.
$PKG_{TX-PLL1}$	Tx PLL peaking corresponding to $BW_{TX-PKG-PLL1}$	(max) 3.0	(max) 3.0	(max) 2.0	(max) 2.0	(max) 2.0	dB	Second order PLL jitter transfer bounding function. Notes 1, 2.
$PKG_{TX-PLL2}$	Tx PLL peaking corresponding to $BW_{TX-PKG-PLL2}$	N/A	1.0 (min)	(max) 1.0	(max) 1.0	N/A	dB	2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter. Notes 1, 2.
$V_{TX-DIFF-PP}$	Differential peak-peak Tx voltage swing for full swing operation	800 (max) 1200	800 (max) 1200	800 (max) 1300	800 (max) 1300	800 (max) 1300	mVPP	As measured with compliance test load. Defined as $2 \times V_{TXD+} - V_{TXD-} $. Note 3.
$V_{TX-DIFF-PP-LOW}$	Differential peak-peak Tx voltage swing for low swing operation	(min) 400 (max) 1200	400 1200	(min) 400 (max) 1300	(min) 400 (max) 1300	(min) 400 (max) 1300	mVPP	As measured with compliance test load. Defined as $2 \times V_{TXD+} - V_{TXD-} $. Note 3.
$V_{TX-EIEOS-FS}$	Minimum voltage swing during EIEOS for full swing signaling	N/A	N/A	250 (min)	250 (min)	250 (min)	mVPP	Note 4
$V_{TX-EIEOS-RS}$	Minimum voltage swing during EIEOS for reduced swing signaling	N/A	N/A	232 (min)	232 (min)	232 (min)	mVPP	Note 4
$ps21_{TX-ROOT-DEVICE}$	Pseudo package loss of a device containing root ports	N/A	N/A	(max) 3.0	(max) 5.0	(max) 8.5	dB	Note 5.
$ps21_{TX-NON-ROOT-DEVICE}$	Pseudo package loss for all devices not containing root ports	N/A	N/A	(max) 3.0	(max) 3.0	(max) 3.7	dB	Note 5.

Symbol	Parameter description	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Notes
$ILfit_{TX-ROOT-DEVICE}$	Fitted insertion loss at Nyquist	N/A	N/A	N/A	N/A	(max) 9.0	dB	Note 8
$ILfit_{TX-NON-ROOT-DEVICE}$	Fitted insertion loss at Nyquist	N/A	N/A	N/A	N/A	(max) 4.0	dB	Note 8
$V_{TX-BOOST-FS}$	Maximum nominal Tx boost ratio for full swing	N/A	N/A	8.0	8.0 (min)	8.0 (min)	dB	Nominal boost beyond 8.0 dB is limited to guarantee that $ps21_{TX}$ limits are satisfied.
$V_{TX-BOOST-RS}$	Maximum nominal Tx boost ratio for reduced swing	N/A	N/A	2.5	~2.5 (min)	~2.5 (min)	dB	Assumes ± 1.0 dB tolerance from diagonal elements in Figure 8-9.
$EQ_{TX-COEFF-RES}$	Tx coefficient resolution	N/A	N/A	1/(min) 63 1/(max) 24	1/(min) 63 1/(max) 24	1/(min) 63 1/(max) 24	N/A	
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis ratio for 2.5 and 5.0 GT/s	(min) 2.5 (max) 4.5	(min) 2.5 (max) 4.5	N/A	N/A	N/A	dB	
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis ratio for 5.0 GT/s	N/A	(min) 4.5 (max) 7.5	N/A	N/A	N/A	dB	
T_{TX-UTJ}	Tx uncorrelated total jitter	(max) 100	(max) 50	(max) 27.55	(max) 11.8	(max) 6.25	ps PP at 10^{-12}	See Section 8.3.5.8 for details. Note 9
$T_{TX-UTJ-SRIS}$	Tx uncorrelated total jitter when testing for the <u>IR</u> clock mode with SSC	(max) 100	(max) 66.51	(max) 33.83	(max) 15.85	(max) 7.15	ps PP at 10^{-12}	See Section 8.3.5.8 for details.
$T_{TX-UDJDD}$	Tx uncorrelated Dj for non-embedded Refclk	(max) 100	(max) 30	(max) 12	(max) 6.25	(max) 3.125	ps PP	See Section 8.3.5.8 for details.
$T_{TX-UPW-TJ}$	Total uncorrelated pulse width jitter	N/A	(max) 40	(max) 24	(max) 12.5	(max) 6.25	ps PP at 10^{-12}	See Section 8.3.5.10 for details
$T_{TX-UPW-DJDD}$	Deterministic DjDD	N/A	(max) 40	(max) 10	(max) 5	(max) 2.5	ps PP	See Section 8.3.5.10 for details

Symbol	Parameter description	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Notes
	uncorrelated pulse width jitter							
T_{TX-RJ}	Tx Random jitter	N/A	1.4 - 3.6	1.17 - 1.97	0.40 - 0.84	0.23 - 0.45	ps RMS	Informative parameter only. Range of R_j possible with zero to maximum allowed $T_{TX-UDJDD}$. Note 9
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	(max) 2.5	(max) 2.0	(max) 1.5	(max) 1.25	(max) 1.25	ns	Between any two Lanes within a single Transmitter.
$RL_{TX-DIFF}$	Tx package plus die differential return loss	See Figure 8-20					dB	Note 6
RL_{TX-CM}	Tx package plus die common mode return loss	See Figure 8-21					dB	Note 6

Notes:

1. A single combination of PLL BW and peaking is specified for 2.5 and 32.0 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a tradeoff between the two parameters.
2. The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.
3. See [Section 8.3.3.6](#) and [Section 8.3.3.7](#) for measurement details.
4. $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.
5. The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB. The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.
6. The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value.
7. The reference plane for all parameters at 2.5 and 5.0 GT/s is the package pins.
8. These are design parameter requirements - a specific test methodology for them is not defined.
9. For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8.0 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

8.3.7 Tx and Rx Return Loss

Return loss measurements for the Tx and Rx are essentially identical, so both are included in the Transmitter section. Return loss measurements are made at the end of the respective breakout channels and require that the breakout channel's contribution to RL be de-embedded, thereby associating the return loss with the Tx or Rx pin. Return loss measurements are made with a reference impedance of 50 ohms. Figure 8-20 defines the pass/fail mask for differential return loss. Both differential and common mode are defined over a frequency range of 50 MHz to 16.0 GHz.

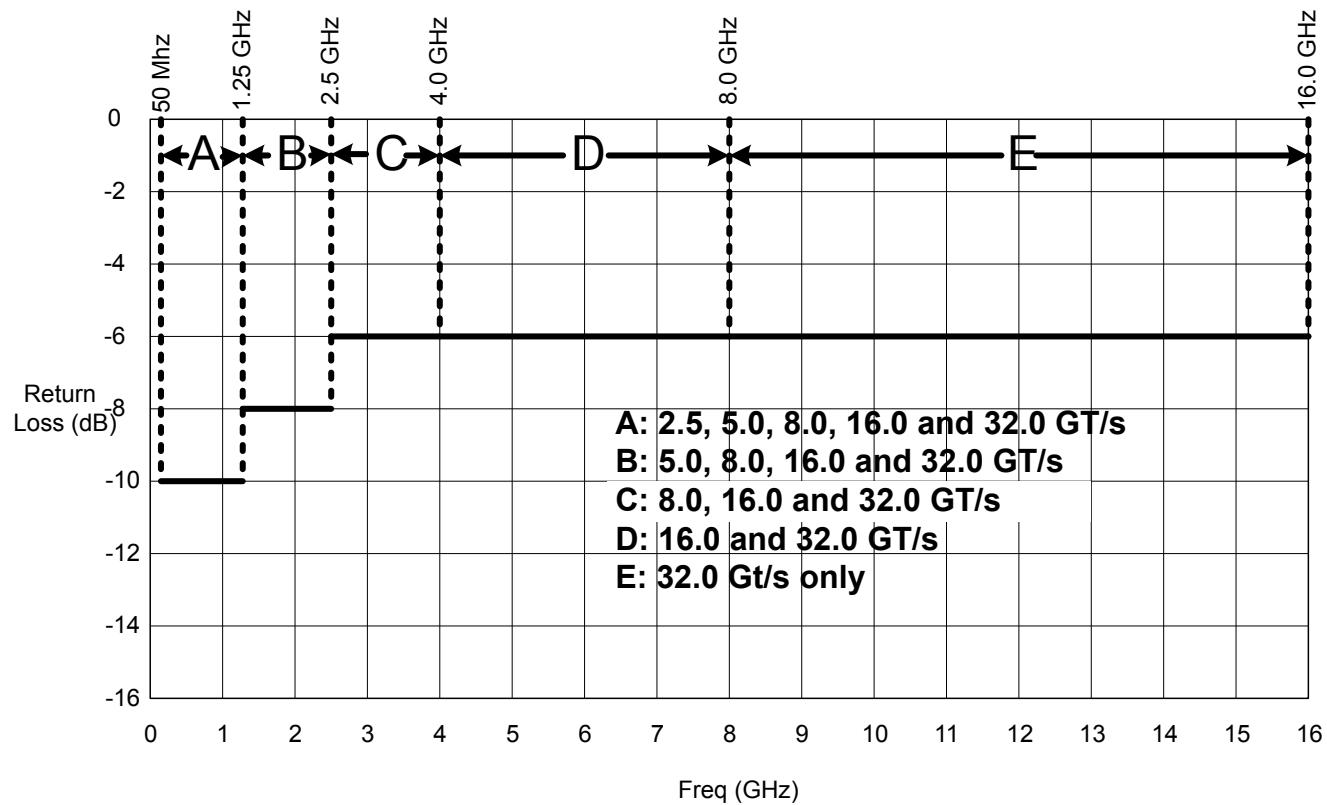


Figure 8-20 Tx, Rx Differential Return Loss Mask with 50 Ohm Reference

The pass/fail mask for common mode return loss is shown in Figure 8-21. Return loss measurements require that both the Tx and Rx are powered up and that their respective termination circuits are enabled.

Microprobing the package may be required to measure RL accurately.

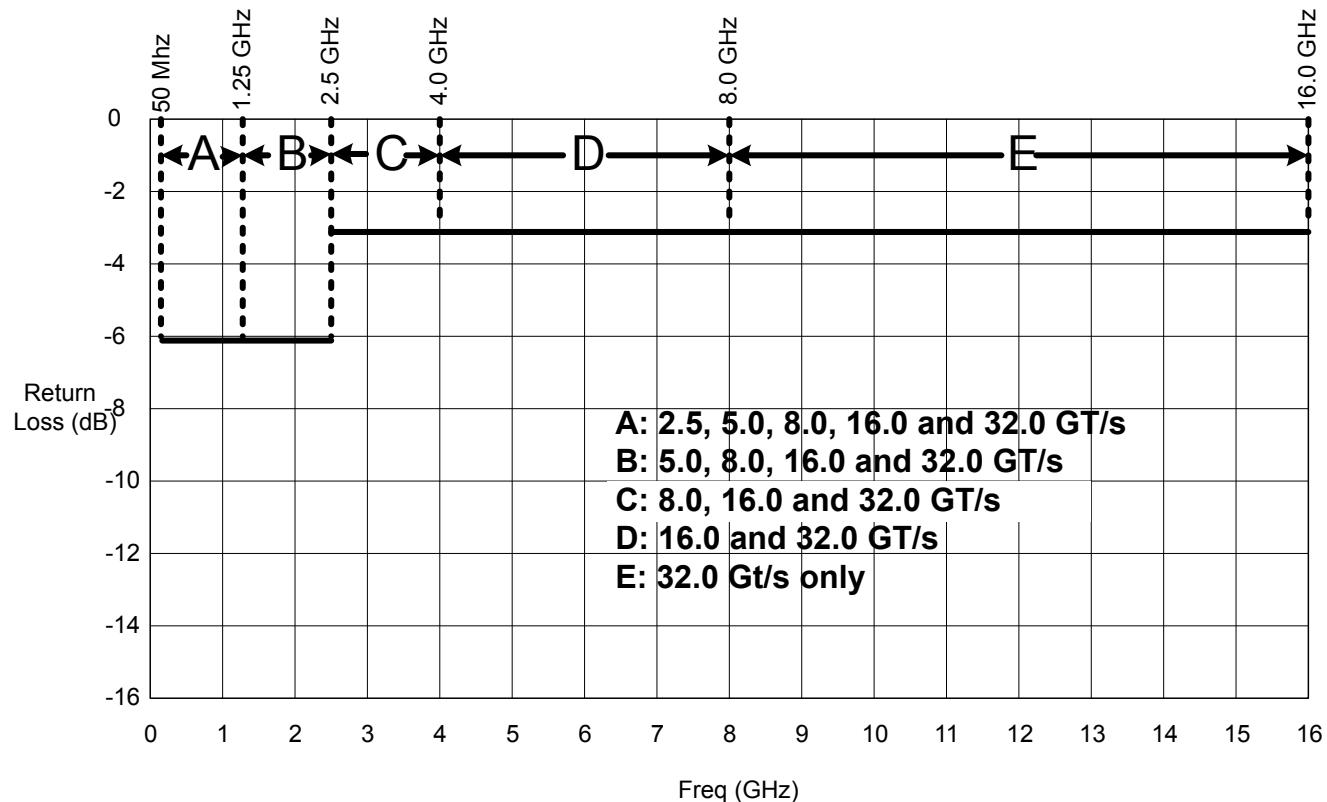


Figure 8-21 Tx, Rx Common Mode Return Loss Mask with 50 Ohm Reference

8.3.8 Transmitter PLL Bandwidth and Peaking

8.3.8.1 2.5 GT/s and 5.0 GT/s Tx PLL Bandwidth and Peaking

PLL bandwidth and peaking are defined for both the Transmitter and Receiver in order to place an upper limit on the amount of Refclk jitter that is propagated to the transmitted data and to the CDR. Defining PLL BW and peaking limits also guarantees a minimum degree of Tx/Rx jitter tracking in those systems utilizing a Common Refclk Rx architecture.

The 2.5 GT/s PLL characteristics have been moved from the 3.0 CEM spec to the Electrical Base Spec. A single PLL bandwidth range from 1.5 to 22 MHz is given, which is identical to that defined in the CEM spec. No range of peaking was given in the CEM spec for the 2.5 GT/s PLL. However, for the Electrical Base Spec a peaking range of 0.01 dB to 3 dB is now defined. It is necessary to place a non-zero lower limit on the peaking, both to define a corner case as well as to maintain a common mathematical expression for the PLL transfer function in terms of ω_n and ζ .

Two sets of bandwidth and peaking are defined for 5.0 GT/s: 8-16 MHz with 3 dB of peaking and 5.0-16.0 MHz with 1 dB of peaking. This gives the designer the option of trading off between a low peaking PLL design vs. a low bandwidth design. For 2.5 GT/s, a single PLL bandwidth and peaking range is specified at 1.5-22 MHz with 0.01 to 3.0 dB of peaking.

8.3.8.2 8.0 GT/s, 16.0 GT/s and 32.0 GT/s Tx PLL Bandwidth and Peaking

The Tx and Rx PLL bandwidth for 8.0 and 16.0 GT/s is 0.5-5 MHz with 1.0 dB of peaking or 0.5-4 MHz with 2.0 dB of peaking. The Tx and Rx PLL bandwidth for 32.0 GT/s is 0.5 to 1.8 MHz with 2.0 dB of peaking. The 8.0 GT/s PLL BW range is substantially lower than the PLL bandwidths specified for 5.0 GT/s or 2.5 GT/s to reduce the amount of Refclk jitter at the

sample latch of the Receiver. A non-zero value of 0.01 dB is given for the lower limit of the peaking to define all the peaking corners.

8.3.8.3 Series Capacitors

PCI Express requires series capacitors to provide a DC block between Tx and Rx. The min/max capacitance spread has been decreased from that of the 2.5 and 5.0 GT/s standards, while the maximum value has been slightly increased. This change is necessary to minimize DC wander effects due to data scrambling implemented at 8.0 GT/s, 16.0 GT/s and 32.0 GT/s. Note that 2.5 GT/s and 5.0 GT/s signaling must also propagate through these larger value capacitors, but the small increase in capacitor size has no adverse impact on either 2.5 GT/s or 5.0 GT/s signaling or low frequency in-band signaling such as Receiver detect.

8.3.9 Data Rate Independent Tx Parameters

Table 8-7 Data Rate Independent Tx Parameters

Symbol	Parameter Description	Value	Units	Notes
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	(max) 150	mVPP	Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50 mVPP at 8.0, 16.0, or 32.0 GT/s. Note 1.
$V_{TX-DC-CM}$	Tx DC peak-peak common mode voltage	(min) 0 (max) 3.6	V	Total single-ended voltage a Tx can supply under any conditions with respect to ground. See also the $I_{TX-SHORT}$. See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC Common Mode Voltage during L0 and Electrical Idle	(min) 0 (max) 100	mV	$ V_{TX-CM-DC} \text{ [during L0]} - V_{TX-CM-Idle-DC} \text{ [during Electrical Idle]} \leq 100 \text{ mV}$ $V_{TX-CM-DC} = \text{DC}_{\text{avg}} \text{ of } V_{TX-D+} + V_{TX-D-} / 2$ $V_{TX-CM-Idle-DC} = \text{DC}_{\text{avg}} \text{ of } V_{TX-D+} + V_{TX-D-} / 2 \text{ [Electrical Idle]}$
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	(min) 0 (max) 25	mV	$ V_{TX-CM-DC-D+} \text{ [during L0]} - V_{TX-CM-DC-D-} \text{ [during L0]} \leq 25 \text{ mV}$ $V_{TX-CM-DC-D+} = \text{DC}_{\text{avg}} \text{ of } V_{TX-D+} \text{ [during L0]} $ $V_{TX-CM-DC-D-} = \text{DC}_{\text{avg}} \text{ of } V_{TX-D-} \text{ [during L0]} $
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	(min) 0 (max) 20	mV	$V_{TX-IDLE-DIFF-AC-p} = V_{TX-Idle-D+} - V_{Tx-Idle-D-} \leq 20 \text{ mV}$. Voltage must be band pass filtered to remove any DC component and HF noise. The bandpass is constructed from two first-order filters, the high pass and low pass 3 dB bandwidths are 10 kHz and 1.25 GHz, respectively.
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	(min) 0 (max) 5	mV	$V_{TX-IDLE-DIFF-DC} = V_{TX-Idle-D+} - V_{Tx-Idle-D-} \leq 5 \text{ mV}$. Voltage must be low pass filtered to remove any AC component. The low pass filter is first-order with a 3 dB bandwidth of 10 kHz.
$V_{TX-RCV-DETECT}$	The amount of voltage change	(max) 600	mV	The total amount of voltage change in a positive direction that a Transmitter can apply to sense whether a low impedance

Symbol	Parameter Description	Value	Units	Notes
	allowed during Receiver detection			Receiver is present. Note: Receivers display substantially different impedance for $V_{IN} < 0$ vs $V_{IN} > 0$.
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	20 (min)	ns	The time a Tx must spend in Electrical Idle before transitioning to another state
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an EOS	(max) 8	ns	After sending the required number of EOSs, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EOS to the Transmitter in Electrical Idle.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving Electrical Idle	(max) 8	ns	Maximum time to transition to valid diff signaling after leaving Electrical Idle. This is considered a debounce time to the Tx.
$T_{CROSSLINK}$	Crosslink random timeout	(max) 1.0	ms	This random timeout helps resolve potential conflicts in the crosslink configuration.
C_{TX}	AC Coupling Capacitor	(min) 176 (max) 265	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$Z_{TX-DIFF-DC}$	DC differential Tx impedance	(max) 120	Ω	Low impedance defined during signaling. The minimum value is bounded by $R_{LTX-DIFF}$.
$I_{TX-SHORT}$	Tx short circuit current	(max) 90	ma	Tx short circuit current. Note 2

Notes:

- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.
- $I_{TX-SHORT}$ and $V_{TX-DC-CM}$ stipulate the maximum current/voltage levels that a Transmitter can generate and therefore define the worst case transients that a Receiver must tolerate.

8.4 Receiver Specifications

8.4.1 Receiver Stressed Eye Specification

All Receiver speeds are tested by means of a stressed eye applied over a calibration channel that approximates the near worst-case loss characteristics encountered in an actual channel. The recovered eye is defined at the input to the Receiver's latch. For 2.5 GT/s and 5.0 GT/s this point is equivalent to the Rx pins; for 8.0 GT/s, 16.0 GT/s and 32.0 GT/s it is equivalent to the signal at the Rx die pad after behavioral Rx equalization has been applied.

8.4.1.1 Breakout and Replica Channels

The closest practical measurement points to the Rx DUT are the coaxial connectors at the end of a breakout channel, while the Rx reference point of interest is the pin of the Rx. By constructing a replica channel that closely matches the electrical characteristics of the breakout channel it is possible to measure the signal as it would appear at the DUT's pin, if the DUT were an ideal termination. Impedance targets for the Rx breakout and replica channels are 85 Ω differential and 42.5 Ω single-ended, and the impedance tolerance should be maintained within ±5% or better. Note that the impedance target for the Tx test breakout and replica channels is still 100 Ω differential and 50 Ω single-ended.

In Figure 8-22 the stressed eye is observed at TP2 with the signal sources connected to the calibration channel. A calibration channel will be required for each data rate. Once the stressed eye has been calibrated, the signal source is applied to the DUT. Note that TP1-TP2 encompasses all the components between the signal source and the equivalent of the DUT pin, thereby capturing all non-ideal characteristics in the overall insertion loss due to cabling and replica/breakout channel, excluding Rx package. The AC and DC loss from generator to TP1 are assumed to be zero or must be otherwise de-embedded. The V_{RX-LAUNCH} (differential voltage swing) and Tx Equalization of the Signal Generator are calibrated at TP3 as shown in Figure 8-22. Some Signal Generators do factory calibration with a cable and trying to de-embed to TP1 for these calibrations can cause inaccuracies. Only the loss from TP3 onward is counted in overall calibration channel loss.

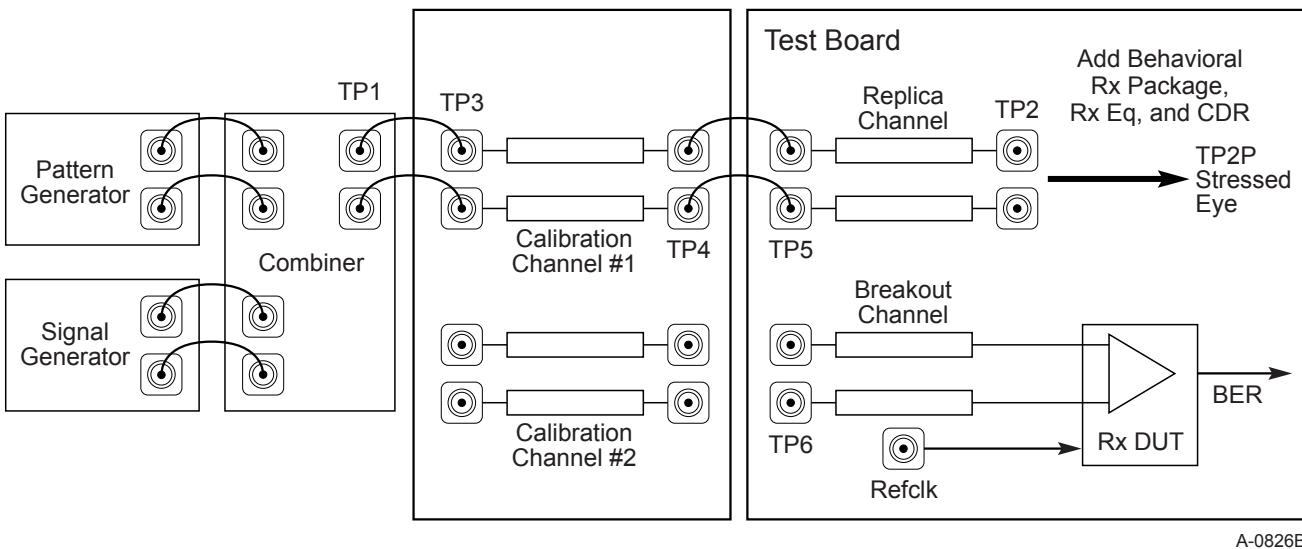


Figure 8-22 Rx Testboard Topology for 16.0 and 32.0 GT/s

8.4.1.2 Calibration Channel Insertion Loss Characteristics

Calibration channels, each with a specified differential insertion loss at one of the PCIe data rates, provide the means of generating prescribed amounts of ISI that approximates a worst case channel. For each data rate a single calibration channel loss mask is defined by means of two pairs of IL limits at a high and a low frequency. It is not acceptable to generate IL by means other than physical channel (PCB traces, cables, switches, small compensation delays, etc. are acceptable), such as specialized filters. The Calibration Channel needs to include all physical loss after TP3 as shown in Figure 8-22 within the IL mask.

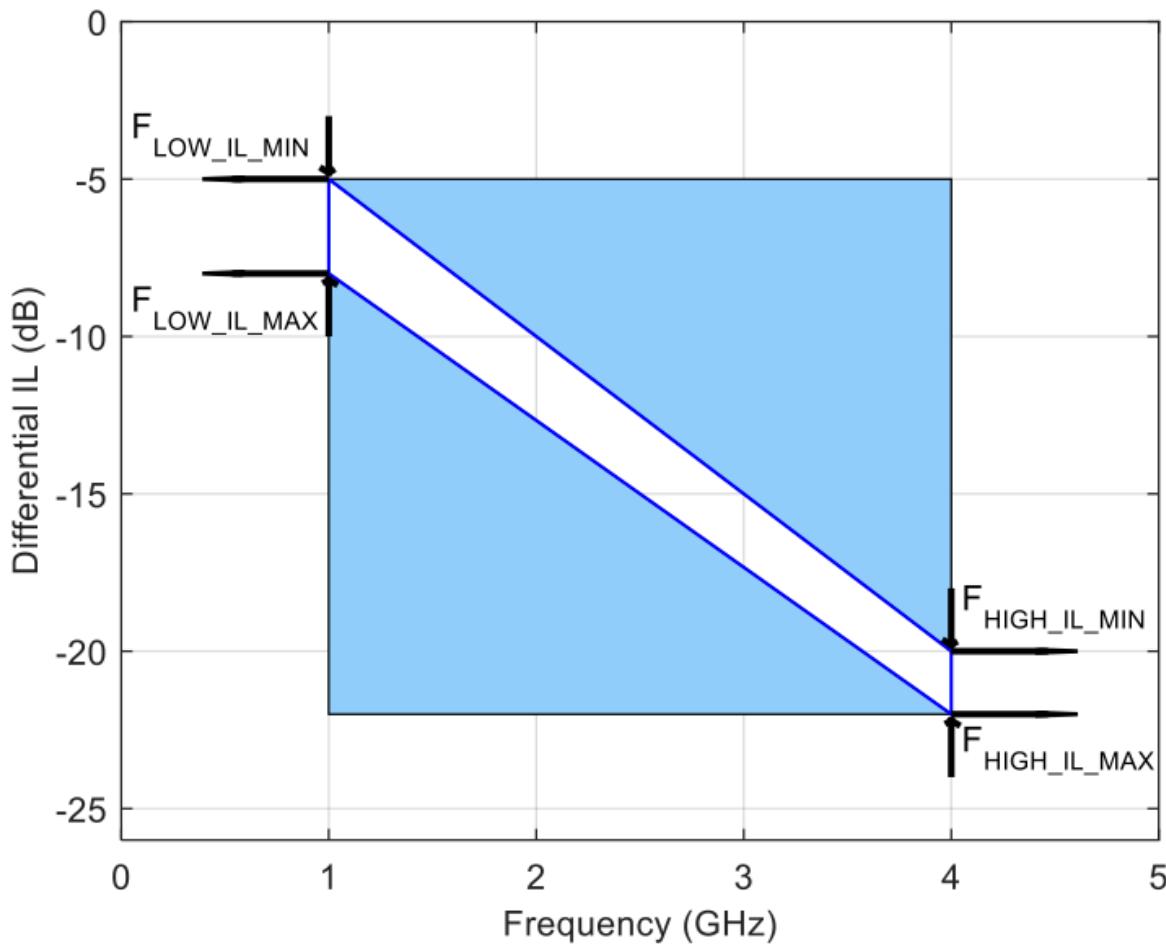


Figure 8-23 Example Calibration Channel IL Mask Excluding Rx Package for 8.0 GT/s

The following table defines the calibration channel IL masks by means of four loss points at two frequency limits, thereby creating a quadrilateral shaped solution area. The calibration channel IL mask is provided as a guideline to minimize reflection so that the channel represents mostly ISI stress for the receiver test.

Table 8-8 Calibration Channel IL Limits

Data Rate	$F_{LOW-IL-MIN}$	$F_{LOW-IL-MAX}$	$F_{HIGH-IL-MIN}$	$F_{HIGH-IL-MAX}$
2.5 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	4.7 dB @ 1.25 GHz	5.2 dB @ 1.25 GHz
5.0 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	10.0 dB @ 2.5 GHz	11.0 dB @ 2.5 GHz
8.0 GT/s	5 dB @ 1 GHz	8 dB @ 1 GHz	20 dB @ 4 GHz	22 dB @ 4 GHz
16.0 GT/s Root Port	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	22.5 dB @ 8 GHz	23.5 dB @ 8 GHz
16.0 GT/s Non-Root Port	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	24.5 dB @ 8 GHz	25.5 dB @ 8 GHz
32.0 GT/s Root Port	3.2 dB @ 1 GHz	4.2 dB @ 1 GHz	26.5 dB @ 16 GHz	27.5 dB @ 16 GHz

Data Rate	$F_{LOW-IL-MIN}$	$F_{LOW-IL-MAX}$	$F_{HIGH-IL-MIN}$	$F_{HIGH-IL-MAX}$
32.0 GT/s Non-Root Port	3.9 dB @ 1 GHz	4.9 dB @ 1 GHz	31.5 dB @ 16 GHz	32.5 dB @ 16 GHz

Notes:

- Calibration channel plus Rx package is 28 dB nominally (informative) for 16.0 GT/s.
- Calibration channel plus Rx package is 36 dB nominally (informative) for 32.0 GT/s.
- Different reference packages are defined for devices containing Root Ports and all other device types at 16.0 GT/s and 32.0 GT/s.
- It is recommended that some validation be done with shorter channels at 16.0 GT/s and 32.0 GT/s.
- For 32.0 GT/s a material at least as good as a Megtron-6 class material with loss of approximately 1.0 dB/inch at 16 GHz at typical room conditions must be used.

The impedance targets for the Rx tolerancing interconnect environment are 100 Ω differential and 50 Ω single-ended for the 2.5, 5.0, and 8.0 GT/s channels and 85 Ω differential and 42.5 Ω single-ended for the 16.0 GT/s and 32.0 GT/s channels; the impedance tolerance should be maintained within $\pm 5\%$ or better.

The calibration channel for 16.0 GT/s must meet the following return loss mask when measured from either end of the calibration channel:

- ≤ -12 dB for < 4 GHz
- ≤ -8 dB for ≥ 4 GHz and < 12 GHz
- ≤ -6 dB for ≥ 12 GHz and ≤ 16 GHz

The calibration channel for 32.0 GT/s must meet the following return loss mask when measured from either end of the calibration channel:

- ≤ -12 dB for < 4 GHz
- ≤ -10 dB for ≥ 4 GHz and < 16 GHz
- ≤ -6 dB for ≥ 16 GHz and ≤ 32 GHz

A calibration channel consists of a differential pair of PCB traces terminated at both ends by coaxial connectors. For 16.0 GT/s and 32.0 GT/s the calibration channel includes a 4.0 (16.0 GT/s) or 5.0 (32.0 GT/s) Card Electromechanical Specification compliant connector and edge finger placed at least 4 dB at nyquist away from the coaxial connectors where the signal generator is connected. The calibration channel's electrical characteristics are defined in terms of differential insertion loss masks as shown in [Figure 8-23](#), where S_{DD21} is measured between TP3 (See [Figure 8-22](#)) and TP2. Connections between TP4-TP5 represent cabling and are included in the S_{DD21} measurement. Loss before TP3 is effectively calibrated out by calibrating differential voltage swing and TX EQ at TP3 and is not included in the S_{DD21} measurement.

While the 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s-parameter masks do not extend below 1.0 GHz, all calibration channels must be well behaved below 1.0 GHz and must not have a DC resistance in excess of 7.5 ohms, as measured by the sum of the resistances of the D+ and D- traces. This limitation on DC resistance guarantees that the calibration channel low frequency characteristic is consistent with the extrapolations of the S_{DD21} masks to DC. The calibration loss targets for devices containing Root Ports and other devices are different because the reference package models have different losses.

For 16.0 GT/s and 32.0 GT/s the insertion loss range $F_{HIGH-IL-MIN}$ to $F_{HIGH-IL-MAX}$ is the nominal loss. The calibration channel must have a series of loss options covering a range from at least 2 dB below $F_{HIGH-IL-MIN}$ to 3 dB above $F_{HIGH-IL-MAX}$ (for example for the non-root case this means a loss range from -22.5 to -28.5 dB) with loss delta between consecutive options of 0.5 dB or less.

IMPLEMENTATION NOTE

16.0 GT/s Calibration Channel Reference Design

This section gives an example of a 16.0 GT/s calibration channel that was built and tested to meet the requirements in this specification. A high level block diagram of the calibration channel is shown in [Figure 8-24](#). Note that this example fixture covers a wider loss range than required by the specification and can cover both root and non-root cases. The test fixture includes four PCBs:

16.0 GT/s Rx Calibration Base Boards

Sixteen differential pairs (85 Ohm Nominal Impedance) routed from SMA connectors to a CEM through-hole connector. There are three different base boards to achieve the following insertion loss ranges - The insertion loss of the differential pairs for the base board is varied as follows @ 8.0 GHz in 0.5 dB steps.

Low-Loss Base Board: 4-11.5 dB

Mid-Loss Base Board: 12-19.5 dB

High-Loss Base Board: 20-27.5 dB

All traces are routed as microstrip on the bottom layer. The SMA connectors and CEM connectors are optimized with layout techniques at 8.0 GHz.

16.0 GT/s Rx Calibration Riser Board

Sixteen differential pairs (85 Ohm Nominal Impedance) routed from SMA connectors to Gold Edge Fingers. The insertion loss of the differential pairs is fixed at 4 dB nominal @ 8.0 GHz for all sixteen pairs. All traces are routed as microstrip on the bottom layer. The SMA connectors and CEM connectors are optimized with layout techniques at 8.0 GHz.

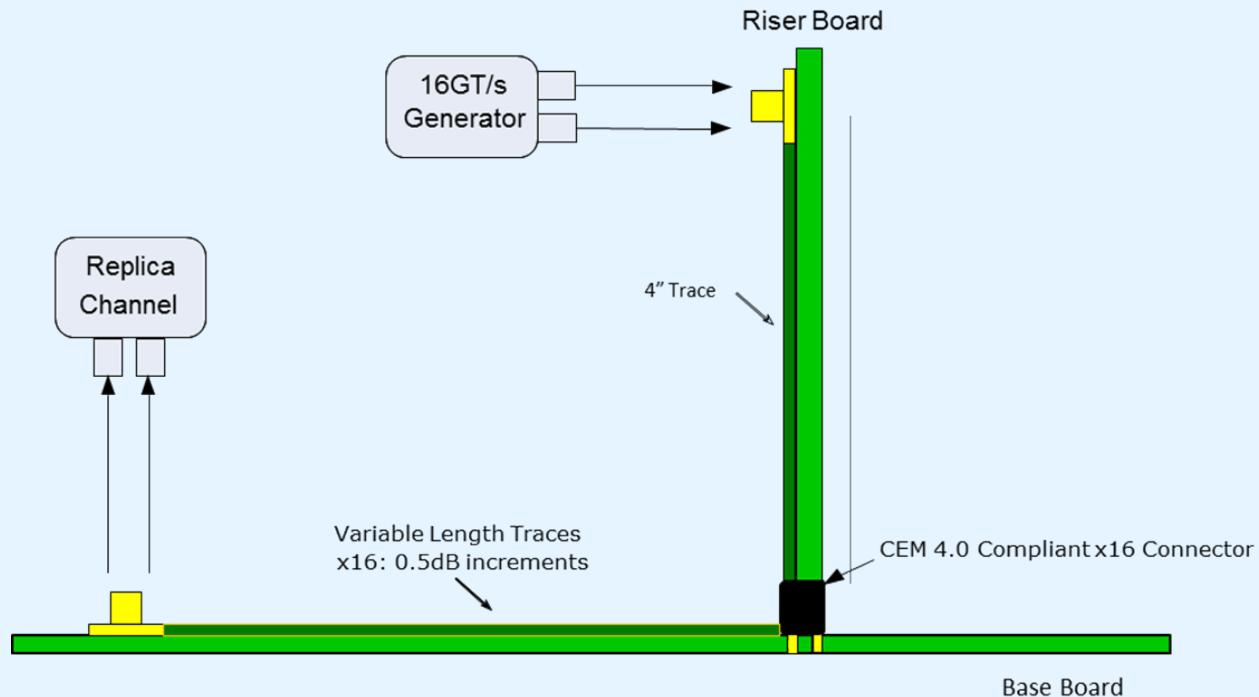


Figure 8-24 Example 16.0 GT/s Calibration Channel

The stackup for both boards is shown in Figure 8-25 where 65% is the estimated copper fill percentage. Figure 8-25 includes stackups for both nominal 85 Ω and 100 Ω stackups - the 85 Ω stackup is used for the calibration channel example.

Material	Layer	Dielectric	Copper Fill / DK	Starting Copper oz	Finished Copper oz	Copper Thickness	Single Ended Impedance	Finished Trace Single Ended	Calculated Impedance	SE Ref Layers	Differential Impedance	Finished Trace/Gap Differential	Calculated Impedance	Diff Ref Layers
1-1080,1-2113	1	.0062		.5	1.5	0.00210	42.5 Ω +/-5%	.0135	42.77	2	85 Ω +/-5%	.0075 / .005	84.95	2
	2		DK=4.0	65%	1	1	50 Ω +/-5%	.010	50.11	2	100 Ω +/-5%	.0052 / .006	100.38	
FILLER		.043												
1-1080,1-2113	3		DK=4.0	65%	1	1	0.00130							
	4	.0062	DK=4.0	.5	1.5	0.00210	42.5 Ω +/-5%	.0135	42.77	3	85 Ω +/-5%	.0075 / .005	84.95	3
		.0622					50 Ω +/-5%	.010	50.11	3	100 Ω +/-5%	.0052 / .006	100.38	3

Figure 8-25 Stackup for Example 16.0 GT/s Calibration Channel

The pad stack for the CEM connector drill holes is shown in Figure 8-26 and the pad stack for the SMA drill holes is shown in Figure 8-27.

Padstack: C40P28P3M3-A59 Type: through Inner pads: Optional								
Layer	Pad Type	Geometry	Width	Height	Offset X	Offset Y	Flash Name	Shape Name
TOP	ANTI	CIRCLE	59.00	59.00	0.00	0.00		
TOP	THERMAL	RECTANGLE	80.00	80.00	0.00	0.00	TH80X60X15_4X45	
TOP	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
GND-2	ANTI	CIRCLE	59.00	59.00	0.00	0.00		
GND-2	THERMAL	RECTANGLE	80.00	80.00	0.00	0.00	TH80X60X15_4X45	
GND-2	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
GND-3	ANTI	CIRCLE	59.00	59.00	0.00	0.00		
GND-3	THERMAL	RECTANGLE	80.00	80.00	0.00	0.00	TH80X60X15_4X45	
GND-3	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
BOTTOM	ANTI	CIRCLE	59.00	59.00	0.00	0.00		
BOTTOM	THERMAL	RECTANGLE	80.00	80.00	0.00	0.00	TH80X60X15_4X45	
BOTTOM	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
internal_pad_def	ANTI	CIRCLE	59.00	59.00	0.00	0.00		
internal_pad_def	THERMAL	RECTANGLE	80.00	80.00	0.00	0.00	TH80X60X15_4X45	
internal_pad_def	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
SOLDERMASK_TOP	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
SOLDERMASK_BOTTOM	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
PASTEMASK_TOP	REGULAR	NULL	0.00	0.00	0.00	0.00		
PASTEMASK_BOTTOM	REGULAR	NULL	0.00	0.00	0.00	0.00		
FILMMASKTOP	REGULAR	NULL	0.00	0.00	0.00	0.00		
FILMMASKBOTTOM	REGULAR	NULL	0.00	0.00	0.00	0.00		

Drill Data for C40P28P3M3-A59

Hole Type	Drill Dia	Plating	Figure	Characters	Width	Height	Offset X	Offset Y	Pos Tolerance	Neg Tolerance	Non-Standard
CIRCLE DRILL	28.00	PLATED	DIAMOND		50.00	50.00	0.00	0.00	3.00	3.00	

Figure 8-26 CEM Connector Drill Hole Pad Stack

Padstack: C60_BOT75P20_SSM40P3M3 Type: through Inner pads: Optional

Layer	Pad Type	Geometry	Width	Height	Offset X	Offset Y	Flash Name	Shape Name
TOP	ANTI	CIRCLE	45.00	45.00	0.00	0.00		
TOP	THERMAL	RECTANGLE	5.00	5.00	0.00	0.00	\$MIL_PAD	
TOP	REGULAR	CIRCLE	60.00	60.00	0.00	0.00		
GND-2	ANTI	CIRCLE	45.00	45.00	0.00	0.00		
GND-2	THERMAL	RECTANGLE	5.00	5.00	0.00	0.00	\$MIL_PAD	
GND-2	REGULAR	CIRCLE	60.00	60.00	0.00	0.00		
GND-3	ANTI	CIRCLE	45.00	45.00	0.00	0.00		
GND-3	THERMAL	RECTANGLE	5.00	5.00	0.00	0.00	\$MIL_PAD	
GND-3	REGULAR	CIRCLE	60.00	60.00	0.00	0.00		
BOTTOM	ANTI	CIRCLE	45.00	45.00	0.00	0.00		
BOTTOM	THERMAL	RECTANGLE	5.00	5.00	0.00	0.00	\$MIL_PAD	
BOTTOM	REGULAR	CIRCLE	75.00	75.00	0.00	0.00		
internal_pad_def	ANTI	CIRCLE	45.00	45.00	0.00	0.00		
internal_pad_def	THERMAL	RECTANGLE	5.00	5.00	0.00	0.00	\$MIL_PAD	
internal_pad_def	REGULAR	CIRCLE	60.00	60.00	0.00	0.00		
SOLDERMASK_TOP	REGULAR	CIRCLE	60.00	60.00	0.00	0.00		
SOLDERMASK_BOTTOM	REGULAR	CIRCLE	40.00	40.00	0.00	0.00		
PASTEMASK_TOP	REGULAR	NULL	0.00	0.00	0.00	0.00		
PASTEMASK_BOTTOM	REGULAR	NULL	0.00	0.00	0.00	0.00		
FILMMASKTOP	REGULAR	NULL	0.00	0.00	0.00	0.00		
FILMMASKBOTTOM	REGULAR	NULL	0.00	0.00	0.00	0.00		

Drill Data for C60_BOT75P20_SSM40P3M3

Hole Type	Drill Dia	Plating	Figure	Characters	Width	Height	Offset X	Offset Y	Pos Tolerance	Neg Tolerance	Non-Standard
CIRCLE DRILL	20.00	PLATED	CIRCLE	E	60.00	60.00	0.00	0.00	3.00	3.00	

Figure 8-27 Pad Stack for SMA Drill Holes

IMPLEMENTATION NOTE

32.0 GT/s Calibration Channel Reference Design

This section gives an example of a 32.0 GT/s calibration channel that was built and tested to meet the requirements in this specification. A high level block diagram of the calibration channel is shown in [Figure 8-28](#). Note this example fixture covers a wider loss range than required by the specification and can cover both root and non-root cases. The test fixture includes two PCBs:

32.0 GT/s Rx Calibration Base Boards

Sixteen differential pairs (85 Ohm Nominal Impedance) routed on a Megtron-6 PCB from MMPX connectors to a CEM surface mount connector. There are three different base boards to achieve the following insertion loss ranges - The insertion loss of the differential pairs for the base board is varied as follows @ 16.0 GHz in 0.5 dB steps.

Low-Loss Base Board:

4.0 - 11.5 dB

Mid-Loss Base Board:

12.0 - 19.5 dB

High-Loss Base Board:

20.0 - 27.5 dB

All traces are routed as microstrip on the top layer. The MMPX connectors and CEM connectors are optimized with layout techniques at 16.0 GHz

For information on MMPX connectors refer to Huber+Suhner microminiature connectors.

32.0 GT/s Rx Calibration Riser Board

Sixteen differential pairs (85 Ohm Nominal Impedance) routed on a Megtron-6 PCB from MMPX connectors to Gold Edge Fingers. The insertion loss of the differential pairs is fixed at 8 dB nominal @ 16.0 GHz for all sixteen pairs. All traces are routed as microstrip on the top layer. The MMPX connectors and CEM connectors are optimized with layout techniques at 16.0 GHz.

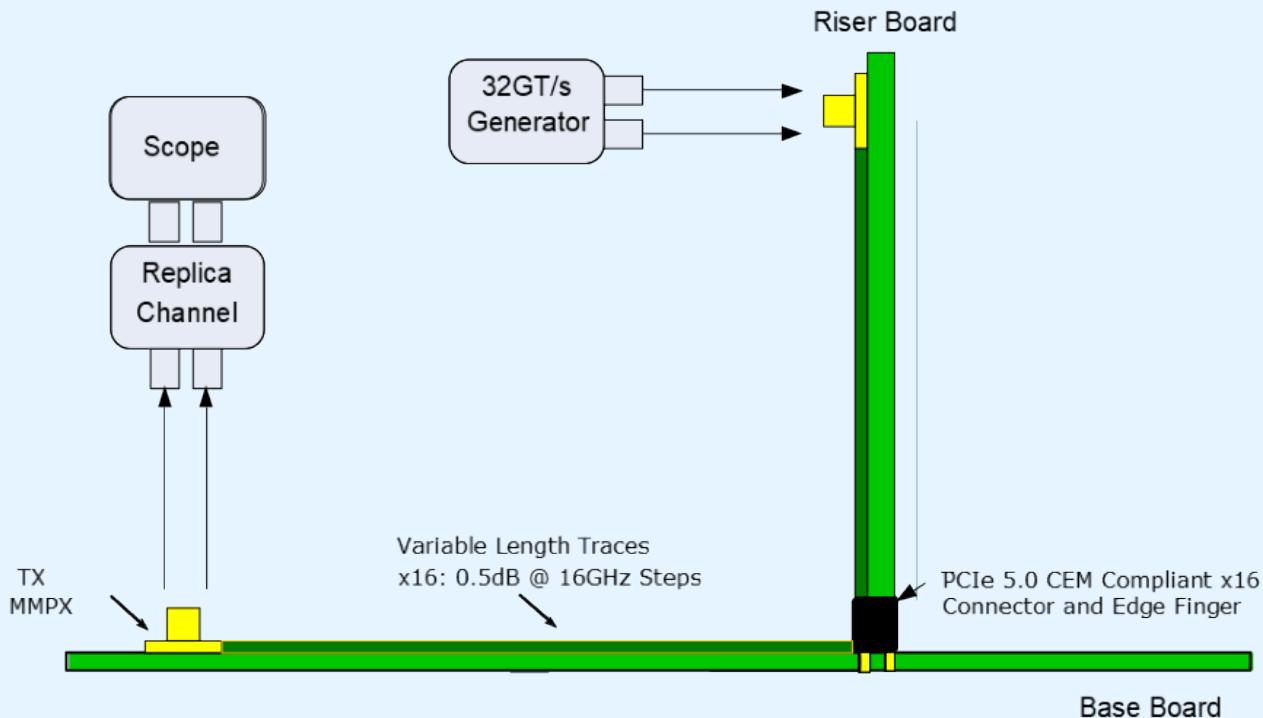


Figure 8-28 Example 32.0 GT/s Calibration Channel

The stack-up for both 85 Ohm boards is shown in Figure 8-29 where 65% is the estimated copper fill percentage.

Material	Layer	Starting Cu oz	Finished Cu oz	Dielectric	Lyr	Single Ended Impedance	Designed Trace Width	Finished Trace Width	Calculated Impedance	Ref Lyr A	Ref Lyr B	Differential Impedance	Designed Trace/Space	Finished Trace/Space	Calculated Impedance	Ref Lyr A	Ref Lyr B
1-3313(54%), 1-1078(75%)	1	Signal .5	1.5	.0065	+/- 0.001	42.5 Ω 50 Ω	.00945 .008	.0155 .0115	42.18 Ω 49.7 Ω	85 Ω 100 Ω	.00675/.00525 .005/.007	.0115/.0095 .006/.006	85.94 Ω 100.45 Ω	2	2		
Filler Material	2	Plane 1	1	.042	+/- 0.003												
1-3313(54%), 1-1078(75%)	3	Plane 1	1	.0065	+/- 0.001	50 Ω 42.5 Ω	.008 .00945	.0115 .0155	49.7 Ω 42.18 Ω	100 Ω 85 Ω	.005/.007 .00675/.00525	.006/.006 .0115/.0095	100.45 Ω 85.94 Ω	2	2		
	4	Signal .5	1.5	.0065	+/- 0.001												
				Final Thickness (After Plating): 0.062													

Figure 8-29 Stack-up for Example 32.0 GT/s Calibration Channel

8.4.1.3 Post Processing Procedures

The Receiver test requires that the stressed eye characteristics be measured at TP2 (which is accessible) and then post-processed to yield a signal as it would appear at test point two post-processed (TP2P) (which is not accessible) for 8.0, 16.0, and 32.0 GT/s. TP2P defines a reference point that comprehends the effects of the behavioral Rx package plus Rx equalization and represents the only location where a meaningful EH and EW limits can be defined.

8.4.1.4 Behavioral Rx Package Models

Behavioral Rx package models are included as part of the post processing to allow the calibrated eye to comprehend package insertion loss. A separate pair of package models is defined for 8.0, 16.0 GT/s and 32.0 GT/s eye calibration. At 8.0 GT/s, separate package models are defined for TX and RX ports to reflect the smaller CPAD capacitance typical in most receiver implementations. At 16.0 and 32.0 GT/s, separate package models are defined for devices containing Root Ports and all other devices. This is necessary to allow a reasonable channel solution space and is based on the assumption that devices containing Root Complexes are usually large and socketed, while all other devices tend to be unsocketed and smaller. The 16.0 GT/s Root and Non-Root behavioral Rx package models have been constructed to represent respective package loss characteristics for high loss, but not worst case loss, packages. The 32.0 GT/s Root and Non-Root behavioral Rx package models have been constructed to represent package loss characteristics for worst case packages.

The 8.0 GT/s and 32.0 GT/s stressed eye test for all devices and the 16.0 GT/s stressed eye test for Non-Root Package devices that support captive channels are required to use the appropriate behavioral package (see [Section 8.3.3.11](#)). For all other device types, if the actual Rx package performance is worse than that of the behavioral package, then the actual package models are permitted to be used. If the actual package models are used, the calibration channel must be adjusted such that the total channel loss including the embedded actual package remains at 28 dB nominal. Note that form factor overall requirements still need to be met. The Rx package performance is assessed using the methodology defined in [Section 8.5.1.2](#).

Details of the behavioral Rx packages are provided in [Section 8.5.1.1](#) of the Channel Tolerancing section. S-parameter models for the behavioral Rx package models are available as design collateral. The reference impedance at the pad side of the packages model is assumed to be $2 \times 50 \Omega$.

8.4.1.5 Behavioral CDR Model

Post processing shall include a behavioral CDR model with a data rate dependent transfer function. A first order CDR transfer function is utilized for Receivers operating with a CC Refclk architecture except for 32.0 GT/s and, optionally, at 16.0 GT/s when 32.0 GT/s is not supported. For Receivers operating in IR Refclk mode an alternate CDR transfer function is required. For a given data rate the behavioral CDR used for Rx testing is the same as the corresponding CDR used for Tx testing. For details on behavioral CDR functions refer to [Section 8.3.5.5](#).

8.4.1.6 No Behavioral Rx Equalization for 2.5 and 5.0 GT/s

The combination of worst case channel, behavioral Rx package, and Tx jitter at 2.5 and 5.0 GT/s will yield open eyes, when the appropriate Tx presets are set. Therefore there is no need to define a behavioral Rx equalization or to adjust the Tx equalization setting. Actual implementations of 2.5 and 5.0 GT/s receivers may, of course, include equalization.

8.4.1.7 Behavioral Rx Equalization for 8.0, 16.0, and 32.0 GT/s

As measured at TP2, stressed eyes at 8.0 GT/s, 16.0 GT/s and 32.0 GT/s will usually be closed, making direct measurement of the stressed eye jitter parameters unfeasible. This problem is overcome by employing a behavioral Receiver equalizer that implements both CTLE and a 1-tap (8.0 GT/s) or 2-tap DFE (16.0 GT/s) or 3-tap DFE (32.0 GT/s).

Rx equalization algorithms of CTLE and DFE are only intended to be a means for obtaining an open eye in the presence of calibration channel ISI plus the other signal impairment terms and for channel compliance. The behavioral Rx equalization algorithms are not intended to serve as a guideline for implementing actual Receiver equalization. For example, additional DFE taps can have significant benefit in actual implementations where the CTLE may differ from the

behavioral equalizer and/or CTLE selection may not always be optimal. Channel loss characteristics can vary significantly with temperature and humidity and a real Receiver must be able to continue to function at the target BER through such variations.

8.4.1.8 Behavioral CTLE (8.0 and 16.0 GT/s)

8.0 and 16.0 GT/s behavioral Rx equalization defines a 1st order CTLE with fixed LF and HF poles, and an adjustable DC gain (A_{DC}) specified according to the family of curves shown in [Figure 8-31](#). For the 8.0 GT/s rates A_{DC} is adjustable over a minimum range of -6 to -12 dB in steps of 1.0 dB.

$$H(s) = \omega_{P2} \times \frac{s + \omega_{P1} \times A_{DC}}{(s + \omega_{P1}) \times (s + \omega_{P2})}$$

$$\omega_{P1} = \text{pole 1} = 2\pi \times 2 \text{ GHz}$$

$$\omega_{P2} = \text{pole 2} = 2\pi \times 8 \text{ GHz}$$

$$A_{DC} = \text{dc gain}$$

Figure 8-30 Transfer Function for 8.0 GT/s Behavioral CTLE

The following diagram illustrates the gain vs. frequency behavior of the CTLE as A_{DC} is varied over its minimum to maximum range in 1.0 dB steps.

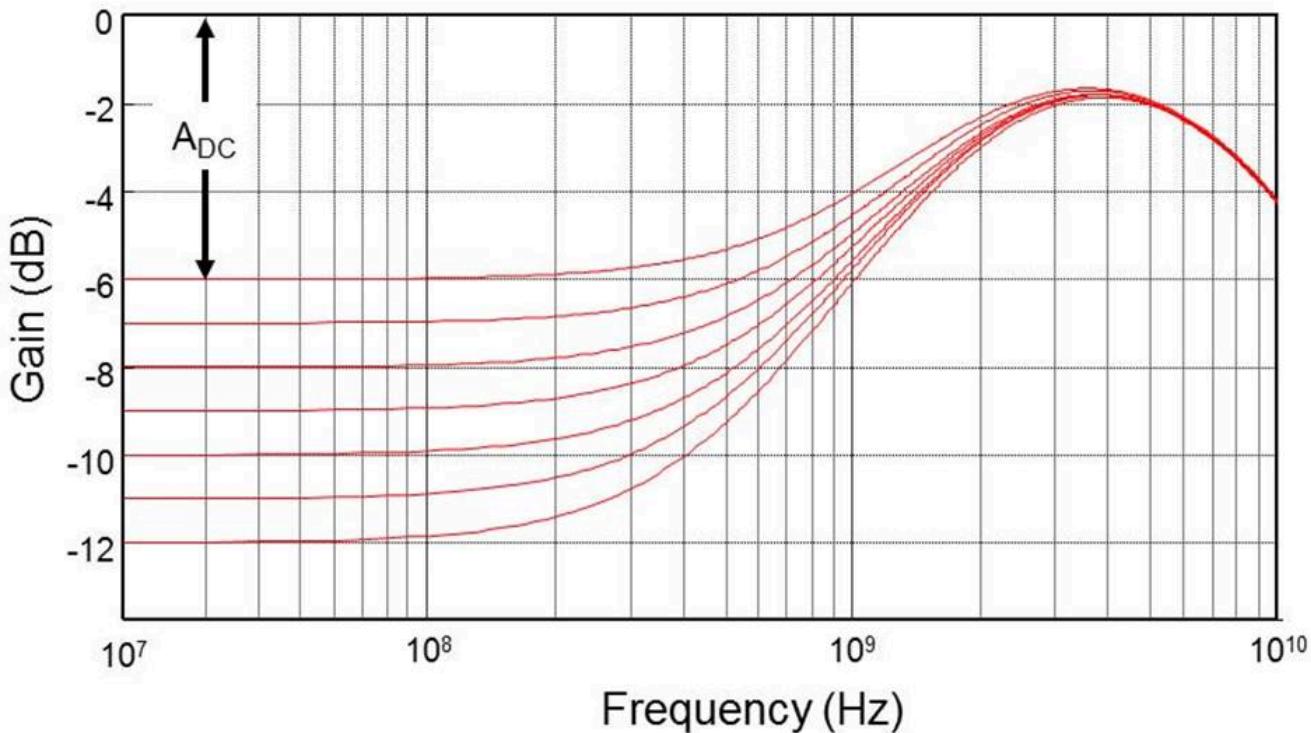


Figure 8-31 Loss Curves for 8.0 GT/s Behavioral CTLE

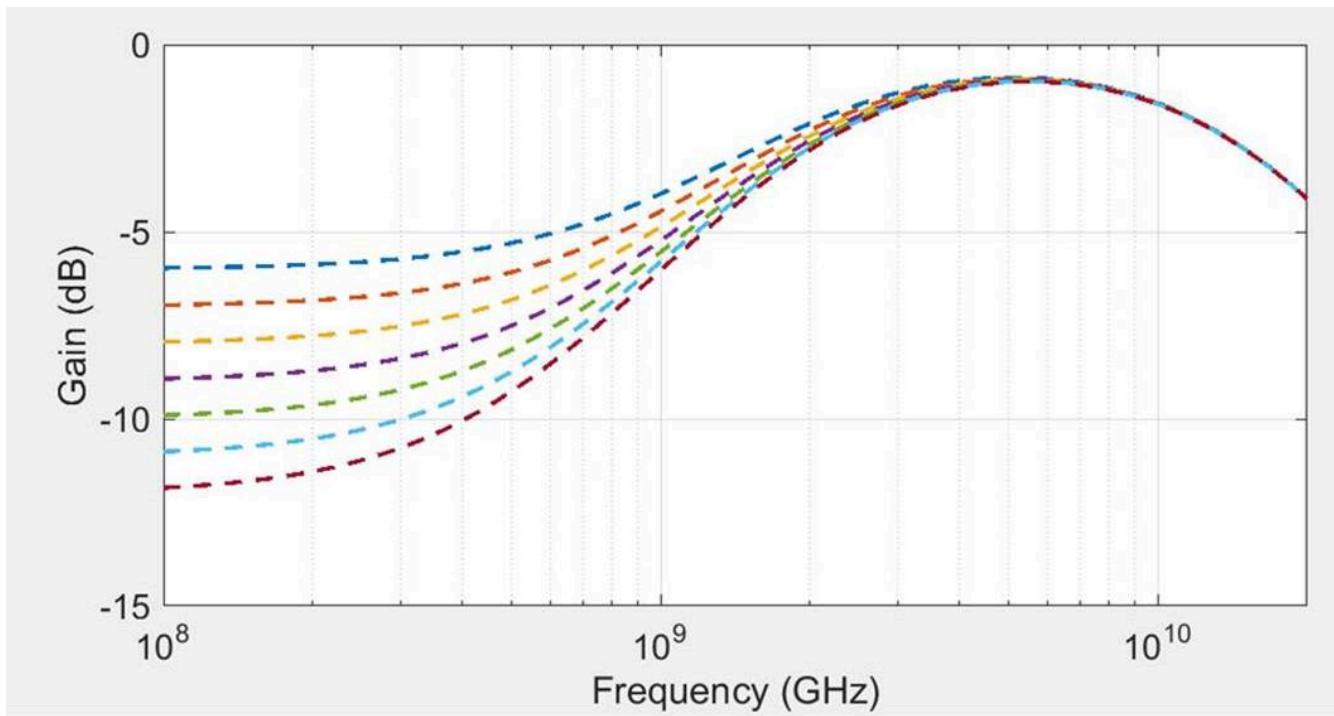


Figure 8-32 Loss Curves for 16.0 GT/s Behavioral CTLE

A Receiver operating at 16.0 GT/s utilizes a similar set of CTLE curves with different pole locations. The difference is that $\omega_{p1} = \text{pole 1} = 2\pi * 2 \text{ GHz}$ and $\omega_{p2} = \text{pole2} = 2\pi * 16.0 \text{ GHz}$. The range for A_{DC} remains the same as that for 8.0 GT/s.

8.4.1.9 Behavioral CTLE (32.0 GT/s)

32.0 GT/s behavioral Rx equalization defines a 2nd order CTLE with fixed poles, and an adjustable DC gain (A_{DC}) specified according to the family of curves shown in Figure 8-33. The A_{DC} is adjustable over a range of -5 to -15 dB in steps of 1.0 dB.

$$H(s) = \frac{\omega_{P1} \times \omega_{P3} \times \omega_{P4}}{\omega_{Z1}} \times \frac{(s + \omega_{Z1})(s + \omega_{P2} \times A_{DC})}{(s + \omega_{P1})(s + \omega_{P2})(s + \omega_{P3})(s + \omega_{P4})}$$

$$\omega_x = 2\pi \times F_x$$

$$F_{P1} = 1.65 \times F_{Z1}$$

$$F_{P2} = 9.5 \text{ GHz}$$

$$F_{P3} = 28 \text{ GHz}$$

$$F_{P4} = 28 \text{ GHz}$$

$$F_{Z1} = 450 \text{ MHz}$$

$$F_{Z2} = \text{mag(DC gain)} \times F_{P2}$$

Equation 8-7 Behavioral CTLE at 32.0 GT/s

Figure 8-33 illustrates the gain vs. frequency behavior of the CTLE as A_{DC} is varied over its minimum to maximum range in 1.0 dB steps. Note that the CTLE curves must be extended to high enough frequency in post-processing tools that the CTLE curves do not significantly limit the simulation performance due to maximum frequency.

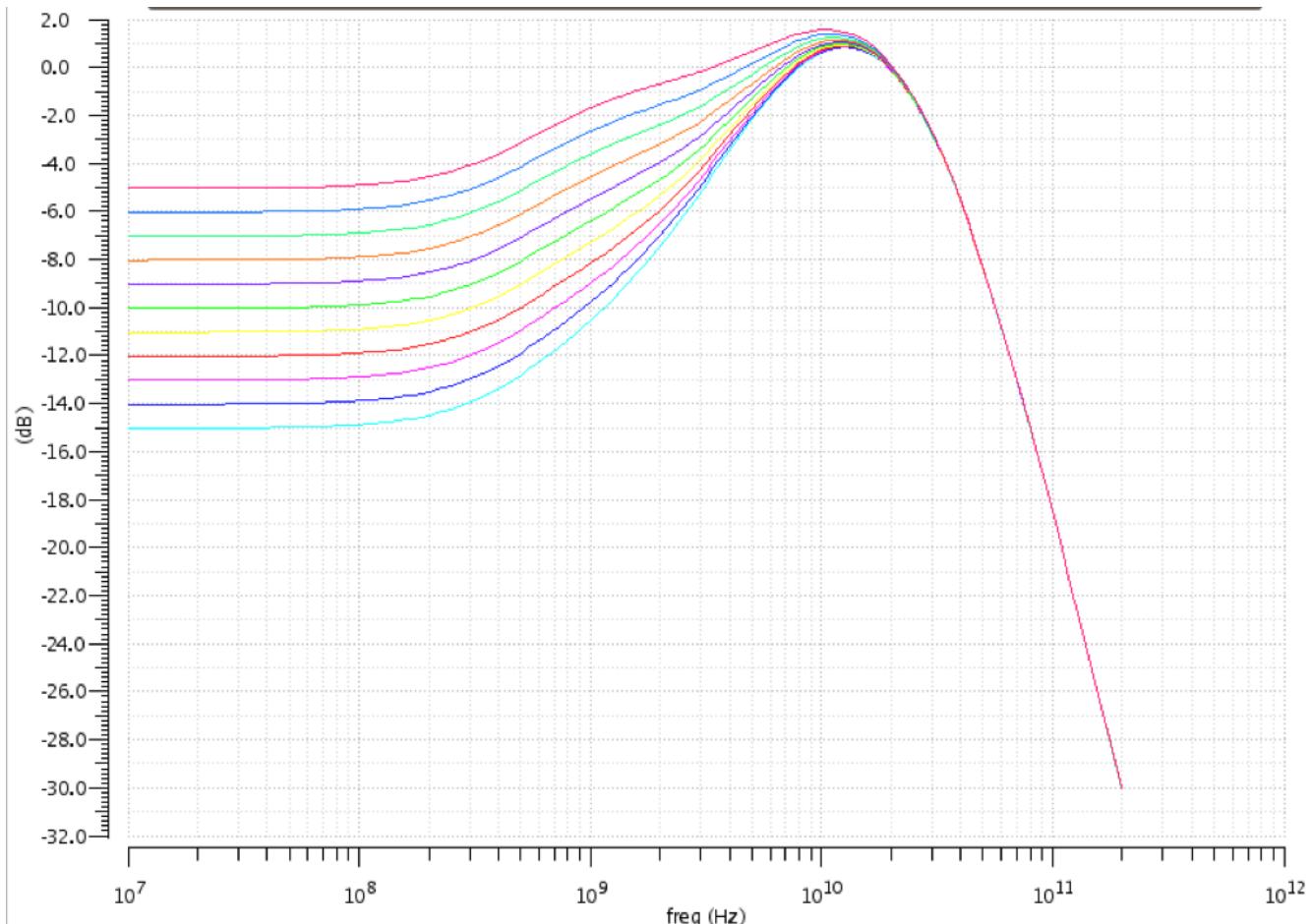


Figure 8-33 Loss Curves for 32.0 GT/s Behavioral CTLE

8.4.1.10 Behavioral DFE (8.0, 16.0, and 32.0 GT/s Only)

At 8.0 GT/s the combination of a 1st order CTLE and a one-tap DFE algorithm is required for calibrating the stressed eye when employing the max length calibration channel. The DFE may be represented by the following equation and flow diagram. For 8.0 GT/s and 16.0 GT/s the limits on d_1 are ± 30 mV. For 32.0 GT/s the limit on d_1 is defined a ratio of the tap magnitude (h_1) to the cursor strength (h_0). The h_1/h_0 ratio must be less than or equal to 0.8. Note that the h_1/h_0 limit of 0.8 is only to bound the behavior of the reference receiver and does not indicate that real implementations will be safe from error bursts due to large h_1/h_0 causing undetected data errors as long as the h_1/h_0 ratio is below 0.8.

Implementors must do their own analysis for their specific designs on the largest safe h_1/h_0 ratio. Note that an optional precoding mechanism is provided at 32.0 GT/s that receivers can optionally enable to reduce the risk of DFE related error bursts in high transition data patterns causing silent data corruption. For 16.0 GT/s the limits on d_2 are ± 20 mV. For 32.0 GT/s the limits on d_2 and d_3 are ± 20 mV.

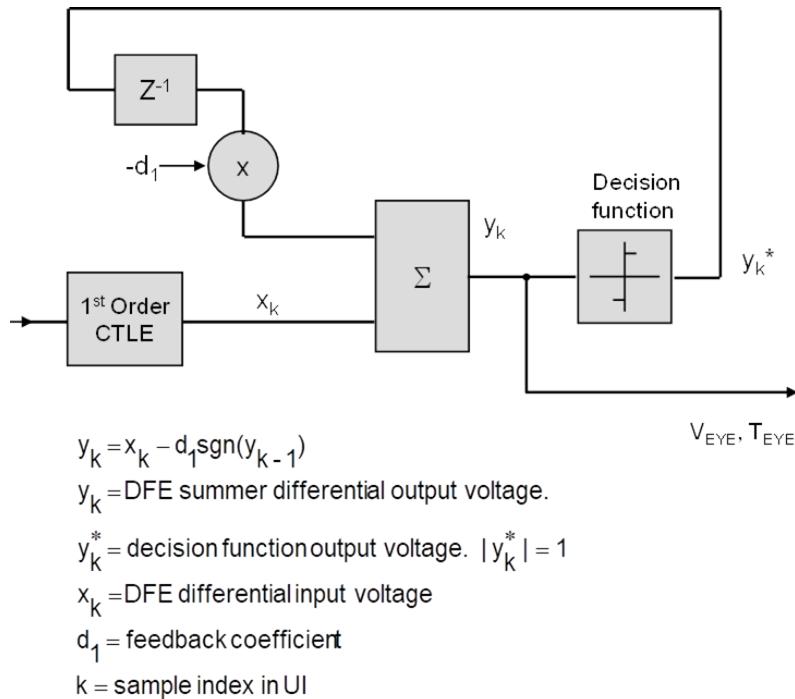


Figure 8-34 Variables Definition and Diagram for 1-tap DFE

16.0 GT/s Receiver tolerancing utilizes a CTLE and a 2-tap behavioral DFE as illustrated below. Other than the inclusion of the second tap, it is identical to the 1-tap DFE shown above. The 32.0 GT/s Receiver tolerancing utilizes a CTLE and a 3-tap behavior DFE.

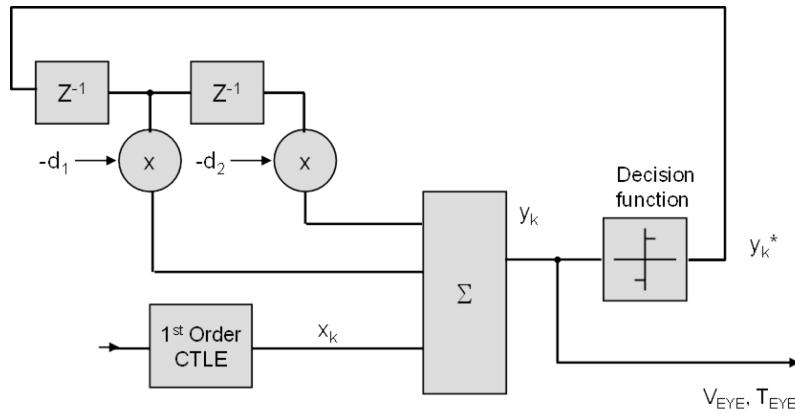


Figure 8-35 Diagram for 2-tap DFE

8.4.2 Stressed Eye Test

Rx testing at 16.0 and 32.0 GT/s requires only a single stressed voltage/stressed jitter test per data rate.

When testing a Receiver it is required to have other PCI Express Lanes on the DUT sending or receiving data. Similarly, if the device supports other I/O, it should also be sending or receiving on these interfaces. The goal is to have the Rx test environment replicate the noise environment found in a real system as closely as possible.

8.4.2.1 Procedure for Calibrating a Stressed EH/EW Eye

The goal of calibrating a stressed voltage/jitter eye is to present the Receiver under test with simultaneously worst case margins whose distortion characteristics are similar to an eye produced by a real channel. Much of the distortion consists of the ISI produced by the calibration channel. Incremental changes of R_j and differential voltage are allowed to adjust the EW and EH, respectively at 8.0 GT/s. Incremental changes of S_j , $V_{RX\text{-}DIFF\text{-}INT}$, and differential voltage swing from nominal values may be used to adjust the EW and EH at 16.0 and 32.0 GT/s.

The reference point where EH/EW is defined corresponds to input to the Receiver latch at 8.0, 16.0, and 32.0 GT/s. Since this point is not physically accessible it is necessary to construct its equivalent by means of a post-processing procedure. A two million unit interval data record of compliance pattern or a step that has been averaged 1024 times at TP2 is first post processed to mathematically include the additional signal distortion caused by the behavioral Receiver package. If a compliance pattern waveform is used then all stresses except $V_{RX\text{-}CM\text{-}INT}$ are turned on if a step is used then all stresses are turned off. Then the resulting signal is recovered by means of Rx equalization, and a behavioral CDR function, resulting in an equivalent eye. The requirements for the waveform post processing tool used for the EH/EW calibration are described further in [Section 8.4.2.1.1](#).

As the calibration procedure of the signal generator output contains steps where the generator is connected directly to measurement instrumentation, the transition time of the output waveform can be very fast. Therefore, it is important that the bandwidth of instrumentation used to calibrate the generator be matched appropriately to the edge rate of the generator output. This specification requires the use of a generator for 16.0 GT/s testing whose outputs have a rise time of 14 ps-19 ps (20% / 80%) which also requires a minimum oscilloscope bandwidth of 25 GHz. This oscilloscope bandwidth is also the minimum required bandwidth for transmitter measurements at 16.0 GT/s. For 32.0 GT/s testing the specification requires the use of a generator whose outputs have a rise time of 7.5 - 15.0 ps (20%/80% measured with P4) which requires a minimum oscilloscope bandwidth of 50 GHz. This oscilloscope bandwidth is also the minimum required for transmitter measurements at 32.0 GT/s. A minimum oscilloscope sampling rate that captures at least 4 samples per unit interval is required for all data rates.

For the eye calibration process, the Tx equalization is fixed to the preset that gives the optimal eye area with the post processing tool being used for calibration. Once the testing procedure is under way the Tx preset may be adjusted to yield the best eye margins with the DUT. During EH/EW calibration S_j is set to 100 MHz and 0.1 UI. Tx EQ and differential voltage swing calibration are done at TP3 as shown in [Figure 8-22](#) and the loss before TP3 is not included in the calibration channel loss. For calibration at 16.0 GT/s the following process is used to calibrate the eye:

1. Calibrate the stress values to the nominal values in [Table 8-9](#).
2. Select an initial test channel length that give a loss at TP2P at 8 GHz of $27 \text{ dB} \pm 0.5 \text{ dB}$.
3. Measure the eye diagram for each TX EQ preset using the nominal TX Eq for the preset $\pm 0.1 \text{ dB}$ and select the TX EQ preset that gives the largest eye area.

For all EH, EW and eye area measurements performed in receiver calibration the A_{DC} in the reference receiver CTLE is varied over its minimum to maximum range in 0.25 dB steps. This is done to improve repeatability and accuracy in automated Rx calibration software and is only done for stressed eye calibration (not for channel compliance, etc.)

4. Increase the calibration channel loss to the next available length/loss and measure the new eye diagram at the selected preset. Continue to increase the length/loss until either the height or width have fallen below the targets in [Table 8-9](#) then the previous calibration channel length/loss is selected. If neither the height or width have fallen below the targets and the TP3 ([Figure 8-22](#)) to TP2P loss at 8 GHz has reached 30.0 dB then advance to the next step.

5. For the selected calibration channel length/loss, measure the eye diagram for each TX EQ preset and select the preset that gives the largest eye area. Note that this may be a different preset than step 3 due to the length/loss change.
6. Adjust S_j , $V_{RX-DIFF-INT}$, and Voltage Swing to make final adjustments to the eye by sweeping them through the following ranges:
 - a. S_j 5 to 10 ps PP.
 - b. $V_{RX-DIFF-INT}$ 10 to 25 mV at TP2.
 - c. Differential Voltage Swing 720 to 800 mV PP at TP1.
7. If the final S_j value is less than 0.1 UI then the R_j level is reduced so the eye width meets the target eye width with 0.1 UI of 100 MHz S_j .
8. If there are multiple combinations of S_j , $V_{RX-DIFF-INT}$, and Voltage Swing that give valid solutions first pick the combination that is closest to the target eye width (18.75 ps). If there are multiple S_j , $V_{RX-DIFF-INT}$, and Voltage Swing combinations that are equally close to the target eye width then pick the one with S_j closest to nominal. The selected values must give a mean eye height and width (over at least 5 measurements exact number of measurements needed for stable values will depend on lab set-up and tools) within the following ranges at BER E-12:
 - a. Eye height 15 mV +/- 1.5 mV
 - b. Eye width 18.75 ps +/- 0.5 ps

For calibration at 32.0 GT/s the following process is used to calibrate the eye:

1. Measure the eye diagram for each TX EQ preset using the nominal TX Eq for the preset +/- 0.3 dB and select the TX EQ preset that gives the largest eye area.

For all EH, EW and eye area measurements performed in receiver calibration the ADC in the reference receiver CTLE is varied over its minimum to maximum range in 1.0 dB steps. Measure the eye diagram varying the following parameters with the maximum indicated step size for each variable parameter:

- Channel loss from TP1 to TP2P varied from 34.0 to 37.0 dB with a maximum 0.5 dB step size.
Note that if your actual channel loss comes out to slightly above 37 or slightly below 34 that these cases are excluded (loss must be between 34.0 and 37.0 dB)
 - S_j varied from 1 to 5 ps PP with a maximum 0.25 ps step size with S_j measured at TP1
 - $V_{RX-DIFF-INT}$ 5 to 30 mV at TP2 with a maximum 2.5 mV step size
2. If the final S_j value is less than 0.1 UI then the R_j level is reduced so the eye width meets the target eye width with 0.1 UI of 100 MHz S_j .
 3. If there are multiple combinations of S_j , $V_{RX-DIFF-INT}$, and channel loss that give valid solutions first pick the combination with the highest channel loss. If there are multiple combinations that work with the highest channel loss then select the combination that is closest to the target eye height (15.0 mV). The selected values must give a mean eye height and width (over at least 5 measurements exact number of measurements needed for stable values will depend on lab set-up and tools) within the following ranges at BER E-12. A specific method for finding the combination of stress values that meet these criteria is outside the scope of this specification. If and only if no stress combinations can be found then the voltage swing may also be varied from 720 to 800 mV:

Note that because the first tie-breaker is highest loss - most approaches will start with the highest allowed channel loss.

- a. Eye height 15 mV +/- 1.5 mV

b. Eye width 9.375 ps +/- 0.5 ps

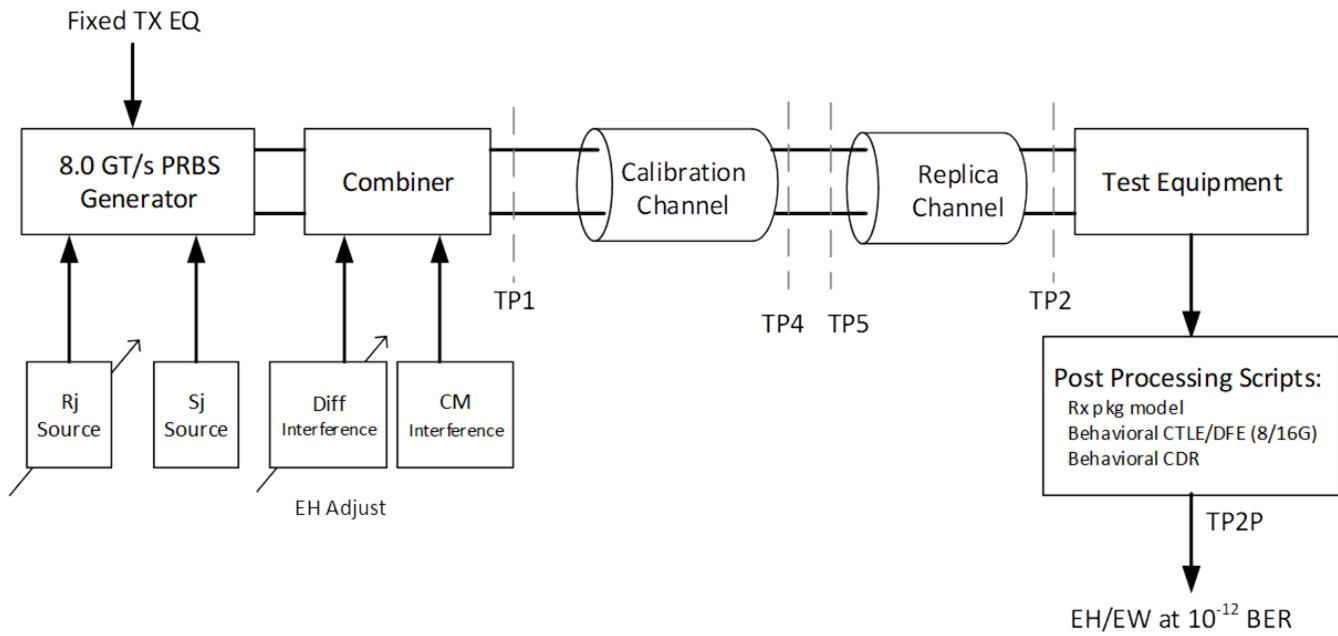


Figure 8-36 Layout for Calibrating the Stressed Jitter Eye at 8.0 GT/s

Based upon the data rate at which the Rx is being tested, Rj or Sj and differential interference sources are adjusted to fall within the VRX-ST and TRX-ST limits. The EH and EW ranges are designed to account for post processing or measurement errors. Figure 8-36 shows the process for calibrating the stressed jitter eye at 8.0 GT/s.

Figure 8-37 shows the process for calibrating the stressed jitter eye at 16.0 GT/s.

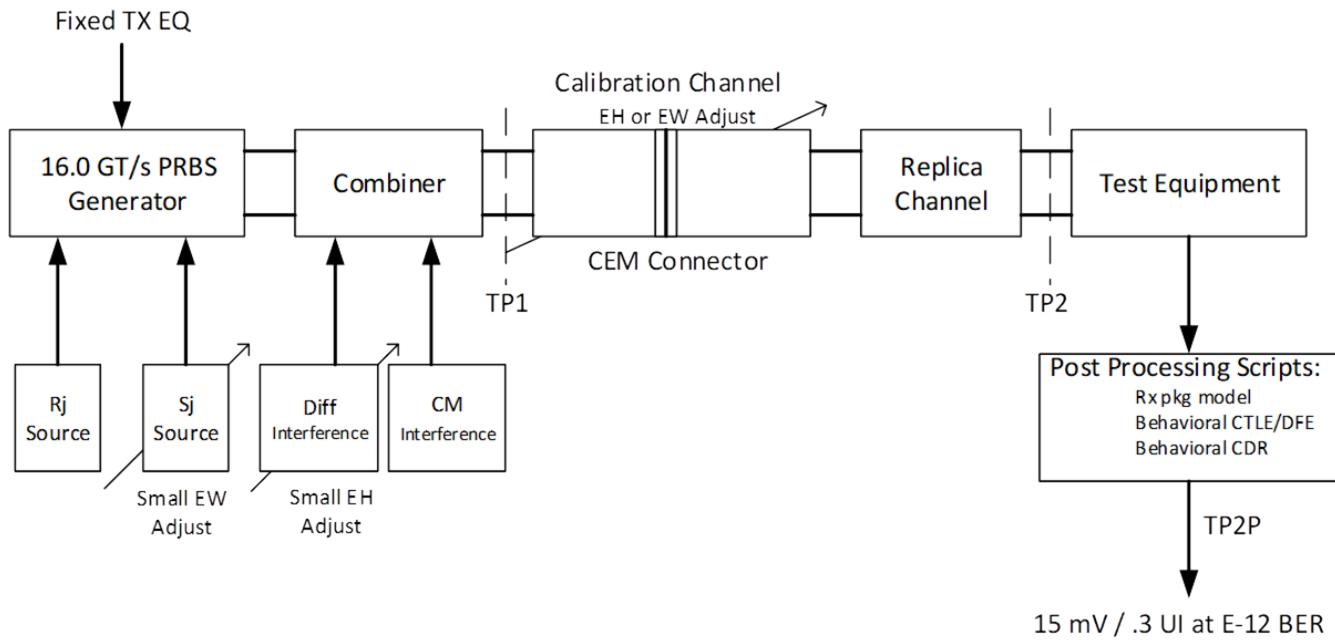


Figure 8-37 Layout for Calibrating the Stressed Jitter Eye at 16.0 GT/s

Table 8-9 Stressed Jitter Eye Parameters

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800 to 1200	800 to 1200	800 to 1200	720 to 800	720 to 800	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	31.25	ps	
T_{RX-ST}	Eye width	≤ 0.4	≤ 0.32	≤ 0.30	≤ 0.30	≤ 0.30	UI	Note 3, 4, 8, 10
V_{RX-ST}	Eye height	≤ 175	≤ 100	≤ 25	≤ 15	≤ 15	mV PP	Note 2, 4, 8, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	75 ps (max) See Note 11	See Section 8.4.2.2.1	See Section 8.4.2.2.1	See Section 8.4.2.2.1	ps	Note 5
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4	(max) 3.0	1.0	0.5	ps RMS	Note 6, 7
$V_{RX-DIFF-INT}$	Differential noise	N/A	N/A	14	14	10	mV PP	Note 7, 12 Adjust to set EH. Frequency = 2.1 GHz.
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	150	mV PP	Note 8

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Details
$V_{SSC-RES}$	SSC Residual	N/A	75	N/A	500	N/A	ps	Note 11, 13

Notes:

1. $V_{RX-LAUNCH}$ may be adjusted to meet V_{RX-ST} as long as the outside eye voltage at TP2 does not exceed 1300 mVPP for calibration at 2.5, 5.0, and 8.0 GT/s. $V_{RX-LAUNCH}$ is adjusted from 720 to 800 mV for 16.0 and 32.0 GT/s calibration.
2. Voltages shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
3. Eye widths shown for 2.5 GT/s and 5.0 GT/s are at the Rx pins.
4. V_{RX-ST} and T_{RX-ST} are referenced to TP2P for 8.0 GT/s, 16.0 GT/s and 32.0 GT/s and TP2 for 2.5 GT/s and 5.0 GT/s. For 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s behavioral equalization are applied to the data at TP2.
5. $T_{RX-ST-SJ}$ may be measured at either TP1 or TP2. Only 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s receivers are tested with Sj mask.
6. $T_{RX-ST-RJ}$ may be adjusted to meet the target value for T_{RX-ST} at 8.0 GT/s. Rj is measured at TP1 to prevent data-channel interaction from adversely affecting the accuracy of the Rj calibration. Rj is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.
7. Both $T_{RX-ST-RJ}$ and $V_{RX-DIFF-INT}$ are limited to prevent the stressed eye from containing excessive amounts of jitter or noise distortion that are unrepresentative of a real channel. Too many of these distortion components produces a signal that cannot be equalized by an actual Receiver.
8. Defined as a single tone at 120 MHz. Measurement made at TP2 without post-processing. Common mode is turned off during T_{RX-ST} and V_{RX-ST} calibration and then turned on for the stressed eye jitter test.
9. For 2.5 GT/s and 5.0 GT/s Rx calibration variable channel loss is used to achieve the target eye height.
10. For 2.5 GT/s Rx calibration 100 MHz Sj is used to achieve the target eye width.
11. For 33 kHz SSC residual for common clock architecture testing only when testing at 5 GT/s.
12. Frequency for $V_{RX-DIFF-INT}$ is chosen to be slightly above the first pole of the reference CTLE.
13. Applied for CC testing only as a triangular phase modulation with a frequency between 30 kHz to 33 kHz when testing at 16.0 GT/s with no 32.0 GT/s support and when the Sj mask of Figure 8-43 and a first order CDR transfer function are used.

8.4.2.1.1 Post Processing Tool Requirements

A waveform post processing tool or a channel compliance methodology tool may be used for Rx stressed eye calibration at 16.0 or 32.0 GT/s. If a waveform post processing tool is used to calibrate the EH/EW for the RX stressed eye testing, the tool must be consistent with the channel compliance methodology tool based on a consistency test defined as follows:

- The test channel is the long Rx calibration channel with the Root reference package applied in post-processing to give a total loss of 28.0 dB at 8 GHz (16.0 GT/s) or 36.0 dB at 16 GHz (32.0 GT/s). This means that the physical channel loss is 23.0 dB (16.0 GT/s) or 27.0 dB (32.0 GT/s).
- All measurements are done at TP2.
- A step pattern with 256 ones and zeros is captured through the test channel by averaging 1024 times on a real time oscilloscope. The step is saved with an x-axis resolution of 1 ps or less to be used as the transmit waveform for the channel compliance methodology. The step pattern is captured for each preset using the nominal Tx EQ for each preset.
- The channel compliance methodology is run with no Tx EQ applied in simulation using the nominal stress values for Rx stressed eye calibration for each of the captured steps. The Tx EQ preset that produced the largest eye area is selected for exact eye height and width calibration.

- The channel compliance methodology is used with the selected Tx EQ preset to produce an EH/EW of 15 mV and 0.3 UI @ E-12 BER (16.0 GT/s) or 15 mV and 0.3 UI @ E-12 BER (32.0 GT/s) by adjusting the Sj, $V_{RX\text{-}DIFF\text{-}INT}$ and voltage swing at the Transmitter output.
- A pattern generator is calibrated to have the same jitter stress levels and Tx Swing as those used in the channel compliance simulations that produced the target eye height and eye width..
- 2 million unit interval waveforms with compliance pattern are captured at each Tx EQ at the end of the channel. The Tx EQ is calibrated to the nominal values for each preset at the pattern generator output before doing the captures.
- For the preset that gives the largest eye area with the waveform post processing tool the EH and EW @ E-12 BER must match the target EH and EW from the channel compliance methodology within +/- 15%.

8.4.2.2 Procedure for Testing Rx DUT

8.4.2.2.1 Sj Mask

Once a calibrated EH and EW have been obtained, the cables are moved to connect the Rx DUT to the far end of calibration channel. The Tx equalization may then be optimized with the assumption that the DUT Rx will also optimize its equalization. Sj is set to an initial value of 0.1 UI at 100 MHz and the Receiver CDR must achieve lock. At 8.0 GT/s, 16.0 GT/s and 32.0 GT/s the 100 MHz Sj initial tone is removed and then the appropriate swept Sj profile is tested. At 16.0 GT/s and 32.0 GT/s an additional Sj tone at 210 MHz is present for all testing. The amplitude of this additional tone is equal to the amplitude of the 100 MHz Sj required to achieve the target eye width minus 0.1 UI. If the calibration Sj level was less than 0.1 UI then no additional tone at 210 MHz is used. Different Sj profiles are used, depending on data rate and whether the Rx under test operates in the CC mode or the IR Refclk mode. See [Table 8-9](#).

The SJ profiles shown in [Figure 8-38](#), [Figure 8-39](#), [Figure 8-40](#), [Figure 8-41](#), and [Figure 8-42](#) consist of a fixed 33 kHz tone and a swept tone from 400 kHz to 100 MHz, representing the swept Sj frequency range. For 8.0 GT/s and 16.0 GT/s SRIS mode with 5000 ppm SSC, the magnitude of the 33 kHz spur is 25 ns pp. For 32.0 GT/s SRIS mode with 3000 ppm SSC, the magnitude of the 33 kHz spur is 15 ns pp. A Receiver must meet the 10^{-12} BER over the entire swept Sj frequency range. It is not necessary to test a Receiver over the entire Sj frequency range, but a sufficient number of frequency points should be tested to guarantee that the Rx does not fail the target BER at some resonance frequency. The 33 kHz frequency point must be tested. Note that no SSC is applied at the source. Swept Sj is required only for testing Receivers at 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s. Receiver operation at 2.5 GT/s and 5.0 GT/s is tested using a single 33 kHz Sj tone.

Receivers operating at 8.0 GT/s in the IR mode use the Sj mask profile shown in [Figure 8-38](#). The magnitude of the 33 kHz spur is 25 ns pp, or 200 UIpp. The equation of the swept Sj curve is shown on [Figure 8-38](#).

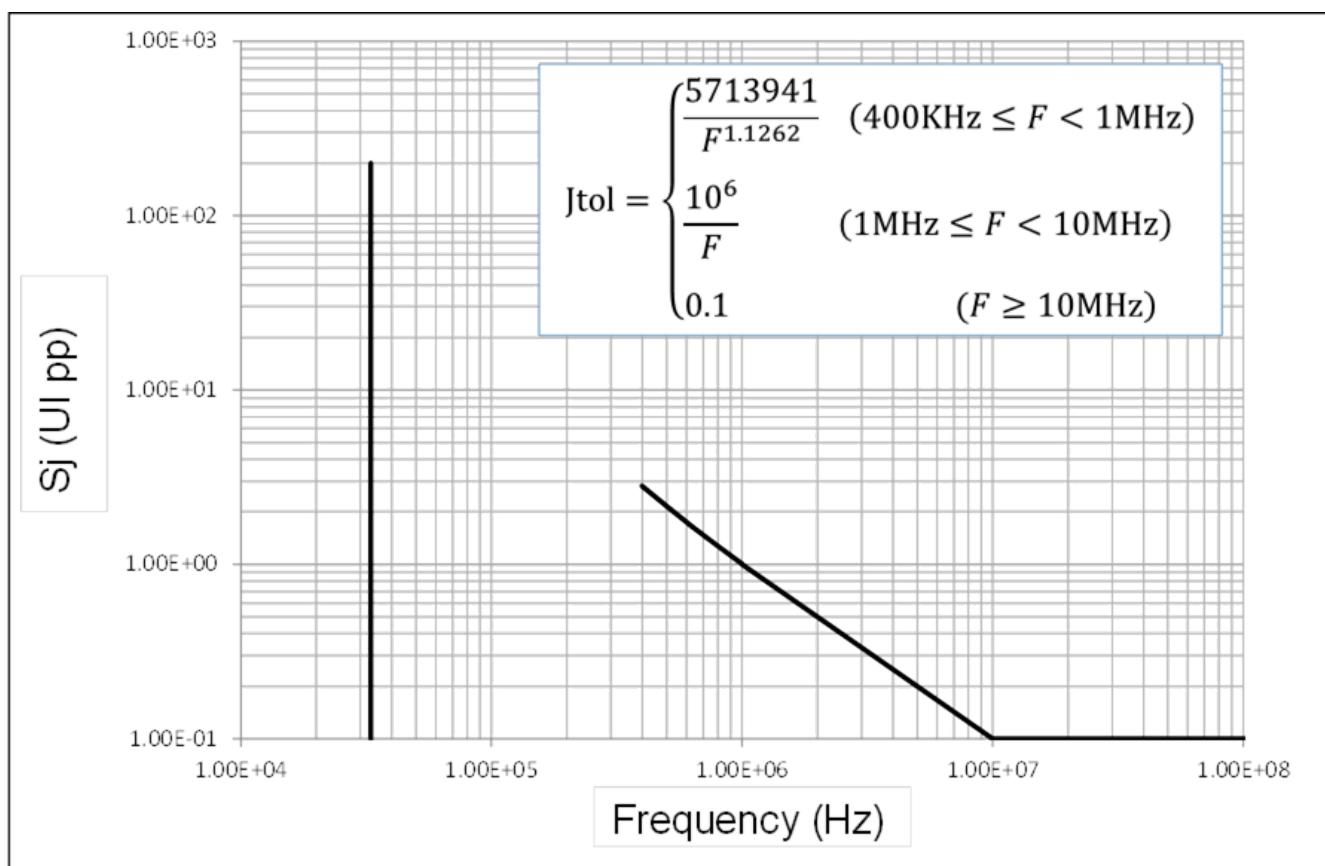


Figure 8-38 S_j Mask for Receivers Operating in IR mode at 8.0 GT/s

Receivers operating at 16.0 GT/s in the Independent Refclk (IR) mode use the S_j mask profile shown in Figure 8-39. The magnitude of the 33 kHz spur is 25 ns pp, or 400 UIpp. The equation of the swept S_j curve is shown on the [Figure 8-39](#).

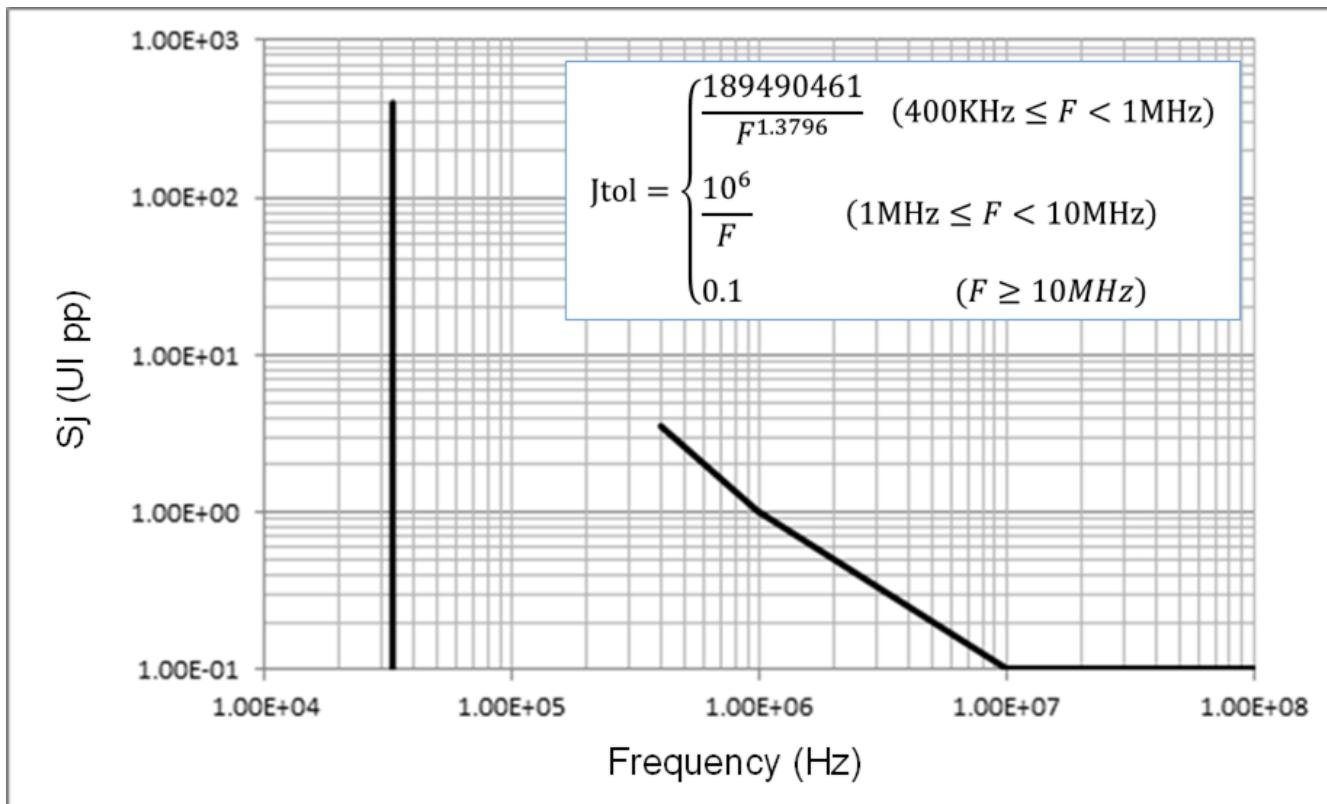


Figure 8-39 *Sj* Mask for Receivers Operating in SRIS mode at 16.0 GT/s

Receivers operating at 16.0 GT/s in the Common Clock (CC) Refclk mode use the *Sj* mask profile shown in Figure 8-40 . The magnitude of the 33 kHz spur is 1 ns pp, or 16 UIpp. The equation of the swept *Sj* curve is shown on the Figure 8-40 . Devices that do not support 32.0 GT/s have the option to use the *Sj* mask defined in Figure 8-43 . In this case, a 500 ps-pp triangular SSC modulation has to be applied at the source for both channel calibration and RX compliance, as specified in Table 8-9 .

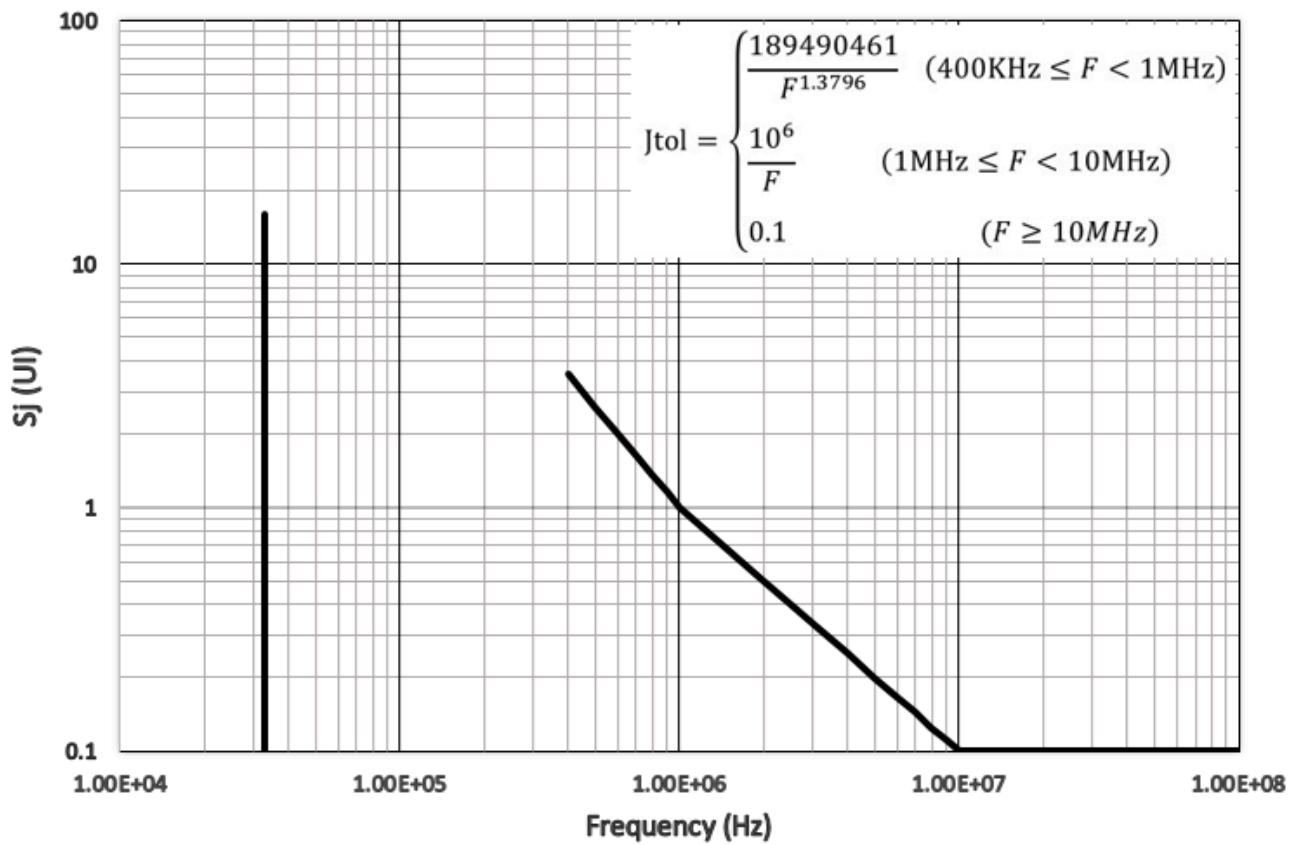


Figure 8-40 Sj Mask for Receivers Operating in CC mode at 16.0 GT/s

Receivers operating at 32.0 GT/s in the IR mode use the Sj mask profile shown in Figure 8-41. The magnitude of the 33 kHz spur is 15 ns pp, or 480 UIpp. The equation of the swept Sj curve is shown on the Figure 8-41.

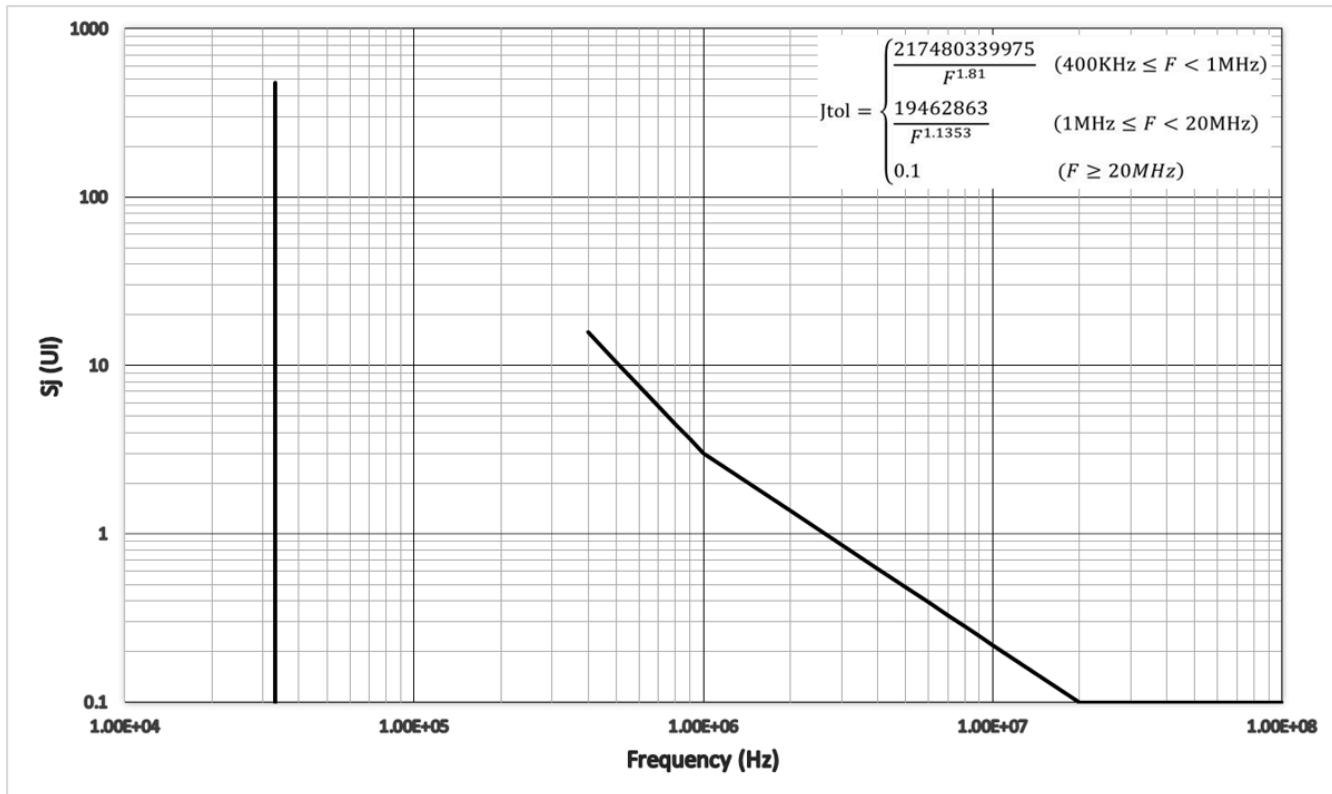


Figure 8-41 Sj Mask for Receivers Operating in SRIS mode at 32.0 GT/s

Receivers operating at 32.0 GT/s in the CC Refclk mode use the Sj mask profile shown in Figure 8-42. The magnitude of the 33 kHz spur is 1 ns pp, or 32 UIpp. The equation of the swept Sj curve is shown on the Figure 8-42.

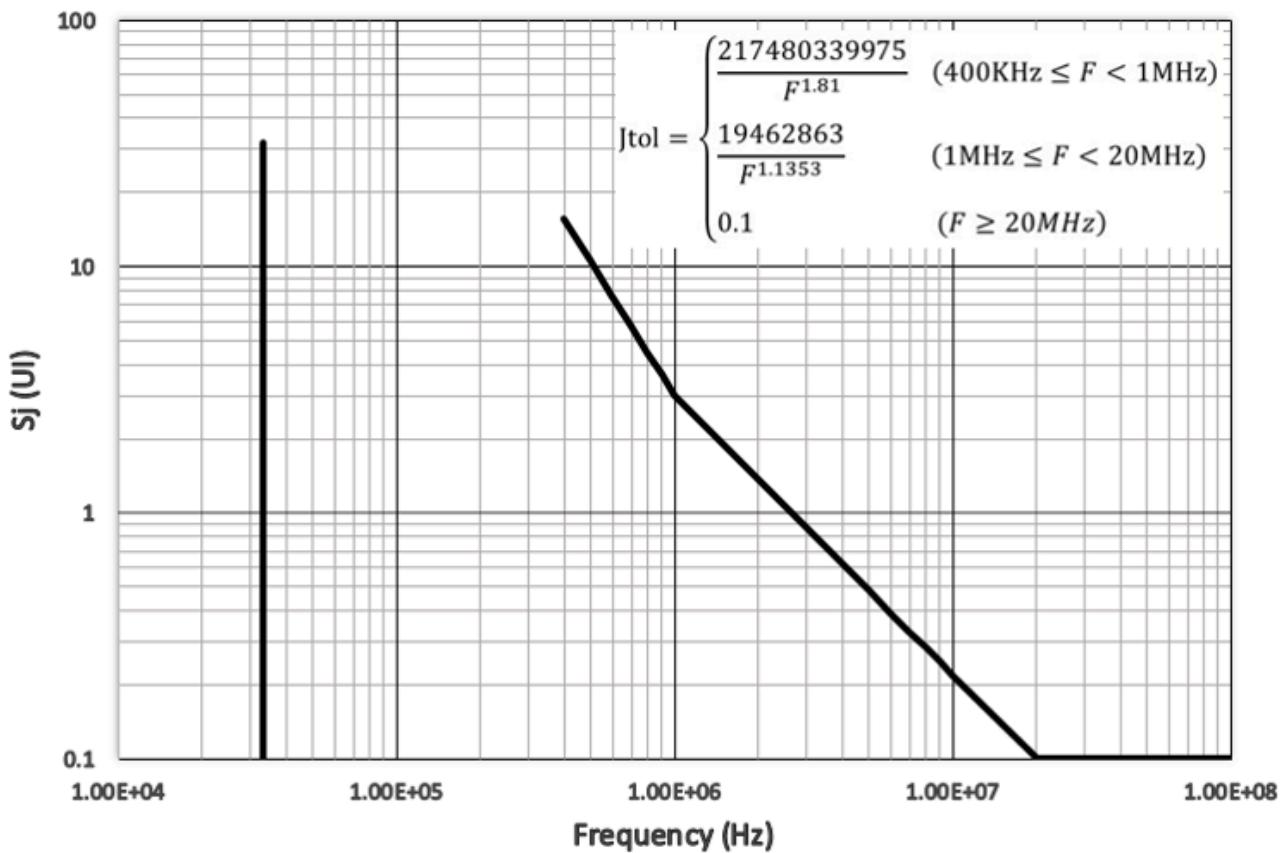


Figure 8-42 Sj Mask for Receivers Operating in CC mode at 32.0 GT/s

Receivers operating in the CC Refclk mode at 8.0 GT/s shall utilize the Sj profile shown in [Figure 8-43](#). The testing procedure is identical to that used for the IR mode, except that the clock topology differs. See [Section 8.4.2.3](#) for details. Receivers operating at 16.0 GT/s in the CC Refclk mode in devices that do not support 32.0 GT/s also have the option to use the Sj mask profile shown in [Figure 8-43](#), with additional residual SSC applied per [Table 8-9](#).

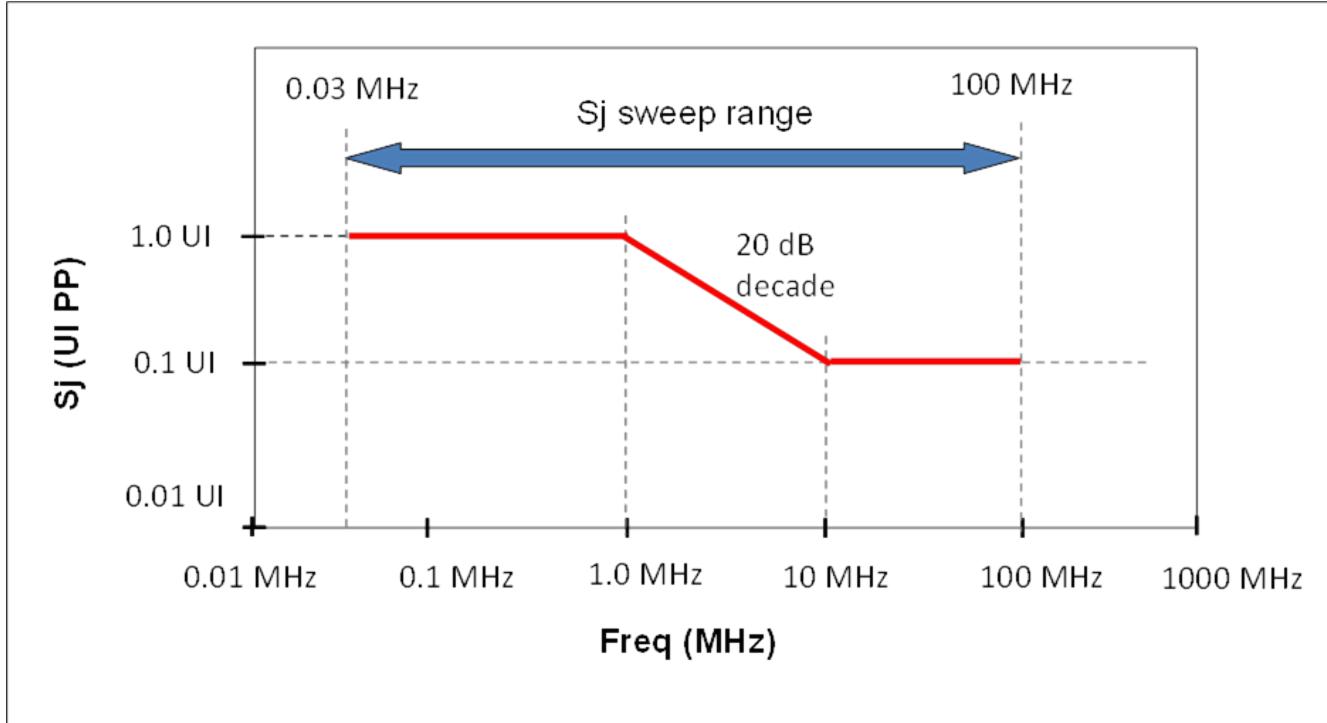


Figure 8-43 Sj Masks for Receivers Operating in CC Mode at 8.0 GT/s

8.4.2.3 Receiver Refclk Modes

A Rx is permitted to support one or both of two clock modes: CC, and IR although only one clock mode may be operational at a given time. Receivers can support more than one Refclk mode by selecting a mode at power-up or by means of strapping pins, etc.

8.4.2.3.1 Common Refclk Mode

Figure 8-44 shows the Refclk connection for a receiver in the Common Clock Refclk mode. A single Refclk source drives both the Generator and the DUT. This test utilizes the Sj mask specified in Section 8.4.2.2.1 .

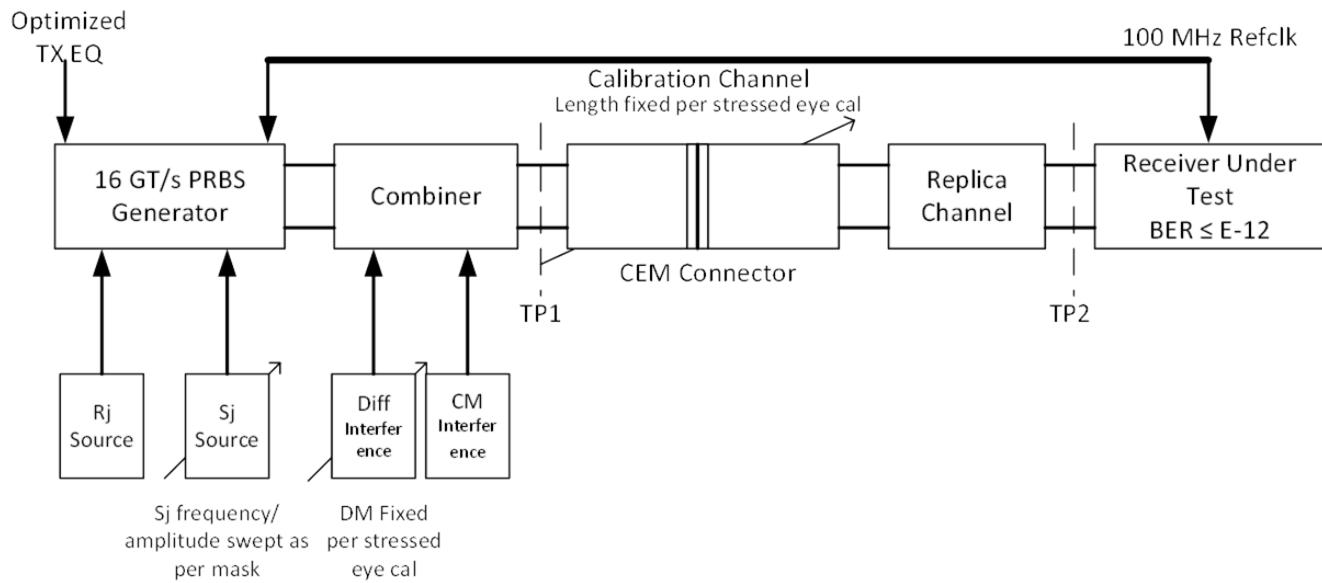


Figure 8-44 Layout for Jitter Testing Common Refclk Rx at 16.0 GT/s

8.4.2.3.2 Independent Refclk Mode

Figure 8-45 illustrates the configuration for testing a Receiver in the IR Refclk mode. A Refclk source with SSC is required for the DUT. The test utilizes the Sj mask specified in Section 8.4.2.2.1. The generator must be able to produce a large 33 KHz Sj tone while Sj is swept as shown in Section 8.4.2.2.1.

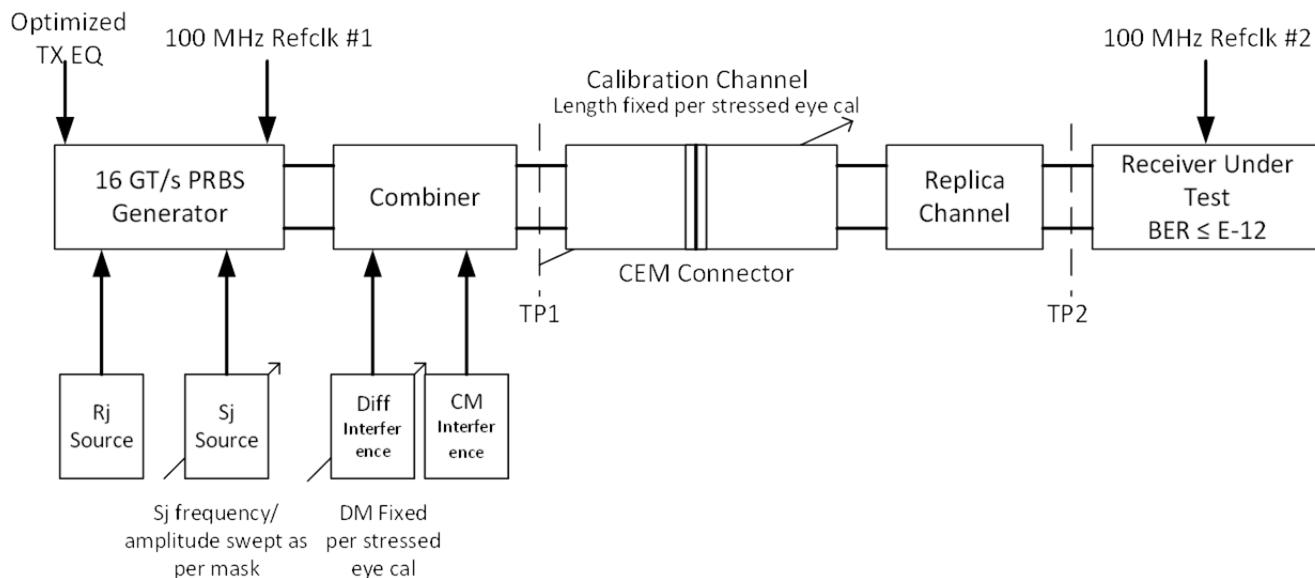


Figure 8-45 Layout for Jitter Testing for Independent Refclk Rx at 16.0 GT/s

8.4.3 Common Receiver Parameters

Table 8-10 lists the common Receiver parameters that are not directly associated with stressed eye tolerancing. Values are separately defined for the four data rates.

Table 8-10 Common Receiver Parameters

Symbol	Parameter	2.5 GT/s value	5.0 GT/s value	8.0 GT/s value	16.0 GT/s value	32.0 GT/s value	Units	Notes
UI (Rx)	Unit Interval	(min) 399.88 (max) 400.12 (300 PPM)	(min) 199.94 (max) 200.06 (300 PPM)	(min) 124.9625 (max) 125.0375 (300 PPM)	(min) 62.48125 (max) 62.51875 (300 PPM)	(min) 31.246875 (max) 31.253125 (100 PPM)	ps	UI tolerance does not include SSC effects
BW_{RX-PKG-PLL1}	Rx PLL bandwidth corresponding to <u>PKG_{RX-PLL1}</u>	(max) 22 (min) 1.5	(max) 16.0 (min) 8	(max) 4.0 (min) 0.5	(max) 4.0 (min) 0.5	(max) 1.8 (min) 0.5	MHz	Second order PLL transfer bounding function. See Note 1.
BW_{RX-PKG-PLL2}	Rx PLL bandwidth corresponding to <u>PKG_{RX-PLL2}</u>	Not Specified	(max) 16.0 , (min) 5.0	(max) 5.0 (min) 0.5	(max) 5.0 (min) 0.5	N/A	MHz	Second order PLL transfer bounding function. See Note 1.
PKG_{RX-PLL1}	Maximum Rx PLL peaking corresponding to <u>BW_{RX-PKG-PLL1}</u>	(max) 3.0	3.0	2.0	2.0	2.0	dB	Second order PLL transfer bounding function. See Note 1.
PKG_{RX-PLL2}	Maximum Rx PLL peaking corresponding to <u>BW_{RX-PKG-PLL2}</u>	Not specified	1.0	1.0	1.0	N/A	dB	Second order PLL transfer bounding function. See Note 1.
RL_{RX-DIFF}	Differential receiver return loss	See Figure <u>8-20</u>	See Figure <u>8-20</u>	See Figure <u>8-20</u>	See Figure <u>8-20</u>	See Figure <u>8-20</u>	dB	Note 2
RL_{RX-CM}	Common mode receiver return loss	See Figure <u>8-21</u>	See Figure <u>8-21</u>	See Figure <u>8-21</u>	See Figure <u>8-21</u>	See Figure <u>8-21</u>	dB	Note 2
T_{RX-GND-FLOAT}	Rx termination float time			(max) 500	(max) 500	(max) 500	μs	Note 5
V_{RX-CM-AC-P}	Rx AC common Mode Voltage	(max) 150	(max) 150	(max) 75 for EH < 100 mVPP (max) 125 for EH ≥ 100 mVPP	(max) 75 for EH < 100 mVPP (max) 125 for EH ≥ 100 mVPP	(max) 75 for EH < 100 mVPP (max) 125 for EH ≥ 100 mVPP	mVPP	Measured at Rx pins into a pair of 50Ω terminations to ground

Symbol	Parameter	2.5 GT/s value	5.0 GT/s value	8.0 GT/s value	16.0 GT/s value	32.0 GT/s value	Units	Notes
Z_{RX-DC}	Receiver DC single ended impedance	(min) 40 (max) 60	(min) 40 (max) 60	Not specified	Not specified	Not specified	Ω	DC impedance limits are needed to guarantee Receiver detect. For 8.0, 16.0, and 32.0 GT/s is bounded by R_{LRX-CM} . See Note 3.
$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for $V \geq 0$ during Reset or power-down	$\geq 10K$ (0-200 mV) $\geq 20K$ (> 200 mV)	Ω	Voltage measured wrt. ground. Parameters may not scale with process technology. See Note 4.				
$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for $V < 0$ during Reset or power-down	1.0K (min)	Ω	Voltage measured wrt. ground. Parameters may not scale with process technology. See Note 4.				
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect threshold	(min) 65 (max) 175	(min) 65 (max) 175	(min) 65 (max) 175	(min) 65 (max) 175	(min) 65 (max) 175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	(max) 10	(max) 10	(max) 10	(max) 10	(max) 10	ms	An unexpected Electrical Idle ($V_{RX-DIFF-PP} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Lane to Lane skew	(max) 20	(max) 8	(max) 6	(max) 5	(max) 5	ns	Across all Lanes on a Port. $L_{RX-SKEW}$ comprehends Lane-Lane variations due to channel and repeater delay differences.

Notes:

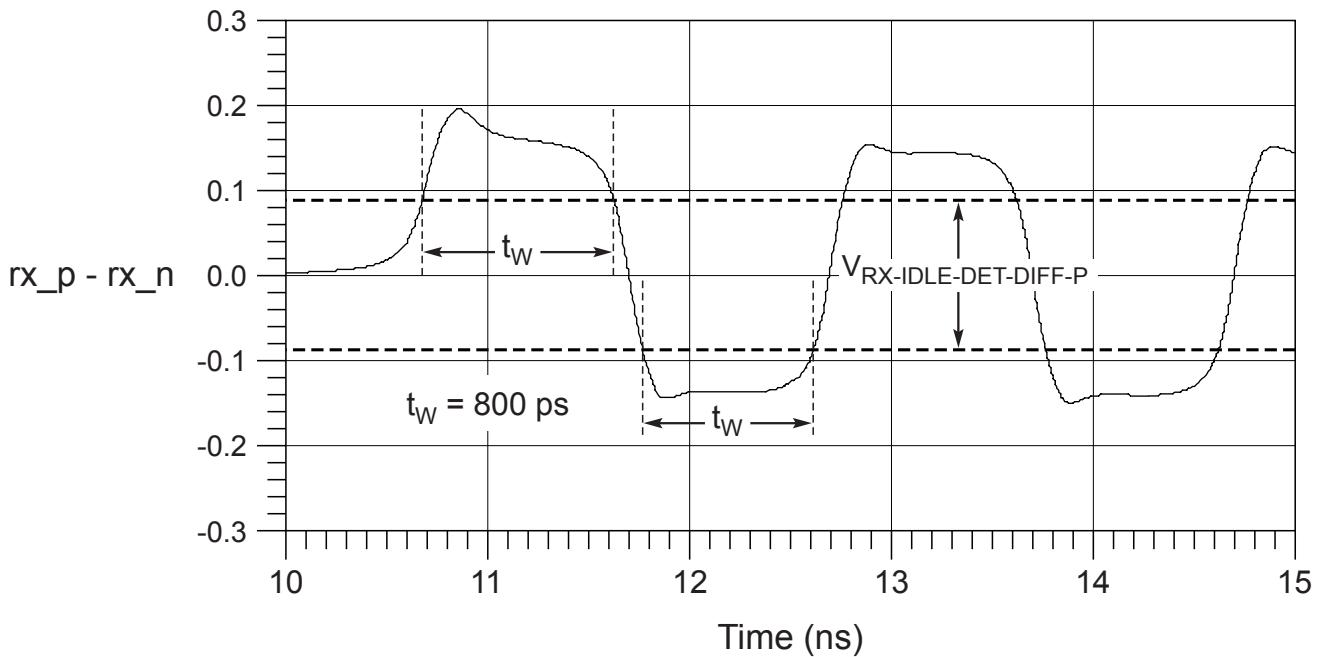
- Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥ 8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥ 5 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.
- Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.

Symbol	Parameter	2.5 GT/s value	5.0 GT/s value	8.0 GT/s value	16.0 GT/s value	32.0 GT/s value	Units	Notes
3.	The Rx DC single ended impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance is permitted to start immediately and the Rx Common Mode Impedance (constrained by R_{LRX-CM} to $50 \Omega \pm 20\%$) must be within the specified range by the time Detect is entered.							

4.	$Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.
5.	Defines the time for the Receiver's input pads to settle to new common-mode on 2.5/5.0 GT/s transition to 8.0, 16.0, and 32.0 GT/s.

8.4.3.1 5.0 GT/s Exit From Idle Detect (EFI)

It is difficult to scale the capabilities of the EFI detect circuits with data rate, and for this reason the 5.0, 8.0, 16.0, and 32.0 GT/s specification defines different data patterns in the FTS and the TS1 and TS2 Ordered Sets than are defined for 2.5 GT/s operation. In particular, repeated K28.7 patterns are defined to guarantee sufficient voltage and time requirements, as illustrated in the figure below. Concatenated EIE Symbols yield alternating one/zero run lengths of five UI each.



A-0564

Figure 8-46 Exit from Idle Voltage and Time Margins

8.4.3.2 Receiver Return Loss

The measurement methodology and frequency binning for differential and common mode Rx RL is identical to that for the Tx. For details refer to [Figure 8-20](#) and [Figure 8-21](#).

8.4.4 Lane Margining at the Receiver - Electrical Requirements

PCI Express components including retimers that support the 16.0 GT/s rate are required to support Lane margining at the Receiver when operating at 16.0 or 32.0 GT/s. Lane Margining enables system software to get the margin information of a given Lane while the Link is in L0 state. The margin information includes both voltage and time, in either direction from the current Receiver position. The margin feature is not permitted to require any additional external hardware to function. Support of Lane margining for voltage is optional at 16.0 GT/s and required at 32.0 GT/s and support of independent timing margin to the left or to the right is optional. For simplicity, the margin commands and requirements described in the protocol chapter(s) of this specification are described in terms of moving the data sample location - but the actual margining method is implementation specific. For example - the timing margin could be implemented on the actual data sampler or an independent/error sampler. Further the timing margin can be achieved by injecting an appropriate amount of stress/jitter to the data sample location, or by actually moving the data/error sample location. The parameters in Table 8-11 are reported for 16.0 and 32.0 GT/s and are allowed to be different for each speed.

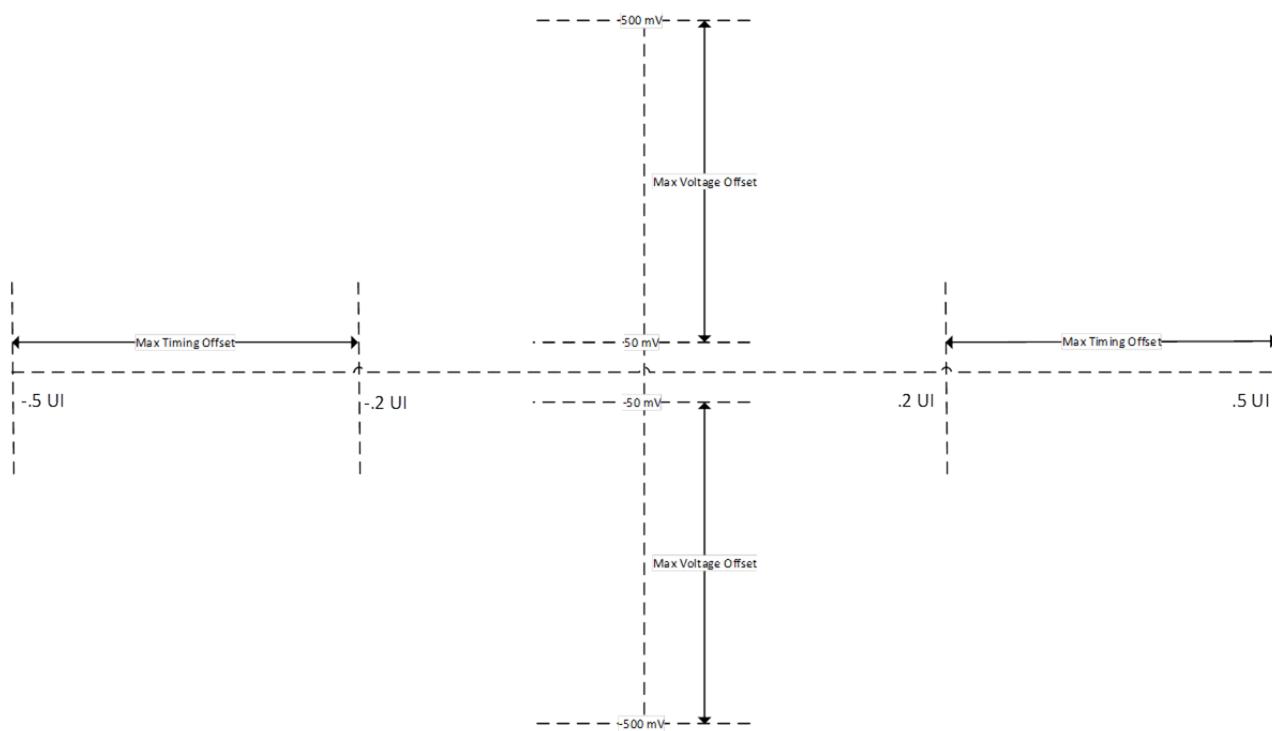


Figure 8-47 Allowed Ranges for Maximum Timing and Voltage Margins

Table 8-11 Lane Margining Timing

Parameter Name	Min	Max	Description
MNumTimingSteps	6	63	<p>Number of time steps from default (to either left or right), range must be at least +/-0.2 UI</p> <p>Timing offset must increase monotonically</p> <p>The number of steps in both positive (toward the end of the unit interval) and negative (toward the beginning of the unit interval) must be identical</p>

Parameter Name	Min	Max	Description
MMaxTimingOffset	20	50	Offset from default at maximum step value as percentage of a nominal UI A 0 value may be reported if the vendor chooses not to report the offset
MNumVoltageSteps	32	127	Number of voltage steps from default (either up or down), minimum range +/-50 mV as measured by the reference equalizer Voltage offset must increase monotonically The number of steps in both positive and negative direction from the default sample location must be identical This value is undefined if <u>MVoltageSupported</u> is 0b
MMaxVoltageOffset	5	50	Offset from default at maximum step value as percentage of one volt A 0 value may be reported if the vendor chooses not to report the offset when <u>MVoltageSupported</u> is 1b This value is undefined if <u>MVoltageSupported</u> is 0b
MSamplingRateVoltage	0	63	The ratio of bits tested to bits received during voltage margining. A value of 0 is a ratio of 1:64 (1 bit of every 64 bits received), and a value of 63 is a ratio of 64:64 (all bits received).
MSamplingRateTiming	0	63	The ratio of bits tested to bits received during timing margining. A value of 0 is a ratio of 1:64 (1 bit of every 64 bits received), and a value of 63 is a ratio of 64:64 (all bits received).
MVoltageSupported	0	1	1b indicates that voltage margining is supported
MIndLeftRightTiming	0	1	1b indicates independent left/right timing margin supported
MIndUpDownVoltage	0	1	1b independent up and down voltage margining supported
MIndErrorSampler	0	1	1b Margining will not produce errors (change in the error rate) in data stream (ie. error sampler is independent) 0b Margining may produce errors in the data stream
MMaxLanes	0	31	Maximum number of Lanes minus 1 that can be margined at the same time. It is recommended that this value be greater than or equal to the number of Lanes in the Link minus 1. Encoding Behavior is undefined if software attempts to margin more than <u>MMaxLanes</u> +1 at the same time. Note: This value is permitted to exceed the number of Lanes in the Link minus 1.
MSampleReportingMethod	0	1	Indicates whether sampling rates (<u>MSamplingRateVoltage</u> and <u>MSamplingRateTiming</u>) are supported (1) or a sample count is supported (0). One of the two methods is supported by each device.
MErrorCount	0	63	If <u>MIndErrorSampler</u> is 1b this is a count of the actual bit errors since margining started. If <u>MIndErrorSampler</u> is 0b this is the actual count of the logical errors since margining started. See the Physical Layer Logical Block chapter for the definition of what errors are counted.

Parameter Name	Min	Max	Description
			The count saturates at 63.
<i>MsampleCount</i>	0	127	<p>Value = $3 \cdot \log_2$ (number of bits margined).</p> <p>Where number of bits margined is a count of the actual number of bits tested during margining. The count stops when margining stops. The count saturates at 127 (after approximately 5.54×10^{12} bits).</p> <p>The count resets to zero when a new margin command is received.</p>

8.4.5 Low Frequency and Miscellaneous Signaling Requirements

8.4.5.1 ESD Standards

All PCI Express signal and power supply pins must be tested for ESD protection levels to the Human Body Model (HBM) and the Charged Device Model (CDM) standards in accordance with [[ESDA-JEDEC-JS-001-2010](#)] (for HBM) and in accordance with [[JEDEC-JESD22-C101](#)] (for CDM). Pins must meet or exceed the minimum levels recommended in [[JEDEC-JEP155-JEP157](#)] (HBM/CDM) or JEDEC approved superseding documents.

8.4.5.2 Channel AC Coupling Capacitors

Each Lane of a PCI Express Link must be AC coupled. The minimum and maximum values for the capacitance are given in [Table 8-7](#). Capacitors must be placed on only one side of an interface that permits adapters to be plugged and unplugged. Form factor specifications must define the required location of the capacitor. In a topology where everything is located on a single substrate, the capacitors may be located anywhere along the channel. External capacitors are assumed because the values required are too large to feasibly construct on-chip.

8.4.5.3 Short Circuit Requirements

All Transmitters and Receivers must support surprise hot insertion/removal without damage to the component. The Transmitter and Receiver must be capable of withstanding sustained short circuit to ground of D+ and D-.

8.4.5.4 Transmitter and Receiver Termination

- The Transmitter is required to meet RL_{TX-DIFF} and RL_{TX-CM} (see [Figure 8-20](#) and [Figure 8-21](#)) any time functional differential signals are being transmitted.
- The Transmitter is required only to meet I_{TX-SHORT} (see [Table 8-7](#)) any time functional differential signals are not being transmitted.
- Note: The differential impedance during this same time is not defined.
- The Receiver is required to meet RL_{RX-DIFF} and RL_{RX-CM} (see [Table 8-10](#)) during all LTSSM states excluding only times during when the device is powered down, Fundamental Reset is asserted, or when explicitly specified.

- The Receiver is required to meet $Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ (see Table 8-7) any time adequate power is not provided to the Receiver, Fundamental Reset is asserted, or when explicitly specified.

8.4.5.5 Electrical Idle

Electrical Idle is a steady state condition where the Transmitter D+ and D- voltages are held constant at the same value. Electrical Idle is primarily used in power saving and inactive states (e.g., Disabled).

Before a Transmitter enters Electrical Idle, it must always send the required number of EIOSs except for the LTSSM substates explicitly exempted from this requirement. After sending the last Symbol of the last of the required number of EIOSs, the Transmitter must be in a valid Electrical Idle state within the time as specified by $T_{TX-IDLE-SET-TO-IDLE}$ in Table 8-7.

The successful reception of an EIOS occurs based on the rules defined in the Physical Layer Logical Block chapter. It should be noted that in substates (e.g., Loopback.Active for a Loopback Slave) where multiple consecutive EIOSs are expected, the Receiver must receive the appropriate number of EIOS sequences comprising of COM, IDL, IDL, IDL.

The low impedance common mode and differential Receiver terminations values (see Table 8-7 and Table 8-10) must be met in Electrical Idle. The Transmitter can be in either a low or high impedance mode during Electrical Idle.

Any time a Transmitter enters Electrical Idle it must remain in Electrical Idle for a minimum of $T_{TX-IDLE-MIN}$. The Receiver should expect the last EIOS followed by a minimum amount of time in Electrical Idle ($T_{TX-IDLE-MIN}$) to arm its Electrical Idle Exit detector.

When the Transmitter transitions from Electrical Idle to a valid differential signal level it must meet the output return loss specifications described in Figure 8-20 and Figure 8-21.

Electrical Idle Exit shall not occur if a signal smaller than $V_{RX-IDLE-DET-DIFFp-p}$ minimum is detected at a Receiver. Electrical Idle Exit shall occur if a signal larger than $V_{RX-IDLE-DET-DIFFp-p}$ maximum is detected at a Receiver. Electrical Idle may be detected on the received signal regardless of its frequency components, or it may be detected only when the received signal is switching at a frequency of 125 MHz or higher.

8.4.5.6 DC Common Mode Voltage

The Receiver DC common mode voltage is nominally 0 V when operating at 2.5 GT/s or 5.0 GT/s.

Transmitter DC common mode voltage is held at the same value during all states unless otherwise specified. The range of allowed Transmitter DC common mode values is specified in Table 8-10 ($V_{TX-DC-CM}$).

8.4.5.7 Receiver Detection

The Receiver detection circuit is implemented as part of a Transmitter and must correctly detect whether a load impedance equivalent to a DC impedance implied by the Z_{RX-DC} parameter (40 Ω-60 Ω) is present. Note: Support for Rx detect, which only occurs at 2.5 GT/s, is the reason why 2.5 GT/s Receivers impedance at DC is specified.

The recommended behavior of the Receiver detection sequence is described below:

- Step 1. A Transmitter must start at a stable voltage prior to the detect common mode shift.
- Step 2. A Transmitter changes the common mode voltage on D+ and D- consistent with meeting the $V_{TX-RCV-DETECT}$ parameter and consistent with detection of Receiver high impedance which is bounded by parameters $Z_{RX-HIGH-IMP-DC-POS}$, $Z_{RX-HIGH-IMP-DC-NEG}$ in Table 8-10. Receiver is detected based on the rate that the lines change to the new voltage.

- a. The Receiver is not present if the voltage at the Transmitter charges at a rate dictated only by the Transmitter impedance and the capacitance of the interconnect and series capacitor.
- b. The Receiver is present if the voltage at the Transmitter charges at a rate dictated by the Transmitter impedance, the series capacitor, the interconnect capacitance, and the Receiver termination.

If the Receiver detection circuit performs the detect sequence on each conductor of the differential pair (both D+ and D-) and detects a load impedance greater than Z_{RX-DC} on either conductor, the Receiver detection circuit shall interpret this as no termination load present and respond as if neither load were present.

It is required that the detect sequence be performed on both conductors of a differential pair.

8.5 Channel Tolerancing

8.5.1 Channel Compliance Testing

This section of the specification is relevant only for those cases where a platform design comprehends the relevant channel between Transmitter device pins and Receiver device pins. These types of platform designs are called “captive channels”. Designs that are not captive channels shall refer to the appropriate form factor (CEM is one example) specification, since in this case the form factor specification takes precedence over this specification and splits the channel between two different types of components.

The key components and processes of channel tolerancing are illustrated in [Figure 8-48](#) and [Figure 8-49](#). The major difference lies in the complexity of the Behavioral Tx and Rx equalization, which depends on the data rate. 2.5 and 5.0 GT/s utilize fixed Tx presets and assume no Rx equalization, whereas 8.0, 16.0 and 32.0 GT/s assume multi-valued, adjustable Tx presets and a combination of Rx DFE and CTLE.

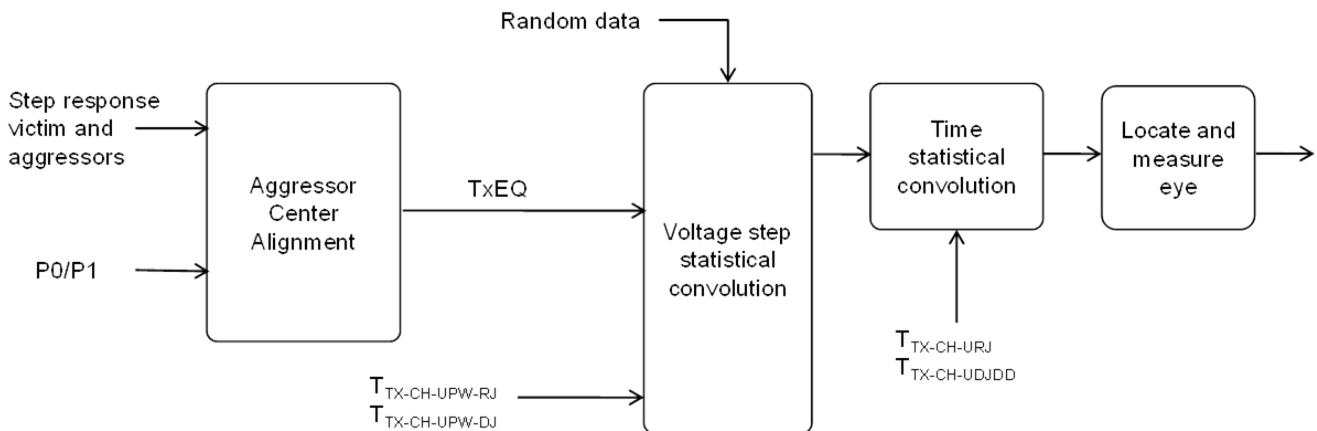


Figure 8-48 Flow Diagram for Channel Tolerancing at 2.5 and 5.0 GT/s

The basic channel compliance approach is to first acquire the channel's characteristics, usually by means of s-parameters or equivalent model. Behavioral Tx and Rx package models are then appended to the channel model to yield a die pad to die pad topology. The model shall include both victim path and a sufficient number of aggressor paths to accurately capture channel crosstalk effects. Using the Tx voltage and jitter limits defined in the Transmitter specification section it is possible to transform these parameters to what would appear at the die pad of a Tx.

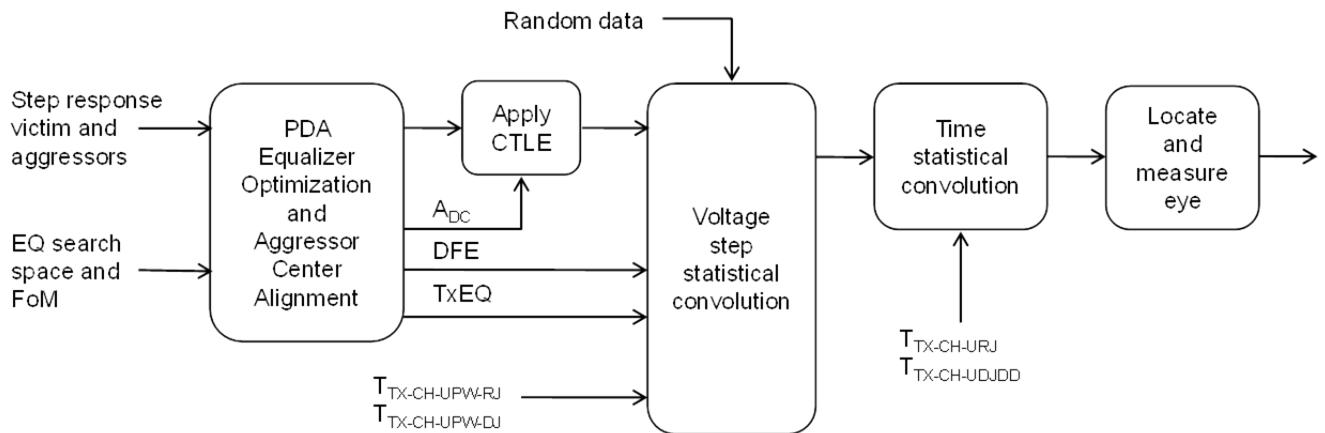


Figure 8-49 Flow Diagram for Channel Tolerancing at 8.0 and 16.0 GT/s

The resulting model is analyzed via simulation, yielding voltage and jitter at a point equivalent to the input latch of the Receiver. The signal observed at the Receiver's latch is referenced to a recovered data clock from which an eye diagram may be constructed.

For 8.0 GT/s, 16.0 and 32.0 GT/s testing the simulation process must properly account for Tx and Rx equalization optimization as must be supported by a minimum capability Tx/Rx pair. This means the simulation process must be able to select the optimum values for the Tx presets or coefficients and Rx equalization settings based upon a 1st order CTLE and a 1-tap DFE for 8.0 GT/s, a 1st order CTLE and a 2-tap DFE for 16.0 GT/s, and a 2nd order CTLE and 3-tap DFE for 32.0 GT/s.

8.5.1.1 Behavioral Transmitter and Receiver Package Models

Behavioral package models are defined in this specification to represent the combined die and package loss that is expected to interoperate with the targeted range of channels. Note that at 16.0 GT/s, the behavioral packages represent a high, but not worst case, loss for many devices. (see [Section 8.3.3.11](#) and [Section 8.4.1.5](#))

A separate pair of package models are defined for 8.0, 16.0 and 32.0 GT/s. At 8.0 GT/s, separate package models are defined for TX and RX ports to reflect the smaller CPAD capacitance typical in most receiver implementations. At 16.0 and 32.0 GT/s, separate package models are defined for devices containing Root Ports and all other devices to reflect the large and socketed nature of most devices containing Root Complexes. Channel testing for both data rates typically requires testing in both directions.

The package models are included with the specification as design collateral. Each model for 8.0 and 16.0 GT/s comprehends C_{PIN} and C_{PA}D parasitic capacitances plus a differential t-line element as illustrated in [Figure 8-50](#).

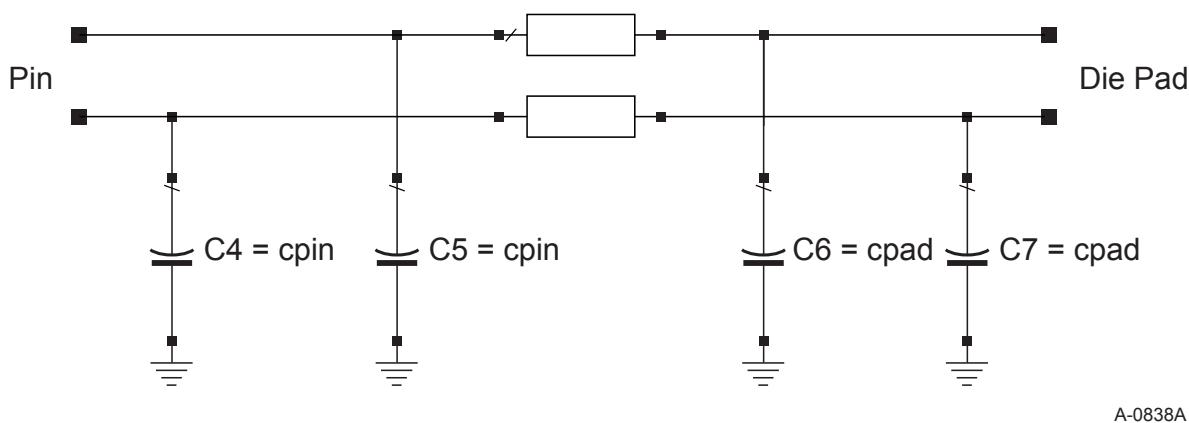


Figure 8-50 Tx/Rx Behavioral Package Models

The C_{PIN} and C_{PAD} values used in the package model generation are provided for informative purposes only.

Table 8-12 Package Model Capacitance Values

	8.0 GT/s Tx	8.0 GT/s Rx	16.0 GT/s
C_{PIN}	0.25 pF	0.25 pF	0.25 pF
C_{PAD}	1.0 pF	0.8 pF	0.5 pF

For ease of incorporation into the post processing flow the 8.0 and 16.0 behavioral package models are specified as 4-port s-parameter files. The files are specified with port designations, frequency range and granularity as listed below. The reference impedance for the s-parameters is 50Ω . File format is Touchstone.

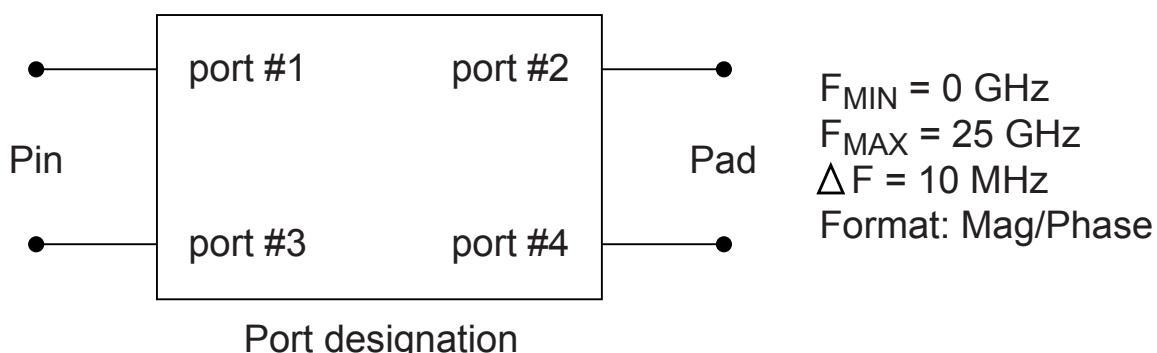


Figure 8-51 Behavioral Tx and Rx S-Port Designation for 8.0 and 16.0 GT/s Packages

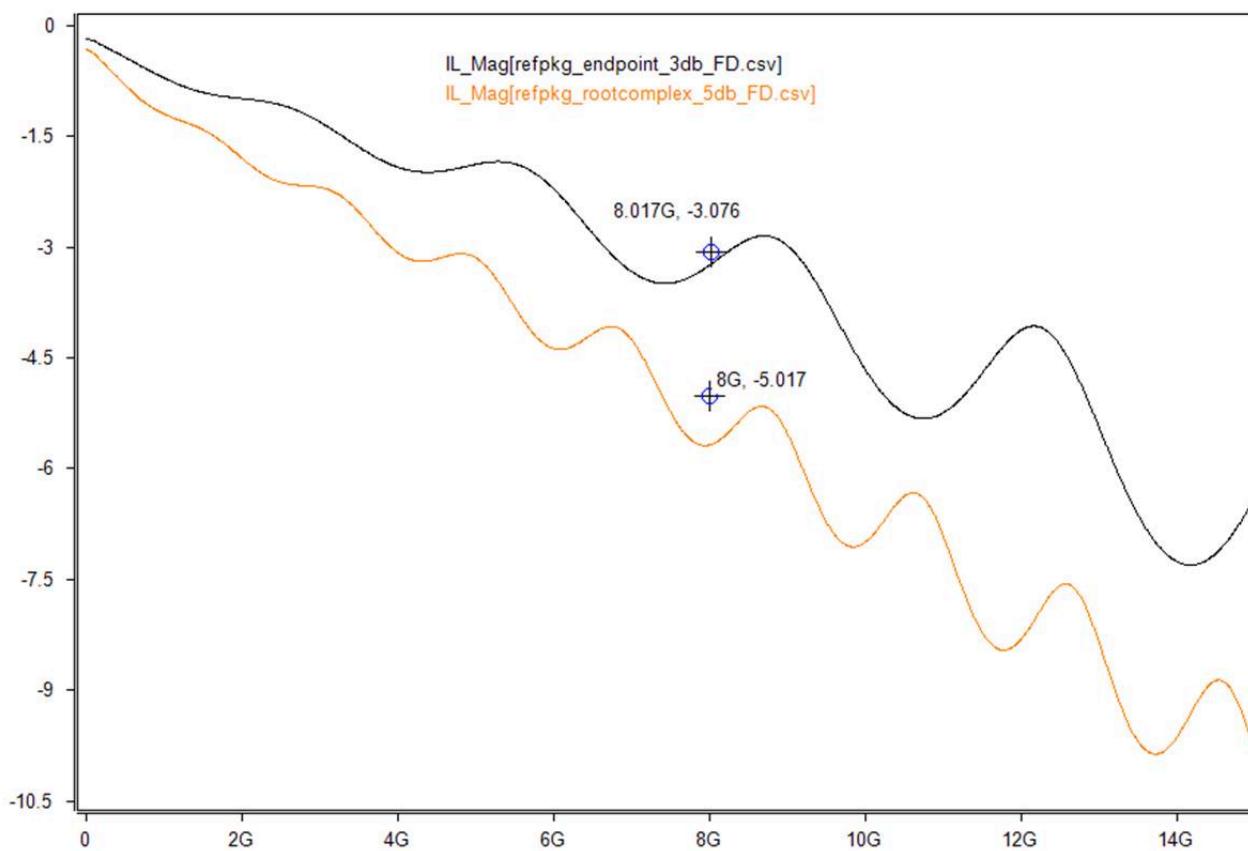


Figure 8-52 SDD21 Plots for Root and Non-Root Packages for 16.0 GT/s

For 32.0 GT/s the package models are based on real package and socket models for the root package and package and BGA models for the non-root package.

For all reference package models the die capacitive loads are included in the models.

Insertion loss

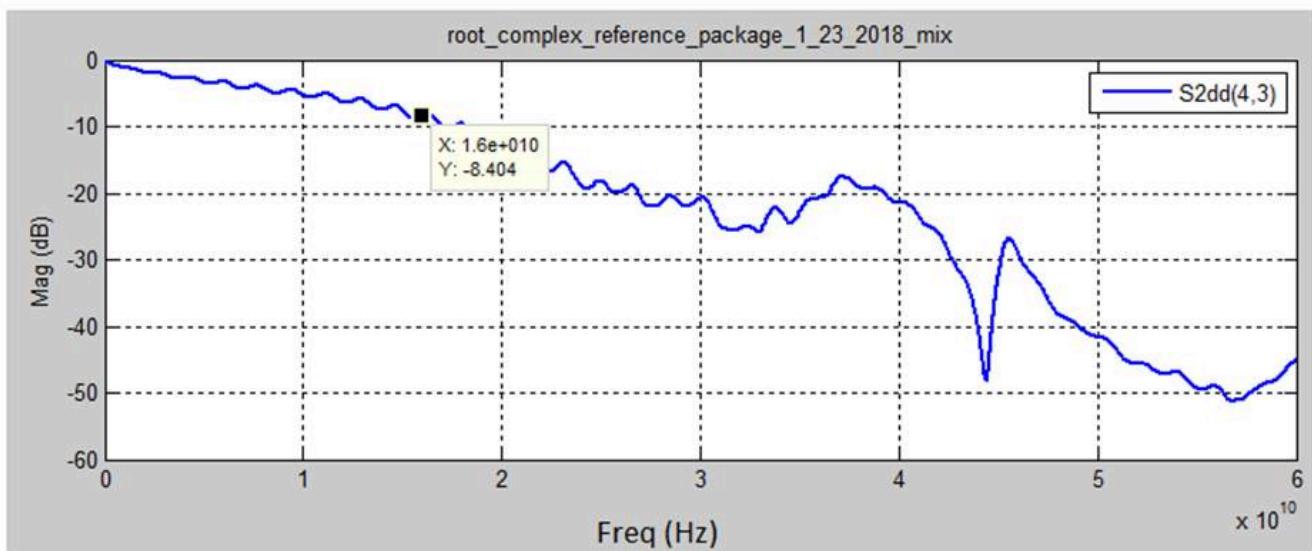


Figure 8-53 Insertion Loss for Root Reference Package for 32.0 GT/s

Return Loss (Board-side)

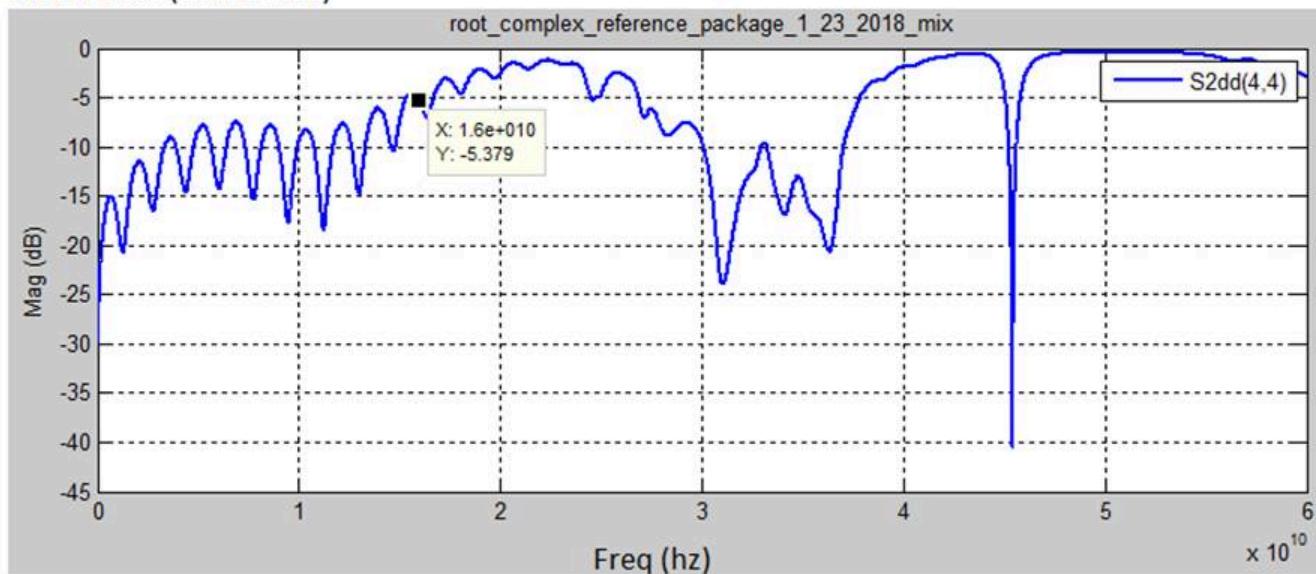


Figure 8-54 Return Loss for Root Reference Package for 32.0 GT/s

NEXT 2

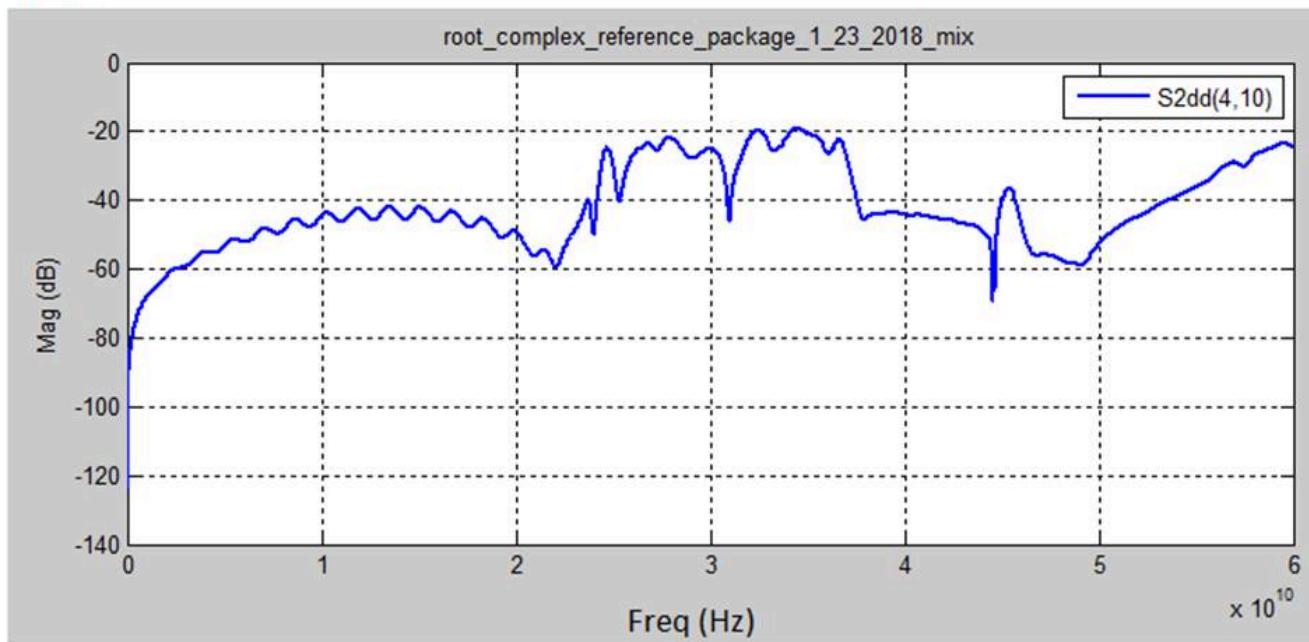


Figure 8-55 NEXT for Root Reference Package (Worst Case) for 32.0 GT/s

FEXT 1

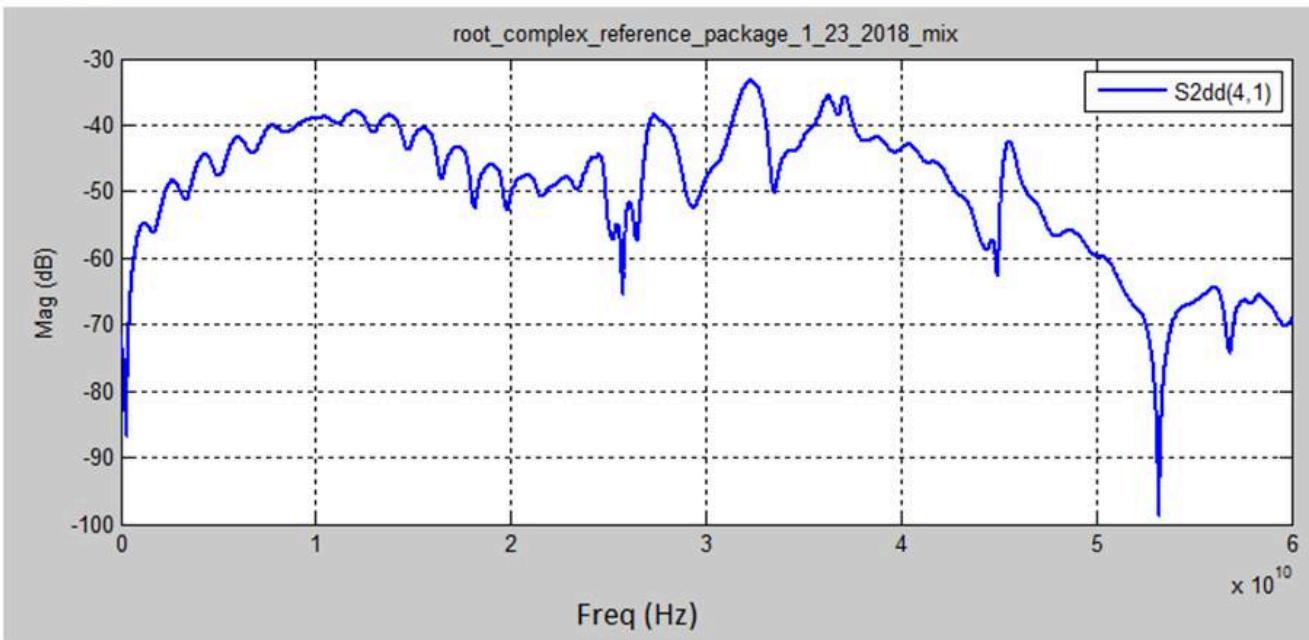


Figure 8-56 FEXT for Root Reference Package (Worst Case) for 32.0 GT/s

Insertion loss

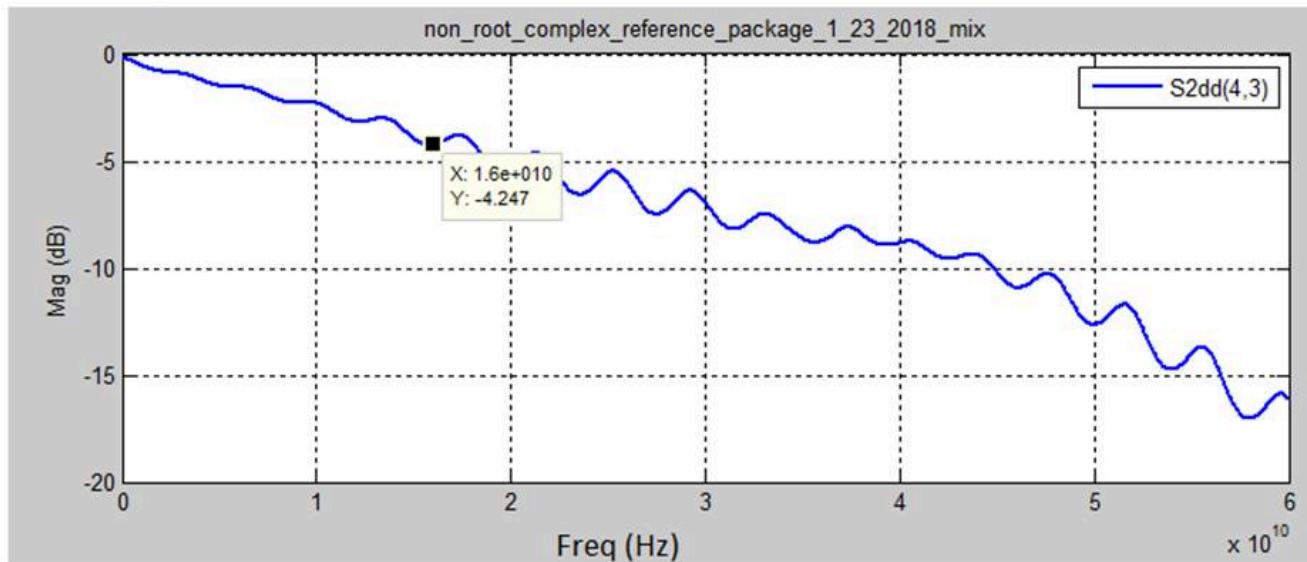


Figure 8-57 Insertion Loss for Non-Root Reference Package for 32.0 GT/s

Return Loss (Board-side)

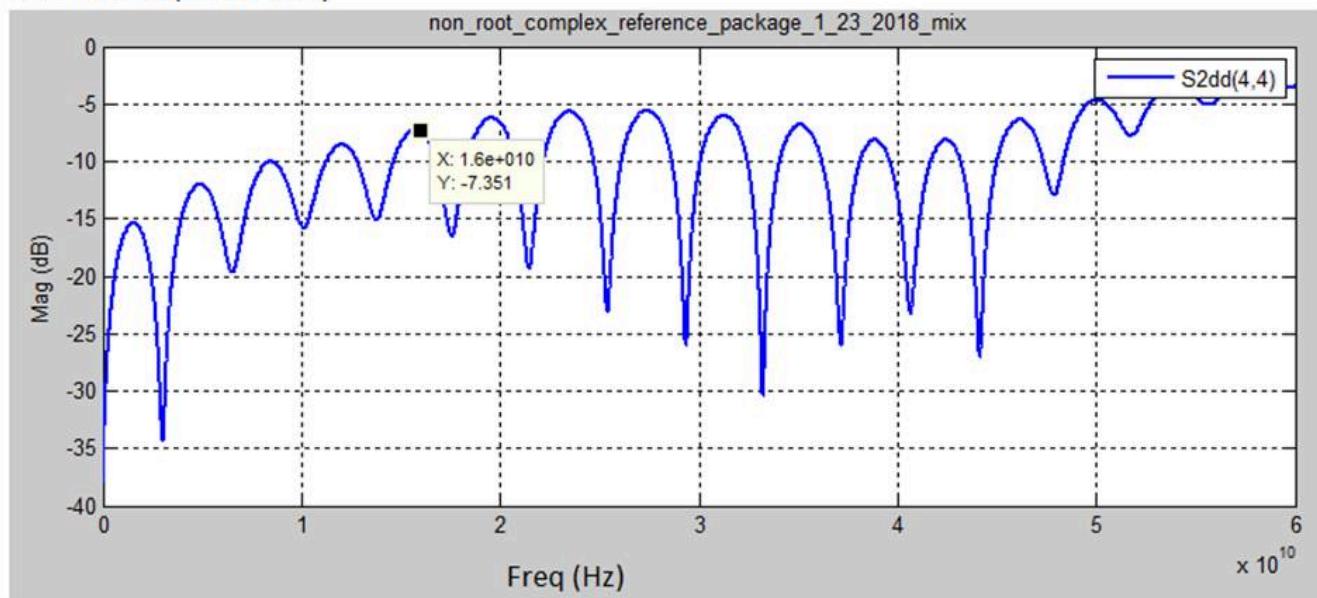


Figure 8-58 Return Loss for Non-Root Reference Package for 32.0 GT/s

NEXT 1

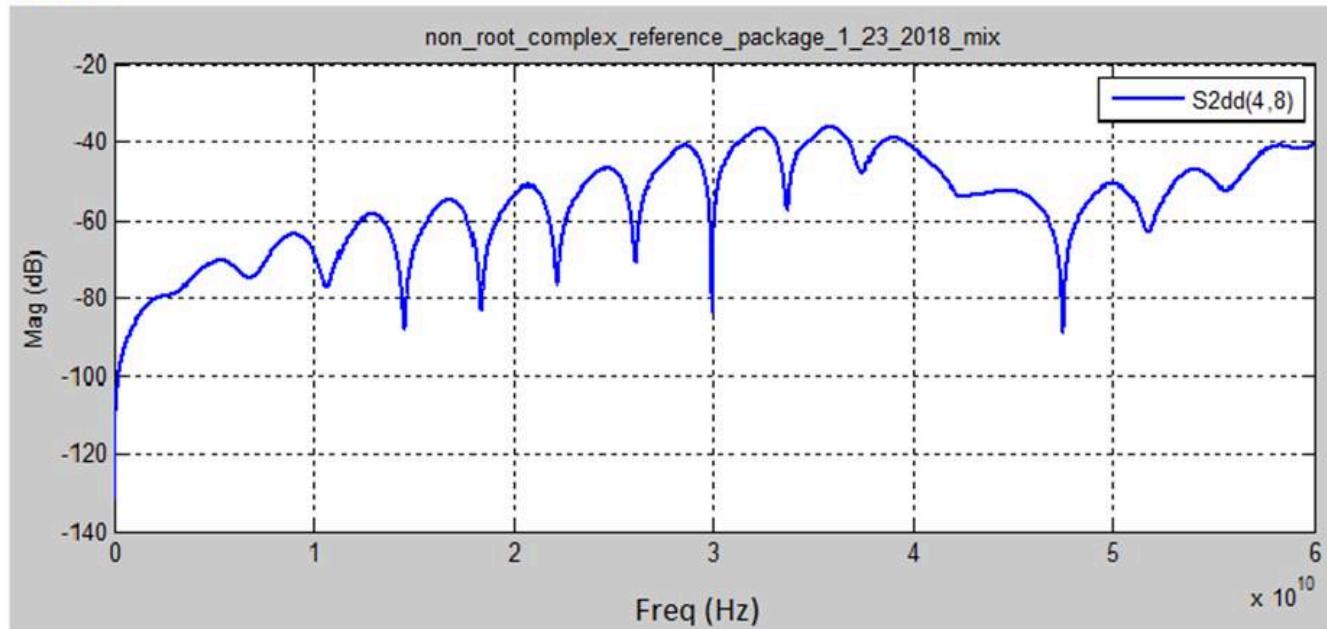


Figure 8-59 NEXT for Non-Root Reference Package (Worst Case) for 32.0 GT/s

FEXT 2 (Die-side)

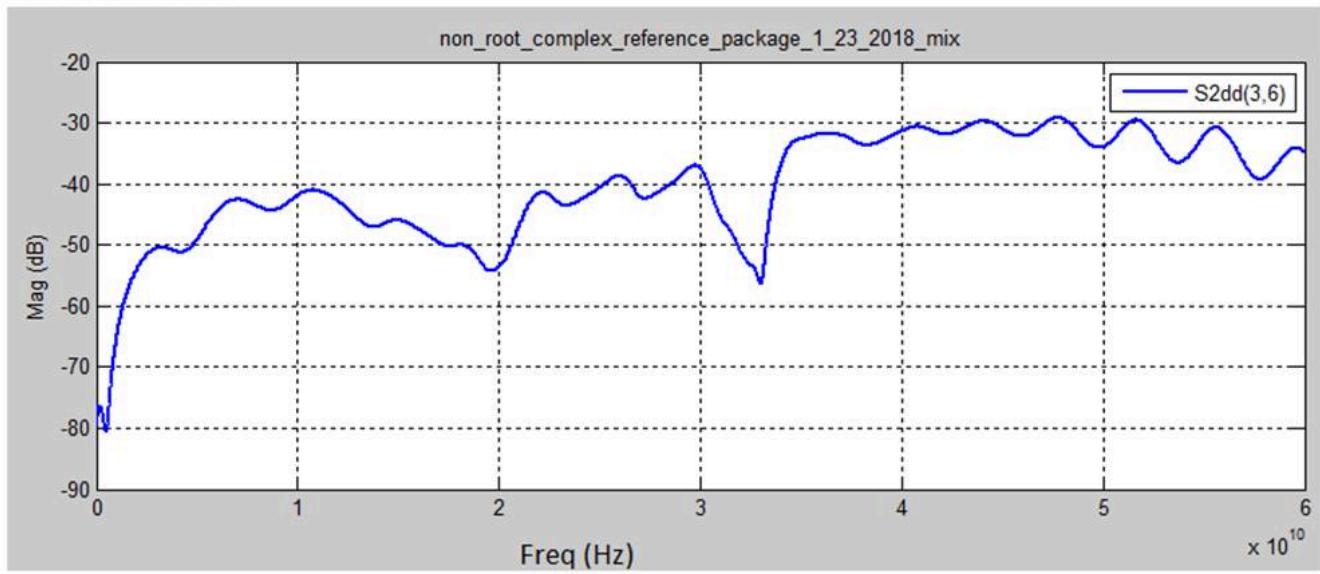
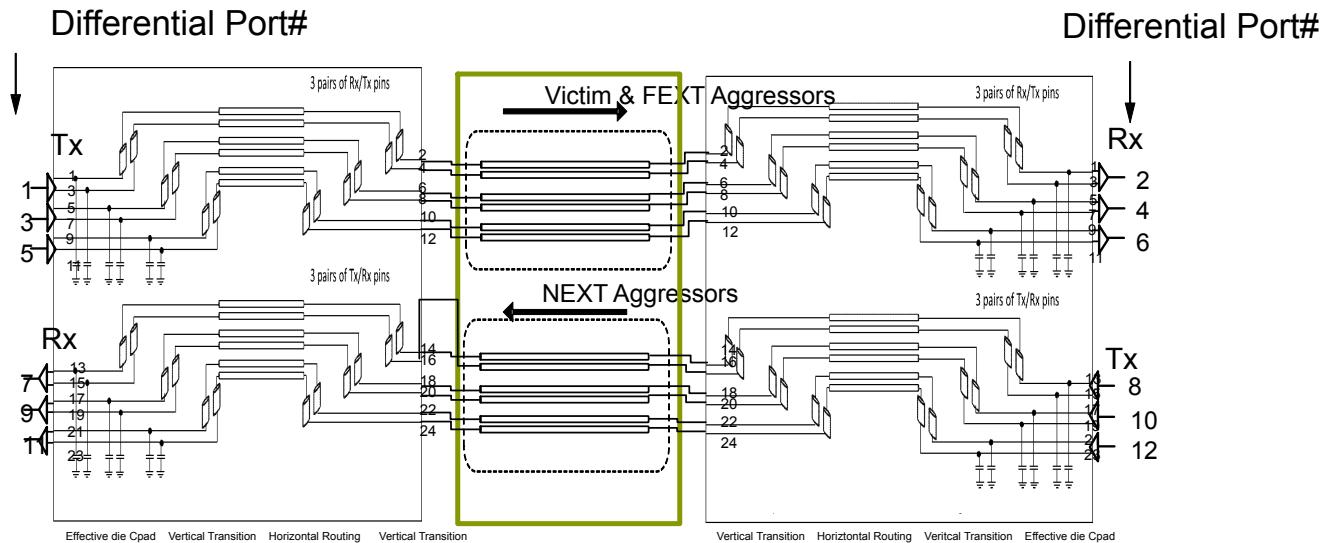


Figure 8-60 FEXT for Non-Root Reference Package (Worst Case) for 32.0 GT/s



Reference Package Channel (Pin to Pin) Reference Package

Figure 8-61 32.0 GT/s Reference Package Port Connections for Pin to Pin Channel Evaluation

Figure 8-61 shows the port connections for using the 32.0 GT/s reference packages to evaluate a pin to pin channel using the channel compliance methodology. Both directions (root transmitting and non-root transmitting) must be evaluated. The lane labeled channel 3 to channel 4 is intended as the worst case victim channel and must be evaluated in both directions. Other channels in the reference package model are intended only for use as cross-talk aggressors (not victim channels).

8.5.1.2 Measuring Package Performance (16.0 GT/s only)

Package insertion loss at 16.0 GT/s is an informative spec parameter. Some implementations at 16.0 GT/s (see Section 8.3.3.11) are allowed to have packages that exceed reference packages in insertion loss and/or cross-talk. Actual package performance must be assessed by performing channel compliance with reference channels provided with the specification on the PCI-SIG website. A set of channel compliance simulations are run on the reference channels with one of the reference packages being replaced by the package that is being evaluated. If the eye height or eye width is smaller for any of the channels with the package that is being evaluated then the package is considered to have worse performance than the reference package. An implementation with a package that has worse performance than the reference package must use the implementation package model in the channel compliance methodology and may optionally use the implementation package in the Receiver stressed eye calibration. Note that form factor and channel compliance (for a captive channel) overall requirements still need to be met regardless of package characteristics.

8.5.1.3 Simulation Tool Requirements

Channel tolerancing is implemented by means of simulation, where the pass/fail criteria are defined in terms of a time domain eye diagram. The simulation tool must accept a prescribed set of inputs, including the channel under consideration and then simulate based upon a set of post processing requirements. This specification does not stipulate the use of any specific tool for simulating channels. However any simulation tool must meet the following requirements.

8.5.1.3.1 Simulation Tool Chain Inputs

- Channel characteristics defined as s-parameters or equivalent model. The model must include the victim differential Lane plus as many aggressors as required to accurately capture crosstalk. In most cases this will be between 2 and 4 additional differential Lanes. Note that 32.0 GT/s is most likely to require additional aggressors to accurately capture worst case cross-talk and most likely to require several NEXT aggressors to capture crosstalk accurately.
- Behavioral Root and Non-Root package models. The models will be included as part of the specification in the form of s-parameter files (see [Section 8.5.1.1](#)).
- Transmitter Jitter and voltage: The voltage and jitter parameters input to the simulator may be directly obtained from a combination of the Transmitter and Refclk jitter. Since these parameters are fixed the simulation tool may choose to hard code their values.
- Transmitter and Receiver Termination Impedance: The simulator shall use a $2 \times 50 \Omega$ termination for both the Transmitter and Receiver. This value matches the assumptions which are implicit in generating and measuring the stressed eye for Rx tolerancing.

8.5.1.3.2 Processing Steps

- Time domain representation of the end-to-end connectivity: Included are the behavioral Tx and Rx packages and the channel under test.
- Tx voltage and jitter: Voltage and jitter parameters defined for the Transmitter, but have been recalculated to properly comprehend high and low frequency jitter components, and also include Refclk jitter contributions.
- Behavioral Transmitter Equalization: The simulator shall replicate the Transmitter equalization capabilities defined in the Transmitter section.
- Behavioral Rx CTLE: The simulation tool shall implement a behavioral CTLE that replicates the CTLE function employed for Rx tolerancing.
- Behavioral DFE: The simulation tool shall implement a 1-tap (8.0 GT/s), 2-tap (16.0 GT/s) or 3 tap DFE (32.0 GT/s), where the dynamic range for the feedback coefficient is defined in [Section 8.4.1.10](#) .
- Optimizing Tx equalization and Rx DFE/CTLE settings: The simulation tool shall implement an optimization algorithm that selects the combination of Tx equalization and Rx CTLE and DFE settings that yields a maximum value for the eye height (at the data sample point) multiplied by the eye width at the far end of the channel. For details refer to [Section 8.4.1.8](#) .
- Statistical Treatment of jitter: In order to avoid overestimating the effect of channel-data and channel-jitter interactions, the tool shall use a statistical analysis of these parameters to generate voltage/jitter eye margins.

8.5.1.3.3 Simulation Tool Outputs

Output eye parameters: The simulator shall generate a statistically defined output that displays the eye width and eye height. EH will be measured as the peak eye height at the data sample location, while EW shall be measured at the zero crossing line. Additionally the simulator shall have the capability to adjust the data sample point by ± 0.1 UI from the mean center of the UI for 8.0 and 16.0 GT/s as shown in [Figure 8-63](#) . For 32.0 GT/s the the simulator shall adjust the sample point up to 0.30 UI to the left of the mean center of the UI sample position in 0.05 UI increments, computing the DFE coefficients for each sample location and selecting the result producing the maximum value for the eye height (at the data sample point) multiplied by the eye width.

8.5.1.3.4 Open Source Simulation Tool

An open source simulation tool shall be provided with the specification as design collateral. The tool will provide a turnkey capability, where the user provides the channel characteristics at the Receiver's die pad as step responses, and the tool calculates a statistical eye showing pass/fail.

8.5.1.4 Behavioral Transmitter Parameters

8.5.1.4.1 Deriving Voltage and Jitter Parameters

This section is for informative purposes. The voltage and jitter parameters may be derived from the Transmitter voltage and jitter parameters, but are referenced to the die pad. This is necessary to allow the channel simulation to include a behavioral Tx package and drive the package from the die pads. Additionally, the Tj terms must be decomposed into separate Rj and DjDD terms.

- $V_{TX-CH-FS-NO-EQ}$ and $V_{TX-CH-RS-NO-EQ}$: These two parameters define the minimum peak-peak voltage corresponding to Vd in Figure 8-5.
- The jitter parameters are derived based on the following set of equations. Algebraic manipulation is used to extract the Rj implicitly defined by the combination of Tj and DjDD terms. The following numbers are based on 8.0 GT/s Tx jitter parameters based on values specified in Table 8-6. The same approach is used to extract jitter parameters for 2.5, 5.0, 16.0, and 32.0 GT/s where it is assumed that maximum data rate supported by the PCIe 5.0 device is 32.0 GT/s and the jitter values in Table 8-6 are used in the extraction process.

$$jit_hfrj_nui = (T_{TX-UTJ} - T_{TX-UDJ-DD})/14.06 = 1.11\text{ps}$$

$$T_{TX-CH-UPW-RJ} = (T_{TX-UPWJ-TJ} - T_{TXUPWJ-DJDD})/14.06 = 1.00\text{ps}$$

$$T_{TX-CH-UPW-DJ} = T_{TXUPWJ-DJDD} = 10.0\text{ps}$$

$$T_{TX-CH-URJ} = \sqrt{(jit_hfrj_nui)^2 - (T_{TX-CH-UPW-RJ} * 0.707)^2 + T_{REFCLK-RMS}^2} = 1.31\text{ps}$$

$$T_{TX-CH-UDJDD} = T_{TX-UDJ-DD} - (T_{TXUPWJ-DJDD})/2 = 7.00\text{ps}$$

A-0840A

Figure 8-62 Example Derivation of 8.0 GT/s Jitter Parameters for Table 8-13

A channel must be tested at all data rates, with the corresponding Tx jitter parameters, that it is intended to support during normal operation. For example, a channel intended to support a max data rate of 8.0 GT/s must be tested at 2.5, 5.0, and 8.0 GT/s.

Table 8-13 Jitter/Voltage Parameters for Channel Tolerancing

Symbol	Parameter	Value	Units	Notes
$V_{TX-CH-FS-NO-EQ}$	Full swing Tx voltage	804	mVPP	Full swing, No Tx Eq.
$V_{TX-CH-RS-NO-EQ}$	Reduced swing Tx voltage	402	mVPP	Reduced swing, No Tx Eq.

2.5 GT/s Jitter Parameters and Voltage Parameters

$T_{TX-CH-URJ-2.5G}$	Tx uncorrelated Rj	3.45	ps RMS	See Note 1
----------------------	--------------------	------	--------	------------

Symbol	Parameter	Value	Units	Notes
$T_{TX-CH-UDJDD-2.5G}$	Tx uncorrelated DjDD	20	ps PP	
$T_{TX-CH-UPW-RJ-2.5G}$	Uncorrelated PW Rj	1.42	ps RMS	See Note 2
$T_{TX-CH-UPW-DJ-2.5G}$	PW DDj	80	ps PP	
$T_{TX-DIEPAD-EDGERATE-2.5G}$	Signal edge rate at behavioral Tx die pad	140	ps	Measured 10% to 90% using a gaussian lowpass filter to shape the edge. See Note 3.

5.0 GT/s Jitter Parameters and Voltage Parameters

$T_{TX-CH-URJ-5G}$	Tx uncorrelated Rj	3.45	ps RMS	See Note 1
$T_{TX-CH-UDJDD-5G}$	Tx uncorrelated DjDD	20-	ps PP	
$T_{TX-CH-UPW-RJ-5G}$	Uncorrelated PW Rj	1.42	ps RMS	
$T_{TX-CH-UPW-DJ-5G}$	PW DDj	40	ps PP	See Note 2.
$T_{TX-DIEPAD-EDGERATE-5G}$	Signal edge rate at behavioral Tx die pad	70	ps	Measured 10% to 90% using a gaussian lowpass filter to shape the edge. See Note 3.

8.0 GT/s Jitter Parameters and Voltage Parameters

$T_{TX-CH-URJ-8G}$	Tx uncorrelated Rj	1.31	ps RMS	No DDj of HF jitter. See Note 1.
$T_{TX-CH-UDJDD-8G}$	Tx uncorrelated DjDD	7.0	ps PP	No DDj of HF jitter
$T_{TX-CH-UPW-RJ-8G}$	Uncorrelated PW Rj	1.0	ps RMS	
$T_{TX-CH-UPW-DJ-8G}$	PW DDj	10	ps PP	See Note 2.
$T_{TX-DIEPAD-EDGERATE-8G}$	Signal edge rate at behavioral Tx die pad	43.75	ps	Measured 10% to 90% using a gaussian lowpass filter to shape the edge. See Note 3.

16.0 GT/s Jitter Parameters and Voltage Parameters

$T_{TX-CH-URJ-16G}$	Tx uncorrelated Rj	0.71	ps RMS	See Note 1.
$T_{TX-CH-UDJDD-16G}$	Tx uncorrelated DjDD	3.75	ps PP	
$T_{TX-CH-UPW-RJ-16G}$	Uncorrelated PW Rj	0.54	ps RMS	
$T_{TX-CH-UPW-DJ-16G}$	PW DDj	5.0	ps PP	See Note 2.
$T_{TX-DIEPAD-EDGERATE-16G}$	Signal edge rate at behavioral Tx die pad	21.875	ps	Measured 10% to 90% using a gaussian lowpass filter to shape the edge. See Note 3.

32.0 GT/s Jitter Parameters and Voltage Parameters

$T_{TX-CH-URJ-32G}$	Tx uncorrelated Rj	0.276	ps RMS	See Note 1.
$T_{TX-CH-UDJDD-32G}$	Tx uncorrelated DjDD	1.875	ps PP	
$T_{TX-CH-UPW-RJ-32G}$	Uncorrelated PW Rj	0.27	ps RMS	
$T_{TX-CH-UPW-DJ-32G}$	PW DDj	2.5	ps PP	See Note 2.

Symbol	Parameter	Value	Units	Notes
$T_{TX-DIEPAD-EDGERATE-32G}$	Signal edge rate at behavioral Tx die pad	10.94	ps	Measured 10% to 90% using a gaussian lowpass filter to shape the edge. See Note 3.

Notes:

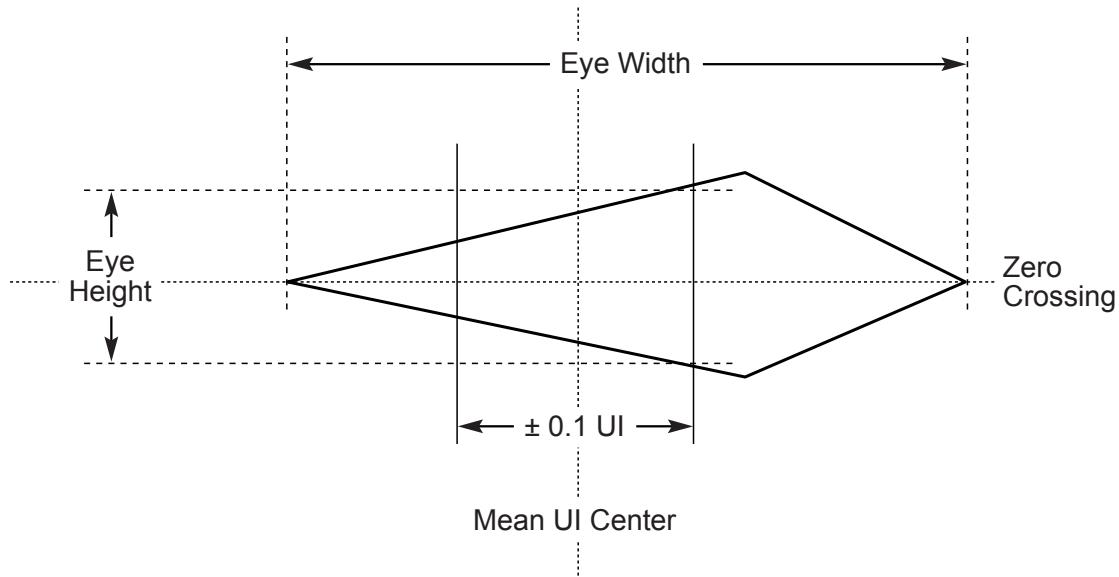
1. Includes low frequency (non F/2) Rj components from the Transmitter and Rj from the Refclk.
2. Applied on a per edge basis as a dual Dirac model.
3. Does not include parasitic die pad capacitance. See [Figure 8-50](#) for details of behavioral package.

8.5.1.4.2 Optimizing Tx/Rx Equalization (8.0 GT/s, 16.0 GT/s and 32.0 GT/s only)

The behavioral receiver selects the combination of Transmitter Equalization, CTLE, DFE and sample location (32.0 GT/s only) that produces the optimal eye area (eye width multiplied by eye height).

8.5.1.4.3 Pass/Fail Eye Characteristics

The output of the simulation tool shall be in the form of pass/fail characteristics as defined by an eye mask as shown in [Figure 8-63](#). EH and EW must meet respectively the voltage and jitter parameters defined in [Table 8-14](#). Eye margins are defined at the die pad of the Receiver after the appropriate Tx and Rx equalization algorithms have been applied. In the case where the channel is being designed for a specific pair of silicon devices and the package models of these silicon devices including cross-talk aggressors are known the actual device packages may be used instead of the reference packages in running the pad to pad channel pass/fail compliance simulations.



A-0841A

Figure 8-63 EH, EW Mask

Note that the pass/fail EH and EW limits shown in [Figure 8-63](#) are identical to the limits defined for Rx testing in [Table 8-9](#) for 8.0 and 16.0 GT/s. For 32.0 the pass/fail EH and EW limits are still identical but they are computed at the optimal sample location. For 2.5 and 5.0 GT/s the limits for Rx testing are referenced to the package pins and the limits for channel tolerancing in this table are referenced to the Receiver pad after applying the same reference package used for 8.0 GT/s channel tolerancing.

Table 8-14 Channel Tolerancing Eye Mask Values

Symbol	Parameter	Value	Units	Comments
2.5 GT/s Eye Margins				
$V_{RX-CH-EH-2.5G}$	Eye height	<130 (min)	mVPP	Eye height at $BER=10^{-12}$. Note 1
$T_{RX-CH-EW-2.5G}$	Eye width at zero crossing	<0.35 (min)	UI	Eye width at $BER=10^{-12}$
$T_{RX-DS-OFFSET-2.5G}$	Peak EH offset from UI center	± 0.1	UI	See Figure 8-63 for details.
5.0 GT/s Eye Margins				
$V_{RX-CH-EH-5G}$	Eye height	< 85 (min)	mVPP	Eye height at $BER=10^{-12}$. Note 1
$T_{RX-CH-EW-5G}$	Eye width at zero crossing	<0.30 (min)	UI	Eye width at $BER=10^{-12}$
$T_{RX-DS-OFFSET-5G}$	Peak EH offset from UI center	± 0.1	UI	See Figure 8-63 for details.
8.0 GT/s Eye Margins				
$V_{RX-CH-EH-8G}$	Eye height	25 (min)	mVPP	Eye height at $BER=10^{-12}$. Note 1.
$T_{RX-CH-EW-8G}$	Eye width at zero crossing	0.3 (min)	UI	Eye width at $BER=10^{-12}$
$T_{RX-DS-OFFSET-8G}$	Peak EH offset from UI center	± 0.1	UI	See Figure 8-63 for details.
$V_{RX-DFE-D1-8G}$	Range for DFE d ₁ coefficient	± 30	mV	
16.0 GT/s Eye Margins				
$V_{RX-CH-EH-16G}$	Eye height	15 (min)	mVPP	Eye height at $BER=10^{-12}$. Note 1.
$T_{RX-CH-EW-16G}$	Eye width at zero crossing	0.3 (min)	UI	Eye width at $BER=10^{-12}$
$T_{RX-DS-OFFSET-16G}$	Peak EH offset from UI center	± 0.1	UI	See Figure 8-63 for details.
$V_{RX-DFE-D1-16G}$	Range for DFE d ₁ coefficient	± 30	mV	
$V_{RX-DFE-D2-16G}$	Range for DFE d ₂ coefficient	± 20	mV	
32.0 GT/s Eye Margins				

Symbol	Parameter	Value	Units	Comments
$V_{RX-CH-EH-32G}$	Eye height	15 (min)	mVPP	Eye height at BER="10" ⁻¹² , Note 1.
$T_{RX-CH-EW-32G}$	Eye width at zero crossing	0.3 (min)	UI	Eye width at BER="10" ⁻¹²
$T_{RX-DS-OFFSET-32G}$	Peak EH offset from <u>UI</u> center	N/A	UI	See Figure 8-63 for details.
$T_{RX-SAMPLE-OFFSET-32G}$	Max sample location offset to the left from <u>UI</u> center	0.30	UI	Note 2
$T_{RX-SAMPLE-GRANULARITY-32G}$	Granularity for sample location offset	0.05	UI	Note 2
$V_{RX-DFE-D1-32G}$	Range for DFE d ₁ coefficient	Abs(D1)/D0 (cursor amplitude) ≤ 0.8		
$V_{RX-DFE-D2-32G}$	Range for DFE d ₂ coefficient	±20	mV	
$V_{RX-DFE-D3-32G}$	Range for DFE d ₃ coefficient	±20	mV	

Notes:

1. $V_{RX-CH-EH}$ is defined as max EH within an aperture of ±0.1 UI from mean UI center.
2. The optimal eye area is computed at each offset from mean UI center -0.30 UI to mean UI center with the specified granularity.

8.5.1.4.4 Characterizing Channel Common Mode Noise

A channel must meet the common mode requirements as they are defined in the receiver specification. In general, it is not possible to accurately simulate all the channel's common mode noise contributions due to the large number of mechanisms that can generate CM noise, including the Transmitter. Typically channel common mode noise is a budgeted parameter, and the limits defined below assume a budgeting process. The channel's CM limit is defined as the amount of CM noise that a channel can add and still meet the Rx CM limits assuming the worst case Tx CM. This limit is 75 mVPP for EH < 100 mV and 125 mVPP for EH ≥ 100 mVPP.

Note that the Tx and channel CM noise parameters cannot simply be added to obtain the Rx CM limit. This is due to the fact that a channel will attenuate some of high frequency Tx CM noise while propagating Tx LF CM noise through with little loss. The channel may also contribute both high and low frequency CM components of its own.

8.5.1.4.5 Verifying V_{CH-IDLE-DET-DIFF-pp}

$V_{CH-IDLE-DET-DIFF-pp}$ is defined to guarantee that, when a Transmitter issues an EIEOS sequence, the Receiver is guaranteed to detect it. Potentially larger Transmitter equalization boost ratios at 8.0, 16.0 and 32.0 GT/s necessitate that this parameter be verified; this procedure was not necessary for 2.5 or 5.0 GT/s, where the max Transmitter equalization boost is smaller. Defining the launch and detect voltages at the Tx/Rx die pad permits V_{CH-IDLE-DET-DIFF-pp} to be verified with the same channel and Tx/Rx package models used to determine eye margins. It is also acceptable to simulate from Tx pin to Rx pin (excluding the Tx and Rx behavioral package models), in which case the EIEOS and idle detect parameters defined in the Tx and Rx sections are applicable.

Long channels, where $V_{TX-EIEOS-FS}$ is applicable, are characterized by driving the channel under test with the EIEOS pattern and -11.0 dB de-emphasis and zero dB preshoot. For short channels, where $V_{TX-EIEOS-RS}$ is applicable, -4.5 dB of de-emphasis and zero dB of preshoot are applied.

Table 8-15 EIEOS Signaling Parameters

Parameter	Description	Value	Units	Comments
$V_{CH-IDLE-EXIT-pp}$	Idle detect voltage seen at the Rx die pad	172	mVPP	Assuming Rx RTERM of $2 \times 50 \Omega$
$V_{CH-EIEOS-FS-Vb}$	PP voltage during Vb interval at behavioral Tx die pad for full swing signaling	255	mVPP	Assuming Tx RS of $2 \times 50 \Omega$
$V_{CH-EIEOS-RS-Vb}$	PP voltage during Vb interval at behavioral Tx die pad for reduced swing signaling	237	mVPP	Assuming Tx RS of $2 \times 50 \Omega$

8.6 Refclk Specifications

This version of the specification consolidates and streamlines the Refclk requirements. The 2.5 GT/s Refclk parameters are moved from the CEM spec to this spec so that all Refclk parameters for all data rates (2.5, 5.0, 8.0, 16.0, and 32.0 GT/s) are now contained in this subsection.

8.6.1 Refclk Test Setup

The test setup for the Refclk assumes that only the Refclk generator itself is present. Provision is made in the test setup to account for signal degradation that occurs between the pins of the Refclk generator and the Transmitter or Receiver in an actual system. The above described setup emulates the worst case signal degradation that is likely to occur at the pins of a PCI Express device. Note that the Refclk signal is tested into a load that represents the series (open) termination appearing at the Refclk input pins of a PCIe device for all requirements except 32.0 GT/s reference clock jitter. Reference clock jitter measured with a phase noise analyzer, and 32.0 GT/s reference clock jitter measured with an oscilloscope, are tested with the reference clock terminated by 50 Ohm terminations without a channel.

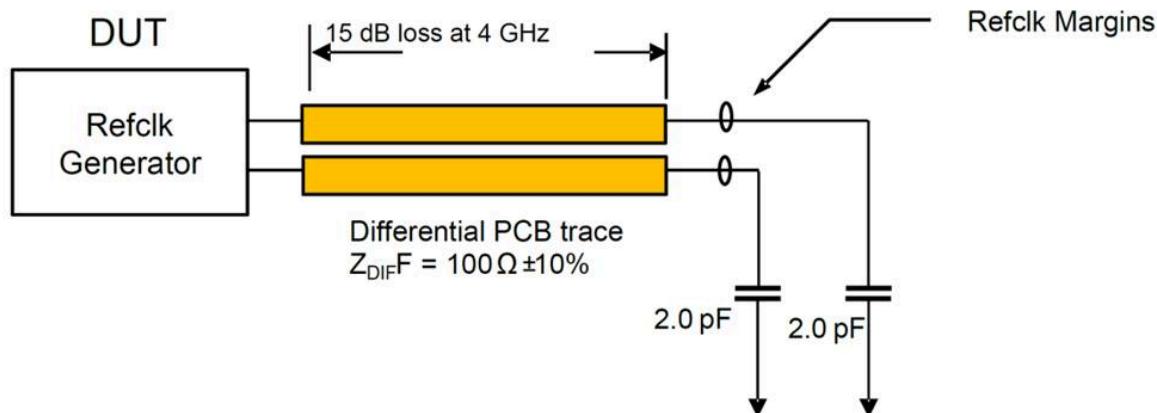


Figure 8-64 Oscilloscope Refclk Test Setup For All Cases Except Jitter at 32.0 GT/s

8.6.2 REFCLK AC Specifications

All specifications in Table 8-16 are to be measured using a test configuration as described in Note 11 with a circuit as shown in Figure 8-64.

Table 8-16 REFCLK DC Specifications and AC Timing Requirements

Symbol	Parameter	100 MHz Input		Unit	Note
		Min	Max		
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150		mV	2
V_{IL}	Differential Input Low Voltage		-150	mV	2
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV	1, 4, 5
V_{CROSS DELTA}	Variation of <u>V_{CROSS}</u> over all rising clock edges		+140	mV	1, 4, 9
V_{RB}	Ring-back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before <u>V_{RB}</u> is allowed	500		ps	2, 12
T_{PERIOD AVG}	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
T_{PERIOD AVG_32G_CC}	Average Clock Period Accuracy for devices that support 32.0 GT/s in CC Mode at any speed	-100	+2600	ppm	2, 10, 13
T_{PERIOD AVG_32G_SRIS}	Average Clock Period Accuracy for devices that support 32.0 GT/s in SRIS Mode at any speed	-100	+1600	ppm	2, 10, 13
T_{PERIOD ABS}	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns	2, 6
T_{PERIOD ABS_32G_CC}	Absolute Period (including Jitter and Spread Spectrum modulation) for devices that support 32.0 GT/s in CC Mode at any speed	9.849	10.201	ns	2, 6
T_{PERIOD ABS_32G_SRIS}	Absolute Period (including Jitter and Spread Spectrum modulation) for devices that support 32.0 GT/s in SRIS Mode at any speed	9.849	10.181	ns	2, 6
T_{CCJITTER}	Cycle to Cycle jitter		150	ps	2
V_{MAX}	Absolute Max input voltage		+1.15	V	1, 7
V_{MIN}	Absolute Min input voltage		-0.3	V	1, 8

Symbol	Parameter	100 MHz Input		Unit	Note
		Min	Max		
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching		20	%	1, 14
Z_{c-DC}	Clock source DC impedance	40	60	W	1, 11

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See [Figure 8-69](#).
4. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See [Figure 8-65](#).
5. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See [Figure 8-65](#).
6. Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation. See [Figure 8-68](#).
7. Defined as the maximum instantaneous voltage including overshoot. See [Figure 8-65](#).
8. Defined as the minimum instantaneous voltage including undershoot. See [Figure 8-65](#).
9. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system. See [Figure 8-66](#).
10. Note deleted.
11. REFCLK+ and REFCLK- are to be measured at the load capacitors C_L . Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load $C_L = 2 \text{ pF}$.
12. T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150 \text{ mV}$ differential voltage after rising/falling edges before it is allowed to droop back into the $V_{RB} \pm 100 \text{ mV}$ differential range. See [Figure 8-70](#).
13. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is $1/1,000,000^{\text{th}}$ of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz / $PPM \times 300 \text{ PPM} = 30 \text{ kHz}$. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.
14. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a $\pm 75 \text{ mV}$ window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 8-67](#).

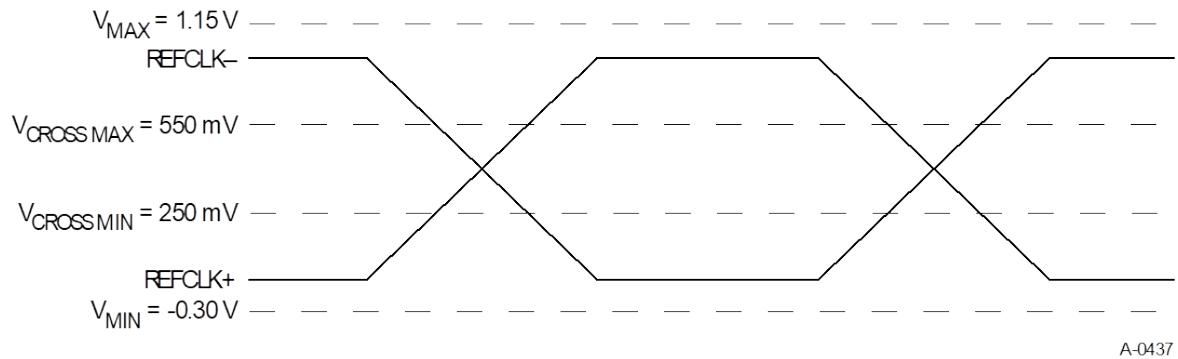


Figure 8-65 Single-Ended Measurement Points for Absolute Cross Point and Swing

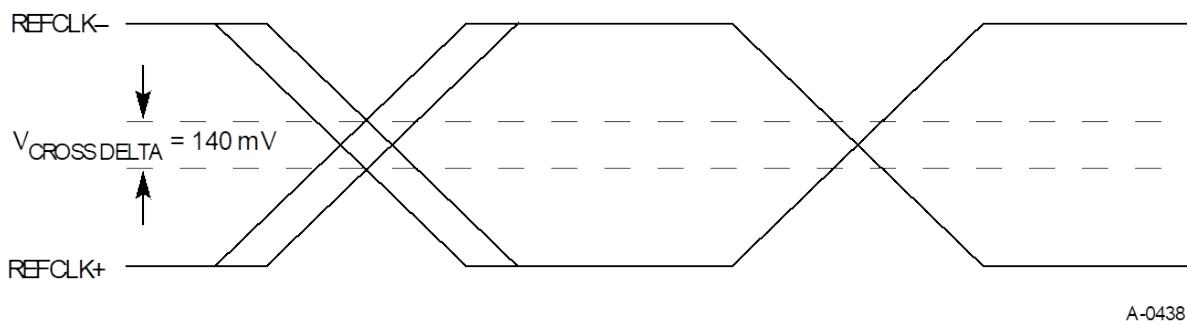


Figure 8-66 Single-Ended Measurement Points for Delta Cross Point

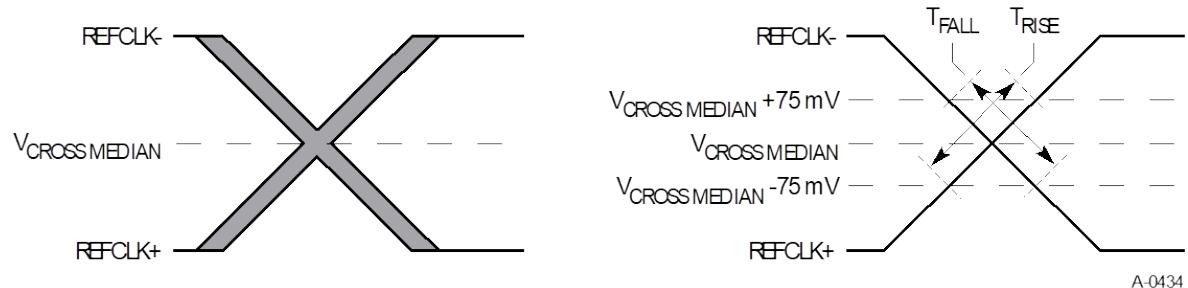


Figure 8-67 Single-Ended Measurement Points for Rise and Fall Time Matching

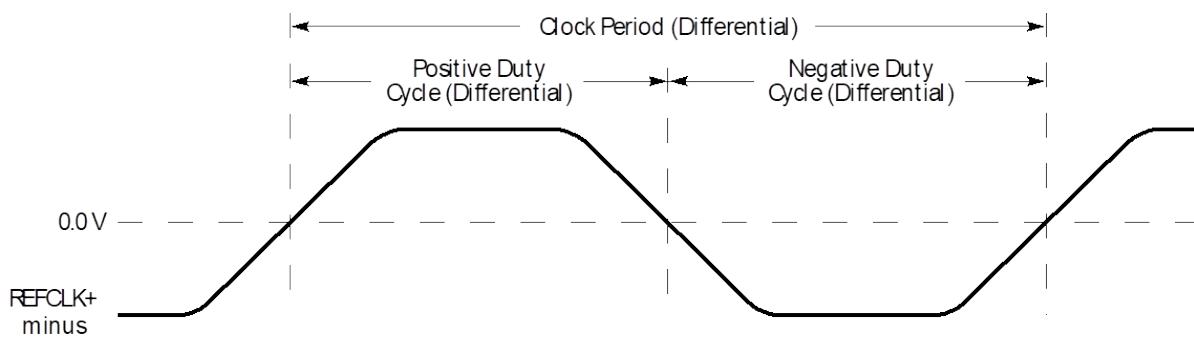


Figure 8-68 Differential Measurement Points for Duty Cycle and Period

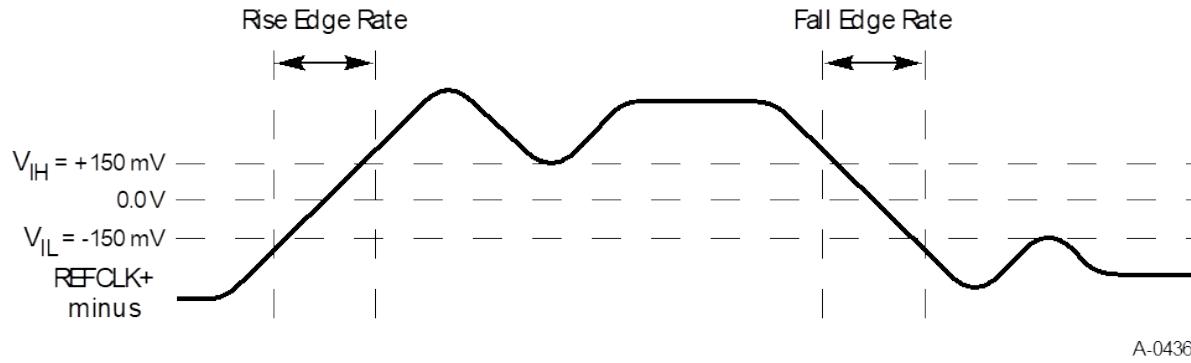


Figure 8-69 Differential Measurement Points for Rise and Fall Time

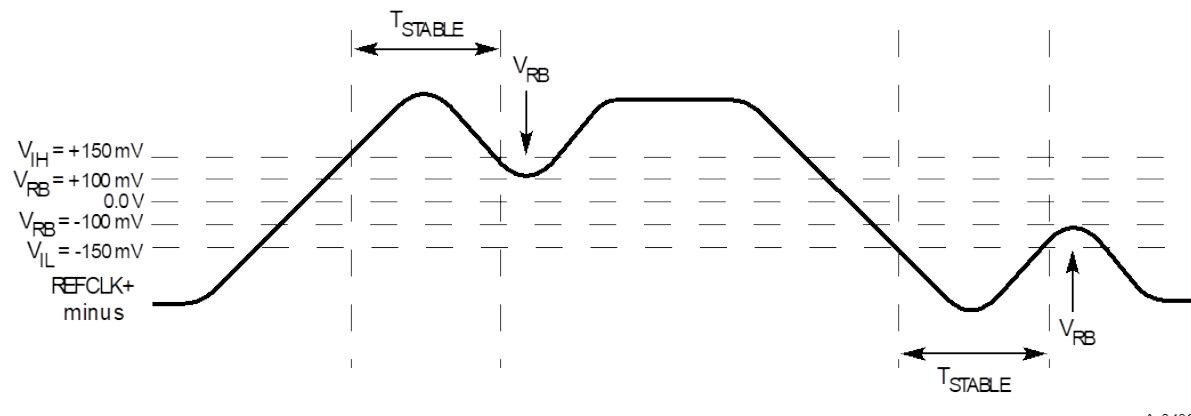


Figure 8-70 Differential Measurement Points for Ringback

8.6.3 Data Rate Independent Refclk Parameters

A number of Refclk parameters are data rate independent and are listed in the table below. $T_{TRANSPORT-DELAY}$ is defined in Section 8.6.6 and illustrated in Figure 8-73. It is relevant only for the Common Refclk architecture. For the SRIS mode the source of the SSC modulation is implementation dependent.

Table 8-17 Data Rate Independent Refclk Parameters

Symbol	Description	Limits	Units	Notes
F_{REFCLK}	Refclk Frequency	99.97 (min) 100.03 (max)	MHz	
F_{REFCLK_32G}	Refclk Frequency for devices that support 32.0 GT/s	99.99 (min) 100.01 (max)	MHz	
F_{SSC}	SSC frequency range	30 (min) 33 (max)	kHz	3
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-0.5 (min) 0.0 (max)	%	3
$T_{SSC-FREQ-DEVIATION_32G_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	-0.3 (min) 0.0 (max)	%	3

Symbol	Description	Limits	Units	Notes
$T_{TRANSPORT-DELAY}$	Tx-Rx transport delay	12 (max)	ns	1, 4
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250	ppm/ μs	2, 3

Notes:

1. Parameter is relevant only for Common Refclk architecture.
2. Measurement is made over 0.5 μs time interval with a 1st order LPF with an f_c of 60x the modulation frequency.
3. When testing the a device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.
4. There are form factors (for example topologies including long cables) that may exceed the transport delay limit. Extra jitter from the large transport delay must be accounted by these form factor specifications.

8.6.3.1 Low Frequency Refclk Jitter Limits

Refclks supporting SSC must meet an additional jitter limit over a range of low frequencies. Low frequency Refclk jitter limits are defined as a continuous, piece-wise linear graph from 30 kHz to 500 kHz as shown below. Unfiltered Refclk phase jitter must fall below this graph over the frequency range of interest.

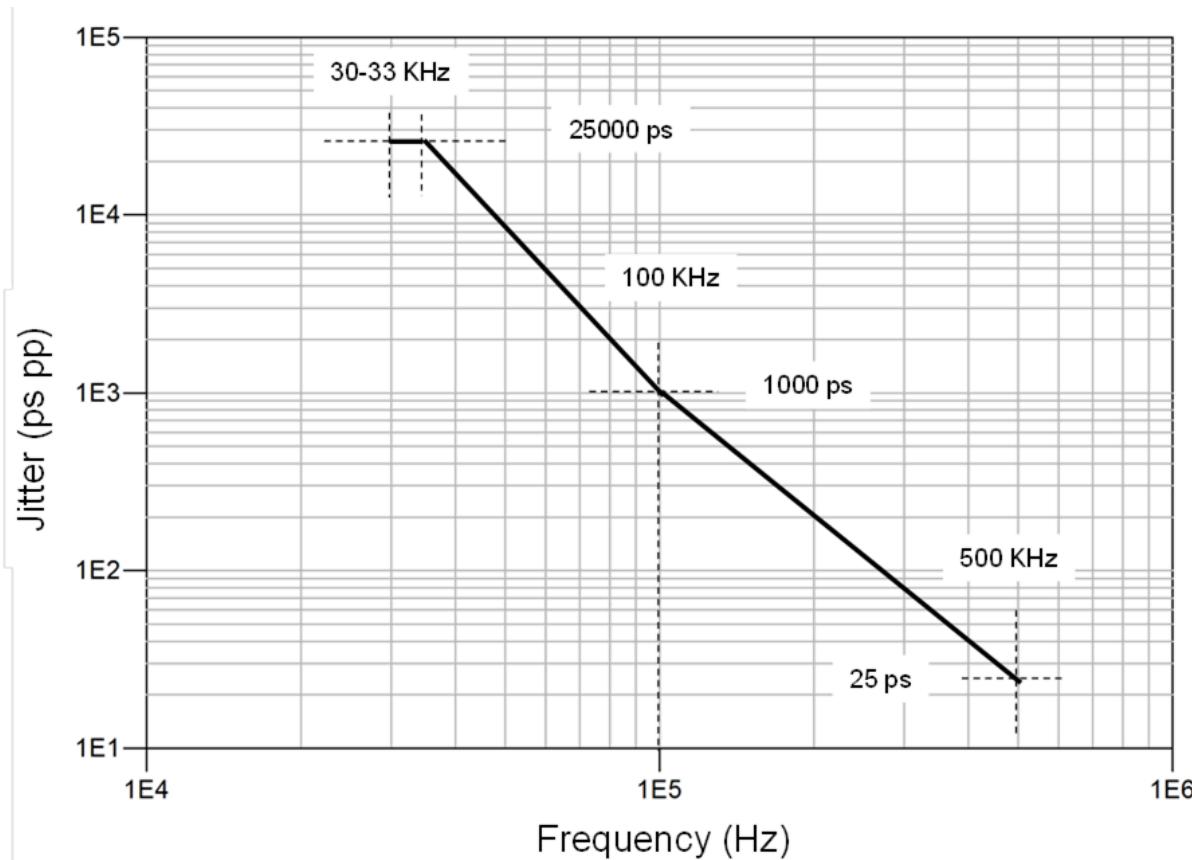


Figure 8-71 Limits for phase jitter from the Reference with 5000 ppm SSC

8.6.4 Refclk Architectures Supported

Two Refclk architectures are supported: **Common Refclk (CC)** and **Independent Refclk (IR)**. The CC clock architecture is described in terms of its topology and its corresponding jitter transfer function based on PLL and CDR characteristics. Finally, the corresponding Refclk jitter limits are given for each data rate. The jitter transfer function and corresponding jitter limits are not defined for the IR clock architecture. It is up to the implementer to trade off reference clock jitter and PLL characteristics to ensure that Transmitter requirements are met in the IR clocking mode.

8.6.5 Filtering Functions Applied to Raw Data

Two types of filtering are applied to the raw Refclk data. The first, edge filtering, minimizes the measurement-induced jitter due to the finite sampling rate of the test equipment. The second, replicates the jitter filtering that is inherent in the combination of Tx/Rx PLLs, the Rx CDR and (where applicable) the transport delay. The combination of the preceding filter functions yields the effective Refclk jitter as it appears at the sample latch of the Receiver.

Note that the PLL and CDR filter functions represent minimally capable approximations to actual Receiver implementations and are not intended to define actual PLL or CDR implementations.

8.6.5.1 PLL Filter Transfer Function Example

All PLLs are behaviorally modeled with a second order transfer function, $H(s)$, as defined in [Figure 8-73](#). The parameters defining the transfer function include the damping factor ζ and the natural frequency ω_n .

The relation between the 2nd order PLL (lowpass) natural frequency, ω_n and the 3 dB point ω_{3dB} , is given by the following expression:

$$\frac{\omega_{3dB}}{\omega_n} = \sqrt{\sqrt{1/(2\zeta^2 + 1)^2 + 1} + 2\zeta^2 + 1}$$

Equation 8-8 Relationship between 2nd order PLL natural frequency and 3 dB point

The following plot of a 2nd order PLL illustrates the transfer function with an f_{3dB} of 5.0 MHz and 1.0 dB of peaking. This corresponds to $\zeta = 1.15$, and $\omega_n = 11.55$ Mrad/sec.

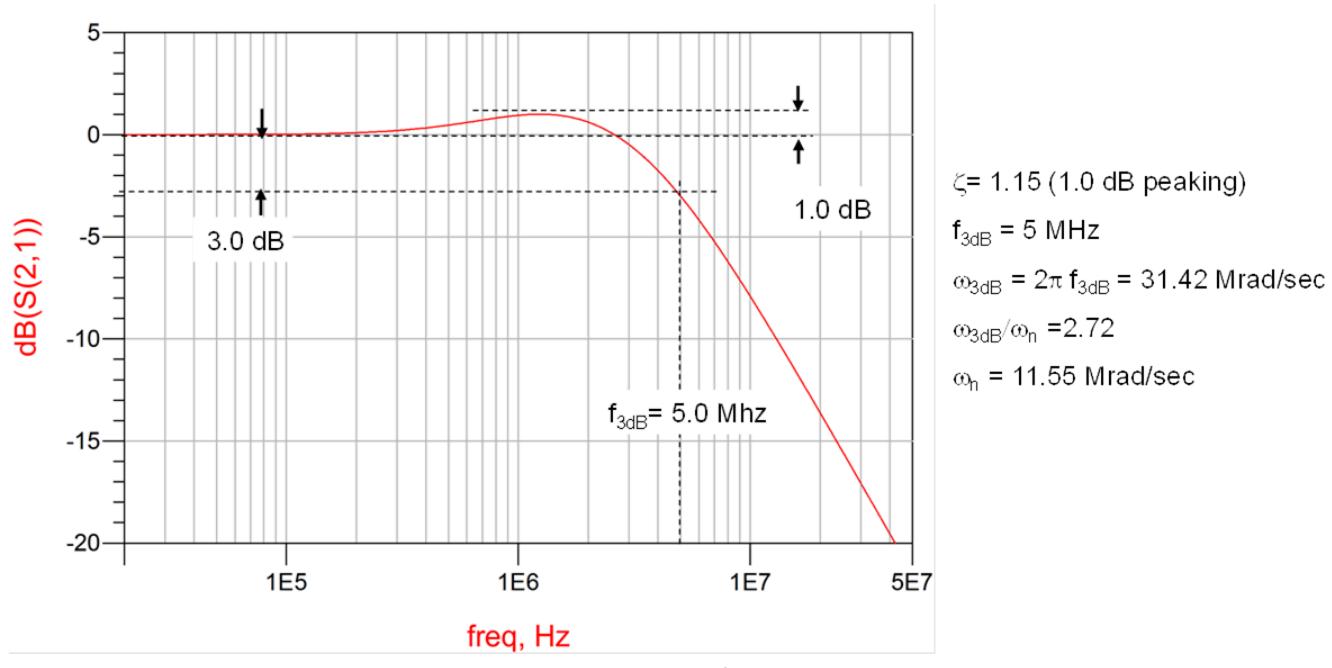


Figure 8-72 5 MHz PLL Transfer Function Example

8.6.5.2 CDR Transfer Function Examples

Depending on the Refclk architecture and data rate, either a first or higher order transfer function shall be used as a behavioral CDR bounding limit.

For behavioral CDR functions refer to [Section 8.3.5.5](#)

8.6.6 Common Refclk Rx Architecture (CC)

This architecture utilizes a single Refclk source that is distributed to both the Tx and Rx. Most of the SSC jitter sourced by the Refclk is propagated equally through Tx and Rx PLLs, and so intrinsically tracks LF jitter. This is particularly true for SSC which tends to be low frequency. Figure 8-73 illustrates the Common Refclk Rx architecture, showing key jitter, delay, and PLL and CDR transfer function sources for all data rates except 32.0 GT/s. At 32.0 GT/s the only difference in the figure is Behavioral CDR transfer function as defined in Section 8.3.5.5. The amount of jitter appearing at the CDR is then defined by the difference function between the Tx and Rx PLLs multiplied by the CDR highpass characteristic.

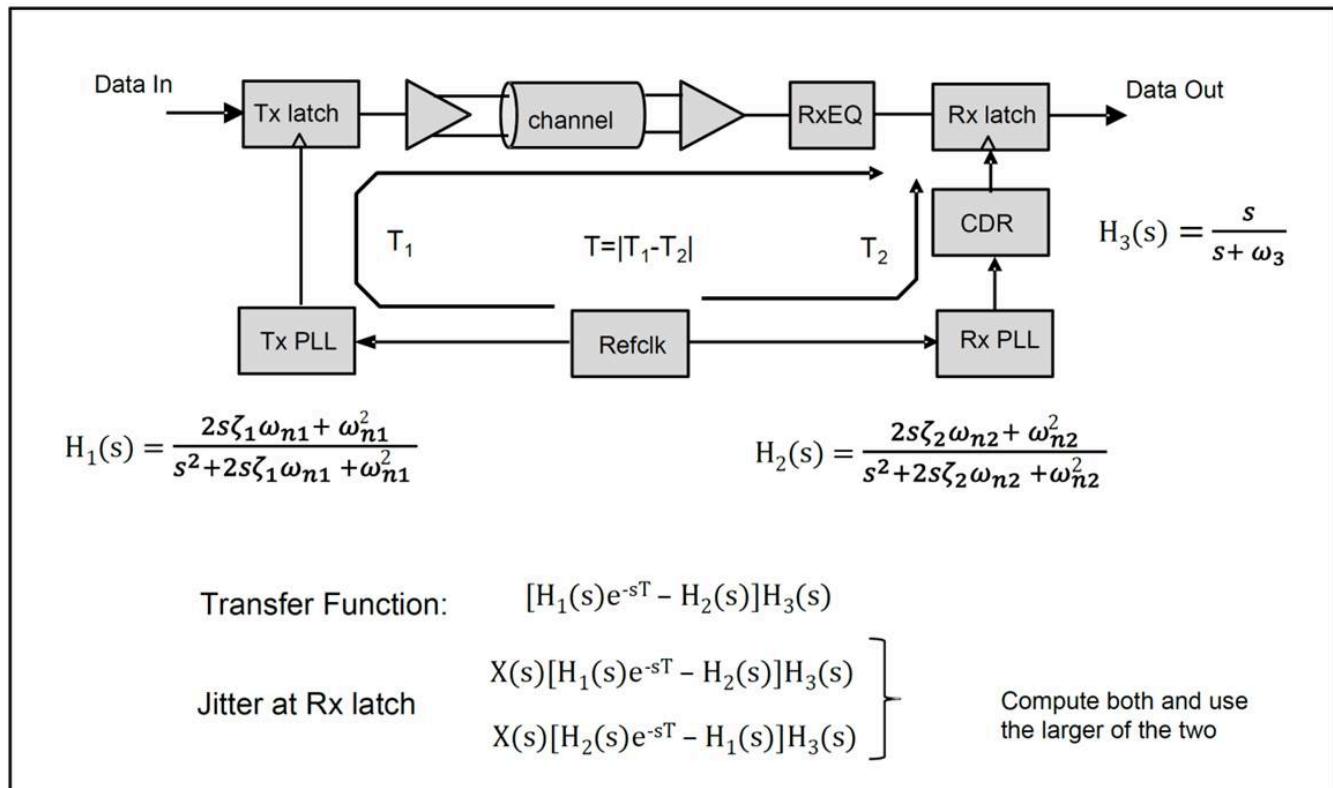


Figure 8-73 Common Refclk Rx Architecture for all Data Rates Except 32.0 GT/s

Based on the above clock architecture, it is possible to define a difference function that corresponds to the worst case mismatch between Tx and Rx PLLs. Second order PLL transfer functions are assumed, (even though most PLL transfer functions are 3rd order or higher), since a 2nd order function tends to yield a slightly conservative difference function vis-a-vis most actual PLL implementations.

In the Common Refclk Rx architecture it is also necessary to comprehend a maximum Transmitter to Receiver transport delay difference. This delay delta is illustrated in Figure 8-73 and represents the delay difference between the Transmitter data and recovered Receiver clock as seen at the inputs to the receive's data latch.

8.6.6.1 Determining the Number of PLL BW and peaking Combinations

A Tx or Rx PLL is defined by the combination of min/max bandwidth and peaking, making for a total of four possible limits. In the CC architecture both the Tx and Rx PLLs contribute to the jitter transfer function. At 2.5 GT/s only one set of

BW/peaking limits is defined. If the combinations for the Tx and Rx PLLs limits are defined by the sets $(A_{TX}, B_{TX}, C_{TX}, D_{TX})$, $(A_{RX}, B_{RX}, C_{RX}, D_{RX})$ then it's easily demonstrated that there are a total of ten ways of selecting one element from each set. The delay term e^{-ST} can be applied to either $H_1(s)$ or $H_2(s)$, adding another six possibilities. Only six, as opposed to ten, terms are added when the delay term is considered because terms like A_{TX}, A_{RX} , are identical to A_{RX}, A_{TX} .

At 5.0 GT/s and higher data rates, two possible sets of limits of PLL bandwidth and peaking are defined, which may be defined by the sets ($A_{TX}, B_{TX}, C_{TX}, D_{TX}$) and ($E_{RX}, F_{RX}, G_{RX}, H_{RX}$). In this case the number of unique 2-element combinations from the above 4-element sets is 36, which increases to 64 when the delay term is considered.

8.6.6.2 CDR and PLL BW and Peaking Limits for Common Refclk

The Common Refclk architecture filter function is dependent on the difference function defined by the BW and peaking of Tx and the Rx PLLs, plus the CDR high-pass characteristic. It is necessary to consider all corner case combinations of Tx and Rx PLL peaking and bandwidth plus the CDR characteristics at their minimum and maximum peaking values.

This procedure must be applied to all five data rates.

Figure 8-74 lists the PLL BW and CDR BW/peaking values that need to be applied as filter functions for 2.5 GT/s data rates. It is necessary to assign a min and a max value for peaking for the 2.5 GT/s PLL. The values of 0.01 dB and 3.0 dB represent best estimates of realistic PLL implementations.

The minimum peaking for 2.5 and 5.0 GT/s has been reduced to 0.01 dB to bring it into line with the 8.0 and 16.0 GT/s cases. Note that the Rx CDR is 1st order, so its natural frequency, ω_n can be directly obtained from its BW, unlike the 2nd order CDRs, where ω_n is a function of both BW and peaking. For 32.0 GT/s, a 2nd-order CDR filter with 20 MHz BW described by Equation 8-6 must be used.

PLL #1, PLL #2	0.01 dB peaking	3.0 dB peaking	BW _{CDR} (min) = 1.5 MHz, 1 st order	CDR
BW _{PLL} (min) = 1.5 MHz	$\omega_{n1} = .336 \text{ Mrad/s}$ $\zeta_1 = 14$	$\omega_{n1} = 5.09 \text{ Mrad/s}$ $\zeta_1 = 0.54$		
BW _{PLL} (max) = 22 MHz	$\omega_{n1} = 4.93 \text{ Mrad/s}$ $\zeta_1 = 14$	$\omega_{n1} = 74.68 \text{ Mrad/s}$ $\zeta_1 = 0.54$		

16 combinations 2.5 GT/s

Figure 8-74 Common Refclk PLL and CDR Characteristics for 2.5 GT/s

PLL and CDR jitter and peaking characteristics for 5.0, 8.0, and 16.0 GT/s yield a larger number of possible combinations because two sets of PLL BW and peaking limits are given. This choice to support two sets of BW and peaking was made to give designers as much latitude as possible when designing PLL circuits.

PLL #1	0.01 dB peaking	1.0 dB peaking	PLL #2	0.01 dB peaking	3.0 dB peaking
$BW_{PLL}(\min) = 5.0$ MHz	$\omega_{n1} = 1.12$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 11.01$ Mrad/s $\zeta_1 = 1.16$	$BW_{PLL}(\min) = 8.0$ MHz	$\omega_{n2} = 1.79$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 26.86$ Mrad/s $\zeta_2 = 0.54$
$BW_{PLL}(\max) = 16$ MHz	$\omega_{n1} = 3.58$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 35.26$ Mrad/s $\zeta_1 = 1.16$	$BW_{PLL}(\max) = 16$ MHz	$\omega_{n2} = 3.58$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 53.73$ Mrad/s $\zeta_2 = 0.54$
$BW_{CDR}(\min) = 5$ MHz, 1 st order			64 combinations		
			5 GT/s		

Figure 8-75 Common Refclk PLL and CDR Characteristics for 5.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
$BW_{PLL}(\min) = 2.0$ MHz	$\omega_{n1} = 0.448$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 6.02$ Mrad/s $\zeta_1 = 0.73$	$BW_{PLL}(\min) = 2.0$ MHz	$\omega_{n2} = 0.448$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 4.62$ Mrad/s $\zeta_2 = 1.15$
$BW_{PLL}(\max) = 4.0$ MHz	$\omega_{n1} = 0.896$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 12.04$ Mrad/s $\zeta_1 = 0.73$	$BW_{PLL}(\max) = 5.0$ MHz	$\omega_{n2} = 1.12$ Mrad/s $\zeta_2 = 14$	$\omega_{n2} = 11.53$ Mrad/s $\zeta_2 = 1.15$
$BW_{CDR}(\min) = 10$ MHz, 1 st order			64 combinations		
			8.0, 16.0 GT/s		

Figure 8-76 Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking	32.0 GT/s CC	CDR
$BW_{PLL}(\min) = 0.5$ MHz	$\omega_{n1} = .112$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 1.51$ Mrad/s $\zeta_1 = 0.73$		
$BW_{PLL}(\max) = 1.8$ MHz	$\omega_{n1} = .403$ Mrad/s $\zeta_1 = 14$	$\omega_{n1} = 5.42$ Mrad/s $\zeta_1 = 0.73$		
16 combinations			32.0 GT/s	

Figure 8-77 Common Refclk PLL and CDR Characteristics for 32.0 GT/s

8.6.7 Jitter Limits for Refclk Architectures

Table 8-18 lists the jitter limits for the CC Refclk architecture at each of the four data rates.

Jitter at 2.5 GT/s is measured as a peak to peak jitter value, because a substantial proportion of the jitter is SSC harmonics which appears at the receiver as Dj. The combination of the 2.5 GT/s PLL and CDR bandwidths passes a significant amount of SSC residual, where it appears Dj.

For 5.0, 8.0, and 16.0 GT/s jitter is specified as an RMS (Rj) value. These signaling speeds utilize a lower PLL BW and a higher CDR BW, and the effect is to suppress SSC harmonics such that almost all the jitter appears as Rj.

Table 8-18 Jitter Limits for CC Architecture

Data Rate	CC jitter Limit	Notes
2.5 GT/s	86 ps pp	1, 2

Data Rate	CC jitter Limit	Notes
5.0 GT/s	3.1 ps RMS	1, 2
8.0 GT/s	1.0 ps RMS	1, 2
16.0 GT/s	0.5 ps RMS	1, 2, 3, 4
32.0 GT/s	0.15 ps RMS	1, 2, 3, 5

Notes:

1. The Refclk jitter is measured after applying the filter function in [Figure 8-73](#)
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.
3. For the 16.0 GT/s and 32.0 GT/s CC measurements SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.

8.6.8 Form Factor Requirements for RefClock Architectures

Each form factor specification must include the following table (see [Table 8-19](#)) to provide a clear summary of the clocking architecture requirements for devices that support the form factor specification. For each clocking architecture the table indicates whether that architecture is required, optional, or not allowed for this form factor. Note that this refers to the operation of the device not the underlying silicon capabilities.

A form factor must provide the CLKREQ# signal if it supports L1 PM Substates. Form factor specifications must indicate if the CLKREQ# signal is required, optional, or not allowed.

Table 8-19 Form Factor Clocking Architecture Requirements

Clock Architecture	System Board (Motherboard)	Add-in Card (Module)	Retimer
Common	**	**	**
SRNS	**	**	**
SRIS	**	**	**

** Each entry in the table must be filled in with one of: Required, Optional, or Not Allowed

If the Common Reference Clock architecture is required or optional for the form factor, then there must be an additional table (see [Table 8-20](#)) providing details for the common clock. Each entry in the table is marked required, optional, not allowed, or NA. “Clock Source” indicates the source of the common reference clock, if applicable. “SSC” indicates whether the clock source is spread.

Table 8-20 Form Factor Common Clock Architecture Details

Common Clock Details	System Board (Motherboard)	Add-in Card (Module)	Retimer
Clock Source			
SSC			

If a form factor has clocking requirements that can not be provided in this simple one or two table form then careful consideration must be given to ensure that the form factor requirements are supported by this specification.

As an example the populated tables are shown for a hypothetical form factor that requires all components use the common clock architecture and does not allow the use of any other clocking architecture (see [Table 8-21](#) and [Table 8-22](#)). The common clock source is required to be provided by the motherboard component and may optionally have SSC. L1 PM Substates are not supported and therefore CLKREQ# is not defined as a connector signal for this example form factor.

Table 8-21 Form Factor Clocking Architecture Requirements Example

Clock Architecture	System Board (Motherboard)	Add-in Card (Module)	Retimer
Common	Required	Required	Required
SRNS	Not Allowed	Not Allowed	Not Allowed
SRIS	Not Allowed	Not Allowed	Not Allowed

Table 8-22 Form Factor Common Clock Architecture Details Example

Common Clock Details	System Board (Motherboard)	Add-in Card (Module)	Retimer
Clock Source	Required	Not Allowed	Not Allowed
SSC	Optional	N/A	N/A

It is important for form factor specifications to recognize that the CLKREQ# signal is required if L1 PM Substates are to be supported, and that for L1 PM Substates the CLKREQ# signal is used even if there is no common reference clock.

If a form factor has clocking requirements that can not be provided in this simple one or two table form then careful consideration must be given to ensure that the form factor requirements are supported by this specification.

Single Root I/O Virtualization and Sharing

9.

9.1 SR-IOV Architectural Overview

Within the industry, significant effort has been expended to increase the effective hardware resource utilization (i.e., application execution) through the use of virtualization technology. Single Root I/O Virtualization and Sharing (SR-IOV) enables multiple System Images (SI) to share PCI hardware resources.

To illustrate how this technology can be used to increase effective resource utilization, consider the generic platform configuration illustrated in Figure 9-1.

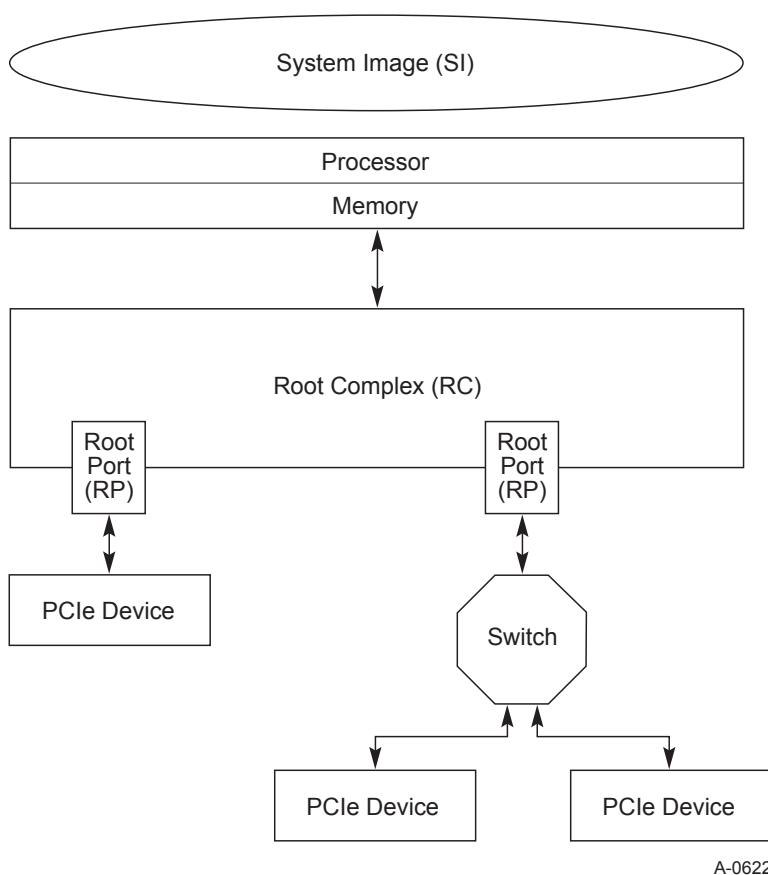


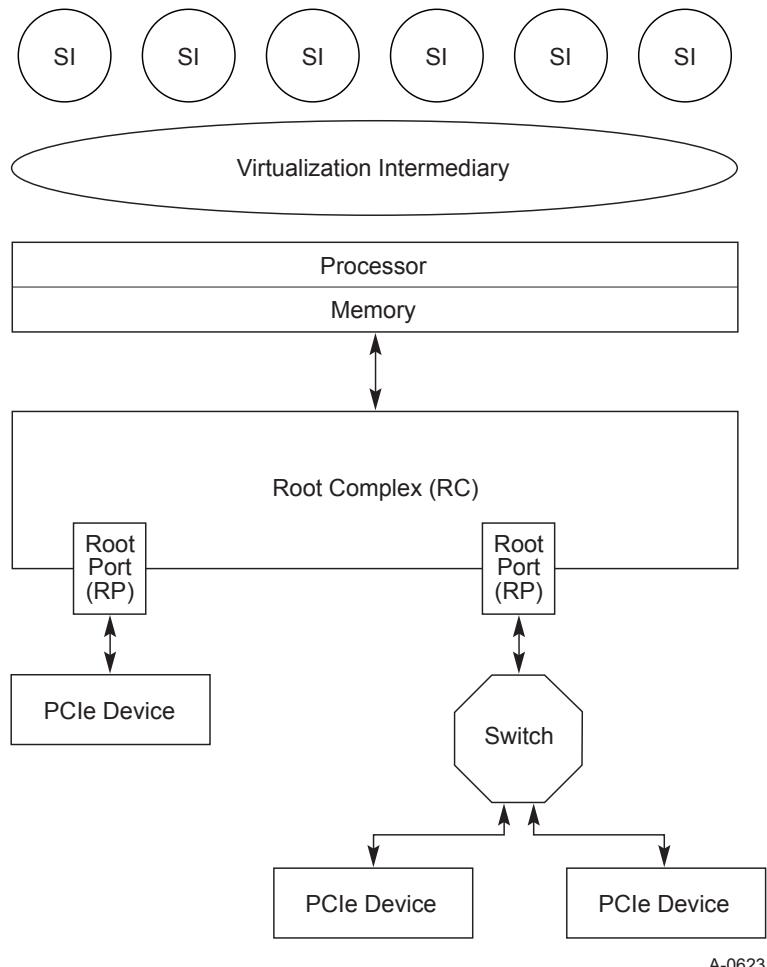
Figure 9-1 Generic Platform Configuration

The generic platform configuration is composed of the following components:

- PCIe Root Complex (RC), which includes:
 - Processor - general purpose, embedded, or specialized processing element

- Memory - general purpose or embedded
- Root Complex Integrated Endpoints (RCiEPs)
- PCIe Root Ports (RP) - Each RP represents a separate hierarchy. Each hierarchy is referred to a single root hierarchy to delineate it from the multiple hierarchy technology defined in [MR-IOV].
- PCIe Switch - provides I/O fan-out and connectivity
 - PCIe Device - multiple I/O device types, (e.g., network, storage, etc.)
 - System Image - software such an operating system that is used to execute applications or trusted services, (e.g., a shared or non-shared I/O device driver.)

In order to increase the effective hardware resource utilization without requiring hardware modifications, multiple SI can be executed. Software termed a Virtualization Intermediary (VI) is interposed between the hardware and the SI as illustrated in Figure 9-2.



A-0623

Figure 9-2 Generic Platform Configuration with a VI and Multiple SI

The VI takes sole ownership of the underlying hardware. Using a variety of methods outside of the scope of this specification, the VI abstracts the hardware to present each SI with its own virtual system. The actual hardware resources available to each SI can vary based on workload or customer-specific policies. While this approach works well