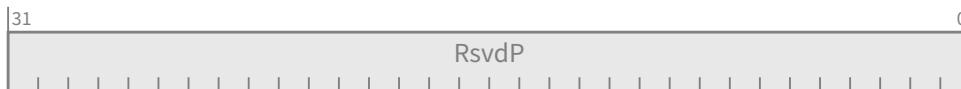


Table 7-62 Physical Layer 16.0 GT/s Extended Capability Header

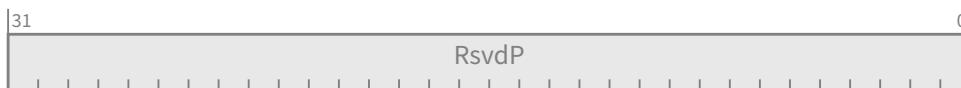
Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 16.0 GT/s Capability is 0026h.	<u>RO</u>
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	<u>RO</u>
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than OFFh.	<u>RO</u>

7.7.5.2 16.0 GT/s Capabilities Register (Offset 04h)

*Figure 7-80 16.0 GT/s Capabilities Register**Table 7-63 16.0 GT/s Capabilities Register*

Bit Location	Register Description	Attributes
31:0	<u>RsvdP</u>	<u>RsvdP</u>

7.7.5.3 16.0 GT/s Control Register (Offset 08h)

*Figure 7-81 16.0 GT/s Control Register**Table 7-64 16.0 GT/s Control Register*

Bit Location	Register Description	Attributes
31:0	<u>RsvdP</u>	<u>RsvdP</u>

7.7.5.4 16.0 GT/s Status Register (Offset 0Ch)

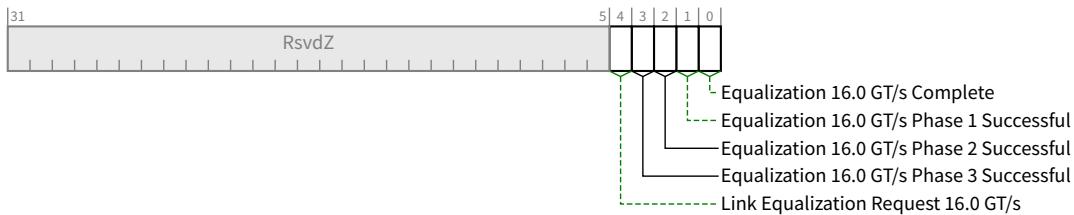


Figure 7-82 16.0 GT/s Status Register

Table 7-65 16.0 GT/s Status Register

Bit Location	Register Description	Attributes
0	<p>Equalization 16.0 GT/s Complete - When Set, this bit indicates that the 16.0 GT/s Transmitter Equalization procedure has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ
1	<p>Equalization 16.0 GT/s Phase 1 Successful - When set to 1b, this bit indicates that Phase 1 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ
2	<p>Equalization 16.0 GT/s Phase 2 Successful - When set to 1b, this bit indicates that Phase 2 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ
3	<p>Equalization 16.0 GT/s Phase 3 Successful - When set to 1b, this bit indicates that Phase 3 of the 16.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ
4	<p>Link Equalization Request 16.0 GT/s - This bit is Set by hardware to request the 16.0 GT/s Link equalization process to be performed on the Link. Refer to Section 4.2.3 and Section 4.2.6.4.2 for details.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	RW1CS/RsvdZ

7.7.5.5 16.0 GT/s Local Data Parity Mismatch Status Register (Offset 10h)

The Local Data Parity Mismatch Status register is a 32-bit vector where each bit indicates if the local receiver detected a Data Parity mismatch on the Lane with the corresponding Lane number. This Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

This register collects parity errors for 16.0 GT/s and higher data rates. When tracking errors for a specific Link Speed, software should clear this register on speed changes.

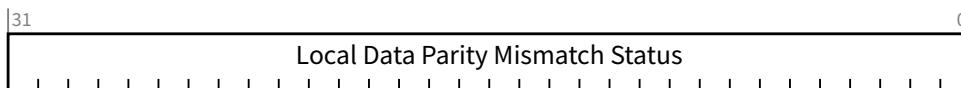


Figure 7-83 16.0 GT/s Local Data Parity Mismatch Status Register

Table 7-66 16.0 GT/s Local Data Parity Mismatch Status Register

Bit Location	Register Description	Attributes
31:0	<p>Local Data Parity Mismatch Status - Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. See Section 4.2.7.2 for more information.</p> <p>The default value of each bit is 0b.</p> <p>For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ.</p>	RW1CS/RsvdZ

7.7.5.6 16.0 GT/s First Retimer Data Parity Mismatch Status Register (Offset 14h)

The First Retimer Data Parity Status register is a 32-bit vector where each bit indicates if the first Retimer of a Path (see [Figure 4-36](#) for more information) detected a Data Parity mismatch on the Lane with the corresponding Lane number. This Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

This register collects parity errors for 16.0 GT/s and higher data rates. When tracking errors for a specific Link Speed, software should clear this register on speed changes.



Figure 7-84 16.0 GT/s First Retimer Data Parity Mismatch Status Register

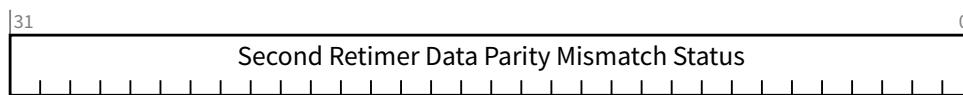
Table 7-67 16.0 GT/s First Retimer Data Parity Mismatch Status Register

Bit Location	Register Description	Attributes
31:0	<p>First Retimer Data Parity Mismatch Status - Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. See Section 4.2.7.2 for more information.</p> <p>The default value of each bit is 0b.</p> <p>The value of this field is undefined when no Retimers are present.</p> <p>For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ.</p>	RW1CS/RsvdZ

7.7.5.7 16.0 GT/s Second Retimer Data Parity Mismatch Status Register (Offset 18h)

The [16.0 GT/s Second Retimer Data Parity Mismatch Status Register](#) is a 32-bit vector where each bit indicates if the second Retimer of a Path (see [Figure 4-36](#) for more information) detected a Data Parity mismatch on the Lane with the corresponding Lane number. This Lane number is the default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

This register collects parity errors for 16.0 GT/s and higher data rates. When tracking errors for a specific Link Speed, software should clear this register on speed changes.

*Figure 7-85 16.0 GT/s Second Retimer Data Parity Mismatch Status Register**Table 7-68 16.0 GT/s Second Retimer Data Parity Mismatch Status Register*

Bit Location	Register Description	Attributes
31:0	<p>Second Retimer Data Parity Mismatch Status - Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. See Section 4.2.7.2 for more information.</p> <p>The default value of each bit is 0b.</p> <p>The value of this field is undefined when no Retimers are present or only one Retimer is present.</p> <p>For Ports that are narrower than 32 Lanes, the unused upper bits [31: Maximum Link Width] are RsvdZ.</p>	RW1CS/RsvdZ

7.7.5.8 Physical Layer 16.0 GT/s Reserved (Offset 1Ch)

This register is [RsvdP](#).

7.7.5.9 16.0 GT/s Lane Equalization Control Register (Offsets 20h to 3Ch)

The Equalization Control register consists of control fields required for per-Lane 16.0 GT/s equalization. It contains entries for at least the number of Lanes defined by the Maximum Link Width (see Section 7.5.3.6 or Section 7.9.9.2), must be implemented in whole DW granularity (e.g., if the Maximum Link Width is x1, the register will still contain entries for 4 Lanes with the entries for Lanes 1, 2 and 3 being undefined), and it is permitted to contain up to 32 entries regardless of the Maximum Link Width. The value of entries beyond the Maximum Link Width is undefined.

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

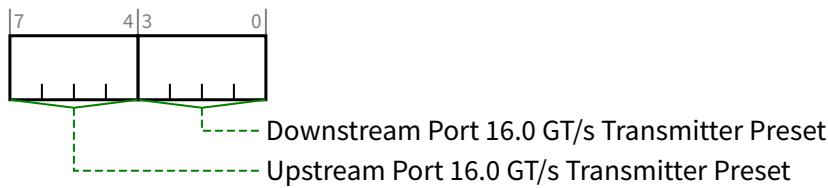


Figure 7-86 16.0 GT/s Lane Equalization Control Register Entry

Table 7-69 16.0 GT/s Lane Equalization Control Register Entry

Bit Location	Register Description	Attributes												
3:0	<p>Downstream Port 16.0 GT/s Transmitter Preset - Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. See Chapter 8 for details. The field encodings are defined in Section 4.2.3.2.</p> <p>For an Upstream Port if <u>Crosslink Supported</u> is 0b, this field is <u>RsvdP</u>. Otherwise, this field is <u>HwInit</u>. See Section 7.5.3.18.</p> <p>The default value is 1111b.</p>	<u>HwInit/RsvdP</u> (see description)												
7:4	<p>Upstream Port 16.0 GT/s Transmitter Preset - Field contains the Transmit Preset value sent or received during 16.0 GT/s Link Equalization. Field usage varies as follows:</p> <table border="1"> <thead> <tr> <th></th> <th>Operating Port Direction</th> <th><u>Crosslink Supported</u></th> <th>Usage</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>Downstream Port</td> <td>Any</td> <td> <p>Field contains the value sent on the associated Lane during Link Equalization.</p> <p>Field is <u>HwInit</u>.</p> </td></tr> <tr> <td>B</td> <td>Upstream Port</td> <td>0b</td> <td> <p>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.</p> <p>Field is <u>RO</u>.</p> <p>When crosslinks are supported, case C (below) applies and this captured information is not visible to software.</p> </td></tr> </tbody> </table>		Operating Port Direction	<u>Crosslink Supported</u>	Usage	A	Downstream Port	Any	<p>Field contains the value sent on the associated Lane during Link Equalization.</p> <p>Field is <u>HwInit</u>.</p>	B	Upstream Port	0b	<p>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.</p> <p>Field is <u>RO</u>.</p> <p>When crosslinks are supported, case C (below) applies and this captured information is not visible to software.</p>	<u>HwInit/RO</u> (see description)
	Operating Port Direction	<u>Crosslink Supported</u>	Usage											
A	Downstream Port	Any	<p>Field contains the value sent on the associated Lane during Link Equalization.</p> <p>Field is <u>HwInit</u>.</p>											
B	Upstream Port	0b	<p>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.</p> <p>Field is <u>RO</u>.</p> <p>When crosslinks are supported, case C (below) applies and this captured information is not visible to software.</p>											

Bit Location	Register Description			Attributes
	Operating Port Direction	Crosslink Supported	Usage	
			Vendors are encouraged to provide an alternate mechanism to obtain this information.	
C	Upstream Port	1b	<p>Field is not used or affected by the current Link Equalization.</p> <p>Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A (above) applies.</p> <p>Field is <u>HwInit</u>.</p>	

See [Section 4.2.3](#) and [Chapter 8](#) for details. The field encodings are defined in [Section 4.2.3.2](#).
The default value is 1111b.

7.7.6 Physical Layer 32.0 GT/s Extended Capability

The [Physical Layer 32.0 GT/s Extended Capability](#) structure must be implemented in Ports where one or more of the following features are supported:

- The [Supported Link Speeds Vector](#) field indicates support for a Link speed of 32.0 GT/s.
- The Function supports sending and/or receiving [Modified TS1/TS2 Ordered Sets](#).

When implemented, this structure must be implemented in:

- A Function associated with a Downstream Port
- A Function of a single-Function Device associated with an Upstream Port
- Function 0 (and only Function 0) of a [Multi-Function Device](#) associated with an Upstream Port

This capability is permitted to be implemented in any of the Functions listed above even if the 32.0 GT/s Link speed is not supported. When the 32.0 GT/s Link speed is not supported, the behavior of registers other than the Capability Header is undefined.

[Figure 7-87](#) details allocation of register fields in the [Physical Layer 32.0 GT/s Extended Capability](#) structure.

Note that parity errors for 32.0 GT/s are recorded in [16.0 GT/s Local Data Parity Mismatch Status Register](#), [16.0 GT/s First Retimer Data Parity Mismatch Status Register](#), and [16.0 GT/s Second Retimer Data Parity Mismatch Status Register](#). When tracking errors for a specific Link Speed, software should clear those registers on speed changes.

Byte Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+000h	PCI Express Extended Capability Header																															
+004h	32.0 GT/s Capabilities Register																															
+008h	32.0 GT/s Control Register																															
+00Ch	32.0 GT/s Status Register																															
+010h	Received Modified TS Data 1 Register																															
+014h	Received Modified TS Data 2 Register																															
+018h	Transmitted Modified TS Data 1 Register																															
+01Ch	Transmitted Modified TS Data 2 Register																															
+020h	32.0 GT/s Eq Ctl: Lane 3	32.0 GT/s Eq Ctl: Lane 2	32.0 GT/s Eq Ctl: Lane 1	32.0 GT/s Eq Ctl: Lane 0																												
+024h	32.0 GT/s Eq Ctl: Lane 7	32.0 GT/s Eq Ctl: Lane 6	32.0 GT/s Eq Ctl: Lane 5	32.0 GT/s Eq Ctl: Lane 4																												
+028h	32.0 GT/s Eq Ctl: Lane 11	32.0 GT/s Eq Ctl: Lane 10	32.0 GT/s Eq Ctl: Lane 9	32.0 GT/s Eq Ctl: Lane 8																												
+02Ch	32.0 GT/s Eq Ctl: Lane 15	32.0 GT/s Eq Ctl: Lane 14	32.0 GT/s Eq Ctl: Lane 13	32.0 GT/s Eq Ctl: Lane 12																												
+030h	32.0 GT/s Eq Ctl: Lane 19	32.0 GT/s Eq Ctl: Lane 18	32.0 GT/s Eq Ctl: Lane 17	32.0 GT/s Eq Ctl: Lane 16																												
+034h	32.0 GT/s Eq Ctl: Lane 23	32.0 GT/s Eq Ctl: Lane 22	32.0 GT/s Eq Ctl: Lane 21	32.0 GT/s Eq Ctl: Lane 20																												
+038h	32.0 GT/s Eq Ctl: Lane 27	32.0 GT/s Eq Ctl: Lane 26	32.0 GT/s Eq Ctl: Lane 25	32.0 GT/s Eq Ctl: Lane 24																												
+03Ch	32.0 GT/s Eq Ctl: Lane 31	32.0 GT/s Eq Ctl: Lane 30	32.0 GT/s Eq Ctl: Lane 29	32.0 GT/s Eq Ctl: Lane 28																												

Figure 7-87 Physical Layer 32.0 GT/s Extended Capability

7.7.6.1 Physical Layer 32.0 GT/s Extended Capability Header (Offset 00h)

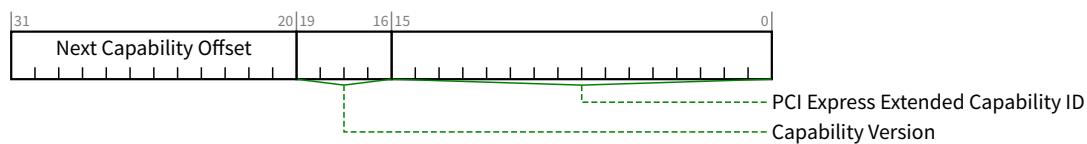


Figure 7-88 Physical Layer 32.0 GT/s Extended Capability Header

Table 7-70 Physical Layer 32.0 GT/s Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 32.0 GT/s Capability is 002Ah.	RO
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than OFFh.	RO

7.7.6.2 32.0 GT/s Capabilities Register (Offset 04h)

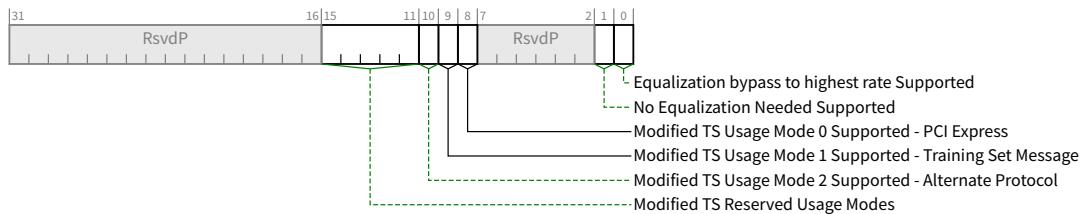


Figure 7-89 32.0 GT/s Capabilities Register

Table 7-71 32.0 GT/s Capabilities Register

Bit Location	Register Description	Attributes
0	Equalization bypass to highest rate Supported - When Set, this Port supports controlling whether the Port negotiates to skip equalization for speeds other than the highest common supported speed. See Section 4.2.3 for details. Must be 1b for Ports that support 32.0 GT/s or higher data rates.	HwInit
1	No Equalization Needed Supported - When Set, this Port supports controlling whether or not Equalization is needed.	HwInit
8	Modified TS Usage Mode 0 Supported - PCI Express - This bit indicates that this Port supports PCI Express (Modified TS Usage 000b). This bit must be 1b.	RO
9	Modified TS Usage Mode 1 Supported - Training Set Message - This bit indicates that this Port supports sending and receiving vendor specific Training Set Messages (Modified TS Usage 001b). See Section 4.2.4.2 for details.	HwInit
10	Modified TS Usage Mode 2 Supported - Alternate Protocol - This bit indicates that this Port supports negotiating to use alternate protocols (Modified TS Usage 010b). See Section 4.2.4.2 for details.	HwInit
15:11	Modified TS Reserved Usage Modes - Reserved bits for future Usage Modes defined by the PCISIG. Must be 0 0000b.	RO

7.7.6.3 32.0 GT/s Control Register (Offset 08h)

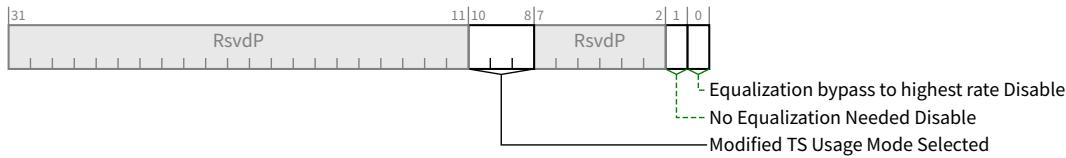


Figure 7-90 32.0 GT/s Control Register

Table 7-72 32.0 GT/s Control Register

Bit Location	Register Description	Attributes
0	<p>Equalization bypass to highest rate Disable - When Clear, this Port indicates during Link Training that it wishes to train to the highest common link data rate and skip equalization of intermediate data rates. See Section 4.2.3 for details.</p> <p>If <u>Equalization bypass to highest rate Supported</u> is Set, this bit is <u>RWS</u> with a default value of 0b.</p> <p>If <u>Equalization bypass to highest rate Supported</u> is Clear, this bit is permitted to be hardwired to 0b.</p>	<u>RWS/RO</u>
1	<p>No Equalization Needed Disable - When Clear, this Port is permitted to indicate that it does not require equalization. When Set, this Port must always indicate that it requires equalization. See Section 4.2.3 for details.</p> <p>If <u>No Equalization Needed Supported</u> is Set, this bit is <u>RWS</u> with a default value of 0b.</p> <p>If <u>No Equalization Needed Supported</u> is Clear, this bit is permitted to be hardwired to 0b.</p>	<u>RWS/RO</u>
10:8	<p>Modified TS Usage Mode Selected - This field indicates which Usage Mode will be used by this Downstream Port the next time the Link enters L0 LTSSM State. See Section 4.2.4.2 for details.</p> <p>Behavior is undefined if this field indicates a Usage Mode that is not supported (i.e., associated Modified TS Usage Mode Supported bit is Clear).</p> <p>Unused bits in this field are permitted to be hardwired to 0b. If the only supported usage mode is PCI Express, this field is permitted to be hardwired to 000b.</p> <p>This field is present in Downstream Ports. In Upstream Ports, this field is <u>RsvdP</u>.</p> <p>Default is 000b.</p>	<u>RWS/RO/RsvdP</u>

7.7.6.4 32.0 GT/s Status Register (Offset 0Ch)

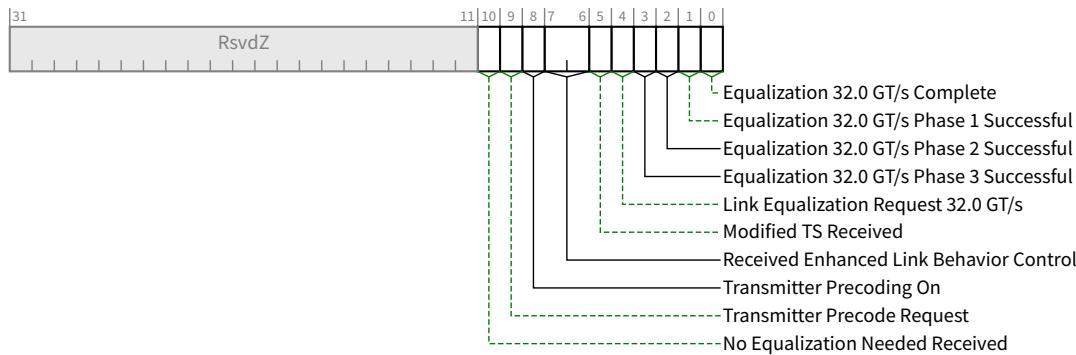


Figure 7-91 32.0 GT/s Status Register

Table 7-73 32.0 GT/s Status Register

Bit Location	Register Description	Attributes
0	<p>Equalization 32.0 GT/s Complete - When Set, this bit indicates that the 32.0 GT/s Transmitter Equalization procedure has completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ
1	<p>Equalization 32.0 GT/s Phase 1 Successful - When set to 1b, this bit indicates that Phase 1 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ
2	<p>Equalization 32.0 GT/s Phase 2 Successful - When set to 1b, this bit indicates that Phase 2 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ
3	<p>Equalization 32.0 GT/s Phase 3 Successful - When set to 1b, this bit indicates that Phase 3 of the 32.0 GT/s Transmitter Equalization procedure has successfully completed. Details of the Transmitter Equalization process and when this bit needs to be set to 1b is provided in Section 4.2.6.4.2.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	ROS/RsvdZ

Bit Location	Register Description	Attributes
4	<p>Link Equalization Request 32.0 GT/s - This bit is Set by hardware to request the 32.0 GT/s Link equalization process to be performed on the Link. Refer to Section 4.2.3 and Section 4.2.6.4.2 for details.</p> <p>The default value of this bit is 0b.</p> <p>For a Multi-Function Upstream Port, this bit must be implemented in Function 0 and RsvdZ in other Functions.</p>	RW1CS/RsvdZ
5	<p>Modified TS Received - If Set, Received Modified TS Data 1 Register and Received Modified TS Data 2 Register contain meaningful data.</p> <p>This bit is Cleared when the Link is Down. This bit is Set when the Modified TS1/TS2 Ordered Set is received (See Section 4.2.6.3.3). Default is 0b.</p>	RO
7:6	<p>Received Enhanced Link Behavior Control - This field contains the Enhanced Link Behavior Control bits from the most recent TS1 or TS2 received in the Polling or Configuration states. See Section 4.2.4.1, Table 4-6 and Table 4-7.</p> <p>This field is Cleared on DL_Down.</p> <p>Default is 00b.</p>	RO
8	<p>Transmitter Precoding On - This field indicates whether the Receiver asked this transmitter to enable Precoding. See Section 4.2.2.5. This bit is cleared on DL_Down.</p> <p>Default is 0b.</p>	RO>
9	<p>Transmitter Precode Request - When Set, this Port will request the transmitter to use Precoding by setting the Transmitter Precode Request bit in the TS1s/TS2s it transmits prior to entry to Recovery.Speed (see Section 4.2.2.5).</p> <p>Default is Implementation Specific.</p>	RO
10	<p>No Equalization Needed Received - When Set, this Port either received a Modified TS1/TS2 with the No Equalization Needed bit Set or received a non-modified TS1/TS2 was received with the No Equalization Needed encoding (also reported in the Received Enhanced Link Behavior Control field).</p> <p>Default is 0b.</p>	RO

7.7.6.5 Received Modified TS Data 1 Register (Offset 10h)

This register contains the values received in the [Modified TS1/TS2 Ordered Set](#) (see [Table 4-8](#)).

If PCI Express (Usage Mode 0) is the only one supported by a Port, this register is permitted to be hardwired to 0000 0000h.

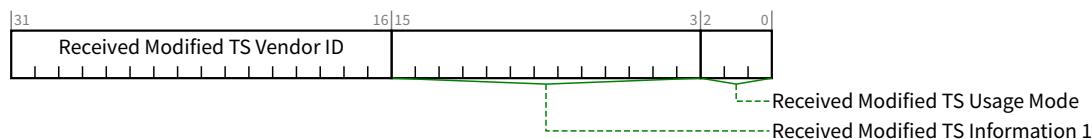


Figure 7-92 Received Modified TS Data 1 Register

Table 7-74 Received Modified TS Data 1 Register

Bit Location	Description	Attributes
2:0	<p>Received Modified TS Usage Mode - If <u>Modified TS Received</u> is Set, this field contains the <u>Modified TS Usage</u> field from the <u>Modified TS1/TS2 Ordered Set</u> (see <u>Section 4.2.6.3.6</u>). If <u>Modified TS Received</u> is Clear, this field contains 000b.</p> <p>Unused bits in this field are permitted to be hardwired to 0b. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 000b.</p> <p>Default is 000b.</p>	RO
15:3	<p>Received Modified TS Information 1 - If <u>Modified TS Received</u> is Set, this field contains the <u>Modified TS Information 1</u> field from the <u>Modified TS1/TS2 Ordered Set</u> (see <u>Section 4.2.6.3.6</u>). If <u>Modified TS Received</u> is Clear, this field contains 0 0000 0000 0000b.</p> <p>Bits 15:8 contain the value of Symbol 9.</p> <p>Bits 7:3 contain bits 7:3 of Symbol 8.</p> <p>If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0 0000 0000 0000b.</p> <p>Default is 0 0000 0000 0000b.</p>	RO
31:16	<p>Received Modified TS Vendor ID - If <u>Modified TS Received</u> is Set, this field contains the <u>Training Set Message Vendor ID or Alternate Protocol Vendor ID</u> field from the <u>Modified TS1/TS2 Ordered Set</u> received (see <u>Section 4.2.6.3.6</u>). If <u>Modified TS Received</u> is Clear, this field contains 0000h.</p> <p>Bits 15:8 contain the value of Symbol 11.</p> <p>Bits 7:0 contain the value of Symbol 10.</p> <p>If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0000h.</p> <p>Default is 0000h.</p>	RO

7.7.6.6 Received Modified TS Data 2 Register (Offset 14h)

This register contains the values received in Symbols 12 through 14 of the Modified TS1/TS2 (see Table 4-8).

If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h.

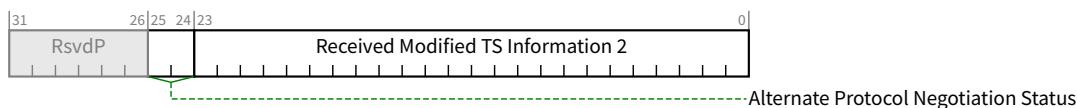


Figure 7-93 Received Modified TS Data 2 Register

Table 7-75 Received Modified TS Data 2 Register

Bit Location	Description	Attributes
23:0	<p>Received Modified TS Information 2 - If <u>Modified TS Received</u> is Set, this field contains the <u>Modified TS Information 2</u> field from the received <u>Modified TS1/TS2 Ordered Set</u> (Section 4.2.6.3.6). If <u>Modified TS Received</u> is Clear, this field contains 00 0000h.</p> <p>Bits 23:16 contain the value of Symbol 14.</p> <p>Bits 16:8 contain the value of Symbol 13.</p> <p>Bits 7:0 contain the value of Symbol 12.</p> <p>If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 00 0000h.</p> <p>Default is 00 0000h.</p>	<u>RO</u>
25:24	<p>Alternate Protocol Negotiation Status - Indicates the status of the Alternate Protocol Negotiation. Encodings are:</p> <ul style="list-style-type: none"> 00b Alternate Protocol Negotiation not supported - <u>Modified TS Usage Mode 2 Supported</u> - <u>Alternate Protocol</u> is Clear. 01b Alternate Protocol Negotiation disabled - <u>Modified TS Usage Mode 2 Supported</u> - <u>Alternate Protocol</u> is Set but <u>Modified TS Usage Mode Selected</u> was not 2 during the appropriate LTSSM State. 10b Alternate Protocol Negotiation failed - Alternate Protocol Negotiation was attempted and did not locate a protocol that was supported on both ends of the Link. 11b Alternate rotocol Negotiation succeeded - Alternate Protocol Negotiation located one or more protocols that were supported on both ends of the Link and the Downstream Port selected one of those protocols for use. <p>If Set, Alternate Protocol Negotiation completed succesfully. If Clear, Alternate Protocol Negotiation negotiation has not completed succesfully. If <u>Modified TS Usage Mode 1 Supported</u> - <u>Training Set Message</u> and <u>Modified TS Usage Mode 2 Supported</u> - <u>Alternate Protocol</u> are both Clear, this register is permitted to be hardwired to 0000 0000h.</p> <p>If <u>Modified TS Usage Mode 2 Supported</u> - <u>Alternate Protocol</u> is Clear, this bit is hardwired to 0b.</p> <p>If <u>Modified TS Usage Mode Selected</u> does not equal 2, this bit contains 0b.</p> <p>This bit is Cleared on <u>Detect LTSSM State</u>.</p> <p>Default is 0b.</p>	<u>RO</u>

7.7.6.7 Transmitted Modified TS Data 1 Register (Offset 18h)

This register contains the values transmitted in the Modified TS1/TS2 Ordered Set (see Table 4-8).

If PCI Express (Usage Mode 0) is the only one supported by a Port, this register is permitted to be hardwired to 0000 0000h.

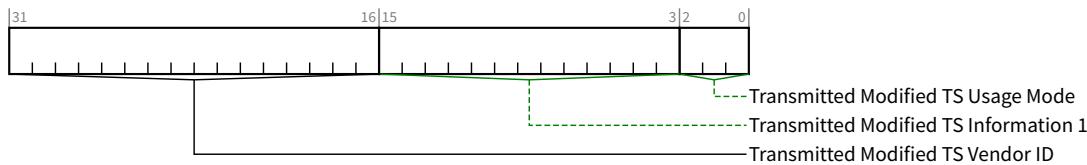


Figure 7-94 Transmitted Modified TS Data 1 Register

Table 7-76 Transmitted Modified TS Data 1 Register

Bit Location	Description	Attributes
2:0	<p>Transmitted Modified TS Usage Mode - If <u>Modified TS Received</u> is Set, this field contains the <u>Modified TS Usage</u> field from the <u>Modified TS2 Ordered Set</u> transmitted during the <u>Configuration.Complete LTSSM State</u> (see <u>Section 4.2.6.3.6</u>).</p> <p>Unused bits in this field are permitted to be hardwired to 0b. If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 000b.</p> <p>Default is 000b.</p>	RO
15:3	<p>Transmitted Modified TS Information 1 - If <u>Modified TS Received</u> is Set, this field contains the <u>Modified TS Information 1</u> field from <u>Modified TS2 Ordered Set</u> transmitted during the <u>Configuration.Complete LTSSM State</u> (see <u>Section 4.2.6.3.6</u>).</p> <p>Bits 15:8 contain the value of Symbol 9.</p> <p>Bits 7:3 contain bits 7:3 of Symbol 8.</p> <p>If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0 0000 0000b.</p> <p>Default is 0 0000 0000b.</p>	RO
31:16	<p>Transmitted Modified TS Vendor ID - If <u>Modified TS Received</u> is Set, this field contains the <u>Training Set Message Vendor ID</u> or <u>Alternate Protocol Vendor ID</u> field from the <u>Modified TS2 Ordered Set</u> transmitted during the <u>Configuration.Complete LTSSM State</u> (see <u>Section 4.2.6.3.6</u>).</p> <p>Bits 15:8 contain the value of Symbol 11.</p> <p>Bits 7:0 contain the value of Symbol 10.</p> <p>If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 0000h.</p> <p>Default is 0000h.</p>	RO

7.7.6.8 Transmitted Modified TS Data 2 Register (Offset 1Ch)

This register contains the values received in Symbols 12 through 14 of the Modified TS1/TS2 (see Table 4-8).

If Modified TS Usage Mode 1 Supported - Training Set Message and Modified TS Usage Mode 2 Supported - Alternate Protocol are both Clear, this register is permitted to be hardwired to 0000 0000h.

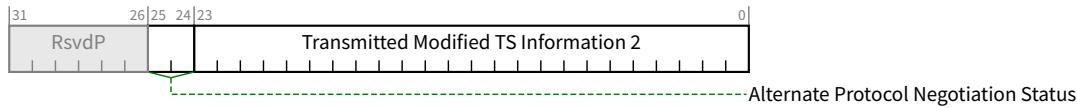


Figure 7-95 Transmitted Modified TS Data 2 Register

Table 7-77 Transmitted Modified TS Data 2 Register

Bit Location	Description	Attributes
23:0	<p>Transmitted Modified TS Information 2 - If Modified TS Received is Set, this field contains the <u>Modified TS Information 2</u> field from the <u>Modified TS2 Ordered Set</u> transmitted during the <u>Configuration.Complete LTSSM State</u> (see <u>Section 4.2.6.3.6</u>).</p> <p>Bits 23:16 contain the value of Symbol 14.</p> <p>Bits 16:8 contain the value of Symbol 13.</p> <p>Bits 7:0 contain the value of Symbol 12.</p> <p>If PCI Express (Usage Mode 0) is the only one supported, this field is permitted to be hardwired to 00 0000h.</p> <p>Default is 00 0000h.</p>	RO
25:24	<p>Alternate Protocol Negotiation Status - Indicates the status of the Alternate Protocol Negotiation. Encodings are:</p> <ul style="list-style-type: none"> 00b Alternate Protocol Negotiation not supported - <u>Modified TS Usage Mode 2 Supported</u> - Alternate Protocol is Clear. 01b Alternate Protocol Negotiation disabled - <u>Modified TS Usage Mode 2 Supported</u> - <u>Alternate Protocol</u> is Set but <u>Modified TS Usage Mode Selected</u> was not 2 during the appropriate LTSSM State. 10b Alternate Protocol Negotiation failed - Alternate Protocol Negotiation was attempted and did not locate a protocol that was supported on both ends of the Link. 11b Alternate protocol Negotiation succeeded - Alternate Protocol Negotiation located one or more protocols that were supported on both ends of the Link and the Downstream Port selected one of those protocols for use. <p>If Set, Alternate Protocol Negotiation completed successfully. If Clear, Alternate Protocol Negotiation negotiation has not completed successfully. If <u>Modified TS Usage Mode 1 Supported</u> - <u>Training Set Message</u> and <u>Modified TS Usage Mode 2 Supported</u> - <u>Alternate Protocol</u> are both Clear, this register is permitted to be hardwired to 0000 0000h.</p> <p>If <u>Modified TS Usage Mode 2 Supported</u> - <u>Alternate Protocol</u> is Clear, this bit is hardwired to 0b.</p> <p>If <u>Modified TS Usage Mode Selected</u> does not equal 2, this bit contains 0b.</p> <p>This bit is Cleared on <u>Detect LTSSM State</u>.</p> <p>Default is 0b.</p>	RO

7.7.6.9 32.0 GT/s Lane Equalization Control Register (Offset 20h)

The 32.0 GT/s Equalization Control register consists of control fields required for per-Lane 32.0 GT/s equalization. It contains entries for at least the number of Lanes defined by the Maximum Link Width (see Section 7.5.3.6 or Section 7.9.9.2), must be implemented in whole DW DW granularity (e.g., if the Maximum Link Width is x1, the register will still

contain entries for 4 Lanes with the entries for Lanes 1, 2 and 3 being undefined), and it is permitted to contain up to 32 entries regardless of the Maximum Link Width. The value of entries beyond the Maximum Link Width is undefined.

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

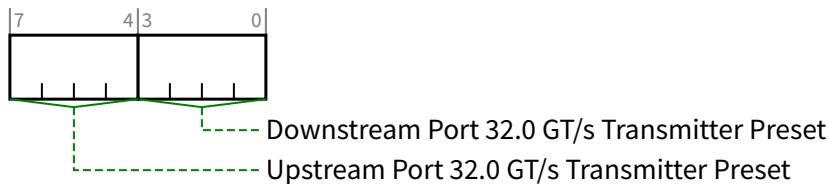


Figure 7-96 32.0 GT/s Lane Equalization Control Register Entry

Table 7-78 32.0 GT/s Lane Equalization Control Register Entry

Bit Location	Register Description	Attributes																
3:0	<p>Downstream Port 32.0 GT/s Transmitter Preset - Transmitter Preset used for 32.0 GT/s equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port. See <u>Chapter 8</u> for details. The field encodings are defined in <u>Section 4.2.3.2</u>.</p> <p>For an Upstream Port if <u>Crosslink Supported</u> is 0b, this field is <u>RsvdP</u>. Otherwise, this field is <u>HwInit</u>. See <u>Section 7.5.3.18</u>.</p> <p>The default value is 1111b.</p>	<u>HwInit/RsvdP</u> (see description)																
7:4	<p>Upstream Port 32.0 GT/s Transmitter Preset - Field contains the Transmit Preset value sent or received during 32.0 GT/s Link Equalization. Field usage varies as follows:</p> <table border="1"> <thead> <tr> <th></th> <th>Operating Port Direction</th> <th>Crosslink Supported</th> <th>Usage</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>Downstream Port</td> <td>Any</td> <td> <p>Field contains the value sent on the associated Lane during Link Equalization.</p> <p>Field is <u>HwInit</u>.</p> </td></tr> <tr> <td>B</td> <td>Upstream Port</td> <td>0b</td> <td> <p>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.</p> <p>Field is <u>RO</u>.</p> <p>When crosslinks are supported, case C (below) applies and this captured information is not visible to software. Vendors are encouraged to provide an alternate mechanism to obtain this information.</p> </td></tr> <tr> <td>C</td> <td>Upstream Port</td> <td>1b</td> <td> <p>Field is not used or affected by the current Link Equalization.</p> <p>Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A (above) applies.</p> </td></tr> </tbody> </table>		Operating Port Direction	Crosslink Supported	Usage	A	Downstream Port	Any	<p>Field contains the value sent on the associated Lane during Link Equalization.</p> <p>Field is <u>HwInit</u>.</p>	B	Upstream Port	0b	<p>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.</p> <p>Field is <u>RO</u>.</p> <p>When crosslinks are supported, case C (below) applies and this captured information is not visible to software. Vendors are encouraged to provide an alternate mechanism to obtain this information.</p>	C	Upstream Port	1b	<p>Field is not used or affected by the current Link Equalization.</p> <p>Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A (above) applies.</p>	<u>HwInit/RO</u> (see description)
	Operating Port Direction	Crosslink Supported	Usage															
A	Downstream Port	Any	<p>Field contains the value sent on the associated Lane during Link Equalization.</p> <p>Field is <u>HwInit</u>.</p>															
B	Upstream Port	0b	<p>Field is intended for debug and diagnostics. It contains the value captured from the associated Lane during Link Equalization.</p> <p>Field is <u>RO</u>.</p> <p>When crosslinks are supported, case C (below) applies and this captured information is not visible to software. Vendors are encouraged to provide an alternate mechanism to obtain this information.</p>															
C	Upstream Port	1b	<p>Field is not used or affected by the current Link Equalization.</p> <p>Field value will be used if a future crosslink negotiation switches the Operating Port Direction so that case A (above) applies.</p>															

Bit Location	Register Description			Attributes
	Operating Port Direction	Crosslink Supported	Usage	
			Field is HwInit.	
See Section 4.2.3 and Chapter 8 for details. The field encodings are defined in Section 4.2.3.2 .				
The default value is 1111b.				

7.7.7 Lane Margining at the Receiver Extended Capability

The [Lane Margining at the Receiver Extended Capability](#) structure must be implemented in:

- A Function associated with a Downstream Port where the [Supported Link Speeds Vector](#) field indicates support for a Link speed of 16.0 GT/s or higher.
- A Function of a single-Function Device associated with an Upstream Port where the [Supported Link Speeds Vector](#) field indicates support for a Link speed of 16.0 GT/s or higher.
- Function 0 (and only Function 0) of a [Multi-Function Device](#) associated with an Upstream Port where the [Supported Link Speeds Vector](#) field indicates support for a Link speed of 16.0 GT/s or higher.

[Figure 7-97](#) shows the layout of the Margining Extended Capability. This capability contains a pair of per-Port registers followed by a set of per-Lane registers.

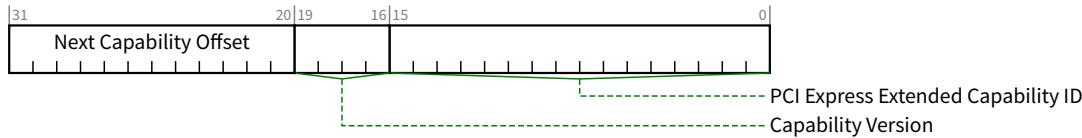
The number of per-Lane entries is determined by the [Maximum Link Width](#) (see [Section 7.5.3.6](#) or [Section 7.9.9.2](#)). Up to 32 entries are permitted regardless of the [Maximum Link Width](#). The value of entries beyond the [Maximum Link Width](#) is undefined.

Each per-Lane entry contains the values for that Lane. Lane numbering uses the default Lane number and is thus invariant to Link width and Lane reversal negotiation that occurs during Link training.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	Byte Offset
PCI Express Extended Capability Header	
Margining Port Status Register	Margining Port Capabilities Register
Margining Lane Status: Lane 0	Margining Lane Control: Lane 0
Margining Lane Status: Lane 1 (Optional)	Margining Lane Control: Lane 1 (Optional)
Margining Lane Status: Lane 2 (Optional)	Margining Lane Control: Lane 2 (Optional)
Margining Lane Status: Lane 3 (Optional)	Margining Lane Control: Lane 3 (Optional)
Margining Lane Status: Lane 4 (Optional)	Margining Lane Control: Lane 4 (Optional)
Margining Lane Status: Lane 5 (Optional)	Margining Lane Control: Lane 5 (Optional)
Margining Lane Status: Lane 6 (Optional)	Margining Lane Control: Lane 6 (Optional)
Margining Lane Status: Lane 7 (Optional)	Margining Lane Control: Lane 7 (Optional)
Margining Lane Status: Lane 8 (Optional)	Margining Lane Control: Lane 8 (Optional)
Margining Lane Status: Lane 9 (Optional)	Margining Lane Control: Lane 9 (Optional)
Margining Lane Status: Lane 10 (Optional)	Margining Lane Control: Lane 10 (Optional)
Margining Lane Status: Lane 11 (Optional)	Margining Lane Control: Lane 11 (Optional)
Margining Lane Status: Lane 12 (Optional)	Margining Lane Control: Lane 12 (Optional)
Margining Lane Status: Lane 13 (Optional)	Margining Lane Control: Lane 13 (Optional)
Margining Lane Status: Lane 14 (Optional)	Margining Lane Control: Lane 14 (Optional)
Margining Lane Status: Lane 15 (Optional)	Margining Lane Control: Lane 15 (Optional)
Margining Lane Status: Lane 16 (Optional)	Margining Lane Control: Lane 16 (Optional)
Margining Lane Status: Lane 17 (Optional)	Margining Lane Control: Lane 17 (Optional)
Margining Lane Status: Lane 18 (Optional)	Margining Lane Control: Lane 18 (Optional)
Margining Lane Status: Lane 19 (Optional)	Margining Lane Control: Lane 19 (Optional)
Margining Lane Status: Lane 20 (Optional)	Margining Lane Control: Lane 20 (Optional)
Margining Lane Status: Lane 21 (Optional)	Margining Lane Control: Lane 21 (Optional)
Margining Lane Status: Lane 22 (Optional)	Margining Lane Control: Lane 22 (Optional)
Margining Lane Status: Lane 23 (Optional)	Margining Lane Control: Lane 23 (Optional)
Margining Lane Status: Lane 24 (Optional)	Margining Lane Control: Lane 24 (Optional)
Margining Lane Status: Lane 25 (Optional)	Margining Lane Control: Lane 25 (Optional)
Margining Lane Status: Lane 26 (Optional)	Margining Lane Control: Lane 26 (Optional)
Margining Lane Status: Lane 27 (Optional)	Margining Lane Control: Lane 27 (Optional)
Margining Lane Status: Lane 28 (Optional)	Margining Lane Control: Lane 28 (Optional)
Margining Lane Status: Lane 29 (Optional)	Margining Lane Control: Lane 29 (Optional)
Margining Lane Status: Lane 30 (Optional)	Margining Lane Control: Lane 30 (Optional)
Margining Lane Status: Lane 31 (Optional)	Margining Lane Control: Lane 31 (Optional)

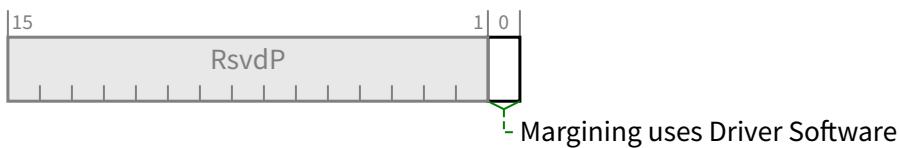
Figure 7-97 Lane Margining at the Receiver Extended Capability

7.7.7.1 Lane Margining at the Receiver Extended Capability Header (Offset 00h)

*Figure 7-98 Lane Margining at the Receiver Extended Capability Header**Table 7-79 Lane Margining at the Receiver Extended Capability Header*

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Physical Layer 16.0 GT/s Margining Extended Capability is 0027h.	<u>RO</u>
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	<u>RO</u>
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than OFFh.	<u>RO</u>

7.7.7.2 Margining Port Capabilities Register (Offset 04h)

*Figure 7-99 Margining Port Capabilities Register**Table 7-80 Margining Port Capabilities Register*

Bit Location	Register Description	Attributes
0	Margining uses Driver Software - If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining	<u>HwInit</u>

Bit Location	Register Description	Attributes
	does not require device driver software. In this case the value read from <u>Margining Software Ready</u> is undefined.	

7.7.7.3 Margining Port Status Register (Offset 06h)

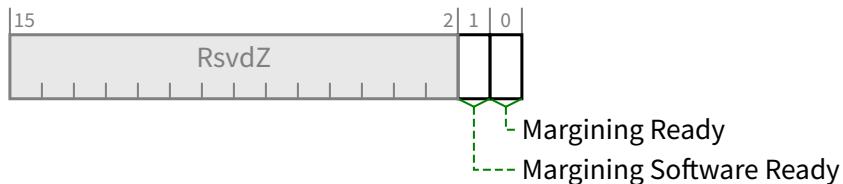


Figure 7-100 Margining Port Status Register

Table 7-81 Margining Port Status Register

Bit Location	Register Description	Attributes
0	<p>Margining Ready. - Indicates when the Margining feature is ready to accept margining commands. Behavior is undefined if this bit is Clear and, for any Lane, any of the Receiver Number, Margin Type, Usage Model, or Margin Payload fields are written (see Section 7.7.7.4).</p> <p>If Margining uses Driver Software is Set, Margining Ready must be Set no later than 100 ms after the later of Margining Software Ready becoming Set or the link training to 16.0 GT/s.</p> <p>If Margining uses Driver Software is Clear, Margining Ready must be Set no later than 100 ms after the Link trains to 16.0 GT/s.</p> <p>Default value is implementation specific.</p>	RO
1	<p>Margining Software Ready - When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization.</p> <p>The value of this bit is undefined if Margining uses Driver Software is Clear. The default value of this bit is implementation specific.</p>	RO

7.7.7.4 Margining Lane Control Register (Offset 08h)

The Margining Lane Control Register consists of control fields required for per-Lane margining.

The number of entries in this register are sized by Maximum Link Width (see Section 7.5.3.6).

See Section 4.2.7.2 for details of this register.

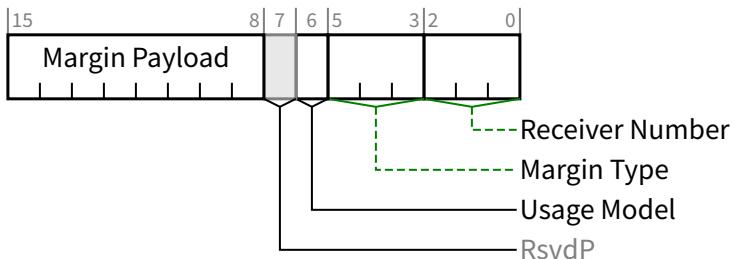


Figure 7-101 Lane N: Margining Control Register Entry

Table 7-82 Lane N: Margining Control Register Entry

Bit Location	Register Description	Attributes
2:0	<p>Receiver Number - See Section 8.4.4 for details.</p> <p>The default value is 000b.</p> <p>This field must be reset to the default value if the Port goes to DL_Down status.</p>	RW (see description)
5:3	<p>Margin Type - See Section 8.4.4 for details.</p> <p>The default value is 111b.</p> <p>This field must be reset to the default value if the Port goes to DL_Down status.</p>	RW (see description)
6	<p>Usage Model - See Section 8.4.4 for details.</p> <p>The default value is 0b.</p> <p>This field must be reset to the default value if the Port goes to DL_Down status.</p>	RW (see description)
15:8	<p>Margin Payload - See Section 8.4.4 for details.</p> <p>This field's value is used in conjunction with the Margin Type field, as described in Section 8.4.4.</p> <p>The default value is 9Ch.</p> <p>This field must be reset to the default value if the Port goes to DL_Down status.</p>	RW (see description)

7.7.7.5 Margining Lane Status Register (Offset 0Ah)

The Margining Lane Status register consists of status fields required for per-Lane margining. The number of entries in this register are sized by [Maximum Link Width](#) (see [Section 7.5.3.6](#)). See [Section 4.2.7.2](#) for details of this register.

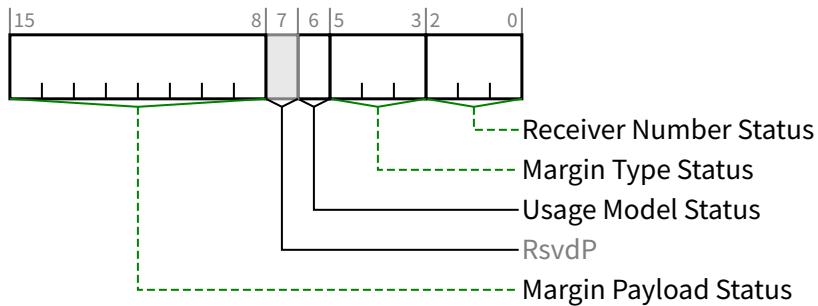


Figure 7-102 Lane N: Margining Lane Status Register Entry

Table 7-83 Lane N: Margining Lane Status Register Entry

Bit Location	Register Description	Attributes
<u>Control Fields</u>		
2:0	Receiver Number Status - See Section 8.4.4 for details. The default value is 000b. For Downstream Ports, this field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)
5:3	Margin Type Status - See Section 8.4.4 for details. The default value is 000b. This field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)
6	Usage Model Status - See Section 8.4.4 for details. The default value is 0b. This field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)
15:8	Margin Payload Status - See Section 8.4.4 for details. This field is only meaningful, when the Margin Type is a defined encoding other than 'No Command'. The default value is 00h. This field must be reset to the default value if the Port goes to DL_Down status.	RO (see description)

7.7.8 ACS Extended Capability

The ACS Extended Capability is an optional capability that provides enhanced access controls (see [Section 6.12](#)). This capability may be implemented by a Root Port, a Switch Downstream Port, or a Multi-Function Device Function. It is never applicable to a PCI Express to PCI Bridge or Root Complex Event Collector. It is not applicable to a Switch Upstream Port unless that Switch Upstream Port is a Function in a Multi-Function Device.

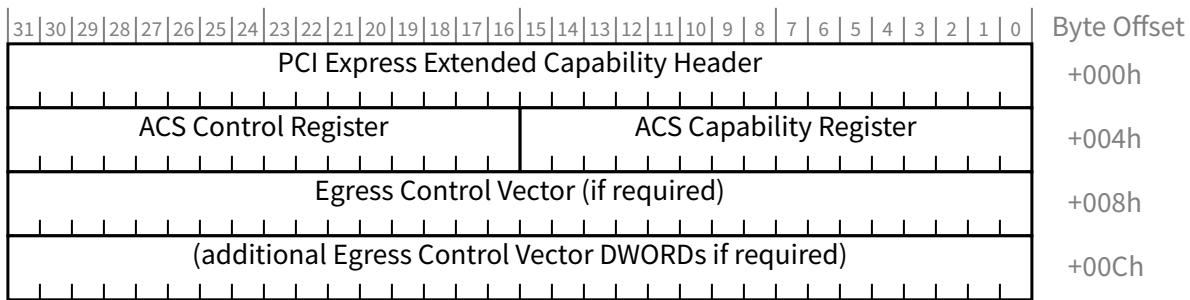


Figure 7-103 ACS Extended Capability

7.7.8.1 ACS Extended Capability Header (Offset 00h)

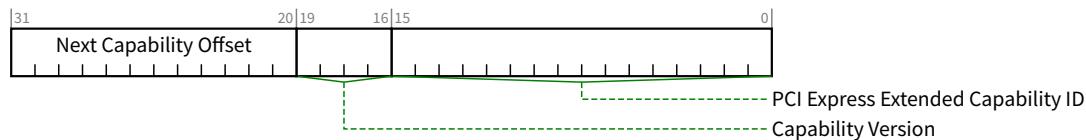


Figure 7-104 ACS Extended Capability Header

Table 7-84 ACS Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the ACS Extended Capability is 000Dh.	RO
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.7.8.2 ACS Capability Register (Offset 04h)

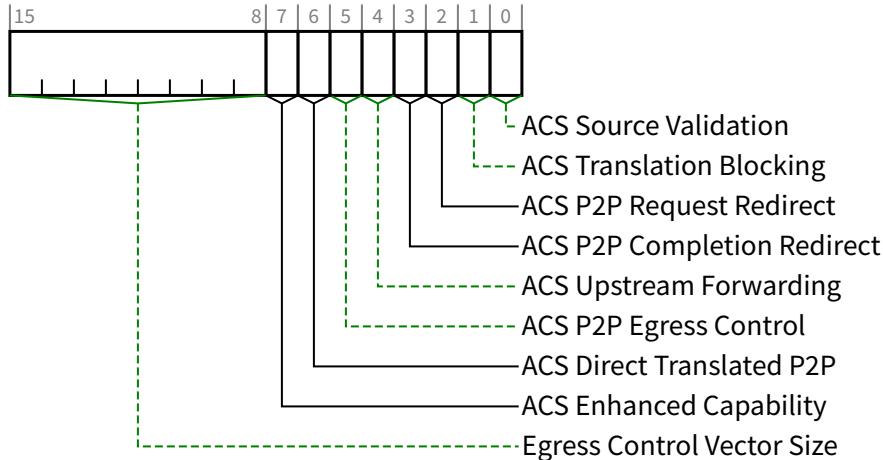


Figure 7-105 ACS Capability Register

Table 7-85 ACS Capability Register

Bit Location	Register Description	Attributes
0	ACS Source Validation - Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements <u>ACS Source Validation</u> .	<u>RO</u>
1	ACS Translation Blocking - Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements <u>ACS Translation Blocking</u> .	<u>RO</u>
2	ACS P2P Request Redirect - Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for <u>Multi-Function Device Functions</u> that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements <u>ACS P2P Request Redirect</u> .	<u>RO</u>
3	ACS P2P Completion Redirect - Required for all Functions that support <u>ACS P2P Request Redirect</u> ; must be hardwired to 0b otherwise. If 1b, indicates that the component implements <u>ACS P2P Completion Redirect</u> .	<u>RO</u>
4	ACS Upstream Forwarding - Required for Root Ports if the RC supports Redirected Request Validation; required for Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements <u>ACS Upstream Forwarding</u> .	<u>RO</u>
5	ACS P2P Egress Control - Optional for Root Ports, Switch Downstream Ports, and <u>Multi-Function Device Functions</u> ; must be hardwired to 0b otherwise. If 1b, indicates that the component implements <u>ACS P2P Egress Control</u> .	<u>RO</u>
6	ACS Direct Translated P2P - Required for Root Ports that support Address Translation Services (ATS) and also support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for <u>Multi-Function Device Functions</u> that support Address Translation Services (ATS) and also support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements <u>ACS Direct Translated P2P</u> .	<u>RO</u>

Bit Location	Register Description	Attributes
7	<p>ACS Enhanced Capability - Required for Root Ports and Switch Downstream Ports that support the ACS Enhanced Capability mechanisms.</p> <p>If Set, indicates that the component supports any of the following mechanisms:</p> <ul style="list-style-type: none"> • <u>ACS I/O Request Blocking</u> • <u>ACS DSP Memory Target Access</u> • <u>ACS USP Memory Target Access</u> • <u>ACS Unclaimed Request Redirect</u> 	RO
15:8	<p>Egress Control Vector Size - Encodings 01h-FFh directly indicate the number of applicable bits in the Egress Control Vector; the encoding 00h indicates 256 bits.</p> <p>If the ACS P2P Egress Control bit is 0b, the value of the size field is undefined, and the <u>Egress Control Vector Register</u> is not required to be present.</p>	HwInit

7.7.8.3 ACS Control Register (Offset 06h)

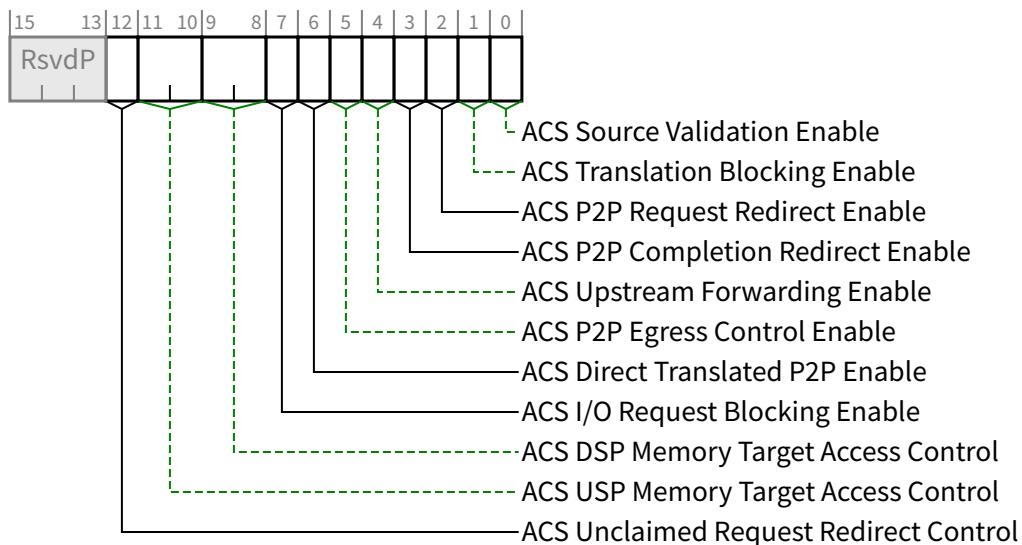


Figure 7-106 ACS Control Register

Table 7-86 ACS Control Register

Bit Location	Register Description	Attributes
0	<p>ACS Source Validation Enable - When Set, the component validates the Bus Number from the Requester ID of Upstream Requests against the secondary/subordinate Bus Numbers.</p> <p>Default value of this bit is 0b. Must be hardwired to 0b if the <u>ACS Source Validation</u> functionality is not implemented.</p>	RW

Bit Location	Register Description	Attributes
1	<p>ACS Translation Blocking Enable - When Set, the component blocks all Upstream Memory Requests whose Address Type (AT) field is not set to the default value.</p> <p>Default value of this bit is 0b. Must be hardwired to 0b if the <u>ACS Translation Blocking</u> functionality is not implemented.</p>	<u>RW</u>
2	<p>ACS P2P Request Redirect Enable - In conjunction with ACS P2P Egress Control and ACS Direct Translated P2P mechanisms, determines when the component redirects peer-to-peer Requests Upstream (see <u>Section 6.12.3</u>). Note that with Downstream Ports, this bit only applies to Upstream Requests arriving at the Downstream Port, and whose normal routing targets a different Downstream Port.</p> <p>Default value of this bit is 0b. Must be hardwired to 0b if the <u>ACS P2P Request Redirect</u> functionality is not implemented.</p>	<u>RW</u>
3	<p>ACS P2P Completion Redirect Enable - Determines when the component redirects peer-to-peer Completions Upstream; applicable only to Completions¹⁴⁶ whose Relaxed Ordering Attribute is clear.</p> <p>Default value of this bit is 0b. Must be hardwired to 0b if the <u>ACS P2P Completion Redirect</u> functionality is not implemented.</p>	<u>RW</u>
4	<p>ACS Upstream Forwarding Enable - When Set, the component forwards Upstream any Request or Completion TLPs it receives that were redirected Upstream by a component lower in the hierarchy. Note that this bit only applies to Upstream TLPs arriving at a Downstream Port, and whose normal routing targets the same Downstream Port.</p> <p>Default value of this bit is 0b. Must be hardwired to 0b if the <u>ACS Upstream Forwarding</u> functionality is not implemented.</p>	<u>RW</u>
5	<p>ACS P2P Egress Control Enable - In conjunction with the <u>Egress Control Vector</u> plus the <u>ACS P2P Request Redirect</u> and <u>ACS Direct Translated P2P</u> mechanisms, determines when to allow, disallow, or redirect peer-to-peer Requests (see <u>Section 6.12.3</u>).</p> <p>Default value of this bit is 0b. Must be hardwired to 0b if the <u>ACS P2P Egress Control</u> functionality is not implemented.</p>	<u>RW</u>
6	<p>ACS Direct Translated P2P Enable - When Set, overrides the <u>ACS P2P Request Redirect</u> and <u>ACS P2P Egress Control</u> mechanisms with peer-to-peer Memory Requests whose Address Type (AT) field indicates a Translated address (see <u>Section 6.12.3</u>).</p> <p>This bit is ignored if <u>ACS Translation Blocking Enable</u> is 1b.</p> <p>Default value of this bit is 0b. Must be hardwired to 0b if the <u>ACS Direct Translated P2P</u> functionality is not implemented.</p>	<u>RW</u>
7	<p>ACS I/O Request Blocking Enable - if Set, Upstream I/O Requests received by the Downstream Port must be handled as ACS Violations.</p> <p>This bit is required for Root Ports and Switch Downstream Ports if the <u>ACS Enhanced Capability</u> bit is Set; otherwise it must be RsvdP. The default value of this bit is 0b.</p>	<u>RW/RsvdP</u>
9:8	<p>ACS DSP Memory Target Access Control - This field controls how a Downstream Port handles Upstream Memory Requests attempting to access any Memory BAR Space on an applicable Root Port or Switch Downstream Port (including the Ingress Port). See <u>Section 6.12.1.1</u>.</p> <p>Defined Encodings are:</p> <ul style="list-style-type: none"> 00b Direct Request access enabled 01b Request blocking enabled 10b Request redirect enabled 	<u>RW/RsvdP</u>

¹⁴⁶. This includes Read Completions, AtomicOp Completions, and other Completions with or without Data.

Bit Location	Register Description	Attributes
	<p>11b Reserved This field is required for Root Ports and Switch Downstream Ports if the <u>ACS Enhanced Capability</u> bit is Set and there is applicable Memory BAR Space to protect; otherwise it must be RsvdP. The default value of this field is 00b.</p>	
11:10	<p>ACS USP Memory Target Access Control - This field controls how a Switch Downstream Port handles Upstream Memory Requests attempting to access any Memory BAR Space on the Switch Upstream Port. See <u>Section 6.12.1.1</u>.</p> <p>Defined Encodings are:</p> <ul style="list-style-type: none"> 00b Direct Request access enabled 01b Request blocking enabled 10b Request redirect enabled 11b Reserved <p>This field is required for Root Ports and Switch Downstream Ports if the <u>ACS Enhanced Capability</u> bit is Set and there is applicable Memory BAR Space to protect; otherwise it must be RsvdP. The default value of this field is 00b.</p>	RW/RsvdP
12	<p>ACS Unclaimed Request Redirect Control - Controls how a Switch Downstream Port handles incoming Requests targeting Memory Space within the Memory aperture of the Switch Upstream Port that is not within a Memory aperture or Memory BAR Space of any Downstream Port within the Switch.</p> <p>When Set, the Switch must forward such Requests Upstream out of the Switch.</p> <p>When Clear, the Switch Downstream Port must handle such Requests as an Unsupported Request (UR).</p> <p>This bit is required for Switch Downstream Ports if the <u>ACS Enhanced Capability</u> bit is Set; otherwise it must be RsvdP. The default value of this bit is 0b.</p>	RW/RsvdP

7.7.8.4 Egress Control Vector Register (Offset 08h)

The Egress Control Vector is a read-write register that contains a bit-array. The number of bits in the register is specified by the Egress Control Vector Size field, and the register spans multiple DWORDs if required. If the ACS P2P Egress Control bit in the ACS Capability Register is 0b, the Egress Control Vector Size field is undefined and the Egress Control Vector Register is not required to be present.

For the general case of an Egress Control Vector spanning multiple DWORDs, the DWORD offset and bit number within that DWORD for a given arbitrary bit K are specified by the formulas¹⁴⁷:

$$\text{DWORD offset} = 08h + (K \text{ div } 32) \times 4$$

$$\text{DWORD bit\#} = K \bmod 32$$

Equation 7-4 Egress Control Vector Access

Bits in a DWORD beyond those specified by the Egress Control Vector Size field are RsvdP.

For Root Ports and Switch Downstream Ports, each bit in the bit-array always corresponds to a Port Number. Otherwise, for Functions¹⁴⁸ within a Multi-Function Device, each bit in the bit-array corresponds to one or more Function Numbers, or a Function Group Number. For example, access to Function 2 is controlled by bit number 2 in the bit-array. For both

147. Div is an integer divide with truncation. Mod is the remainder from an integer divide.

148. Including Switch Upstream Ports.

Port Number cases and Function Number cases, the bit corresponding to the Function that implements this Extended Capability structure must be hardwired to 0b.¹⁴⁹

If an ARI Device implements ACS Function Groups (ACS Function Groups Capability is Set), its Egress Control Vector Size is required to be a power-of-2 from 8 to 256, and all of its implemented Egress Control Vector bits must be RW. With ARI Devices, multiple Functions can be associated with a single bit, so for each Function, its associated bit determines how Requests from it targeting other Functions (if any) associated with the same bit are handled.

If ACS Function Groups are enabled in an ARI Device (ACS Function Groups Enable is Set), the first 8 Egress Control Vector bits in each Function are associated with Function Group Numbers instead of Function Numbers. In this case, access control is enforced between Function Groups instead of Functions, and any implemented Egress Control Vector bits beyond the first 8 are unused.

Independent of whether an ARI Device implements ACS Function Groups, its Egress Control Vector Size is not required to cover the entire Function Number range of all Functions implemented by the Device. If ACS Function Groups are not enabled, Function Numbers are mapped to implemented Egress Control Vector bits by taking the modulo of the Egress Control Vector Size, which is constrained to be a power-of-2.

With RCs, some Port Numbers may refer to internal Ports instead of Root Ports. For Root Ports in such RCs, each bit in the bit-array that corresponds to an internal Port must be hardwired to 0b.

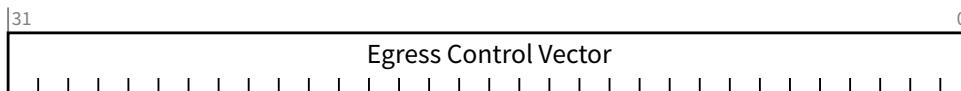


Figure 7-107 Egress Control Vector Register

Table 7-87 Egress Control Vector Register

Bit Location	Register Description	Attributes
31:0	<p>Egress Control Vector - An N-bit bit-array configured by software, where N is given by the value in the <u>Egress Control Vector Size</u> field. When a given bit is set, peer-to-peer Requests targeting the associated Port, Function, or <u>Function Group</u> are blocked or redirected (if enabled) (see <u>Section 6.12.3</u>).</p> <p><u>Figure 7-107</u> shows a single DWORD register. This register is always an integral number of DWORDs.</p> <p>Default value of each bit is 0b.</p>	<u>RW</u>

The following examples illustrate how the vector might be configured:

- For an 8-Port Switch, each Port will have a separate vector indicating which Downstream Egress Ports it may forward Requests to.
Port 1 being not allowed to communicate with any other Downstream Ports would be configured as:
1111 1100b with bit 0 corresponding to the Upstream Port (hardwired to 0b) and bit 1 corresponding to the Ingress Port (hardwired to 0b).
Port 2 being allowed to communicate with Ports 3, 5, and 7 would be configured as: 0101 0010b.
- For a 4-Function device, each Function will have a separate vector that indicates which Function it may forward Requests to.
Function 0 being not allowed to communicate with any other Functions would be configured as: 1110b with bit 0 corresponding to Function 0 (hardwired to 0b).

¹⁴⁹. For ARI Devices, the bit must be RW. See subsequent description.

Function 1 being allowed to communicate with Functions 2 and 3 would be configured as: 0001b with bit 1 corresponding to Function 1 (hardwired to 0b).

7.8 Common PCI and PCIe Capabilities

This section, contains a description of common PCI and PCIe capabilities that are individually optional in this but may be required by other PCISIG specifications.

7.8.1 Power Budgeting Extended Capability

The Power Budgeting Extended Capability allows the system to allocate power to devices that are added to the system at runtime. Through this Capability, a device can report the power it consumes on a variety of power rails, in a variety of device power-management states, in a variety of operating conditions. The system can use this information to ensure that the system is capable of providing the proper power and cooling levels to the device. Failure to indicate proper device power consumption may risk device or system failure.

Implementation of the Power Budgeting Extended Capability is optional for PCI Express devices that are implemented either in a form factor which does not require Hot-Plug support, or that are integrated on the system board. PCI Express form factor specifications may require support for power budgeting. Figure 7-108 details allocation of register fields in the Power Budgeting Extended Capability.

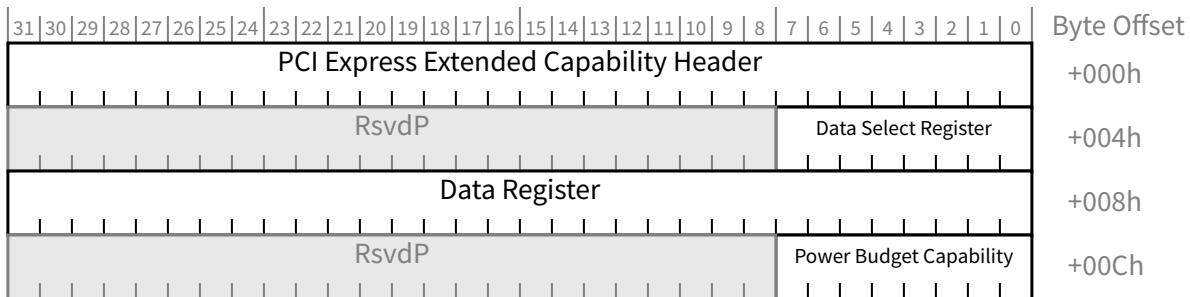


Figure 7-108 Power Budgeting Extended Capability

7.8.1.1 Power Budgeting Extended Capability Header (Offset 00h)

Figure 7-109 details allocation of register fields in the Power Budgeting Extended Capability Header; Table 7-88 provides the respective bit definitions. Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. The Extended Capability ID for the Power Budgeting Extended Capability is 0004h.

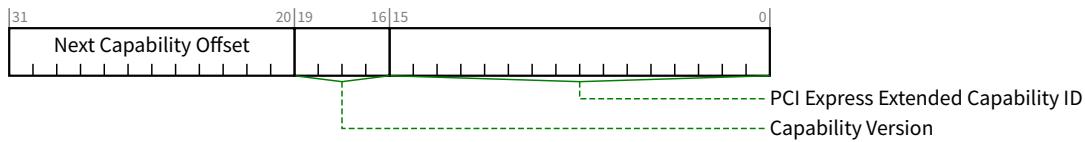


Figure 7-109 Power Budgeting Extended Capability Header

Table 7-88 Power Budgeting Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Power Budgeting Extended Capability is 0004h.	RO
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than OFFh.	RO

7.8.1.2 Power Budgeting Data Select Register (Offset 04h)

The Power Budgeting Data Select Register is an 8-bit read-write register that indexes the Power Budgeting Data reported through the Power Budgeting Data Register and selects the DWORD of Power Budgeting Data that is to appear in the Power Budgeting Data Register. Values for this register start at zero to select the first DWORD of Power Budgeting Data; subsequent DWORDs of Power Budgeting Data are selected by increasing index values. The default value of this register is undefined.

7.8.1.3 Power Budgeting Data Register (Offset 08h)

This read-only register returns the DWORD of Power Budgeting Data selected by the Power Budgeting Data Select Register. Each DWORD of the Power Budgeting Data describes the power usage of the device in a particular operating condition. Power Budgeting Data for different operating conditions is not required to be returned in any particular order, as long as incrementing the Power Budgeting Data Select Register causes information for a different operating condition to be returned. If the Power Budgeting Data Select Register contains a value greater than or equal to the number of operating conditions for which the device provides power information, this register must return all zeros. The default value of this register is undefined. Figure 7-110 details allocation of register fields in the Power Budgeting Data Register; Table 7-89 provides the respective bit definitions.

The Base Power and Data Scale fields describe the power usage of the device; the Power Rail, Type, PM State, and PM Sub State fields describe the conditions under which the device has this power usage.

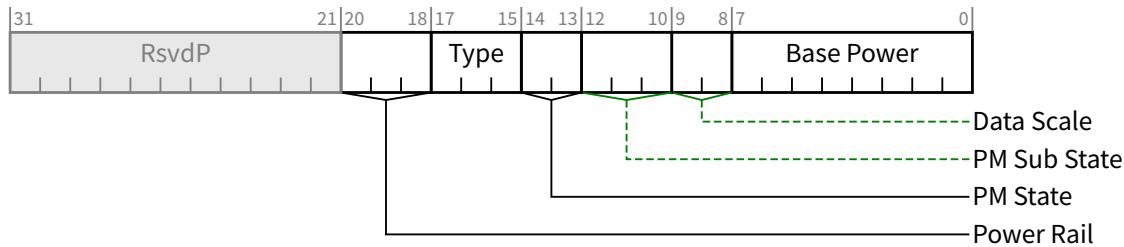


Figure 7-110 Power Budgeting Data Register

Table 7-89 Power Budgeting Data Register

Bit Location	Register Description	Attributes
7:0	<p>Base Power - Specifies in watts the base power value in the given operating condition. This value must be multiplied by the data scale to produce the actual power consumption value except when the <u>Data Scale</u> field equals 00b (1.0x) and <u>Base Power</u> exceeds EFh, the following alternative encodings are used:</p> <ul style="list-style-type: none"> F0h greater than 239 W and less than or equal to 250 W Slot Power Limit F1h greater than 250 W and less than or equal to 275 W Slot Power Limit F2h greater than 275 W and less than or equal to 300 W Slot Power Limit F3h to FFh Reserved for values greater than 300 W 	<u>RO</u>
9:8	<p>Data Scale - Specifies the scale to apply to the <u>Base Power</u> value. The power consumption of the device is determined by multiplying the contents of the <u>Base Power</u> field with the value corresponding to the encoding returned by this field, except as noted above.</p> <p>Defined encodings are:</p> <ul style="list-style-type: none"> 00b 1.0x 01b 0.1x 10b 0.01x 11b 0.001x 	<u>RO</u>
12:10	<p>PM Sub State - Specifies the power management sub state of the operating condition being described.</p> <p>Defined encodings are:</p> <ul style="list-style-type: none"> 000b Default Sub State 001b - 111b Device Specific Sub State 	<u>RO</u>
14:13	<p>PM State - Specifies the power management state of the operating condition being described.</p> <p>Defined encodings are:</p> <ul style="list-style-type: none"> 00b D0 01b D1 10b D2 11b D3 <p>A device returns 11b in this field and Aux or PME Aux in the Type field to specify the <u>D3Cold PM State</u>. An encoding of 11b along with any other <u>Type</u> field value specifies the <u>D3Hot state</u>.</p>	<u>RO</u>

Bit Location	Register Description	Attributes
17:15	<p>Type - Specifies the type of the operating condition being described. Defined encodings are:</p> <ul style="list-style-type: none"> 000b PME Aux 001b Auxiliary 010b Idle 011b Sustained 100b Sustained - Emergency Power Reduction State (see Section 6.25) 101b Maximum - Emergency Power Reduction State (see Section 6.25) 111b Maximum Others All other encodings are Reserved. 	<u>RO</u>
20:18	<p>Power Rail - Specifies the thermal load or power rail of the operating condition being described.</p> <p>Defined encodings are:</p> <ul style="list-style-type: none"> 000b Power (12V) 001b Power (3.3V) 010b Power (1.5V or 1.8V) 111b Thermal Others All other encodings are Reserved. 	<u>RO</u>

A device that implements the Power Budgeting Extended Capability is required to provide data values for the D0 Maximum and D0 Sustained PM State and Type combinations for every power rail from which it consumes power; data for the D0 Maximum and D0 Sustained for Thermal must also be provided if these values are different from the sum of the values for an operating condition reported for D0 Maximum and D0 Sustained on the power rails.

Devices that support auxiliary power or PME from auxiliary power must provide data for the appropriate power Type (Auxiliary or PME Aux).

If a device implements Emergency Power Reduction State, it must report Power Budgeting values for the following:

- Maximum Emergency Power Reduction State, PM State D0, all power rails used by the device
- Maximum Emergency Power Reduction State, PM State D0, Thermal (if different from the sum of the preceding values)
- Sustained Emergency Power Reduction State, PM State D0, all power rails used by the device
- Sustained Emergency Power Reduction State, PM State: D0, Thermal (if different from the sum of the preceding values)

7.8.1.4 Power Budgeting Capability Register (Offset 0Ch)

This register indicates the power budgeting capabilities of a device. Figure 7-111 details allocation of register fields in the Power Budgeting Capability Register; Table 7-90 provides the respective bit definitions.

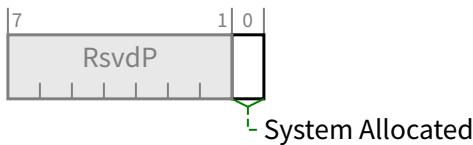


Figure 7-111 Power Budgeting Capability Register

Table 7-90 Power Budgeting Capability Register

Bit Location	Register Description	Attributes
0	System Allocated - When Set, this bit indicates that the power budget for the device is included within the system power budget. Reported <u>Power Budgeting Data</u> for this device must be ignored by software for power budgeting decisions if this bit is Set.	<u>HwInit</u>

7.8.2 Latency Tolerance Reporting (LTR) Extended Capability

The PCI Express Latency Tolerance Reporting (LTR) Extended Capability is an optional Extended Capability that allows software to provide platform latency information to components with Upstream Ports (Endpoints and Switches), and is required for Switch Upstream Ports and Endpoints if the Function supports the LTR mechanism. It is not applicable to Root Ports, Bridges, or Switch Downstream Ports.

For a Multi-Function Device associated with the Upstream Port of a component that implements the LTR mechanism, this Capability structure must be implemented only in Function 0, and must control the component's Link behavior on behalf of all the Functions of the Device.

RCiEPs implemented as Multi-Function Devices are permitted to implement this Capability structure in more than one Function of the Multi-Function Device.

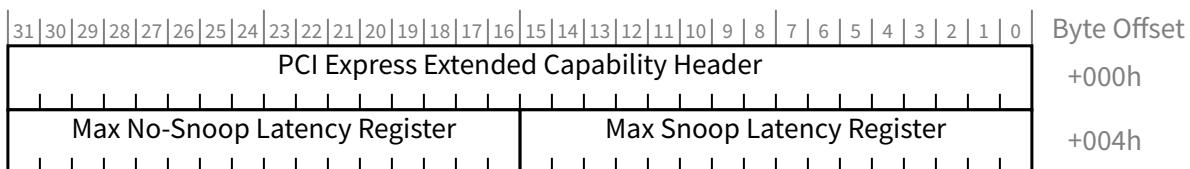


Figure 7-112 LTR Extended Capability Structure

7.8.2.1 LTR Extended Capability Header (Offset 00h)

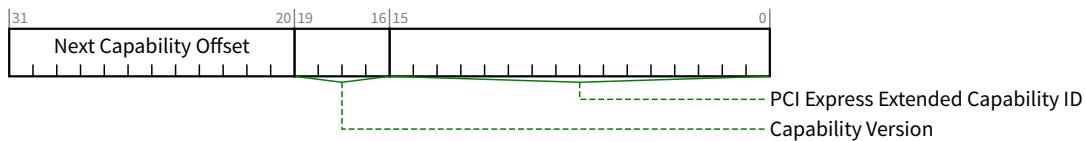


Figure 7-113 LTR Extended Capability Header

Table 7-91 LTR Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability for the LTR Extended Capability is 0018h.	<u>RO</u>
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	<u>RO</u>
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	<u>RO</u>

7.8.2.2 Max Snoop Latency Register (Offset 04h)

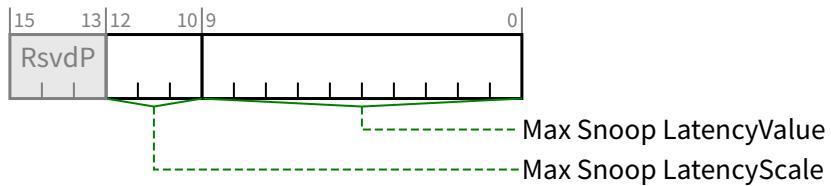


Figure 7-114 Max Snoop Latency Register

Table 7-92 Max Snoop Latency Register

Bit Location	Register Description	Attributes
9:0	Max Snoop LatencyValue - Along with the Max Snoop LatencyScale field, this register specifies the maximum snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms. The default value for this field is 00 0000 0000b.	<u>RW</u>

Bit Location	Register Description	Attributes
12:10	<p>Max Snoop LatencyScale - This register provides a scale for the value contained within the <u>Max Snoop LatencyValue</u> field. Encoding is the same as the LatencyScale fields in the LTR Message. See <u>Section 6.18</u>. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms.</p> <p>The default value for this field is 000b.</p> <p>Hardware operation is undefined if software writes a Not Permitted value to this field.</p>	RW

7.8.2.3 Max No-Snoop Latency Register (Offset 06h)

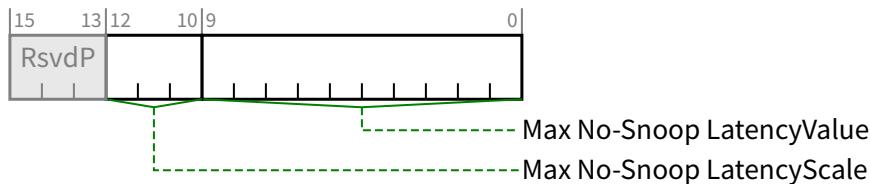


Figure 7-115 Max No-Snoop Latency Register

Table 7-93 Max No-Snoop Latency Register

Bit Location	Register Description	Attributes
9:0	<p>Max No-Snoop LatencyValue - Along with the <u>Max No-Snoop LatencyScale</u> field, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms.</p> <p>The default value for this field is 00 0000 0000b.</p>	RW
12:10	<p>Max No-Snoop LatencyScale - This register provides a scale for the value contained within the <u>Max No-Snoop LatencyValue</u> field. Encoding is the same as the LatencyScale fields in the LTR Message. See <u>Section 6.18</u>. It is strongly recommended that any updates to this field are reflected in LTR Message(s) sent by the device within 1 ms.</p> <p>The default value for this field is 000b.</p> <p>Hardware operation is undefined if software writes a Not Permitted value to this field.</p>	RW

7.8.3 L1 PM Substates Extended Capability

The L1 PM Substates Extended Capability is an optional Extended Capability, that is required if L1 PM Substates is implemented at a Port. The L1 PM Substates Extended Capability structure is defined as shown in Figure 7-116.

For a Multi-Function Device associated with an Upstream Port implementing L1 PM Substates, this Extended Capability Structure must be implemented only in Function 0, and must control the Upstream Port's Link behavior on behalf of all the Functions of the device.

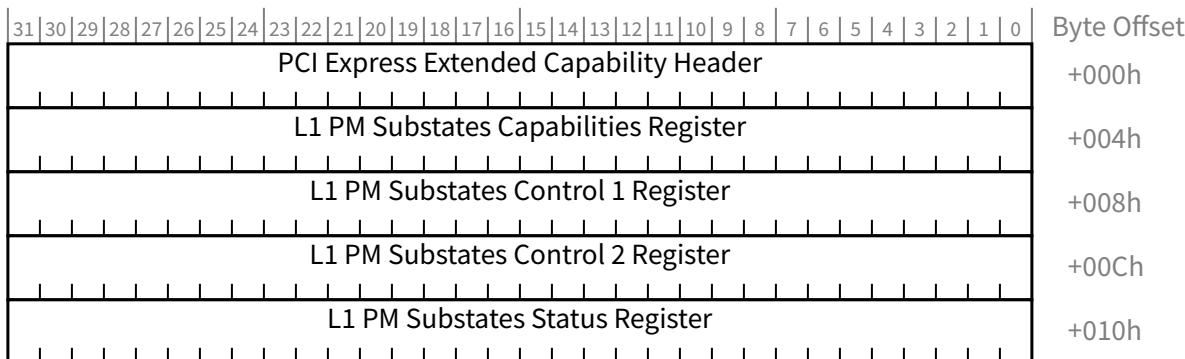


Figure 7-116 L1 PM Substates Extended Capability

7.8.3.1 L1 PM Substates Extended Capability Header (Offset 00h)

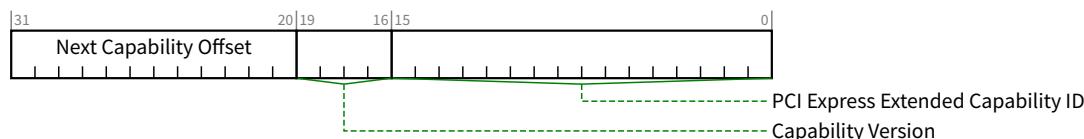


Figure 7-117 L1 PM Substates Extended Capability Header

Table 7-94 L1 PM Substates Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for L1 PM Substates is 001Eh.	RO
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the <u>L1 PM Substates Status Register</u> is implemented and must be 1h otherwise.	RO
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than OFFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b although software must mask them to allow for future uses of these bits.	RO

7.8.3.2 L1 PM Substates Capabilities Register (Offset 04h)

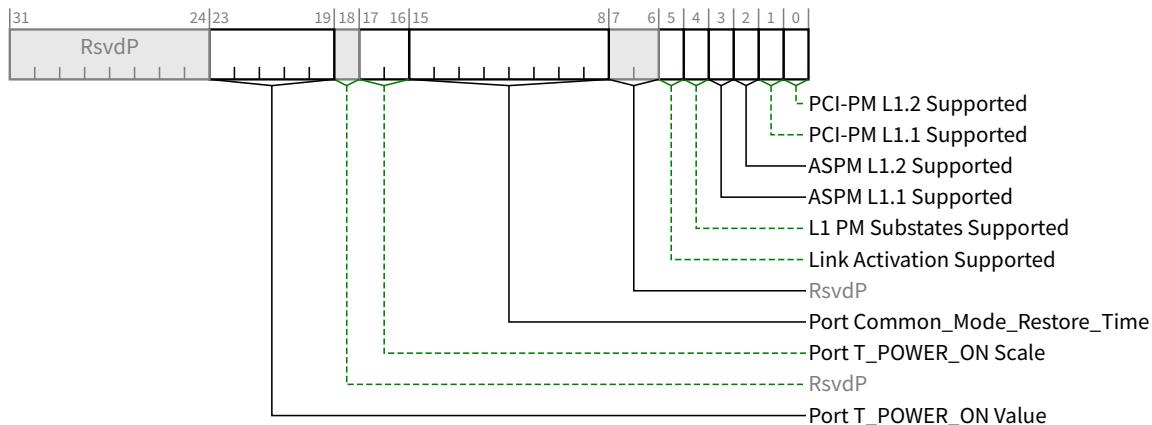


Figure 7-118 L1 PM Substates Capabilities Register

Table 7-95 L1 PM Substates Capabilities Register

Bit Location	Register Description	Attributes
0	PCI-PM L1.2 Supported - When Set this bit indicates that PCI-PM L1.2 is supported.	<u>HwInit</u>
1	PCI-PM L1.1 Supported - When Set this bit indicates that PCI-PM L1.1 is supported, and must be Set by all Ports implementing L1 PM Substates.	<u>HwInit</u>
2	ASPM L1.2 Supported - When Set this bit indicates that ASPM L1.2 is supported.	<u>HwInit</u>
3	ASPM L1.1 Supported - When Set this bit indicates that ASPM L1.1 is supported.	<u>HwInit</u>
4	L1 PM Substates Supported - When Set this bit indicates that this Port supports L1 PM Substates.	<u>HwInit</u>
5	Link Activation Supported - For Downstream Ports, when Set, this bit indicates that this Port supports Link Activation. See Section 5.5.6 for details. This bit is of type RsvdP for Upstream Ports.	<u>HwInit/RsvdP</u>
15:8	Port Common_Mode_Restore_Time - Time (in μ s) required for this Port to re-establish common mode as described in Table 5-11. Required for all Ports for which either the <u>PCI-PM L1.2 Supported</u> bit is Set, <u>ASPM L1.2 Supported</u> bit is Set, or both are Set, otherwise this field is of type RsvdP.	<u>HwInit/RsvdP</u> (See description)
17:16	Port T_POWER_ON Scale - Specifies the scale used for the <u>Port T_POWER_ON Value</u> field in the L1 PM Substates Capabilities Register. Range of Values 00b 2 μ s 01b 10 μ s 10b 100 μ s 11b Reserved	<u>HwInit/RsvdP</u>

Bit Location	Register Description	Attributes
	<p>Required for all Ports for which either the <u>PCI-PM L1.2 Supported</u> bit is Set, <u>ASPM L1.2 Supported</u> bit is Set, or both are Set, otherwise this field is of type <u>RsvdP</u>.</p> <p>Default value is 00b</p>	
23:19	<p>Port T_POWER_ON Value - Along with the <u>Port T_POWER_ON Scale</u> field in the <u>L1 PM Substates Capabilities Register</u> sets the time (in μs) that this Port requires the port on the opposite side of Link to wait in <u>L1.2.Exit</u> after sampling CLKREQ# asserted before actively driving the interface.</p> <p>The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the <u>Port T_POWER_ON Scale</u> field in the <u>L1 PM Substates Capabilities Register</u>.</p> <p>Default value is 00101b</p> <p>Required for all Ports for which either the <u>PCI-PM L1.2 Supported</u> bit is Set, <u>ASPM L1.2 Supported</u> bit is Set, or both are Set, otherwise this field is of type <u>RsvdP</u>.</p>	HwInit/RsvdP

7.8.3.3 L1 PM Substates Control 1 Register (Offset 08h)

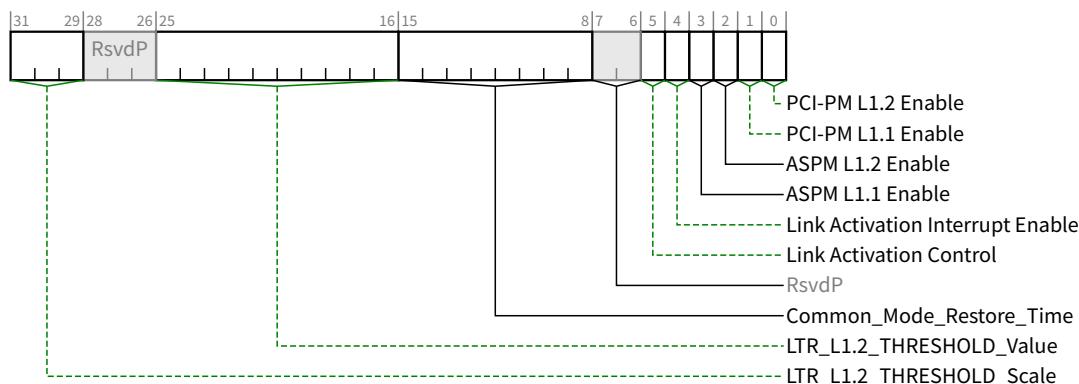


Figure 7-119 L1 PM Substates Control 1 Register

Table 7-96 L1 PM Substates Control 1 Register

Bit Location	Register Description	Attributes
0	<p>PCI-PM L1.2 Enable - When Set this bit enables PCI-PM L1.2.</p> <p>Required for both Upstream and Downstream Ports. For Ports for which the <u>PCI-PM L1.2 Supported</u> bit is Clear this bit is permitted to be hardwired to 0.</p> <p>For compatibility with possible future extensions, software must not enable L1 PM Substates unless the <u>L1 PM Substates Supported</u> bit in the <u>L1 PM Substates Capabilities Register</u> is Set.</p> <p>Default value is 0b.</p>	RW
1	<p>PCI-PM L1.1 Enable - When Set this bit enables PCI-PM L1.1.</p> <p>Required for both Upstream and Downstream Ports.</p> <p>For compatibility with possible future extensions, software must not enable L1 PM Substates unless the <u>L1 PM Substates Supported</u> bit in the <u>L1 PM Substates Capabilities Register</u> is Set.</p> <p>Default value is 0b.</p>	RW

Bit Location	Register Description	Attributes
2	<p>ASPM L1.2 Enable - When Set this bit enables ASPM L1.2. Required for both Upstream and Downstream Ports. For Ports for which the <u>ASPM L1.2 Supported</u> bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the <u>L1 PM Substates Supported</u> bit in the <u>L1 PM Substates Capabilities Register</u> is Set. Default value is 0b.</p>	RW
3	<p>ASPM L1.1 Enable - When Set this bit enables ASPM L1.1. Required for both Upstream and Downstream Ports. For Ports for which the <u>ASPM L1.1 Supported</u> bit is Clear this bit is permitted to be hardwired to 0. For compatibility with possible future extensions, software must not enable L1 PM Substates unless the <u>L1 PM Substates Supported</u> bit in the <u>L1 PM Substates Capabilities Register</u> is Set. Default value is 0b.</p>	RW
4	<p>Link Activation Interrupt Enable - When set this bit enables the generation of an interrupt to indicate the completion of the <u>Link Activation</u> process. See <u>Section 5.5.6</u> for details. Required for Downstream Ports when the <u>Link Activation Supported</u> bit is Set, otherwise it is permitted to be hardwired to 0b. Must be <u>RsvdP</u> for Upstream Ports. Default value is 0b.</p>	RW/RsvdP
5	<p>Link Activation Control - When this bit is Set, the Port must initiate the <u>Link Activation</u> process. See <u>Section 5.5.6</u> for details. Required for Downstream Ports when the <u>Link Activation Supported</u> bit is Set, otherwise it is permitted to be hardwired to 0b. Must be <u>RsvdP</u> for Upstream Ports. Default value is 0b.</p>	RW/RsvdP
15:8	<p>Common_Mode_Restore_Time - Sets value of $T_{COMMONMODE}$ (in μs), which must be used by the Downstream Port for timing the re-establishment of common mode, as described in <u>Table 5-11</u>. This field must only be modified when the <u>ASPM L1.2 Enable</u> and <u>PCI-PM L1.2 Enable</u> bits are both Clear. The Port behavior is undefined if this field is modified when either the <u>ASPM L1.2 Enable</u> and/or <u>PCI-PM L1.2 Enable</u> bit(s) are Set. Required for Downstream Ports for which either the <u>PCI-PM L1.2 Supported</u> bit is Set, <u>ASPM L1.2 Supported</u> bit is Set, or both are Set, otherwise this field is of type <u>RsvdP</u>. This field is of type <u>RsvdP</u> for Upstream Ports. Default value is implementation specific.</p>	RW/RsvdP (See Description)
25:16	<p>LTR_L1.2_THRESHOLD_Value - Along with the <u>LTR_L1.2_THRESHOLD_Scale</u>, this field indicates the LTR threshold used to determine if entry into <u>L1</u> results in <u>L1.1</u> (if enabled) or <u>L1.2</u> (if enabled). The default value for this field is 00 0000 0000b. This field must only be modified when the <u>ASPM L1.2 Enable</u> bit is Clear. The Port behavior is undefined if this field is modified when the <u>ASPM L1.2 Enable</u> bit is Set. Required for all Ports for which the <u>ASPM L1.2 Supported</u> bit is Set, otherwise this field is of type <u>RsvdP</u>.</p>	RW/RsvdP (See Description)

Bit Location	Register Description	Attributes
31:29	<p>LTR_L1.2_THRESHOLD_Scale - This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. Encoding is the same as the LatencyScale fields in the LTR Message (see Section 6.18).</p> <p>The default value for this field is 000b.</p> <p>Hardware operation is undefined if software writes a Not-Permitted value to this field.</p> <p>This field must only be modified when the ASPM L1.2 Enable bit is Clear. The Port behavior is undefined if this field is modified when the <u>ASPM L1.2 Enable</u> bit is Set.</p> <p>Required for all Ports Ports for which the <u>ASPM L1.2 Supported</u> bit is Set, otherwise this field is of type RsvdP.</p>	RW/RsvdP (See description)

7.8.3.4 L1 PM Substates Control 2 Register (Offset 0Ch)

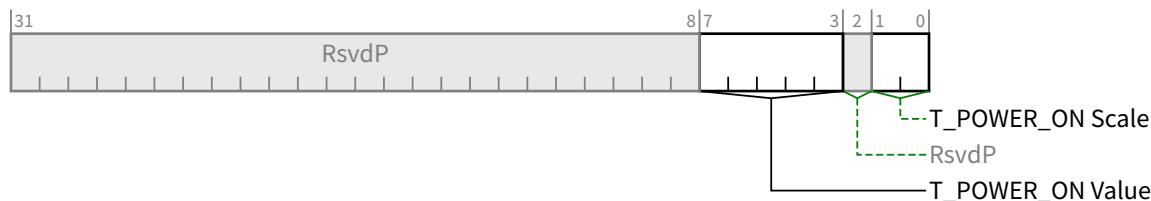


Figure 7-120 L1 PM Substates Control 2 Register

Table 7-97 L1 PM Substates Control 2 Register

Bit Location	Register Description	Attributes
1:0	<p>T_POWER_ON Scale - Specifies the scale used for <u>T_POWER_ON Value</u>.</p> <p>Range of Values:</p> <ul style="list-style-type: none"> 00b 2 µs 01b 10 µs 10b 100 µs 11b Reserved <p>Required for all Ports that support L1.2, otherwise this field is of type RsvdP.</p> <p>This field must only be modified when the <u>ASPM L1.2 Enable</u> and <u>PCI-PM L1.2 Enable</u> bits are both Clear. The Port behavior is undefined if this field is modified when either the <u>ASPM L1.2 Enable</u> and/or <u>PCI-PM L1.2 Enable</u> bit(s) are Set.</p> <p>Default value is 00b</p>	RW/RsvdP
7:3	<p>T_POWER_ON Value - Along with the <u>T_POWER_ON Scale</u> sets the minimum amount of time (in µs) that the Port must wait in <u>L1.2.Exit</u> after sampling CLKREQ# asserted before actively driving the interface.</p> <p>T_POWER_ON is calculated by multiplying the value in this field by the value in the <u>T_POWER_ON Scale</u> field.</p> <p>This field must only be modified when the <u>ASPM L1.2 Enable</u> and <u>PCI-PM L1.2 Enable</u> bits are both Clear. The Port behavior is undefined if this field is modified when either the <u>ASPM L1.2 Enable</u> and/or <u>PCI-PM L1.2 Enable</u> bit(s) are Set.</p>	RW/RsvdP

Bit Location	Register Description	Attributes
	<p>Default value is 00101b</p> <p>Required for all Ports that support L1.2, otherwise this field is of type RsvdP.</p>	

7.8.3.5 L1 PM Substates Status Register (Offset 10h)

Hardware must implement this register if the Capability Version in the L1 PM Substates Extended Capability Header is 2h or greater. This register is not present if the Capability Version is 1h.

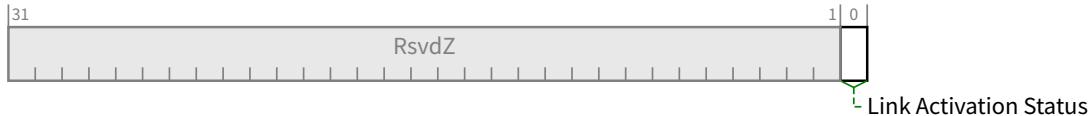


Figure 7-121 L1 PM Substates Status Register

Table 7-98 L1 PM Substates Status Register

Bit Location	Register Description	Attributes
0	<p>Link Activation Status - Indicates the status of Link Activation. See Section 5.5.6 for details.</p> <p>Required for Downstream Ports when the Link Activation Supported bit is Set, otherwise it is hardwired to 0b.</p> <p>Must be RsvdZ for Upstream Ports.</p> <p>Default value is 0b.</p>	RW1C/RsvdZ

7.8.4 Advanced Error Reporting Extended Capability

The PCI Express Advanced Error Reporting Capability is an optional Extended Capability that may be implemented by PCI Express device Functions supporting advanced error control and reporting. The Advanced Error Reporting Capability structure definition has additional interpretation for Root Ports and Root Complex Event Collectors; software must interpret the Device/Port Type field in the PCI Express Capabilities register to determine the availability of additional registers for Root Ports and Root Complex Event Collectors.

Figure 7-122 shows the PCI Express Advanced Error Reporting Extended Capability structure.

Note that if an error reporting bit field is marked as optional in the error registers, the bits must be implemented or not implemented as a group across the Status, Mask and Severity registers. In other words, a Function is required to implement the same error bit fields in corresponding Status, Mask and Severity registers. Bits corresponding to bit fields that are not implemented must be hardwired to 0, unless otherwise specified.

Except for Root Ports and Root Complex Event Collectors, if the End-End TLP Prefix Supported bit is Set, the Root Error Command and Error Source Identification Registers must be RsvdP and the Root Error Status Register must be RsvdZ.

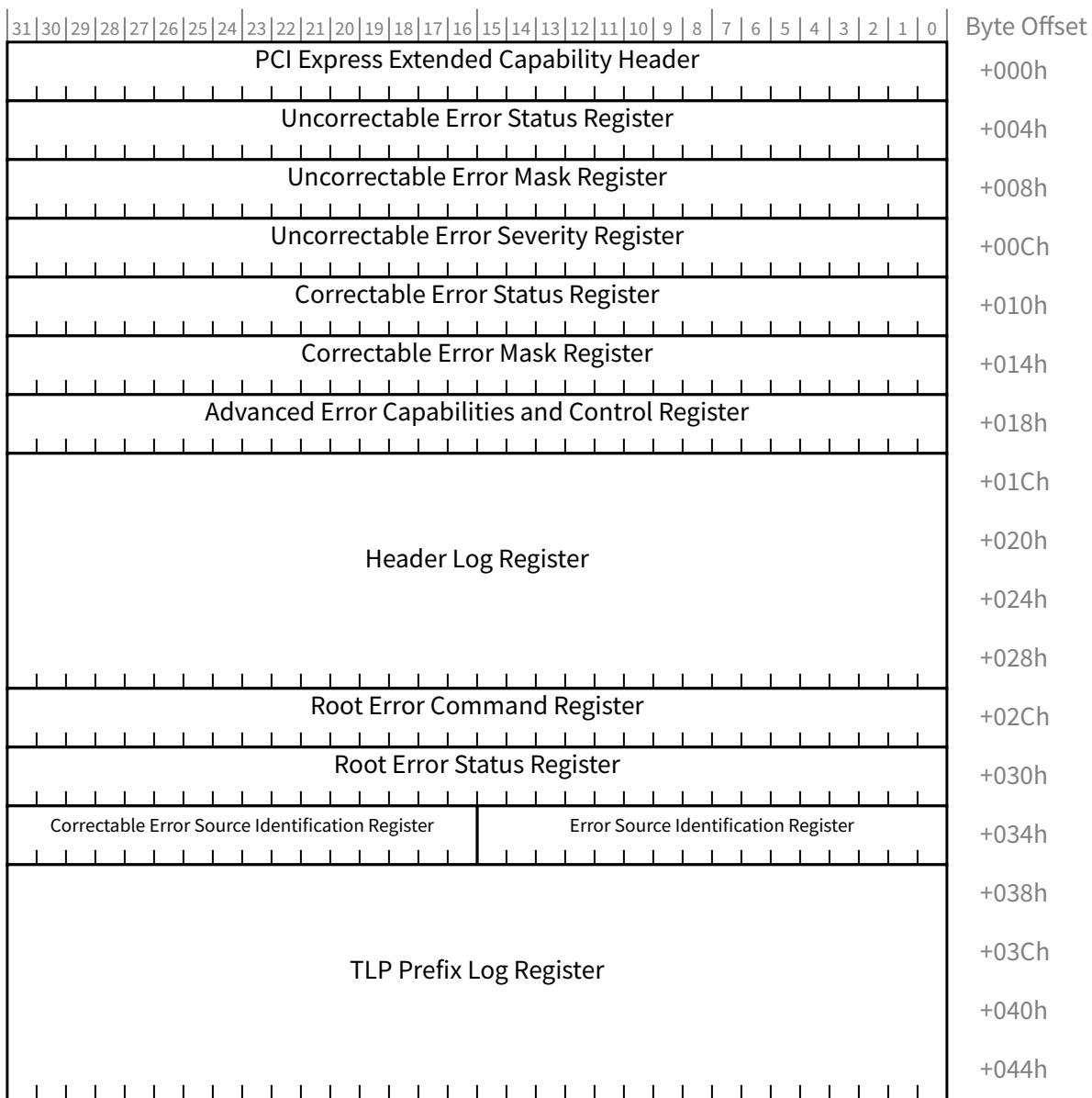


Figure 7-122 Advanced Error Reporting Extended Capability Structure

7.8.4.1 Advanced Error Reporting Extended Capability Header (Offset 00h)

Figure 7-123 details the allocation of register fields of an Advanced Error Reporting Extended Capability header; Table 7-99 provides the respective bit definitions.

Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h.



Figure 7-123 Advanced Error Reporting Extended Capability Header

Table 7-99 Advanced Error Reporting Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. The Extended Capability ID for the Advanced Error Reporting Capability is 0001h.	<u>RO</u>
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. This field must be 2h if the End-End TLP Prefix Supported bit (see Section 7.5.3.15) is Set and must be 1h or 2h otherwise.	<u>RO</u>
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh.	<u>RO</u>

7.8.4.2 Uncorrectable Error Status Register (Offset 04h)

The Uncorrectable Error Status Register indicates error detection status of individual errors on a PCI Express device Function. An individual error status bit that is Set indicates that a particular error was detected; software may clear an error status by writing a 1b to the respective bit. Refer to [Section 6.2](#) for further details. Register bits not implemented by the Function are hardwired to 0b. [Figure 7-124](#) details the allocation of register fields of the [Uncorrectable Error Status Register](#); [Section 7.8.4.2](#) provides the respective bit definitions.

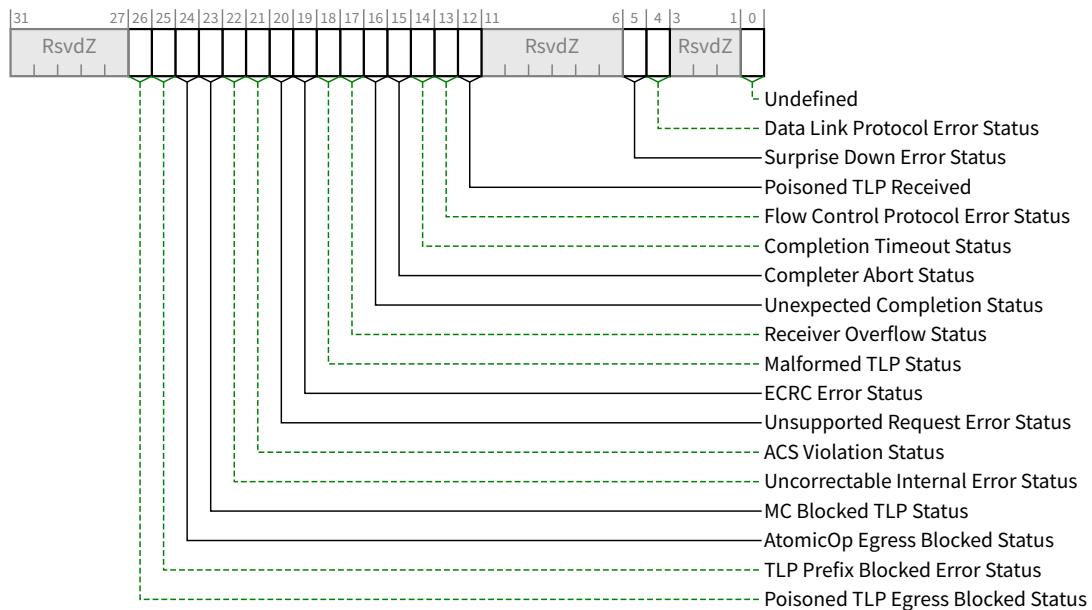


Figure 7-124 Uncorrectable Error Status Register

Table 7-100 Uncorrectable Error Status Register

Bit Location	Register Description	Attributes	Default
0	Undefined - The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.	Undefined	Undefined
4	Data Link Protocol Error Status	RW1CS	0b
5	Surprise Down Error Status (Optional)	RW1CS	0b
12	Poisoned TLP Received Status	RW1CS	0b
13	Flow Control Protocol Error Status (Optional)	RW1CS	0b
14	Completion Timeout Status ¹⁵⁰	RW1CS	0b
15	Completer Abort Status (Optional)	RW1CS	0b
16	Unexpected Completion Status	RW1CS	0b
17	Receiver Overflow Status (Optional)	RW1CS	0b
18	Malformed TLP Status	RW1CS	0b
19	ECRC Error Status (Optional)	RW1CS	0b
20	Unsupported Request Error Status	RW1CS	0b

150. For Switch Ports, required if the Switch Port issues Non-Posted Requests on its own behalf (vs. only forwarding such Requests generated by other devices). If the Switch Port does not issue such Requests, then the Completion Timeout mechanism is not applicable and this bit must be hardwired to 0b.

Bit Location	Register Description	Attributes	Default
21	ACS Violation Status (Optional)	<u>RW1CS</u>	0b
22	Uncorrectable Internal Error Status (Optional)	<u>RW1CS</u>	0b
23	MC Blocked TLP Status (Optional)	<u>RW1CS</u>	0b
24	AtomicOp Egress Blocked Status (Optional)	<u>RW1CS</u>	0b
25	TLP Prefix Blocked Error Status (Optional)	<u>RW1CS</u>	0b
26	Poisoned TLP Egress Blocked Status (Optional)	<u>RW1CS</u>	0b

7.8.4.3 Uncorrectable Error Mask Register (Offset 08h)

The Uncorrectable Error Mask Register controls reporting of individual errors by the device Function to the PCI Express Root Complex via a PCI Express error Message. A masked error (respective bit Set in the mask register) is not recorded or reported in the Header Log, TLP Prefix Log, or First Error Pointer, and is not reported to the PCI Express Root Complex by this Function. Refer to Section 6.2 for further details. There is a mask bit per error bit of the Uncorrectable Error Status register. Register fields for bits not implemented by the Function are hardwired to 0b. Figure 7-125 details the allocation of register fields of the Uncorrectable Error Mask Register; Table 7-101 provides the respective bit definitions.

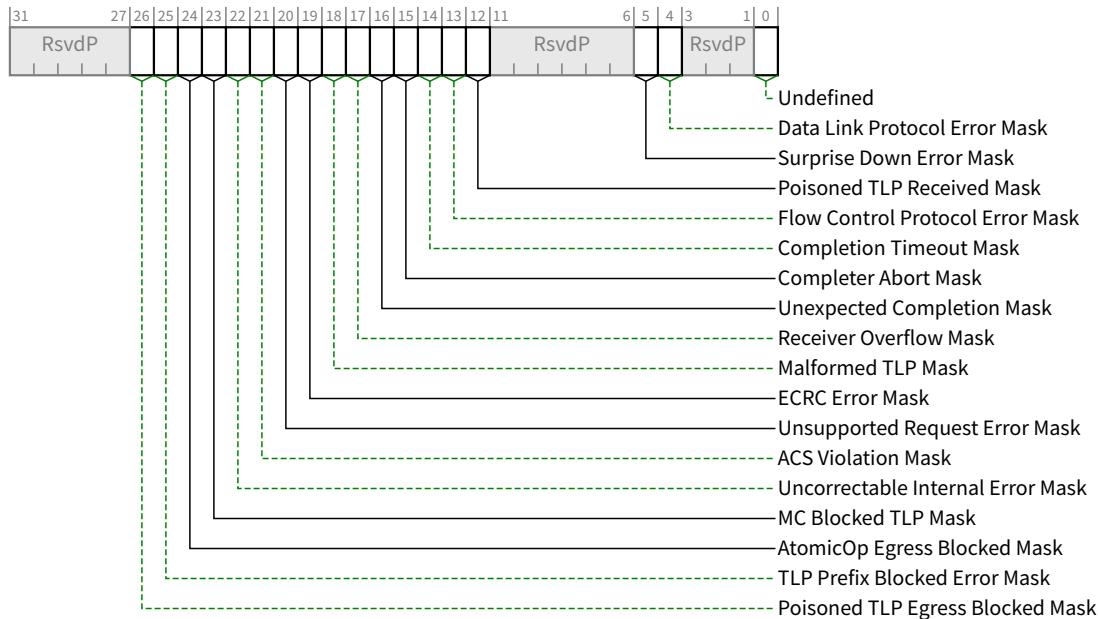


Figure 7-125 Uncorrectable Error Mask Register

Table 7-101 Uncorrectable Error Mask Register

Bit Location	Register Description	Attributes	Default
0	Undefined - The value read from this bit is undefined. In previous versions of this specification, this bit was used to mask a Link Training Error. System software must ignore the value read from this bit. System software must only write a value of 1b to this bit.	Undefined	Undefined
4	Data Link Protocol Error Mask	RWS	0b
5	Surprise Down Error Mask (Optional)	RWS	0b
12	Poisoned TLP Received Mask	RWS	0b
13	Flow Control Protocol Error Mask (Optional)	RWS	0b
14	Completion Timeout Mask ¹⁵¹	RWS	0b
15	Completer Abort Mask (Optional)	RWS	0b
16	Unexpected Completion Mask	RWS	0b
17	Receiver Overflow Mask (Optional)	RWS	0b
18	Malformed TLP Mask	RWS	0b
19	ECRC Error Mask (Optional)	RWS	0b
20	Unsupported Request Error Mask	RWS	0b
21	ACS Violation Mask (Optional)	RWS	0b
22	Uncorrectable Internal Error Mask (Optional)	RWS	1b
23	MC Blocked TLP Mask (Optional)	RWS	0b
24	AtomicOp Egress Blocked Mask (Optional)	RWS	0b
25	TLP Prefix Blocked Error Mask (Optional)	RWS	0b
26	Poisoned TLP Egress Blocked Mask (Optional)	RWS	1b

7.8.4.4 Uncorrectable Error Severity Register (Offset 0Ch)

The Uncorrectable Error Severity Register controls whether an individual error is reported as a Non-fatal or Fatal error. An error is reported as fatal when the corresponding error bit in the severity register is Set. If the bit is Clear, the corresponding error is considered non-fatal. Refer to Section 6.2 for further details. Register fields for bits not implemented by the Function are hardwired to an implementation specific value. Figure 7-126 details the allocation of register fields of the Uncorrectable Error Severity Register; Table 7-102 provides the respective bit definitions.

151. For Switch Ports, required if the Switch Port issues Non-Posted Requests on its own behalf (vs. only forwarding such Requests generated by other devices). If the Switch Port does not issue such Requests, then the Completion Timeout mechanism is not applicable and this bit must be hardwired to 0b.

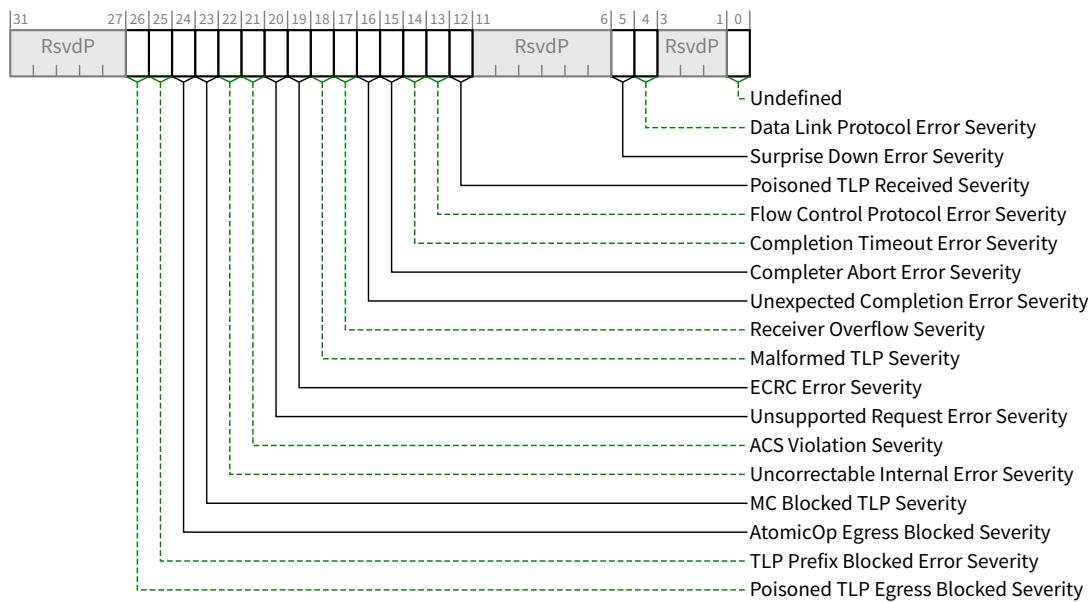


Figure 7-126 Uncorrectable Error Severity Register

Table 7-102 Uncorrectable Error Severity Register

Bit Location	Register Description	Attributes	Default
0	Undefined - The value read from this bit is undefined. In previous versions of this specification, this bit was used to Set the severity of a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.	Undefined	Undefined
4	Data Link Protocol Error Severity	RWS	1b
5	Surprise Down Error Severity (Optional)	RWS	1b
12	Poisoned TLP Received Severity	RWS	0b
13	Flow Control Protocol Error Severity (Optional)	RWS	1b
14	Completion Timeout Error Severity ¹⁵²	RWS	0b
15	Completer Abort Error Severity (Optional)	RWS	0b
16	Unexpected Completion Error Severity	RWS	0b
17	Receiver Overflow Severity (Optional)	RWS	1b
18	Malformed TLP Severity	RWS	1b
19	ECRC Error Severity (Optional)	RWS	0b
20	Unsupported Request Error Severity	RWS	0b

152. For Switch Ports, required if the Switch Port issues Non-Posted Requests on its own behalf (vs. only forwarding such Requests generated by other devices). If the Switch Port does not issue such Requests, then the Completion Timeout mechanism is not applicable and this bit must be hardwired to 0b.

Bit Location	Register Description	Attributes	Default
21	ACS Violation Severity (Optional)	RWS	0b
22	Uncorrectable Internal Error Severity (Optional)	RWS	1b
23	MC Blocked TLP Severity (Optional)	RWS	0b
24	AtomicOp Egress Blocked Severity (Optional)	RWS	0b
25	TLP Prefix Blocked Error Severity (Optional)	RWS	0b
26	Poisoned TLP Egress Blocked Severity (Optional)	RWS	0b

7.8.4.5 Correctable Error Status Register (Offset 10h)

The Correctable Error Status register reports error status of individual correctable error sources on a PCI Express device Function. When an individual error status bit is Set, it indicates that a particular error occurred; software may clear an error status by writing a 1b to the respective bit. Refer to [Section 6.2](#) for further details. Register bits not implemented by the Function are hardwired to 0b. [Figure 7-127](#) details the allocation of register fields of the Correctable Error Status register; [Table 7-103](#) provides the respective bit definitions.

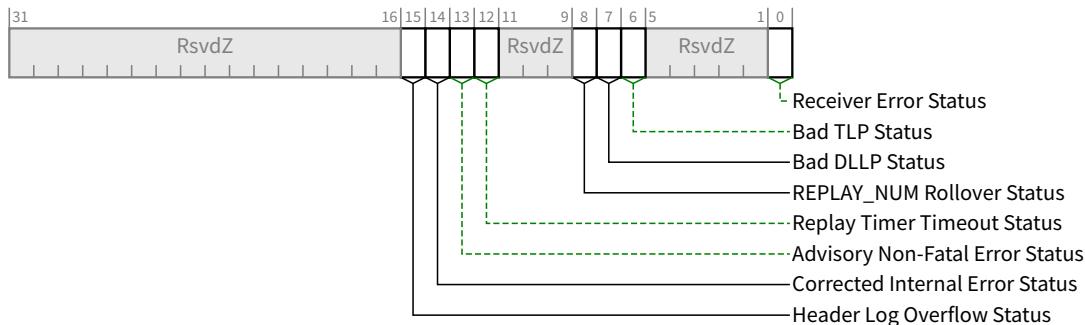


Figure 7-127 Correctable Error Status Register

Table 7-103 Correctable Error Status Register

Bit Location	Register Description	Attributes	Default
0	Receiver Error Status ¹⁵³	RW1CS	0b
6	Bad TLP Status	RW1CS	0b
7	Bad DLLP Status	RW1CS	0b
8	REPLAY_NUM Rollover Status	RW1CS	0b
12	Replay Timer Timeout Status	RW1CS	0b
13	Advisory Non-Fatal Error Status	RW1CS	0b

153. For historical reasons, implementation of this bit is optional. If not implemented, this bit must be RsvdZ, and bit 0 of the Correctable Error Mask Register must also not be implemented. Note that some checking for Receiver Errors is required in all cases (see [Section 4.2.1.1.3](#), [Section 4.2.4.8](#), and [Section 4.2.6](#)).

Bit Location	Register Description	Attributes	Default
14	Corrected Internal Error Status (Optional)	RW1CS	0b
15	Header Log Overflow Status (Optional)	RW1CS	0b

7.8.4.6 Correctable Error Mask Register (Offset 14h)

The **Correctable Error Mask Register** controls reporting of individual correctable errors by this Function to the PCI Express Root Complex via a PCI Express error Message. A masked error (respective bit Set in the mask register) is not reported to the PCI Express Root Complex by this Function. Refer to [Section 6.2](#) for further details. There is a mask bit per error bit in the **Correctable Error Status** register. Register fields for bits not implemented by the Function are hardwired to 0b. [Figure 7-128](#) details the allocation of register fields of the **Correctable Error Mask Register**; [Table 7-104](#) provides the respective bit definitions.

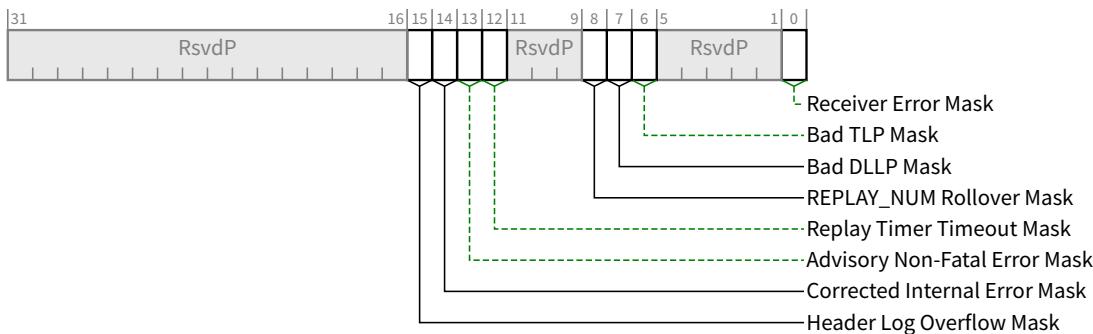


Figure 7-128 Correctable Error Mask Register

Table 7-104 Correctable Error Mask Register

Bit Location	Register Description	Attributes	Default
0	Receiver Error Mask ¹⁵⁴	RWS	0b
6	Bad TLP Mask	RWS	0b
7	Bad DLLP Mask	RWS	0b
8	REPLAY_NUM Rollover Mask	RWS	0b
12	Replay Timer Timeout Mask	RWS	0b
13	Advisory Non-Fatal Error Mask - This bit is Set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.	RWS	1b
14	Corrected Internal Error Mask (Optional)	RWS	1b
15	Header Log Overflow Mask (Optional)	RWS	1b

154. For historical reasons, implementation of this bit is optional. If not implemented, this bit must be RsvdP, and bit 0 of the **Correctable Error Status** register must also not be implemented. Note that some checking for Receiver Errors is required in all cases (see [Sections 4.2.1.1.3, 4.2.4.7, and 4.2.6](#)).

7.8.4.7 Advanced Error Capabilities and Control Register (Offset 18h)

Figure 7-129 details allocation of register fields in the Advanced Error Capabilities and Control register; Table 7-105 provides the respective bit definitions. Handling of multiple errors is discussed in Section 6.2.4.2.

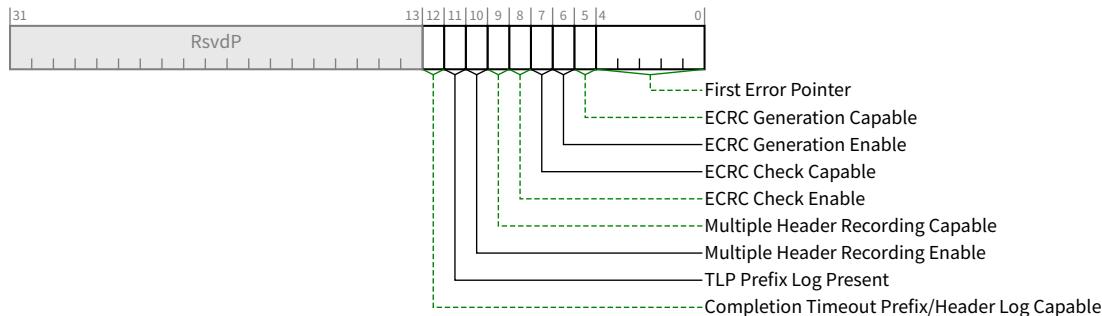


Figure 7-129 Advanced Error Capabilities and Control Register

Table 7-105 Advanced Error Capabilities and Control Register

Bit Location	Register Description	Attributes
4:0	First Error Pointer - The First Error Pointer is a field that identifies the bit position of the first error reported in the Uncorrectable Error Status register. Refer to Section 6.2 for further details.	<u>ROS</u>
5	ECRC Generation Capable - If Set, this bit indicates that the Function is capable of generating ECRC (see Section 2.7).	<u>RO</u>
6	ECRC Generation Enable - When Set, ECRC generation is enabled (see Section 2.7). Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	<u>RWS</u>
7	ECRC Check Capable - If Set, this bit indicates that the Function is capable of checking ECRC (see Section 2.7).	<u>RO</u>
8	ECRC Check Enable - When Set, ECRC checking is enabled (see Section 2.7). Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	<u>RWS</u>
9	Multiple Header Recording Capable - If Set, this bit indicates that the Function is capable of recording more than one error header. Refer to Section 6.2 for further details.	<u>RO</u>
10	Multiple Header Recording Enable - When Set, this bit enables the Function to record more than one error header. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b. Default value of this bit is 0b.	<u>RWS</u>
11	TLP Prefix Log Present - If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is <u>RsvdP</u> if the End-End TLP Prefix Supported bit is Clear.	<u>ROS</u>

Bit Location	Register Description	Attributes
12	Completion Timeout Prefix/Header Log Capable - If Set, this bit indicates that the Function records the prefix/header of Request TLPs that experience a Completion Timeout error.	RO

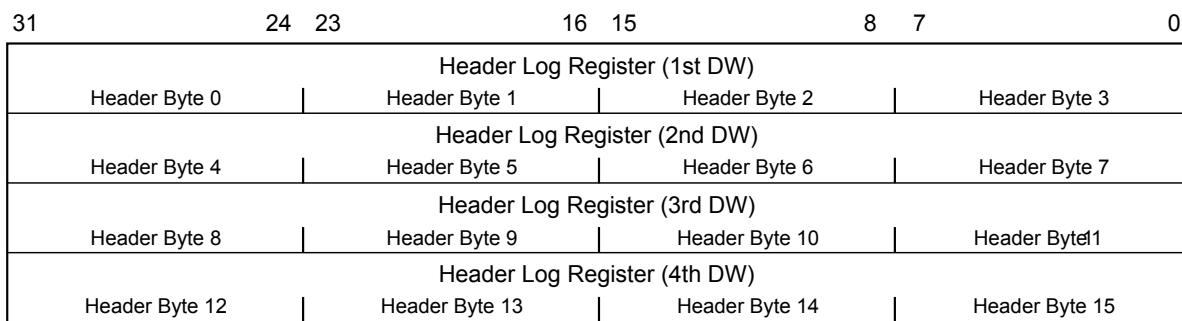
7.8.4.8 Header Log Register (Offset 1Ch)

The Header Log Register contains the header for the TLP corresponding to a detected error; refer to [Section 6.2](#) for further details. [Section 6.2](#) also describes the conditions where the packet header is recorded. This register is 16 bytes and adheres to the format of the headers defined throughout this specification.

The header is captured such that, when read using DW accesses, the fields of the header are laid out in the same way the headers are presented in this document. Therefore, byte 0 of the header is located in byte 3 of the [Header Log Register](#), byte 1 of the header is in byte 2 of the [Header Log Register](#) and so forth. For 12-byte headers, only bytes 0 through 11 of the [Header Log Register](#) are used and values in bytes 12 through 15 are undefined.

In certain cases where a Malformed TLP is reported, the [Header Log Register](#) may contain TLP Prefix information. See [Section 6.2.4.4](#) for details.

[Figure 7-130](#) details allocation of register fields in the [Header Log Register](#); [Table 7-106](#) provides the respective bit definitions.



OM14549A

[Figure 7-130 Header Log Register](#)

[Table 7-106 Header Log Register](#)

Bit Location	Register Description	Attributes	Default
127:0	Header of TLP associated with error	ROS	0

7.8.4.9 Root Error Command Register (Offset 2Ch)

The [Root Error Command Register](#) allows further control of Root Complex response to Correctable, Non-Fatal, and Fatal error Messages than the basic Root Complex capability to generate system errors in response to error Messages (either received or internally generated). Bit fields (see [Figure 7-131](#)) enable or disable generation of interrupts (claimed by the Root Port or Root Complex Event Collector) in addition to system error Messages according to the definitions in [Table 7-107](#).

For both Root Ports and Root Complex Event Collectors, in order for a received error Message or an internally generated error Message to generate an interrupt enabled by this register, the error Message must be enabled for “transmission” by the Root Port or Root Complex Event Collector (see [Section 6.2.4.1](#) and [Section 6.2.8.1](#)).

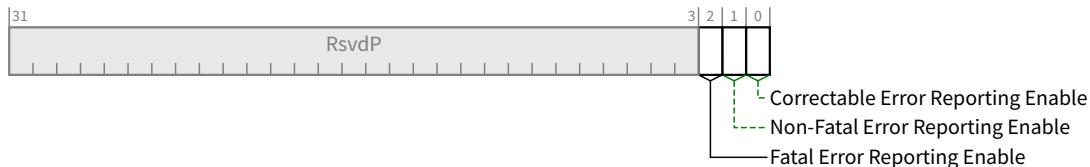


Figure 7-131 Root Error Command Register

Table 7-107 Root Error Command Register

Bit Location	Register Description	Attributes	Default
0	<p>Correctable Error Reporting Enable - When Set, this bit enables the generation of an interrupt when a correctable error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port.</p> <p>Root Complex Event Collectors provide support for the above described functionality for RCIEPs.</p> <p>Refer to Section 6.2 for further details.</p>	RW	0b
1	<p>Non-Fatal Error Reporting Enable - When Set, this bit enables the generation of an interrupt when a Non-fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port.</p> <p>Root Complex Event Collectors provide support for the above described functionality for RCIEPs.</p> <p>Refer to Section 6.2 for further details.</p>	RW	0b
2	<p>Fatal Error Reporting Enable - When Set, this bit enables the generation of an interrupt when a Fatal error is reported by any of the Functions in the Hierarchy Domain associated with this Root Port.</p> <p>Root Complex Event Collectors provide support for the above described functionality for RCIEPs.</p> <p>Refer to Section 6.2 for further details.</p>	RW	0b

System error generation in response to PCI Express error Messages may be turned off by system software using the PCI Express Capability structure described in [Section 7.5.3](#) when advanced error reporting via interrupts is enabled. Refer to [Section 6.2](#) for further details.

7.8.4.10 Root Error Status Register (Offset 30h)

The [Root Error Status Register](#) reports status of error Messages ([ERR_COR](#), [ERR_NONFATAL](#), and [ERR_FATAL](#)) received by the Root Port, and of errors detected by the Root Port itself (which are treated conceptually as if the Root Port had sent an error Message to itself). In order to update this register, error Messages received by the Root Port and/or internally generated error Messages must be enabled for “transmission” by the primary interface of the Root Port. [ERR_NONFATAL](#) and [ERR_FATAL](#) Messages are grouped together as uncorrectable. Each correctable and uncorrectable (Non-fatal and Fatal) error source has a first error bit and a next error bit associated with it respectively. When an error is received by a Root Complex, the respective first error bit is Set and the Requester ID is logged in the [Error Source Identification](#)

Register. A Set individual error status bit indicates that a particular error category occurred; software may clear an error status by writing a 1b to the respective bit. If software does not clear the first reported error before another error Message is received of the same category (correctable or uncorrectable), the corresponding next error status bit will be set but the Requester ID of the subsequent error Message is discarded. The next error status bits may be cleared by software by writing a 1b to the respective bit as well. Refer to Section 6.2 for further details. This register is updated regardless of the settings of the Root Control register and the Root Error Command Register. Figure 7-132 details allocation of register fields in the Root Error Status Register; Table 7-108 provides the respective bit definitions. Root Complex Event Collectors provide support for the above-described functionality for RCiEPs (and for the Root Complex Event Collector itself). In order to update this register, error Messages received by the Root Complex Event Collector from its associated RCiEPs and/or internally generated error Messages must be enabled for “transmission” by the Root Complex Event Collector.

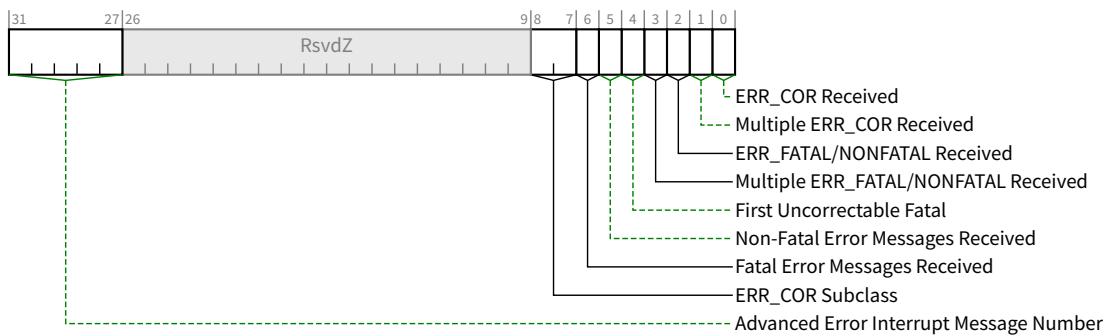


Figure 7-132 Root Error Status Register

Table 7-108 Root Error Status Register

Bit Location	Register Description	Attributes
0	ERR_COR Received - Set when a Correctable error Message is received and this bit is not already Set. Default value of this bit is 0b.	RW1CS
1	Multiple ERR_COR Received - Set when a Correctable error Message is received and <u>ERR_COR Received</u> is already Set. Default value of this bit is 0b.	RW1CS
2	ERR_FATAL/NONFATAL Received - Set when either a Fatal or a Non-fatal error Message is received and this bit is not already Set. Default value of this bit is 0b.	RW1CS
3	Multiple ERR_FATAL/NONFATAL Received - Set when either a Fatal or a Non-fatal error is received and <u>ERR_FATAL/NONFATAL Received</u> is already Set. Default value of this bit is 0b.	RW1CS
4	First Uncorrectable Fatal - Set when the first Uncorrectable error Message received is for a Fatal error. Default value of this field is 0b.	RW1CS
5	Non-Fatal Error Messages Received - Set when one or more Non-Fatal Uncorrectable error Messages have been received. Default value of this bit is 0b.	RW1CS

Bit Location	Register Description	Attributes
6	<p>Fatal Error Messages Received - Set when one or more Fatal Uncorrectable error Messages have been received.</p> <p>Default value of this bit is 0b.</p>	RW1CS
8:7	<p>ERR_COR Subclass - If the Function is ERR_COR Subclass capable and the <u>ERR_COR Received</u> bit is not already Set, this field is loaded with the value of the <u>ERR_COR Subclass</u> field in the received <u>ERR_COR Message</u>. See <u>Section 2.2.8.3</u>. The value in this field is only valid when the <u>ERR_COR Received</u> bit is Set. If the Function is not ERR_COR Subclass capable, this field is Reserved.</p> <p>If the Function is ERR_COR Subclass capable and a SIG_SFW <u>ERR_COR Message</u> is received, system firmware should be signaled using a system-specific mechanism.</p> <p>Default value of this field is 00b.</p>	ROS/RsvdZ
31:27	<p>Advanced Error Interrupt Message Number - This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability.</p> <p>For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the <u>Message Control Register for MSI</u>.</p> <p>For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant.</p> <p>If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined.</p>	RO

7.8.4.11 Error Source Identification Register (Offset 34h)

The Error Source Identification Register identifies the source (Requester ID) of first correctable and uncorrectable (Non-fatal/Fatal) errors reported in the Root Error Status Register. Refer to Section 6.2 for further details. This register is updated regardless of the settings of the Root Control register and the Root Error Command Register. Figure 7-133 details allocation of register fields in the Error Source Identification Register; Table 7-109 provides the respective bit definitions.

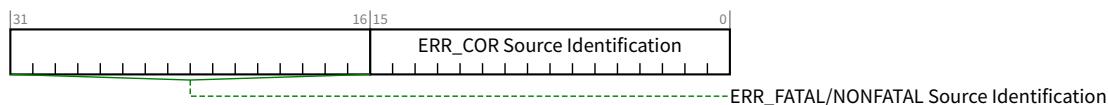


Figure 7-133 Error Source Identification Register

Table 7-109 Error Source Identification Register

Bit Location	Register Description	Attributes
15:0	ERR_COR Source Identification - Loaded with the Requester ID indicated in the received <u>ERR_COR Message</u> when the <u>ERR_COR Received</u> bit is not already set.	ROS

Bit Location	Register Description	Attributes
	Default value of this field is 0000h.	
31:16	ERR_FATAL/NONFATAL Source Identification - Loaded with the Requester ID indicated in the received <u>ERR_FATAL</u> or <u>ERR_NONFATAL</u> Message when the <u>ERR_FATAL/NONFATAL Received</u> bit is not already set. Default value of this field is 0000h.	<u>ROS</u>

7.8.4.12 TLP Prefix Log Register (Offset 38h)

The TLP Prefix Log Register captures the End-End TLP Prefix(s) for the TLP corresponding to the detected error; refer to Section 6.2 for further details. The TLP Prefix Log Register is only meaningful when the TLP Prefix Log Present bit is Set (see Section 7.8.4.7).

The TLP Prefixes are captured such that, when read using DW accesses, the fields of the TLP Prefix are laid out in the same way the fields of the TLP Prefix are described. Therefore, byte 0 of a TLP Prefix is located in byte 3 of the associated TLP Prefix Log Register; byte 1 of a TLP Prefix is located in byte 2; and so forth.

The First TLP Prefix Log Register contains the first End-End TLP Prefix from the TLP (see Section 6.2.4.4). The Second TLP Prefix Log Register contains the second End-End TLP Prefix and so forth. If the TLP contains fewer than four End-End TLP Prefixes, the remaining TLP Prefix Log Registers contain zero. A TLP that contains more End-End TLP Prefixes than are indicated by the Function's Max End-End TLP Prefixes field must be handled as an error (see Section 2.2.10.2 for specifics). To allow software to detect this condition, the supported number of End-End TLP Prefixes are logged in this register, the first overflow End-End TLP Prefix is logged in the first DW of the Header Log register and the remaining DWs of the Header Log register are undefined (see Section 6.2.4.4).

The TLP Prefix Log Registers beyond the number supported by the Function are hardwired to zero. For example, if a Functions, Max End-End TLP Prefixes field contains 10b (indicating 2 DW of buffering) then the third and fourth TLP Prefix Log Registers are hardwired to zero. If the End-End TLP Prefix Supported bit (Section 7.5.3.15) is Clear, the TLP Prefix Log Register is not required to be implemented.

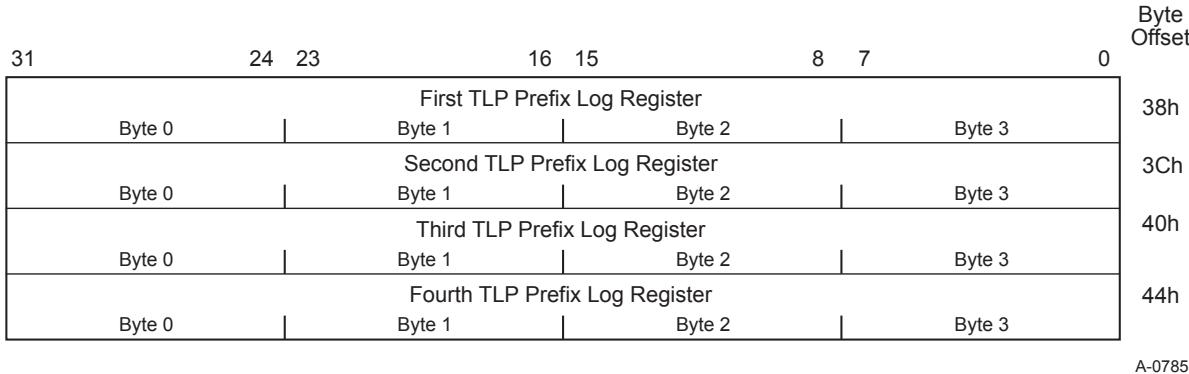


Figure 7-134 TLP Prefix Log Register

Table 7-110 TLP Prefix Log Register

Bit Location	Register Description	Attributes	Default
127:0	TLP Prefix Log	<u>ROS</u>	0

7.8.5 Enhanced Allocation Capability Structure (EA)

Each function that supports the Enhanced Allocation mechanism must implement the Enhanced Allocation capability structure.

Each field is defined in the following sections. Reserved registers must return 0 when read and write operations must have no effect. Read-only registers return valid data when read, and write operations must have no effect.

7.8.5.1 Enhanced Allocation Capability First DW (Offset 00h)

The first DW of the Enhanced Allocation capability is illustrated in [Figure 7-135](#), and is documented in [Table 7-111](#).

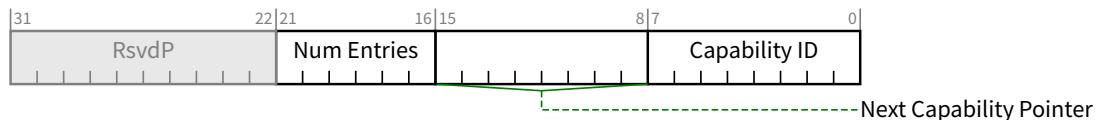


Figure 7-135 First DW of Enhanced Allocation Capability

Table 7-111 First DW of Enhanced Allocation Capability

Bit Location	Register Description	Attributes
7:0	Capability ID - Must be set to 14h to indicate Enhanced Allocation capability. This field is read only.	HwInit
15:8	Next Capability Pointer - Pointer to the next item in the capabilities list. Must be NULL for the final item in the list. This field is read only.	HwInit
21:16	Num Entries - Number of entries following the first DW of the capability. Value of 00 0000b is permitted and means there are no entries. This field is read only.	HwInit

7.8.5.2 Enhanced Allocation Capability Second DW (Offset 04h) [Type 1 Functions Only]

For [Type 1 Functions](#) only, there is a second DW in the capability, preceding the first entry. This second DW must be included in the Enhanced Allocation Capability whenever this capability is implemented in a [Type 1 Function](#). The second DW of the Enhanced Allocation capability is illustrated in [Figure 7-136](#), and is documented in [Table 7-112](#).

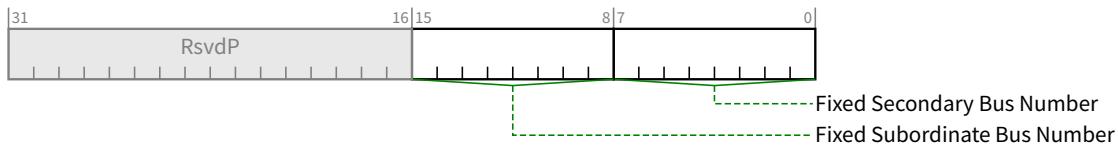


Figure 7-136 Second DW of Enhanced Allocation Capability

Table 7-112 Second DW of Enhanced Allocation Capability

Bit Location	Register Description	Attributes
7:0	Fixed Secondary Bus Number - If at least one Function that uses EA is located behind this Function, then this field must be set to indicate the Bus Number for the secondary interface of this Function. If no Function that uses EA is located behind this Function, then this field must be set to 00h.	<u>HwInit</u>
15:8	Fixed Subordinate Bus Number - If at least one Function that uses EA is located behind this Function, then this field must be set to indicate the the highest Bus Number below this Function. If no Function that uses-EA is located behind this Function, then this field must be set to 00h.	<u>HwInit</u>

7.8.5.3 Enhanced Allocation Per-Entry Format (Offset 04h or 08h)

An Enhanced Allocation Entry consists of a First DW followed by between 2 and 4 DW of Base / MaxOffset information.

- For Type 0 Functions, Enhanced Allocation Entries start at offset 04h of this capability.
- For Type 1 Functions, Enhanced Allocation Entries start at offset 08h of this capability.
- Subsequent Enhanced Allocation Entries immediately follow each other.

The first DW of each entry in the Enhanced Allocation capability is illustrated in [Figure 7-137](#), and is defined in [Table 7-113](#).

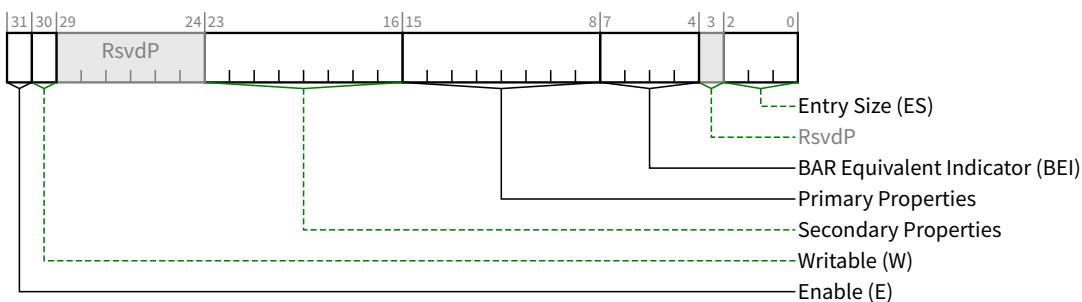


Figure 7-137 First DW of Each Entry for Enhanced Allocation Capability

Table 7-113 First DW of Each Entry for Enhanced Allocation Capability

Bit Location	Register Description	Attributes																								
2:0	<p>Entry Size (ES) - Number of DW following the initial DW in this entry.</p> <p>When processing this capability, software is required to use the value in this field to determine the size of this entry, and if this entry is not the final entry, the start of the following entry in the capability. This requirement must be strictly followed by software, even if the indicated entry size does not correspond to any entry defined in this specification.</p> <p>Value of 000b indicates only the first DW (containing the Entry Size field) is included in the entry.</p>	<u>HwInit</u>																								
7:4	<p>BAR Equivalent Indicator (BEI) - This field indicates the equivalent BAR for this entry.</p> <p>Specific rules for use of this field are given in the text following this table.</p> <table border="1"> <thead> <tr> <th>BEI Value</th><th>Description</th></tr> </thead> <tbody> <tr><td>0</td><td>Entry is equivalent to BAR at location 10h</td></tr> <tr><td>1</td><td>Entry is equivalent to BAR at location 14h</td></tr> <tr><td>2</td><td>Entry is equivalent to BAR at location 18h</td></tr> <tr><td>3</td><td>Entry is equivalent to BAR at location 1Ch</td></tr> <tr><td>4</td><td>Entry is equivalent to BAR at location 20h</td></tr> <tr><td>5</td><td>Entry is equivalent to BAR at location 24h</td></tr> <tr><td>6</td><td>Permitted to be used by a Function with a Type 1 Configuration Space Header only, optionally used to indicate a resource that is located behind the Function</td></tr> <tr><td>7</td><td>Equivalent Not Indicated</td></tr> <tr><td>8</td><td>Expansion ROM Base Address</td></tr> <tr><td>9-14</td><td>Entry relates to VF BARs 0-5 respectively</td></tr> <tr><td>15</td><td>Reserved - Software must treat values in this range as “Equivalent Not Indicated”</td></tr> </tbody> </table>	BEI Value	Description	0	Entry is equivalent to BAR at location 10h	1	Entry is equivalent to BAR at location 14h	2	Entry is equivalent to BAR at location 18h	3	Entry is equivalent to BAR at location 1Ch	4	Entry is equivalent to BAR at location 20h	5	Entry is equivalent to BAR at location 24h	6	Permitted to be used by a Function with a Type 1 Configuration Space Header only, optionally used to indicate a resource that is located behind the Function	7	Equivalent Not Indicated	8	Expansion ROM Base Address	9-14	Entry relates to VF BARs 0-5 respectively	15	Reserved - Software must treat values in this range as “Equivalent Not Indicated”	<u>HwInit</u>
BEI Value	Description																									
0	Entry is equivalent to BAR at location 10h																									
1	Entry is equivalent to BAR at location 14h																									
2	Entry is equivalent to BAR at location 18h																									
3	Entry is equivalent to BAR at location 1Ch																									
4	Entry is equivalent to BAR at location 20h																									
5	Entry is equivalent to BAR at location 24h																									
6	Permitted to be used by a Function with a Type 1 Configuration Space Header only, optionally used to indicate a resource that is located behind the Function																									
7	Equivalent Not Indicated																									
8	Expansion ROM Base Address																									
9-14	Entry relates to VF BARs 0-5 respectively																									
15	Reserved - Software must treat values in this range as “Equivalent Not Indicated”																									
15:8	Primary Properties - Indicates the entry properties as defined in Table 7-114 .	<u>HwInit</u>																								
23:16	Secondary Properties - Optionally used to indicate a different but compatible entry property, using properties as defined in Table 7-114 .	<u>HwInit</u>																								
30	<p>Writable (W) - The value 1b indicates that the <u>Base</u> and <u>MaxOffset</u> fields for this entry are <u>RW</u> and that the Field Size bits for this entry are either <u>RW</u> or <u>HwInit</u>. The value 0b indicates those fields are <u>HwInit</u>. See Table 7-114 for additional requirements on the value of this field.</p>	<u>HwInit</u>																								
31	<p>Enable (E) - 1b indicates this entry is enabled, 0b indicates this entry is disabled.</p> <p>If system software disables this entry, the resource indicated must still be associated with this function, and it is not permitted to reallocate this resource to any other entity.</p> <p>This field is permitted to be implemented as <u>HwInit</u> for functions that require the allocation of the associated resource, or as <u>RW</u> for functions that can allow system software to disable this resource, for example if BAR mechanisms are to be used instead of this resource.</p>	<u>RW/HwInit</u>																								

Rules for use of BEI field:

- A Type 0 Function is permitted to use EA to allocate resources for itself, and such resources must indicate a BEI value of 0-5, 7 or 8.
- A Physical Function (Type 0 Function that supports SR-IOV) is permitted to use EA to allocate resources for its associated Virtual Functions, and such resources must indicate a BEI value of 9-14.
- A Type 1 Function (bridge) is permitted to use EA to allocate resources for itself, and such resources must indicate a BEI value of 0, 1 or 7.
- A Type 1 Function is permitted but not required to indicate resources mapped behind that Function, but if such resources are indicated by the Type 1 Function, the entry must indicate a BEI value of 6.
- For a 64-bit Base Address Register, the BEI indicates the equivalent BAR location for lower DWORD.
- For Memory BARs where the Primary or Secondary Properties is 00h or 01h, it is permitted to assign the same BEI in the range of 0 to 5 once for a range where Base + MaxOffset is below 4 GB, and again for a range where Base + MaxOffset is greater than 4 GB; It is not otherwise permitted to assign the same BEI in the range 0 to 5 for more than one entry.
- For Virtual Function BARs where the Primary or Secondary Properties is 03h or 04h it is permitted to assign the same BEI in the range of 9 to 14 once for a range where Base + MaxOffset is below 4 GB, and again for a range where Base + MaxOffset is greater than 4 GB; It is not otherwise permitted to assign the same BEI in the range 9 to 14 for more than one VF entry.
- For all cases where two entries with the same BEI are permitted, Software must enable use of only one of the two ranges at a time for a given Function.
- It is permitted for an arbitrary number of entries to assign a BEI of 6 or 7.
- At most one entry is permitted with a BEI of 8; if such an entry is present, behavior of the Expansion ROM Base Address Register is changed (see Section 7.5.1.2.4).
- For Type 1 Functions, BEI values 2 through 5 are reserved.

Figure 7-138 illustrates the format of a complete Enhanced Allocation entry for a Type 0 Function. For the Base and MaxOffset fields, bit 1 indicates if the field is a 32b (0) or 64b (1) field.

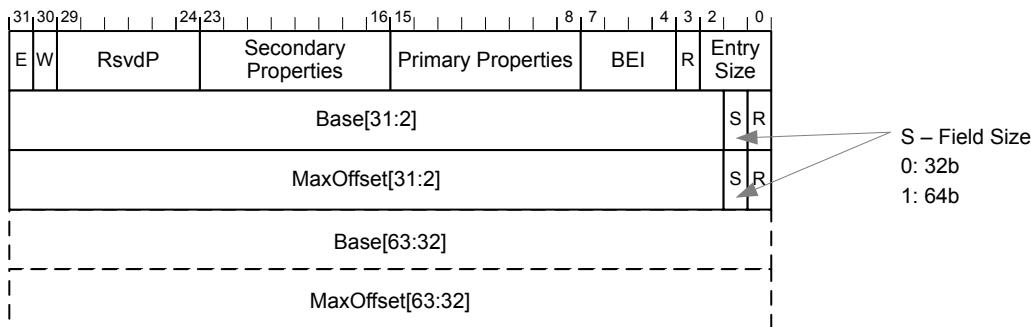


Figure 7-138 Format of Entry for Enhanced Allocation Capability

The value in the **Base** field ([63:2] or [31:2]) indicates the DW address of the start of the resource range. Bits [1:0] of the address are not included in the Base field, and must always be interpreted as 00b.

The value in the Base field plus the value in the MaxOffset field ([63:2] or [31:2]) indicates the address of the last included DW of the resource range. Bits [1:0] of the MaxOffset are not included in the MaxOffset field, and must always be interpreted as 11b.

For the Base and MaxOffset fields, when bits [63:32] are not provided then those bits must be interpreted as all 0's.

Although it is permitted for a Type 0 Function to indicate the use of a range that is not naturally aligned and/or not a power of two in size, some system software may fail if this is done. Particularly for ranges that are mapped to legacy BARs by indicating a BEI in the range of 0 to 5, it is strongly recommended that the Base and MaxOffset fields for a Type 0 Function indicate a naturally aligned region.

The Primary Properties[7:0] field must be set by hardware to identify the type of resource indicated by the entry. It is strongly recommended that hardware set the Secondary Properties[7:0] to indicate an alternate resource type which can be used by software when the Primary Properties[7:0] field value is not comprehended by that software, for example when older system software is used with new hardware that implements resources using a value for Primary Properties that was reserved at the time the older system software was implemented. When this is done, hardware must ensure that software operating using the resource according to the value indicated in the Secondary Properties field will operate in a functionally correct way, although it is not required that this operation will result in optimal system performance or behavior.

The Primary Properties[7:0] and Secondary Properties[7:0] fields are defined in [Table 7-114](#). This table also defines whether or not the entry is permitted to be writeable. The Writeable bit in any entry must be 0b unless both the Primary and Secondary properties of that entry allow otherwise.

Table 7-114 Enhanced Allocation Entry Field Value Definitions for both the Primary Properties and Secondary Properties Fields

Value (h)	Resource Definition	Writeable permitted
00	Memory Space, Non-Prefetchable.	No
01	Memory Space, Prefetchable.	No
02	I/O Space.	No
03	For use only by <u>Physical Functions</u> to indicate resources for <u>Virtual Function</u> use, Memory Space, Prefetchable.	No
04	For use only by <u>Physical Functions</u> to indicate resources for <u>Virtual Function</u> use, Memory Space, Non-Prefetchable.	No
05	For use only by <u>Type 1 Functions</u> to indicate Memory, Non-Prefetchable, for Allocation Behind that Bridge.	No
06	For use only by <u>Type 1 Functions</u> to indicate Memory, Prefetchable, for Allocation Behind that Bridge.	No
07	For use only by <u>Type 1 Functions</u> to indicate I/O Space for Allocation Behind that Bridge.	No
08-FC	Reserved for future use; System firmware/software must not write to this entry, and must not attempt to interpret this entry or to use this resource. When software reads a Primary Properties value that is within this range, is it strongly recommended that software treat this resource according to the value in the Secondary Properties field, if that field contains a non-reserved value.	Yes
FD	Memory Space Resource Unavailable For Use -- System firmware/software must not write to this entry, and must not attempt to use the resource described by this entry for any purpose.	No

Value (h)	Resource Definition	Writeable permitted
FE	I/O Space Resource Unavailable For Use -- System firmware/software must not write to this entry, and must not attempt to use the resource described by this entry for any purpose.	No
FF	Entry Unavailable For Use - System firmware/software must not write to this entry, and must not attempt to interpret this entry as indicating any resource. It is strongly recommended that hardware use this value in the Secondary Properties field to indicate that for proper operation, the hardware requires the use of the resource definition indicated in the Primary Properties field .	No

The following figures illustrate the layout of Enhanced Allocation entries for various cases.

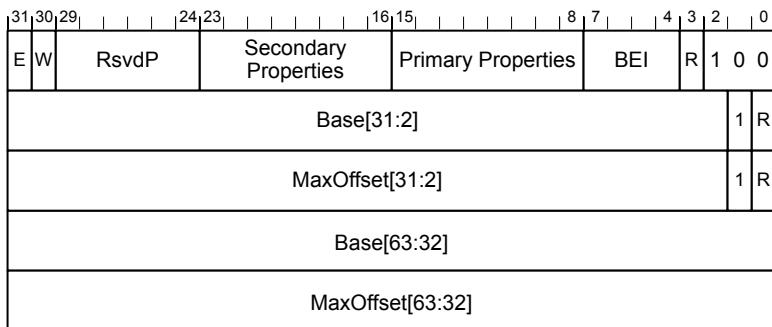


Figure 7-139 Example Entry with 64b Base and 64b MaxOffset

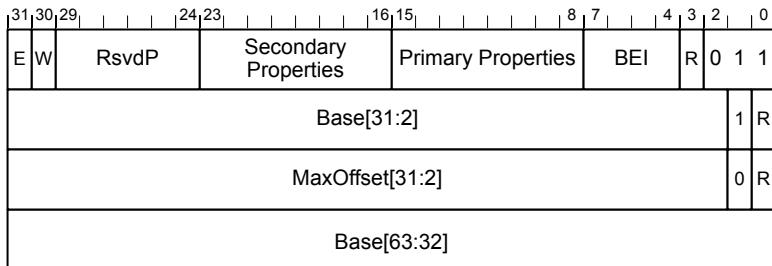


Figure 7-140 Example Entry with 64b Base and 32b MaxOffset

31	30	29			24	23			16	15			8	7		4	3	2	1	0
E	W	RsvdP		Secondary Properties		Primary Properties		BEI	R	0	1	1								
Base[31:2]																0	R			
MaxOffset[31:2]																1	R			
MaxOffset[63:32]																				

Figure 7-141 Example Entry with 32b Base and 64b MaxOffset

31	30	29			24	23			16	15			8	7		4	3	2	1	0
E	W	RsvdP		Secondary Properties		Primary Properties		BEI	R	0	1	0								
Base[31:2]																0	R			
MaxOffset[31:2]																0	R			

Figure 7-142 Example Entry with 32b Base and 32b MaxOffset

7.8.6 Resizable BAR Extended Capability

The Resizable BAR Extended Capability is an optional capability that allows hardware to communicate resource sizes, and system software, after determining the optimal size, to communicate this optimal size back to the hardware. Hardware communicates the resource sizes that are acceptable for operation via the Resizable BAR Capability and Control registers. Hardware must support at least one size in the range from 1 MB to 512 GB.

IMPLEMENTATION NOTE

Resizable BAR Backward Compatibility With Software

The Resizable BAR Extended Capability initially supported 20 sizes, ranging from 1 MB to 512 GB, and was later expanded with 16 larger sizes. The hardware requirement to support at least one of the initial sizes ensures backward compatibility with software that comprehends only the initial sizes.

Software determines, through a proprietary mechanism, what the optimal size is for the resource, and programs that size via the BAR Size field of the Resizable BAR Control register. Hardware immediately reflects the size inference in the read-only bits of the appropriate Base Address register. Hardware must Clear any bits that change from RW to read-only, so that subsequent reads return zero. Software must clear the Memory Space Enable bit in the Command register before

writing the BAR Size field. After writing the BAR Size field, the contents of the corresponding BAR are undefined. To ensure that it contains a valid address after resizing the BAR, system software must reprogram the BAR, and Set the Memory Space Enable bit (unless the resource is not allocated).

The Resizable BAR Capability and Control registers are permitted to indicate the ability to operate at 4 GB or greater only if the associated BAR is a 64-bit BAR.

This capability is applicable to Functions that have Base Address registers only. It is strongly recommended that a Function not advertise any supported BAR sizes that are larger than the space it would effectively utilize if allocated.

IMPLEMENTATION NOTE

Using the Capability During Resource Allocation

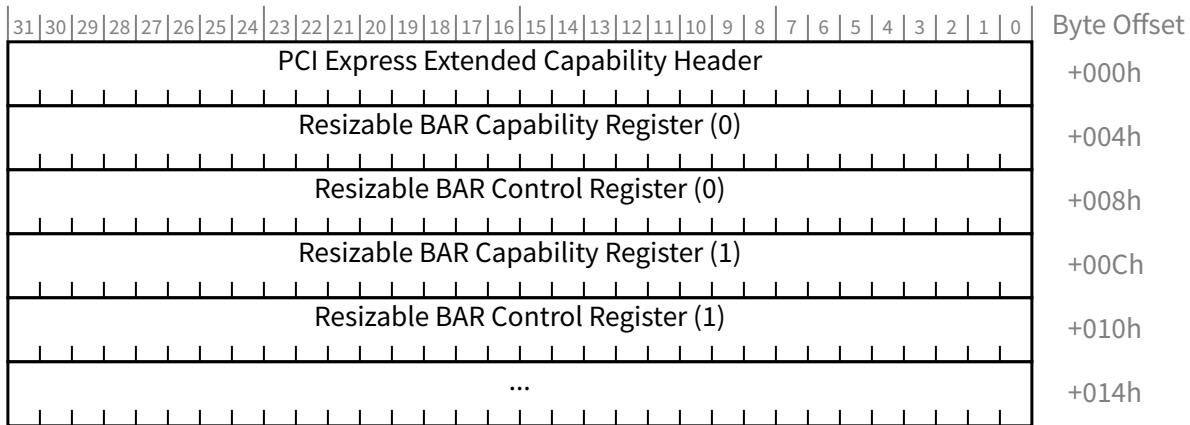
System software that allocates resources can use this capability to resize the resources inferred by the Function's BAR's read-only bits. Previous versions of this software determined the resource size by writing FFFFh to the BAR, reading back the value, and determining the size by the number of bits that are Set. Following this, the base address is written to the BAR.

System software uses this capability in place of the above mentioned method of determining the resource size, and prior to assigning the base address to the BAR. Potential usable resource sizes are reported by the Function via its Resizable BAR Capability and Control registers. It is intended that the software allocate the largest of the reported sizes that it can, since allocating less address space than the largest reported size can result in lower performance. Software then writes the size to the Resizable BAR Control register for the appropriate BAR for the Function. Following this, the base address is written to the BAR.

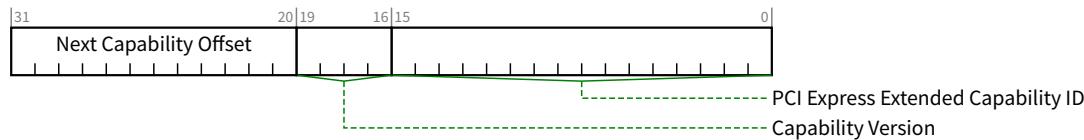
For interoperability reasons, it is possible that hardware will set the default size of the BAR to a low size; that is, a size lower than the largest reported in the Resizable BAR Capability and Control registers. Software that does not use this capability to size resources will likely result in sub-optimal resource allocation, where the resources are smaller than desirable, or not allocatable because there is no room for them.

With the Resizable BAR capability, the amount of address space consumed by a device can change. In a resource constrained environment, the allocation of more address space to a device may result in allocation of less of the address space to other memory-mapped hardware, like system RAM. System software responsible for allocating resources in this kind of environment is recommended to distribute the limited address space appropriately.

The Resizable BAR Capability structure defines a PCI Express Extended Capability, which is located in PCI Express Extended Configuration Space, that is, above the first 256 bytes, and is shown below in [Figure 7-143](#). This structure allows devices with this capability to be identified and controlled. A Capability and a Control register is implemented for each BAR that is resizable. Since a maximum of six BARs may be implemented by any Function, the Resizable BAR Capability structure can range from 12 bytes long (for a single BAR) to 52 bytes long (for all six BARs).

Figure 7-143 Resizable BAR Extended Capability

7.8.6.1 Resizable BAR Extended Capability Header (Offset 00h)

Figure 7-144 Resizable BAR Extended Capability HeaderTable 7-115 Resizable BAR Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. The PCI Express Extended Capability ID for the Resizable BAR Capability is 0015h.	RO
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	RO
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	RO

7.8.6.2 Resizable BAR Capability Register

For backward compatibility with software, hardware must Set at least one bit in the range from 4 to 23. See the associated Implementation Note in Section 7.8.6.

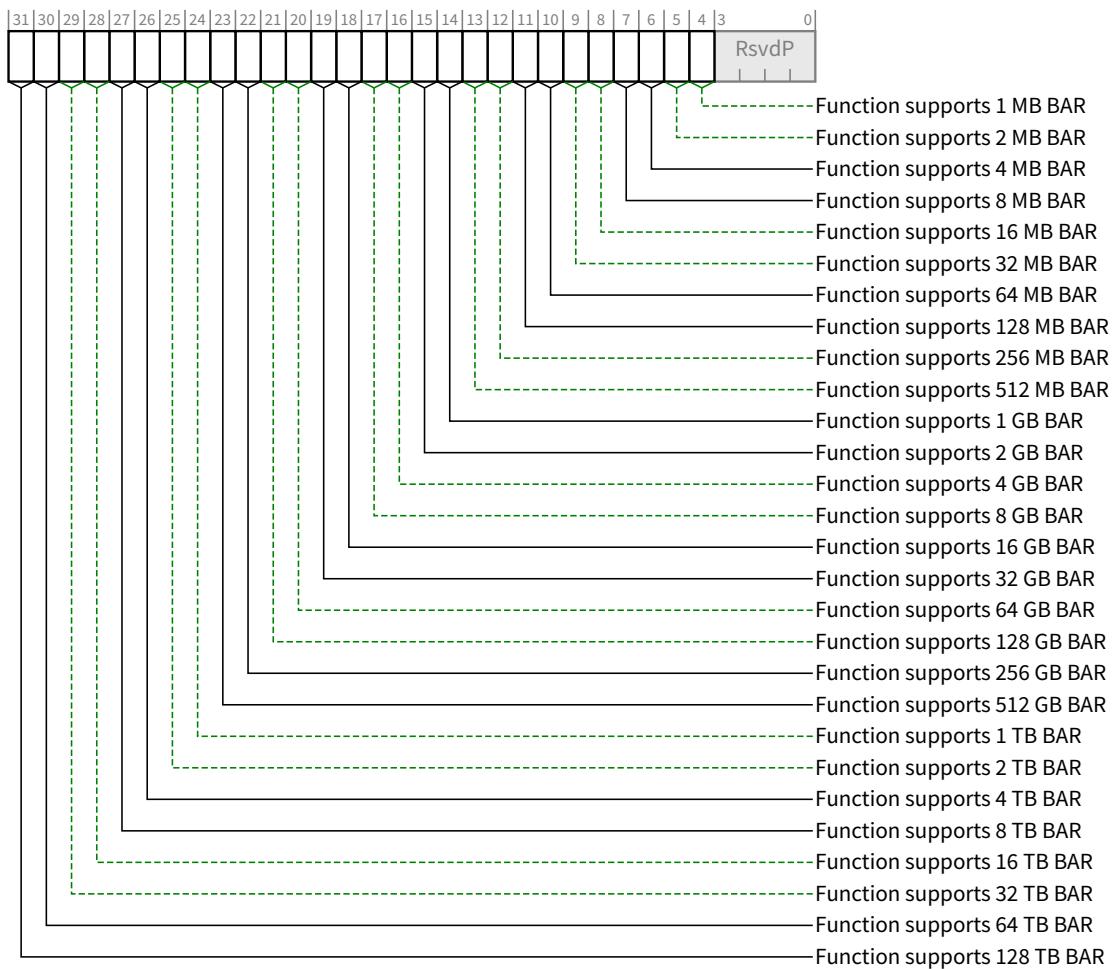


Figure 7-145 Resizable BAR Capability Register

Table 7-116 Resizable BAR Capability Register

Bit Location	Register Description	Attributes
4	Function supports 1 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 1 MB (2^{20} bytes)	RO
5	Function supports 2 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 2 MB (2^{21} bytes)	RO
6	Function supports 4 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 4 MB (2^{22} bytes)	RO
7	Function supports 8 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 8 MB (2^{23} bytes)	RO
8	Function supports 16 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 16 MB (2^{24} bytes)	RO

Bit Location	Register Description	Attributes
9	Function supports 32 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 32 MB (2^{25} bytes)	<u>RO</u>
10	Function supports 64 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 64 MB (2^{26} bytes)	<u>RO</u>
11	Function supports 128 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 128 MB (2^{27} bytes)	<u>RO</u>
12	Function supports 256 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 256 MB (2^{28} bytes)	<u>RO</u>
13	Function supports 512 MB BAR - When Set, indicates that the Function supports operating with the BAR sized to 512 MB (2^{29} bytes)	<u>RO</u>
14	Function supports 1 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 1 GB (2^{30} bytes)	<u>RO</u>
15	Function supports 2 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 2 GB (2^{31} bytes)	<u>RO</u>
16	Function supports 4 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 4 GB (2^{32} bytes)	<u>RO</u>
17	Function supports 8 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 8 GB (2^{33} bytes)	<u>RO</u>
18	Function supports 16 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 16 GB (2^{34} bytes)	<u>RO</u>
19	Function supports 32 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 32 GB (2^{35} bytes)	<u>RO</u>
20	Function supports 64 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 64 GB (2^{36} bytes)	<u>RO</u>
21	Function supports 128 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 128 GB (2^{37} bytes)	<u>RO</u>
22	Function supports 256 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 256 GB (2^{38} bytes)	<u>RO</u>
23	Function supports 512 GB BAR - When Set, indicates that the Function supports operating with the BAR sized to 512 GB (2^{39} bytes)	<u>RO</u>
24	Function supports 1 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 1 TB (2^{40} bytes)	<u>RO</u>
25	Function supports 2 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 2 TB (2^{41} bytes)	<u>RO</u>
26	Function supports 4 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 4 TB (2^{42} bytes)	<u>RO</u>

Bit Location	Register Description	Attributes
27	Function supports 8 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 8 TB (2^{43} bytes)	<u>RO</u>
28	Function supports 16 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 16 TB (2^{44} bytes)	<u>RO</u>
29	Function supports 32 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 32 TB (2^{45} bytes)	<u>RO</u>
30	Function supports 64 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 64 TB (2^{46} bytes)	<u>RO</u>
31	Function supports 128 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 128 TB (2^{47} bytes)	<u>RO</u>

7.8.6.3 Resizable BAR Control Register

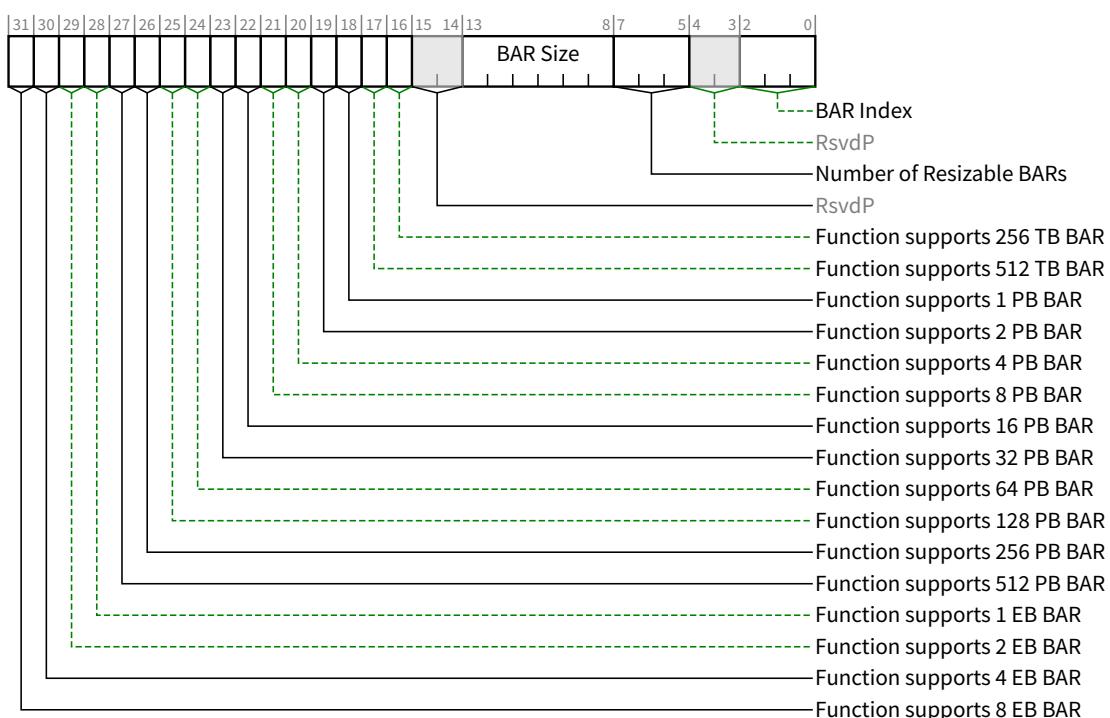


Figure 7-146 Resizable BAR Control Register

Table 7-117 Resizable BAR Control Register

Bit Location	Register Description	Attributes
2:0	BAR Index - This encoded value points to the beginning of the BAR. 0 BAR located at offset 10h	<u>RO</u>

Bit Location	Register Description	Attributes
	<p>1 BAR located at offset 14h 2 BAR located at offset 18h 3 BAR located at offset 1Ch 4 BAR located at offset 20h 5 BAR located at offset 24h Others All other encodings are Reserved. For a 64-bit Base Address register, the BAR Index indicates the lower DWORD. This value indicates which BAR supports a negotiable size.</p>	
7:5	<p>Number of Resizable BARs - Indicates the total number of resizable BARs in the capability structure for the Function. See Figure 7-143.</p> <p>The value of this field must be in the range of 01h to 06h. The field is valid in Resizable BAR Control register (0) (at offset 008h), and is RsvdP for all others.</p>	RO/RsvdP
13:8	<p>BAR Size - This is an encoded value.</p> <p>0 1 MB (2^{20} bytes) 1 2 MB (2^{21} bytes) 2 4 MB (2^{22} bytes) 3 8 MB (2^{23} bytes) ... 43 8 EB (2^{63} bytes)</p> <p>The default value of this field is equal to the default size of the address space that the BAR resource is requesting via the BAR's read-only bits. For backward compatibility with software, the default value must be in the range from 0 to 19.</p> <p>When this register field is programmed, the value is immediately reflected in the size of the resource, as encoded in the number of read-only bits in the BAR.</p> <p>Software must only write values that correspond to those indicated as supported in the Resizable BAR Capability and Control registers. Writing an unsupported value will produce undefined results. BAR Size bits that never need to be Set in order to indicate every supported size are permitted to be hardwired to 0.</p>	RW
16	Function supports 256 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 256 TB (2^{48} bytes)	RO
17	Function supports 512 TB BAR - When Set, indicates that the Function supports operating with the BAR sized to 512 TB (2^{49} bytes)	RO
18	Function supports 1 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 1 PB (2^{50} bytes)	RO
19	Function supports 2 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 2 PB (2^{51} bytes)	RO
20	Function supports 4 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 4 PB (2^{52} bytes)	RO

Bit Location	Register Description	Attributes
21	Function supports 8 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 8 PB (2^{53} bytes)	<u>RO</u>
22	Function supports 16 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 16 PB (2^{54} bytes)	<u>RO</u>
23	Function supports 32 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 32 PB (2^{55} bytes)	<u>RO</u>
24	Function supports 64 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 64 PB (2^{56} bytes)	<u>RO</u>
25	Function supports 128 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 128 PB (2^{57} bytes)	<u>RO</u>
26	Function supports 256 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 256 PB (2^{58} bytes)	<u>RO</u>
27	Function supports 512 PB BAR - When Set, indicates that the Function supports operating with the BAR sized to 512 PB (2^{59} bytes)	<u>RO</u>
28	Function supports 1 EB BAR - When Set, indicates that the Function supports operating with the BAR sized to 1 EB (2^{60} bytes)	<u>RO</u>
29	Function supports 2 EB BAR - When Set, indicates that the Function supports operating with the BAR sized to 2 EB (2^{61} bytes)	<u>RO</u>
30	Function supports 4 EB BAR - When Set, indicates that the Function supports operating with the BAR sized to 4 EB (2^{62} bytes)	<u>RO</u>
31	Function supports 8 EB BAR - When Set, indicates that the Function supports operating with the BAR sized to 8 EB (2^{63} bytes)	<u>RO</u>

7.8.7 ARI Extended Capability

ARI is an optional capability. This capability must be implemented by each Function in an ARI Device. It is not applicable to a Root Port, a Switch Downstream Port, an RCiEP, or a Root Complex Event Collector.

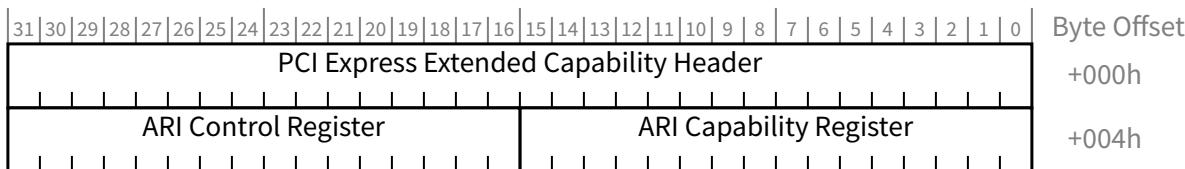


Figure 7-147 ARI Extended Capability

7.8.7.1 ARI Extended Capability Header (Offset 00h)



Figure 7-148 ARI Extended Capability Header

Table 7-118 ARI Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. PCI Express Extended Capability ID for the <u>ARI Extended Capability</u> is 000Eh.	<u>RO</u>
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	<u>RO</u>
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of Capabilities.	<u>RO</u>

7.8.7.2 ARI Capability Register (Offset 04h)

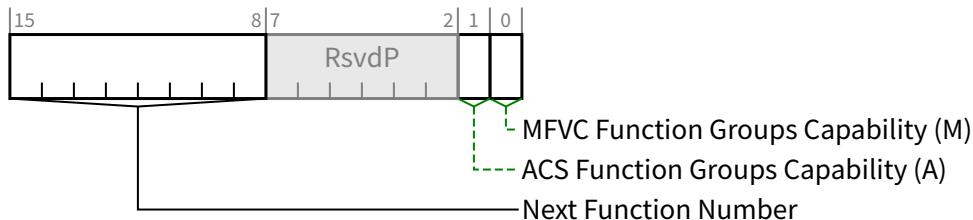


Figure 7-149 ARI Capability Register

Table 7-119 ARI Capability Register

Bit Location	Register Description	Attributes
0	MFVC Function Groups Capability (M) - Applicable only for Function 0; must be 0b for all other Functions. If 1b, indicates that the <u>ARI Device</u> supports <u>Function Group</u> level arbitration via its Multi-Function Virtual Channel (MFVC) Capability structure.	<u>RO</u>
1	ACS Function Groups Capability (A) - Applicable only for Function 0; must be 0b for all other Functions. If 1b, indicates that the <u>ARI Device</u> supports <u>Function Group</u> level granularity for ACS P2P Egress Control via its ACS Capability structures.	<u>RO</u>

Bit Location	Register Description	Attributes
15:8	Next Function Number - This field indicates the Function Number of the next higher numbered Function in the Device, or 00h if there are no higher numbered Functions. Function 0 starts this linked list of Functions.	RO

7.8.7.3 ARI Control Register (Offset 06h)

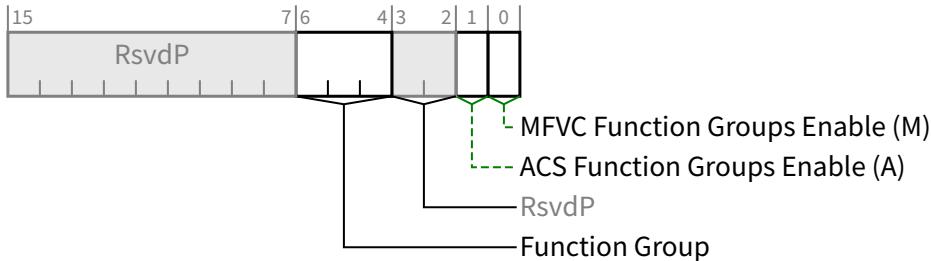


Figure 7-150 ARI Control Register

Table 7-120 ARI Control Register

Bit Location	Register Description	Attributes
0	MFVC Function Groups Enable (M) - Applicable only for Function 0; must be hardwired to 0b for all other Functions. When set, the ARI Device must interpret entries in its <u>Function Arbitration Table</u> as <u>Function Group Numbers</u> rather than Function Numbers. Default value of this bit is 0b. Must be hardwired to 0b if the MFVC Function Groups Capability bit is 0b.	RW
1	ACS Function Groups Enable (A) - Applicable only for Function 0; must be hardwired to 0b for all other Functions. When set, each Function in the ARI Device must associate bits within its <u>Egress Control Vector</u> with <u>Function Group Numbers</u> rather than Function Numbers. Default value of this bit is 0b. Must be hardwired to 0b if the ACS Function Groups Capability bit is 0b.	RW
6:4	Function Group - Assigns a <u>Function Group Number</u> to this Function. Default value of this field is 000b. Must be hardwired to 000b if in Function 0, the MFVC Function Groups Capability bit and ACS Function Groups Capability bit are both 0b.	RW

7.8.8 PASID Extended Capability Structure

The presence of a PASID Extended Capability indicates that the Endpoint supports sending and receiving TLPs containing a PASID TLP Prefix. Separate support and enables are provided for the various optional features.

This capability is applicable to Endpoints and RCIEPs. For Root Ports, support and control is outside the scope of this specification.

This capability is independent of both the ATS and PRI features defined in Chapter 10. Endpoints that contain a PASID Extended Capability need not support ATS or PRI. Endpoints that support ATS or PRI need not support PASID.

Figure 7-151 details allocation of the register bits in the PASID Extended Capability structure.

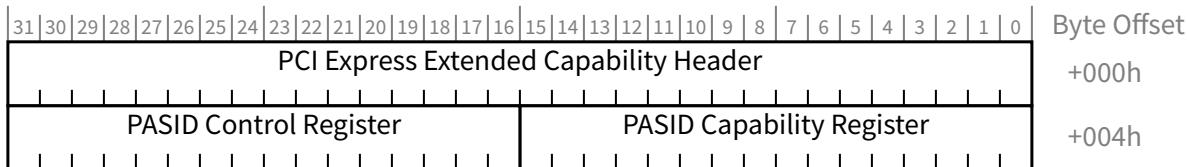


Figure 7-151 PASID Extended Capability Structure

7.8.8.1 PASID Extended Capability Header (Offset 00h)

Figure 7-152 details allocation of the register fields in the PASID Extended Capability Header; Table 7-121 provides the respective bit definitions.

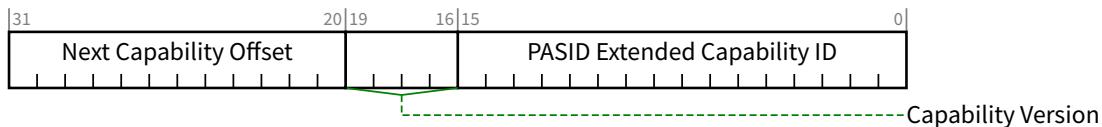


Figure 7-152 PASID Extended Capability Header

Table 7-121 PASID Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PASID Extended Capability ID - Indicates the PASID Extended Capability structure. This field must return a Capability ID of 001Bh indicating that this is a <u>PASID Extended Capability</u> structure.	RO
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	Next Capability Offset - The offset to the next PCI Extended Capability structure or 000h if no other items exist in the linked list of capabilities.	RO

7.8.8.2 PASID Capability Register (Offset 04h)

Figure 7-153 details the allocation of register bits of the PASID Capability register; Table 7-122 provides the respective bit definitions.

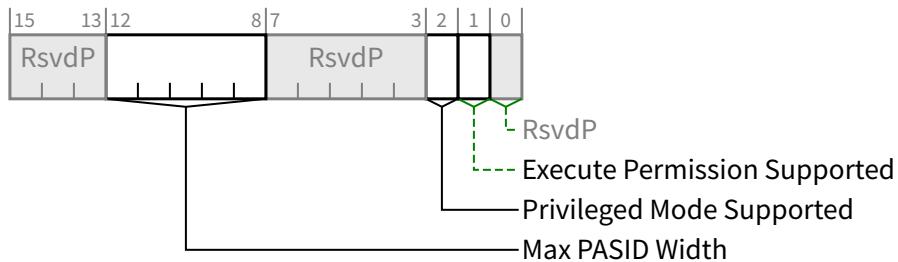


Figure 7-153 PASID Capability Register

Table 7-122 PASID Capability Register

Bit Location	Register Description	Attributes
1	Execute Permission Supported - If Set, the Endpoint supports sending TLPs that have the <u>Execute Requested</u> bit Set. If Clear, the Endpoint will never Set the <u>Execute Requested</u> bit.	<u>RO</u>
2	Privileged Mode Supported - If Set, the Endpoint supports operating in Privileged and Non-Privileged modes, and supports sending requests that have the <u>Privileged Mode Requested</u> bit Set. If Clear, the Endpoint will never Set the <u>Privileged Mode Requested</u> bit.	<u>RO</u>
12:8	Max PASID Width - Indicates the width of the PASID field supported by the Endpoint. The value n indicates support for PASID values 0 through 2^n-1 (inclusive). The value 0 indicates support for a single PASID (0). The value 20 indicates support for all PASID values (20 bits). This field must be between 0 and 20 (inclusive).	<u>RO</u>

7.8.8.3 PASID Control Register (Offset 06h)

Figure 7-154 details the allocation of register bits of the PASID Control register; Table 7-123 provides the respective bit definitions.

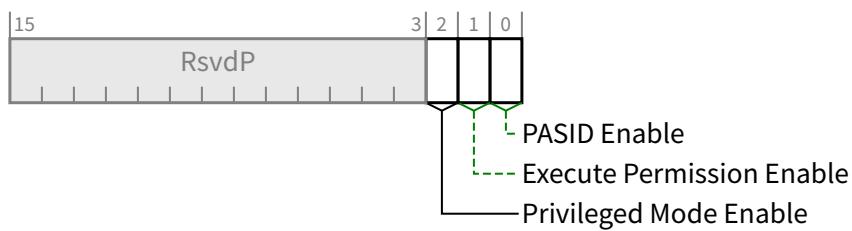


Figure 7-154 PASID Control Register

Table 7-123 PASID Control Register

Bit Location	Register Description	Attributes
0	<p>PASID Enable - If Set, the Endpoint is permitted to send and receive TLPs that contain a PASID TLP Prefix. If Clear, the Endpoint is not permitted to do so.</p> <p>Behavior is undefined if the Endpoint supports ATS and this bit changes value when the Enable (E) bit in the ATS Control register is Set (see Section 10.5.1.3).</p> <p>Default is 0b.</p>	RW
1	<p>Execute Permission Enable - If Set, the Endpoint is permitted to send Requests that have the <u>Execute Requested</u> bit Set. If Clear, the Endpoint is not permitted to do so.</p> <p>Behavior is undefined if the Endpoint supports ATS and this bit changes value when the Enable bit in the ATS Control register is Set (see Section 10.5.1.3).</p> <p>If Execute Permission Supported is Clear, this bit is <u>RsvdP</u>.</p> <p>Default is 0b.</p>	RW/RsvdP (see description)
2	<p>Privileged Mode Enable - If Set, the Endpoint is permitted to send Requests that have the <u>Privileged Mode Requested</u> bit Set. If Clear, the Endpoint is not permitted to do so.</p> <p>Behavior is undefined if the Endpoint supports ATS and this bit changes value when the Enable bit in the ATS Control register is Set (see Section 10.5.1.3).</p> <p>If Privileged Mode Supported is Clear, this bit is <u>RsvdP</u>.</p> <p>Default is 0b.</p>	RW/RsvdP (see description)

7.8.9 FRS Queueing Extended Capability

The FRS Queueing Extended Capability is required for Root Ports and Root Complex Event Collectors that support the optional normative FRS Queueing capability. See [Section 6.23](#). This extended capability is only permitted in Root Ports and Root Complex Event Collectors.

If this capability is present in a Function, that Function must also implement either MSI, MSI-X, or both.

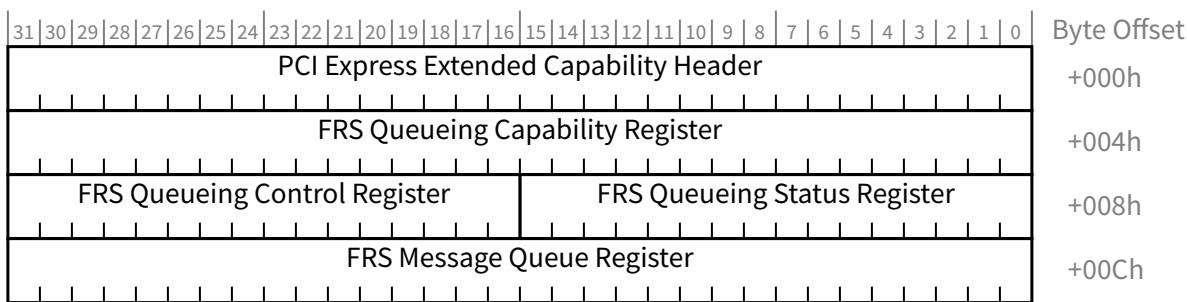


Figure 7-155 FRS Queueing Extended Capability

7.8.9.1 FRS Queueing Extended Capability Header (Offset 00h)

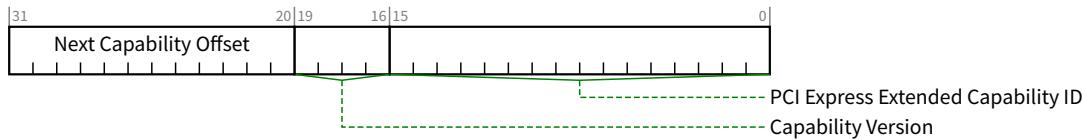


Figure 7-156 FRS Queueing Extended Capability Header

Table 7-124 FRS Queueing Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. PCI Express Extended Capability ID for the FRS Queueing Extended Capability is 0021h.	<u>RO</u>
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.	<u>RO</u>
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Extended Capability structure or 000h if no other items exist in the linked list of capabilities.	<u>RO</u>

7.8.9.2 FRS Queueing Capability Register (Offset 04h)

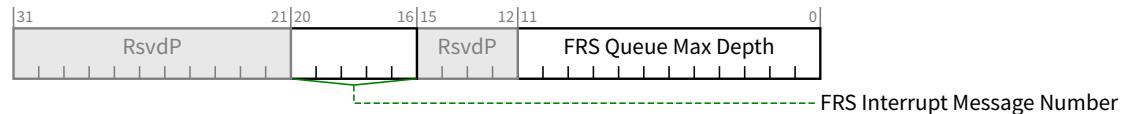


Figure 7-157 FRS Queueing Capability Register

Table 7-125 FRS Queueing Capability Register

Bit Location	Register Description	Attributes
11:0	FRS Queue Max Depth - Indicates the implemented queue depth, with valid values ranging from 001h (queue depth of 1) to FFFh (queue depth of 4095) The value of <u>FRS Message Queue Depth</u> must not exceed this value. The value 000h is Reserved.	<u>HwInit</u>
20:16	FRS Interrupt Message Number - This register indicates which MSI/MSI-X vector is used for the interrupt message generated in association with <u>FRS Message Received</u> or <u>FRS Message Overflow</u> . For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of	<u>RO</u>

Bit Location	Register Description	Attributes
	<p>MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the Message Control Register for MSI.</p> <p>For MSI-X, the value in this register indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant.</p> <p>If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this register must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this register must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this register is undefined.</p>	

7.8.9.3 FRS Queueing Status Register (Offset 08h)

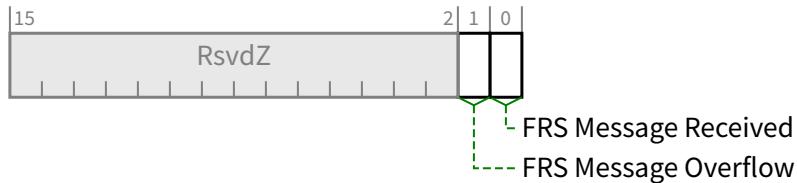


Figure 7-158 FRS Queueing Status Register

Table 7-126 FRS Queueing Status Register

Bit Location	Register Description	Attributes
0	<p>FRS Message Received - This bit is Set when a new FRS Message is Received or generated by this Root Port or Root Complex Event Collector.</p> <p>Root Ports must Clear this bit when the Link is DL_Down.</p> <p>Default value of this bit is 0b.</p>	RW1C
1	<p>FRS Message Overflow - This bit is set if the FRS Message queue is full and a new FRS Message is received or generated by this Root Port or Root Complex Event Collector.</p> <p>Root Ports must Clear this bit when the Link is DL_Down.</p> <p>Default value of this bit is 0b.</p>	RW1C

7.8.9.4 FRS Queueing Control Register (Offset 0Ah)

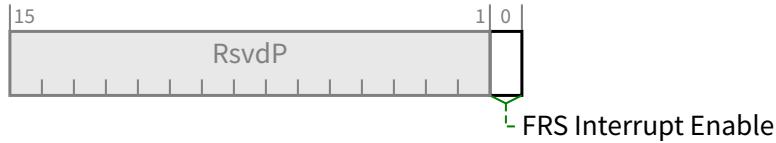


Figure 7-159 FRS Queueing Control Register

Table 7-127 FRS Queueing Control Register

Bit Location	Register Description	Attributes
0	<p>FRS Interrupt Enable - When Set and MSI or MSI-X is enabled, the Port must issue an MSI/MSI-X interrupt to indicate the 0b to 1b transition of either the <u>FRS Message Received</u> or the <u>FRS Message Overflow</u> bits.</p> <p>Default value of this bit is 0b.</p>	RW

7.8.9.5 FRS Message Queue Register (Offset 0Ch)

The FRS Message Queue Register contains fields from the oldest FRS message in the queue. It also indicates the number of FRS messages in the queue.

A write of any value that includes byte 0 to this register removes the oldest FRS Message from the queue and updates these fields. A write to this register when the queue is empty has no effect.

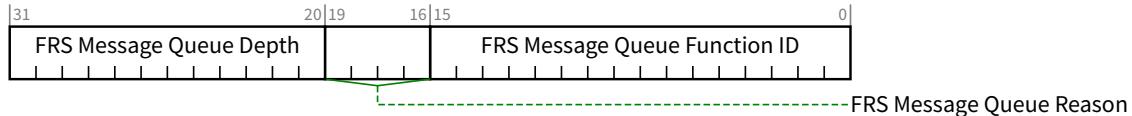


Figure 7-160 FRS Message Queue Register

Table 7-128 FRS Message Queue Register

Bit Location	Register Description	Attributes
15:0	<p>FRS Message Queue Function ID - Recorded from the Requester ID of the oldest <u>FRS Message Received</u> or generated by this Root Port or Root Complex Event Collector and still in the queue.</p> <p>Undefined if <u>FRS Message Queue Depth</u> is 000h.</p>	RO
19:16	<p>FRS Message Queue Reason - Recorded from the FRS Reason of the oldest <u>FRS Message Received</u> or generated by this Root Port or Root Complex Event Collector and still in the queue.</p> <p>Undefined if <u>FRS Message Queue Depth</u> is 000h.</p>	RO
31:20	FRS Message Queue Depth - indicates the current number of <u>FRS Messages</u> in the queue.	RO

Bit Location	Register Description	Attributes
	The value of 000h indicates an empty queue. Default value of this field is 000h.	

7.8.10 Flattening Portal Bridge (FPB) Capability

The Flattening Portal Bridge (FPB) Capability is an optional Capability that is required for any bridge Function that implements FPB. The FPB Capability structure is shown in Figure 7-161.

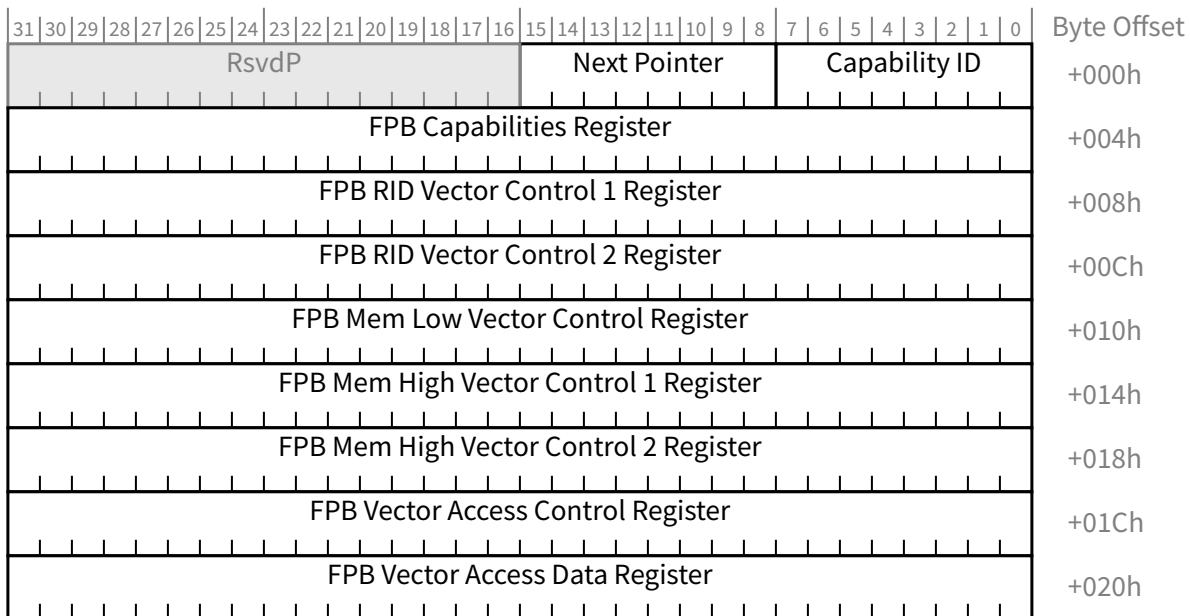


Figure 7-161 FPB Capability Structure

If a Switch implements FPB then each of its Ports of the Switch must implement an FPB Capability Structure. A Root Complex is permitted to implement the FPB Capability Structure on some or on all of its Root Ports. A Root Complex is permitted to implement the FPB Capability for internal logical busses.

7.8.10.1 FPB Capability Header (Offset 00h)

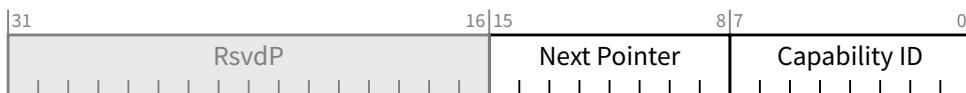


Figure 7-162 FPB Capability Header

Table 7-129 FPB Capability Header

Bit Location	Register Description	Attributes
7:0	Capability ID - Must be set to 15h	RO
15:8	Next Pointer - Pointer to the next item in the capabilities list. Must be 00h for the final item in the list.	RO

7.8.10.2 FPB Capabilities Register (Offset 04h)

Figure 7-163 details allocation of register fields for FPB Capabilities register and Table 7-130 describes the requirements for this register.

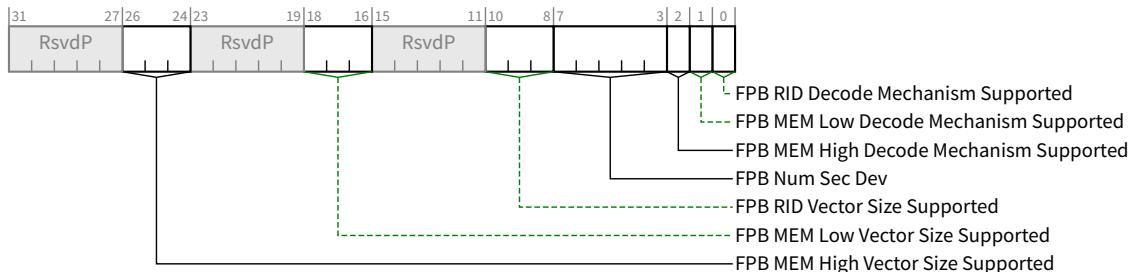


Figure 7-163 FPB Capabilities Register

Table 7-130 FPB Capabilities Register

Bit Location	Register Description	Attributes
0	FPB RID Decode Mechanism Supported - If Set, indicates that the FPB RID Vector mechanism is supported.	HwInit
1	FPB MEM Low Decode Mechanism Supported - If Set, indicates that the FPB MEM Low Vector mechanism is supported.	HwInit
2	FPB MEM High Decode Mechanism Supported - If Set, indicates that the FPB Mem High mechanism is supported.	HwInit
7:3	FPB Num Sec Dev - For Upstream Ports of Switches only, this field indicates the quantity of Device Numbers associated with the Secondary Side of the Upstream Port bridge. The quantity is determined by adding one to the numerical value of this field. Although it is recommended that Switch implementations assign Downstream Ports using all 8 allowed Functions per allocated Device Number, such that all Downstream Ports are assigned within a contiguous range of Device and Function Numbers, it is, however, explicitly permitted to assign Downstream Ports to Function Numbers that are not contiguous within the indicated range of Device Numbers, and system software is required to scan for Switch Downstream Ports at every Function Number within the indicated quantity of Device Numbers associated with the Secondary Side of the Upstream Port. This field is Reserved for Downstream Ports.	HwInit/RsvdP
10:8	FPB RID Vector Size Supported - Indicates the size of the FPB RID Vector implemented in hardware, and constrains the allowed values software is permitted to write to the FPB RID Vector Granularity field.	HwInit

Bit Location	Register Description	Attributes																		
	<p>Defined encodings are:</p> <table border="1" data-bbox="518 291 1062 519"> <thead> <tr> <th data-bbox="518 291 621 354">Value</th><th data-bbox="621 291 703 354">Size</th><th data-bbox="703 291 1062 354">Allowed Granularities in RID units</th></tr> </thead> <tbody> <tr> <td data-bbox="518 354 621 403">000b</td><td data-bbox="621 354 703 403">256 bits</td><td data-bbox="703 354 1062 403">8, 64, 256</td></tr> <tr> <td data-bbox="518 403 621 451">010b</td><td data-bbox="621 403 703 451">1 K bits</td><td data-bbox="703 403 1062 451">8, 64</td></tr> <tr> <td data-bbox="518 451 621 500">101b</td><td data-bbox="621 451 703 500">8 K bits</td><td data-bbox="703 451 1062 500">8</td></tr> </tbody> </table> <p>All other encodings are Reserved.</p> <p>If the <u>FPB RID Decode Mechanism Supported</u> bit is Clear, then the value in this field is undefined and must be ignored by software.</p>	Value	Size	Allowed Granularities in RID units	000b	256 bits	8, 64, 256	010b	1 K bits	8, 64	101b	8 K bits	8							
Value	Size	Allowed Granularities in RID units																		
000b	256 bits	8, 64, 256																		
010b	1 K bits	8, 64																		
101b	8 K bits	8																		
18:16	<p>FPB MEM Low Vector Size Supported - Indicates the size of the FPB MEM Low Vector implemented in hardware, and constrains the allowed values software is permitted to write to the <u>FPB MEM Low Vector Start</u> field.</p> <p>Defined encodings are:</p> <table border="1" data-bbox="518 798 1062 1148"> <thead> <tr> <th data-bbox="518 798 621 861">Value</th><th data-bbox="621 798 703 861">Size</th><th data-bbox="703 798 1062 861">Allowed Granularities in MB units</th></tr> </thead> <tbody> <tr> <td data-bbox="518 861 621 910">000b</td><td data-bbox="621 861 703 910">256 bits</td><td data-bbox="703 861 1062 910">1, 2, 4, 8, 16</td></tr> <tr> <td data-bbox="518 910 621 958">001b</td><td data-bbox="621 910 703 958">512 bits</td><td data-bbox="703 910 1062 958">1, 2, 4, 8</td></tr> <tr> <td data-bbox="518 958 621 1007">010b</td><td data-bbox="621 958 703 1007">1 K bits</td><td data-bbox="703 958 1062 1007">1, 2, 4</td></tr> <tr> <td data-bbox="518 1007 621 1056">011b</td><td data-bbox="621 1007 703 1056">2 K bits</td><td data-bbox="703 1007 1062 1056">1, 2</td></tr> <tr> <td data-bbox="518 1056 621 1104">100b</td><td data-bbox="621 1056 703 1104">4 K bits</td><td data-bbox="703 1056 1062 1104">1</td></tr> </tbody> </table> <p>All other encodings are Reserved.</p> <p>If the <u>FPB MEM Low Decode Mechanism Supported</u> bit is Clear, then the value in this field is undefined and must be ignored by software.</p>	Value	Size	Allowed Granularities in MB units	000b	256 bits	1, 2, 4, 8, 16	001b	512 bits	1, 2, 4, 8	010b	1 K bits	1, 2, 4	011b	2 K bits	1, 2	100b	4 K bits	1	HwInit
Value	Size	Allowed Granularities in MB units																		
000b	256 bits	1, 2, 4, 8, 16																		
001b	512 bits	1, 2, 4, 8																		
010b	1 K bits	1, 2, 4																		
011b	2 K bits	1, 2																		
100b	4 K bits	1																		
26:24	<p>FPB MEM High Vector Size Supported - Indicates the size of the FPB MEM High Vector implemented in hardware.</p> <p>Defined encodings are:</p> <table border="1" data-bbox="698 1396 882 1788"> <thead> <tr> <th data-bbox="698 1396 784 1459">Value</th><th data-bbox="784 1396 882 1459">Size</th></tr> </thead> <tbody> <tr> <td data-bbox="698 1459 784 1507">000b</td><td data-bbox="784 1459 882 1507">256 bits</td></tr> <tr> <td data-bbox="698 1507 784 1556">001b</td><td data-bbox="784 1507 882 1556">512 bits</td></tr> <tr> <td data-bbox="698 1556 784 1605">010b</td><td data-bbox="784 1556 882 1605">1 K bits</td></tr> <tr> <td data-bbox="698 1605 784 1653">011b</td><td data-bbox="784 1605 882 1653">2 K bits</td></tr> <tr> <td data-bbox="698 1653 784 1702">100b</td><td data-bbox="784 1653 882 1702">4 K bits</td></tr> <tr> <td data-bbox="698 1702 784 1750">101b</td><td data-bbox="784 1702 882 1750">8 K bits</td></tr> </tbody> </table> <p>All other encodings are Reserved.</p> <p>All defined Granularities are allowed for all defined vector sizes.</p>	Value	Size	000b	256 bits	001b	512 bits	010b	1 K bits	011b	2 K bits	100b	4 K bits	101b	8 K bits	HwInit				
Value	Size																			
000b	256 bits																			
001b	512 bits																			
010b	1 K bits																			
011b	2 K bits																			
100b	4 K bits																			
101b	8 K bits																			

Bit Location	Register Description	Attributes
	If the <u>FPB MEM High Decode Mechanism Supported</u> bit is Clear, then the value in this field is undefined and must be ignored by software.	

7.8.10.3 FPB RID Vector Control 1 Register (Offset 08h)

Figure 7-164 details allocation of register fields for FPB RID Control 1 register and Table 7-131 describes the requirements for this register.

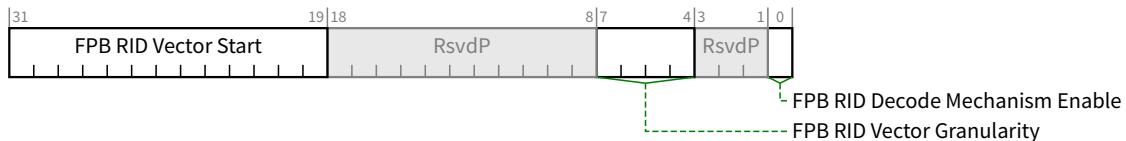


Figure 7-164 FPB RID Vector Control 1 Register

Table 7-131 FPB RID Vector Control 1 Register

Bit Location	Register Description	Attributes								
0	<p>FPB RID Decode Mechanism Enable - When Set, enables the FPB RID Decode mechanism If the <u>FPB RID Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this bit as <u>RO</u>, and in this case the value in this field is undefined. Default value of this bit is 0b.</p>	<u>RW/RO</u>								
7:4	<p>FPB RID Vector Granularity - The value written by software to this field controls the granularity of the FPB RID Vector and the required alignment of the <u>FPB RID Vector Start</u> field (below). Defined encodings are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Granularity</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>8 RIDs</td> </tr> <tr> <td>0011b</td> <td>64 RIDs</td> </tr> <tr> <td>0101b</td> <td>256 RIDs</td> </tr> </tbody> </table> <p>All other encodings are Reserved. Based on the implemented FPB RID Vector size, hardware is permitted to implement as <u>RW</u> only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0. If the <u>FPB RID Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this field as <u>RO</u>, and the value in this field is undefined. For Downstream Ports, if the ARI Forwarding Enable bit in the Device Control 2 Register and the <u>FPB RID Decode Mechanism Enable</u> bit are Set, then software must program 0101b into this field, if this field is programmable. Default value for this field is 0000b.</p>	Value	Granularity	0000b	8 RIDs	0011b	64 RIDs	0101b	256 RIDs	<u>RW/RO</u>
Value	Granularity									
0000b	8 RIDs									
0011b	64 RIDs									
0101b	256 RIDs									

Bit Location	Register Description	Attributes								
31:19	<p>FPB RID Vector Start - The value written by software to this field controls the offset at which the FPB RID Vector is applied.</p> <p>The value represents a RID offset in units of 8 RIDs, such that bit 0 of the FPB RID Vector represents the range of RIDs starting from the value represented in this register up to that value plus the <u>FPB RID Vector Granularity</u> minus 1, and bit 1 represents range from this register value plus granularity up to that value plus <u>FPB RID Vector Granularity</u> minus 1, etc.</p> <p>Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0's) according to the value in the <u>FPB RID Vector Granularity</u> Field as indicated here:</p> <table border="1"> <thead> <tr> <th>FPB RID Vector Granularity</th> <th>Start Alignment Constraint</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td><no constraint></td> </tr> <tr> <td>0011b</td> <td>...00 0b</td> </tr> <tr> <td>0101b</td> <td>...0000 0b</td> </tr> </tbody> </table> <p>All other encodings are Reserved.</p> <p>If this requirement is violated, the hardware behavior is undefined.</p> <p>For Downstream Ports, if the ARI Forwarding Enable bit in the Device Control 2 Register and the <u>FPB RID Decode Mechanism Enable</u> bit are Set, then software must program bits 23:19 of this field to a value of 0000 0b, and the hardware behavior is undefined if any other value is programmed.</p> <p>If the <u>FPB RID Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined.</p> <p>Default value for this field is 0000 0000 0000 0b.</p>	FPB RID Vector Granularity	Start Alignment Constraint	0000b	<no constraint>	0011b	...00 0b	0101b	...0000 0b	RW/RO
FPB RID Vector Granularity	Start Alignment Constraint									
0000b	<no constraint>									
0011b	...00 0b									
0101b	...0000 0b									

7.8.10.4 FPB RID Vector Control 2 Register (Offset 0ch)

Figure 7-165 details allocation of register fields for FPB RID Vector Control 2 register and Table 7-132 describes the requirements for this register

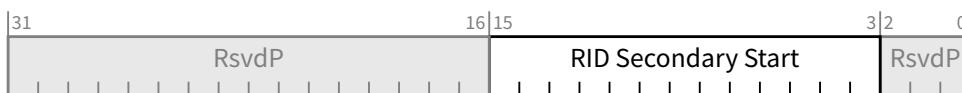


Figure 7-165 FPB RID Vector Control 2 Register

Table 7-132 FPB RID Vector Control 2 Register

Bit Location	Register Description	Attributes
15:3	<p>RID Secondary Start - The value written by software to this field controls the RID offset at which Type 1 Configuration Requests passing downstream through the bridge must be converted to Type 0.</p> <p>Bits[2:0] of the RID offset are fixed by hardware as 000b and cannot be modified.</p> <p>For Downstream Ports, if the ARI Forwarding Enable bit in the Device Control 2 register is Set, then software must write bits 7:3 of this field to 0 0000b.</p>	RW/RO

Bit Location	Register Description	Attributes
	If the <u>FPB RID Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this field as <u>RO</u> , and the value in this field is undefined. Default value for this field is 0000 0000 0000 0b.	

7.8.10.5 FPB MEM Low Vector Control Register (Offset 10h)

Figure 7-166 details allocation of register fields for FPB MEM Low Vector Control Register and Table 7-133 describes the requirements for this register.

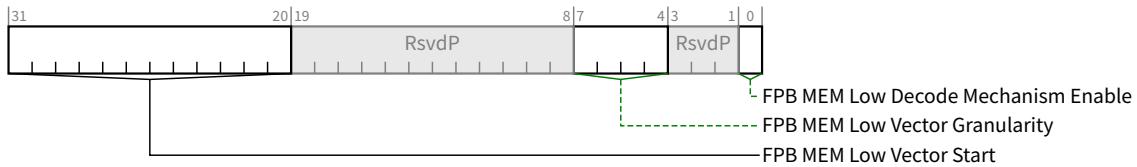


Figure 7-166 FPB MEM Low Vector Control Register

Table 7-133 FPB MEM Low Vector Control Register

Bit Location	Register Description	Attributes												
0	FPB MEM Low Decode Mechanism Enable - When Set, enables the FPB MEM Low Decode mechanism. If the <u>FPB MEM Low Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this bit as <u>RO</u> , and in this case the value in this field is undefined. Default value of this bit is 0b.	<u>RW/RO</u>												
7:4	FPB MEM Low Vector Granularity - The value written by software to this field controls the granularity of the FPB MEM Low Vector, and the required alignment of the <u>FPB MEM Low Vector Start</u> field (below). Defined encodings are: <table border="1"> <thead> <tr> <th>Value</th> <th>Granularity</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>1 MB</td> </tr> <tr> <td>0001b</td> <td>2 MB</td> </tr> <tr> <td>0010b</td> <td>4 MB</td> </tr> <tr> <td>0011b</td> <td>8 MB</td> </tr> <tr> <td>0100b</td> <td>16 MB</td> </tr> </tbody> </table> All other encodings are Reserved. Based on the implemented FPB MEM Low Vector size, hardware is permitted to implement as <u>RW</u> only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0. If the <u>FPB MEM Low Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this field as <u>RO</u> , and the value in this field is undefined.	Value	Granularity	0000b	1 MB	0001b	2 MB	0010b	4 MB	0011b	8 MB	0100b	16 MB	<u>RW/RO</u>
Value	Granularity													
0000b	1 MB													
0001b	2 MB													
0010b	4 MB													
0011b	8 MB													
0100b	16 MB													

Bit Location	Register Description	Attributes												
	<p>Default value for this field is 0000b.</p>													
31:20	<p>FPB MEM Low Vector Start - The value written by software to this field sets bits 31:20 of the base address at which the FPB MEM Low Vector is applied.</p> <p>Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0's) according to the value in the FPB MEM Low Vector Granularity field as indicated here:</p> <table border="1"> <thead> <tr> <th>FPB MEM Low Vector Granularity</th> <th>Constraint</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td><no constraint></td> </tr> <tr> <td>0001b</td> <td>...0b</td> </tr> <tr> <td>0010b</td> <td>...00b</td> </tr> <tr> <td>0011b</td> <td>...000b</td> </tr> <tr> <td>0100b</td> <td>...0000b</td> </tr> </tbody> </table> <p>If this requirement is violated, the hardware behavior is undefined.</p> <p>If the FPB MEM Low Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined.</p> <p>Default value for this field is 000h.</p>	FPB MEM Low Vector Granularity	Constraint	0000b	<no constraint>	0001b	...0b	0010b	...00b	0011b	...000b	0100b	...0000b	RW/RO
FPB MEM Low Vector Granularity	Constraint													
0000b	<no constraint>													
0001b	...0b													
0010b	...00b													
0011b	...000b													
0100b	...0000b													

7.8.10.6 FPB MEM High Vector Control 1 Register (Offset 14h)

Figure 7-167 details allocation of register fields for FPB MEM High Vector Control 1 Register and Table 7-134 describes the requirements for this register.

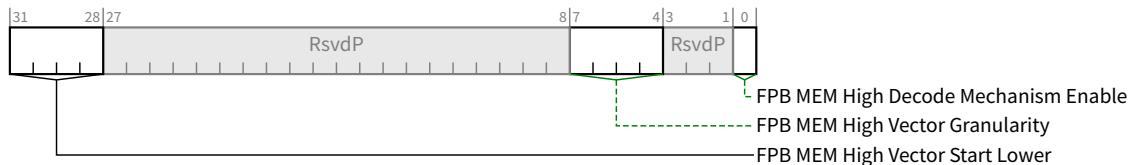


Figure 7-167 FPB MEM High Vector Control 1 Register

Table 7-134 FPB MEM High Vector Control 1 Register

Bit Location	Register Description	Attributes
0	<p>FPB MEM High Decode Mechanism Enable - When Set, enables the FPB MEM High Decode mechanism.</p> <p>If the FPB MEM High Decode Mechanism Supported bit is Clear, then it is permitted for hardware to implement this bit as RO, and in this case the value in this field is undefined.</p> <p>Default value of this bit is 0b.</p>	RW/RO

Bit Location	Register Description	Attributes																		
7:4	<p>FPB MEM High Vector Granularity - The value written by software to this field controls the granularity of the FPB MEM High Vector, and the required alignment of the <u>FPB MEM High Vector Start Lower</u> field (below).</p> <p>Software is permitted to select any allowed Granularity from the table below regardless of the value in the <u>FPB MEM High Vector Size Supported</u> field.</p> <p>Defined encodings are:</p> <table border="1"> <thead> <tr> <th>Value</th><th>Granularity</th></tr> </thead> <tbody> <tr><td>0000b</td><td>256 MB</td></tr> <tr><td>0001b</td><td>512 MB</td></tr> <tr><td>0010b</td><td>1 GB</td></tr> <tr><td>0011b</td><td>2 GB</td></tr> <tr><td>0100b</td><td>4 GB</td></tr> <tr><td>0101b</td><td>8 GB</td></tr> <tr><td>0110b</td><td>16 GB</td></tr> <tr><td>0111b</td><td>32 GB</td></tr> </tbody> </table> <p>All other encodings are Reserved.</p> <p>Based on the implemented FPB MEM High Vector size, hardware is permitted to implement as RW only those bits of this field that can be programmed to non-zero values, in which case the upper order bits are permitted but not required to be hardwired to 0.</p> <p>If the <u>FPB MEM High Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this field as RO, and the value in this field is undefined.</p> <p>Default value for this field is 0000b.</p>	Value	Granularity	0000b	256 MB	0001b	512 MB	0010b	1 GB	0011b	2 GB	0100b	4 GB	0101b	8 GB	0110b	16 GB	0111b	32 GB	RW/RO
Value	Granularity																			
0000b	256 MB																			
0001b	512 MB																			
0010b	1 GB																			
0011b	2 GB																			
0100b	4 GB																			
0101b	8 GB																			
0110b	16 GB																			
0111b	32 GB																			
31:28	<p>FPB MEM High Vector Start Lower - The value written by software to this field sets the lower bits of the base address at which the FPB MEM High Vector is applied.</p> <p>Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0's) according to the value in the <u>FPB MEM High Vector Granularity</u> Field as indicated here:</p> <table border="1"> <thead> <tr> <th>FPB MEM High Vector Granularity</th><th>Constraint</th></tr> </thead> <tbody> <tr><td>0000b</td><td><no constraint></td></tr> <tr><td>0001b</td><td>...0b</td></tr> <tr><td>0010b</td><td>...00b</td></tr> <tr><td>0011b</td><td>...000b</td></tr> <tr><td>0100b</td><td>...0000b</td></tr> <tr><td>0101b</td><td>...0 0000b</td></tr> <tr><td>0110b</td><td>...00 0000b</td></tr> <tr><td>0111b</td><td>...000 0000b</td></tr> </tbody> </table>	FPB MEM High Vector Granularity	Constraint	0000b	<no constraint>	0001b	...0b	0010b	...00b	0011b	...000b	0100b	...0000b	0101b	...0 0000b	0110b	...00 0000b	0111b	...000 0000b	RW/RO
FPB MEM High Vector Granularity	Constraint																			
0000b	<no constraint>																			
0001b	...0b																			
0010b	...00b																			
0011b	...000b																			
0100b	...0000b																			
0101b	...0 0000b																			
0110b	...00 0000b																			
0111b	...000 0000b																			

Bit Location	Register Description	Attributes
	<p>If this requirement is violated, the hardware behavior is undefined.</p> <p>If the <u>FPB MEM High Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this field as <u>RO</u>, and the value in this field is undefined.</p> <p>Default value for this field is 0h.</p>	

7.8.10.7 FPB MEM High Vector Control 2 Register (Offset 18h)

Figure 7-168 details allocation of register fields for FPB MEM High Vector Control 2 Register and Table 7-135 describes the requirements for this register.

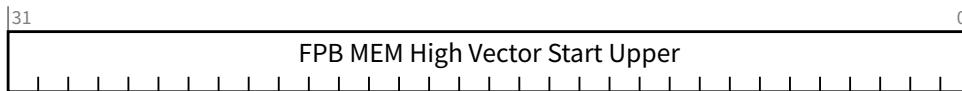


Figure 7-168 FPB MEM High Vector Control 2 Register

Table 7-135 FPB MEM High Vector Control 2 Register

Bit Location	Register Description	Attributes																		
31:0	<p>FPB MEM High Vector Start Upper - The value written by software to this field sets bits 63:32 of the base address at which the FPB MEM High Vector is applied.</p> <p>Software must program this field to a value that is naturally aligned (meaning the lower order bits must be 0's) according to the value in the <u>FPB MEM High Vector Granularity Field</u> as indicated here:</p> <table border="1"> <thead> <tr> <th>FPB MEM High Vector Granularity</th> <th>Constraint</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td><no constraint></td> </tr> <tr> <td>0001b</td> <td><no constraint></td> </tr> <tr> <td>0010b</td> <td><no constraint></td> </tr> <tr> <td>0011b</td> <td><no constraint></td> </tr> <tr> <td>0100b</td> <td><no constraint></td> </tr> <tr> <td>0101b</td> <td>...0b</td> </tr> <tr> <td>0110b</td> <td>...00b</td> </tr> <tr> <td>0111b</td> <td>...000b</td> </tr> </tbody> </table> <p>If this requirement is violated, the hardware behavior is undefined</p> <p>If the <u>FPB MEM High Decode Mechanism Supported</u> bit is Clear, then it is permitted for hardware to implement this field as <u>RO</u>, and the value in this field is undefined.</p> <p>Default value for this field is 0000 0000h.</p>	FPB MEM High Vector Granularity	Constraint	0000b	<no constraint>	0001b	<no constraint>	0010b	<no constraint>	0011b	<no constraint>	0100b	<no constraint>	0101b	...0b	0110b	...00b	0111b	...000b	RW/ <u>RO</u>
FPB MEM High Vector Granularity	Constraint																			
0000b	<no constraint>																			
0001b	<no constraint>																			
0010b	<no constraint>																			
0011b	<no constraint>																			
0100b	<no constraint>																			
0101b	...0b																			
0110b	...00b																			
0111b	...000b																			

7.8.10.8 FPB Vector Access Control Register (Offset 1Ch)

Figure 7-169 details allocation of register fields for FPB Vector Access Control register and Table 7-136 describes the requirements for this register.

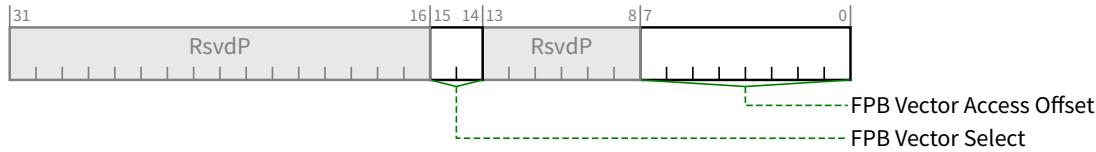


Figure 7-169 FPB Vector Access Control Register

Table 7-136 FPB Vector Access Control Register

Bit Location	Register Description	Attributes																					
7:0	<p>FPB Vector Access Offset - The value in this field indicates the offset of the DWORD portion of the FPB RID, MEM Low or MEM High, Vector that can be read or written by means of the FPB Vector Access Data register.</p> <p>The selection of RID, MEM Low or MEM High is made by the value written to the FPB Vector Select field.</p> <p>The bits of this field map to the offset according to the value in the corresponding FPB RID, MEM Low, or MEM High Vector Size Supported field as shown here:</p> <table border="1"> <thead> <tr> <th>Vector Size Supported</th><th>Offset Bits</th><th>Vector Access Offset</th></tr> </thead> <tbody> <tr> <td>000b</td><td>2:0</td><td>2:0 (7:3 unused)</td></tr> <tr> <td>001b</td><td>3:0</td><td>3:0 (7:4 unused)</td></tr> <tr> <td>010b</td><td>4:0</td><td>4:0 (7:5 unused)</td></tr> <tr> <td>011b</td><td>5:0</td><td>5:0 (7:6 unused)</td></tr> <tr> <td>100b</td><td>6:0</td><td>6:0 (7 unused)</td></tr> <tr> <td>101b</td><td>7:0</td><td>7:0</td></tr> </tbody> </table> <p>All other encodings are Reserved.</p> <p>Bits in this field that are unused per the table above must be written by software as 0b, and are permitted but not required to be implemented as RO.</p> <p>Default value for this field is 00h</p>	Vector Size Supported	Offset Bits	Vector Access Offset	000b	2:0	2:0 (7:3 unused)	001b	3:0	3:0 (7:4 unused)	010b	4:0	4:0 (7:5 unused)	011b	5:0	5:0 (7:6 unused)	100b	6:0	6:0 (7 unused)	101b	7:0	7:0	RW/RO
Vector Size Supported	Offset Bits	Vector Access Offset																					
000b	2:0	2:0 (7:3 unused)																					
001b	3:0	3:0 (7:4 unused)																					
010b	4:0	4:0 (7:5 unused)																					
011b	5:0	5:0 (7:6 unused)																					
100b	6:0	6:0 (7 unused)																					
101b	7:0	7:0																					
15:14	<p>FPB Vector Select - The value written to this field selects the Vector to be accessed at the indicated FPB Vector Access Offset. Software must only write this field with values that correspond to supported FPB mechanisms, otherwise the results are undefined.</p> <p>Defined encodings are:</p> <ul style="list-style-type: none"> 00b RID 01b MEM Low 10b MEM High 	RW																					

Bit Location	Register Description	Attributes
11b	Reserved Default value for this field is 00b	

7.8.10.9 FPB Vector Access Data Register (Offset 20h)

Figure 7-170 details allocation of register fields for [FPB Vector Access Data Register](#) and [Table 7-137](#) describes the requirements for this register.

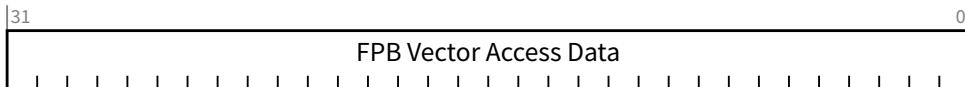


Figure 7-170 FPB Vector Access Data Register

Table 7-137 FPB Vector Access Data Register

Bit Location	Register Description	Attributes
31:0	FPB Vector Access Data - Reads from this register return the DW of data from the FPB Vector at the location determined by the value in the FPB Vector Access Offset Register . Writes to this register replace the DW of data from the FPB Vector at the location determined by the value in the FPB Vector Access Offset Register . Behavior of this field is undefined if software programs unsupported values for FPB Vector Select or FPB Vector Access Offset fields, however hardware is required to complete the access to this register normally. Default value for this field is 0000 0000h	RW

7.9 Additional PCI and PCIe Capabilities

This section, contains a description of additional PCI and PCIe capabilities that are individually optional in this but may be required by other PCISIG specifications.

7.9.1 Virtual Channel Extended Capability

The [Virtual Channel Extended Capability \(VC Capability\)](#) is an optional Extended Capability required for devices that have Ports (or for individual Functions) that support functionality beyond the default Traffic Class (TC0) over the default Virtual Channel (VC0). This may apply to devices with only one VC that support TC filtering or to devices that support multiple VCs. Note that a PCI Express device that supports only TC0 over VC0 does not require VC Extended Capability and associated registers. [Figure 7-171](#) provides a high level view of the [Virtual Channel Extended Capability](#) structure. This structure controls Virtual Channel assignment for PCI Express Links and may be present in any device (or [RCRB](#)) that contains (controls) a Port, or any device that has a Multi-Function Virtual Channel (MFVC) Capability structure. Some registers/fields in the [Virtual Channel Extended Capability](#) structure may have different interpretation for Endpoints,

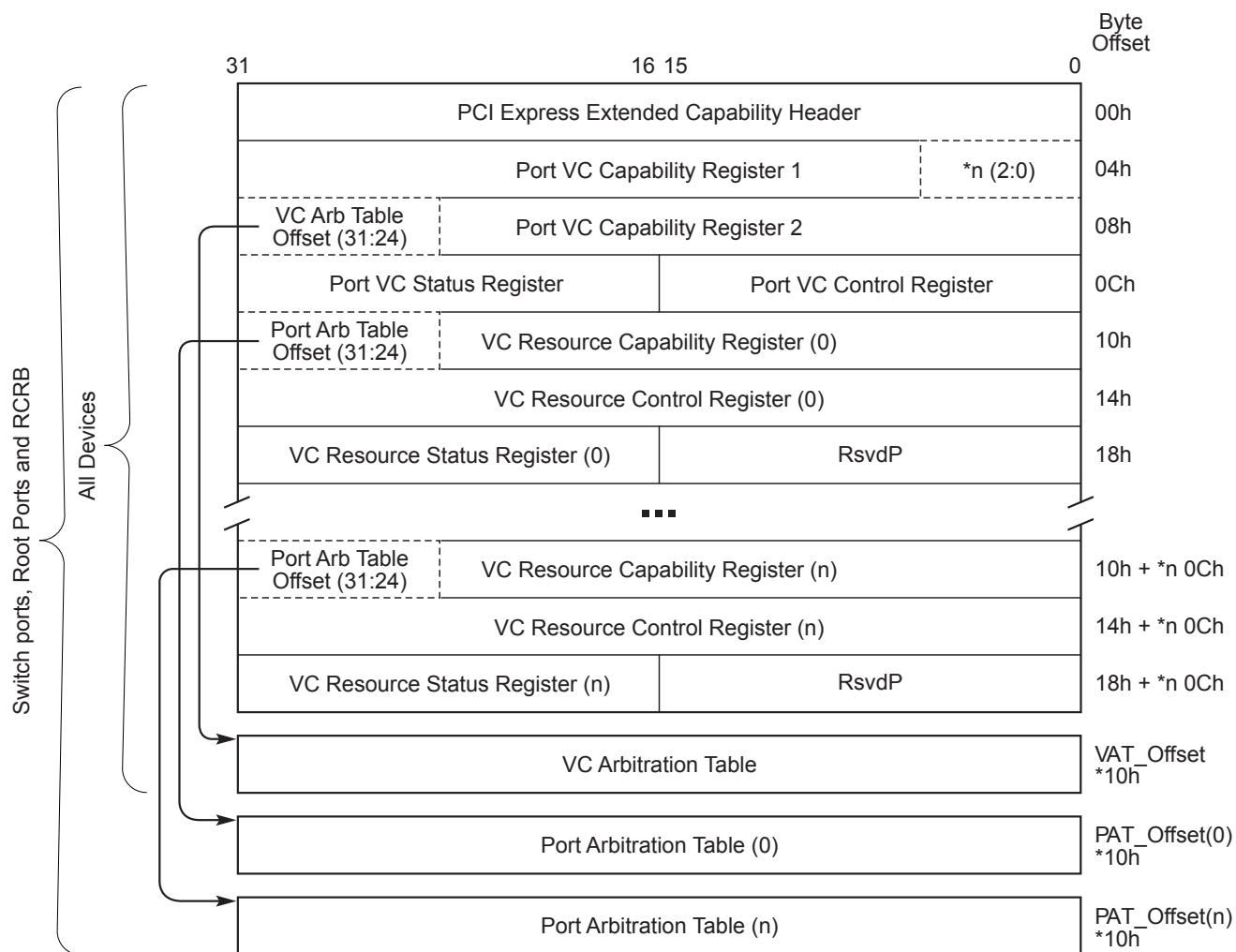
Switch Ports, Root Ports and RCRB. Software must interpret the Device/Port Type field in the PCI Express Capabilities register to determine the availability and meaning of these registers/fields.

The number of (extended) Virtual Channels is indicated by the Extended VC Count field in the Port VC Capability Register 1. Software must interpret this field to determine the availability of extended VC Resource registers.

The VC Capability structure is permitted in the Extended Configuration Space of all single-Function devices or in RCRBs.

A Multi-Function Device at an Upstream Port is permitted to optionally contain a Multi-Function Virtual Channel (MFVC) Capability structure (see Section 7.9.2). If a Multi-Function Device contains an MFVC Capability structure, any or all of its Functions are permitted to contain a VC Capability structure. Per-Function VC Capability structures are also permitted for devices inside a Switch that contain only Switch Downstream Port Functions, or for RCiEPs. Otherwise, only Function 0 is permitted to contain a VC Capability structure.

To preserve software backward compatibility, two Extended Capability IDs are permitted for VC Capability structures: 0002h and 0009h. Any VC Capability structure in a device that also contains an MFVC Capability structure must use the Extended Capability ID 0009h. A VC Capability structure in a device that does not contain an MFVC Capability structure must use the Extended Capability ID 0002h.



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Figure 7-171 Virtual Channel Extended Capability Structure

The following sections describe the registers/fields of the Virtual Channel Extended Capability structure.

7.9.1.1 Virtual Channel Extended Capability Header (Offset 00h)

Refer to Section 7.6.3 for a description of the PCI Express Extended Capability header. A Virtual Channel Extended Capability must use one of two Extended Capability IDs: 0002h or 0009h. Refer to Section 7.9.1 for rules governing when each should be used. Figure 7-172 details allocation of register fields in the Virtual Channel Extended Capability Header; Table 7-138 provides the respective bit definitions.

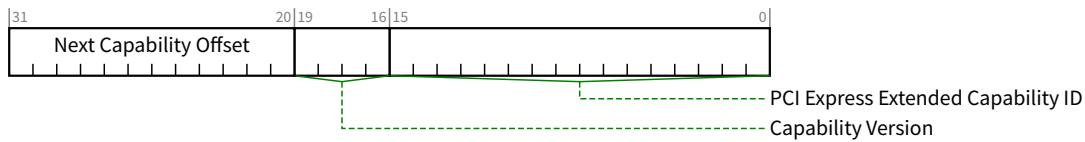


Figure 7-172 Virtual Channel Extended Capability Header

Table 7-138 Virtual Channel Extended Capability Header

Bit Location	Register Description	Attributes
15:0	PCI Express Extended Capability ID - This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. Extended Capability ID for the Virtual Channel Extended Capability is either 0002h or 0009h.	RO
19:16	Capability Version - This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.	RO
31:20	Next Capability Offset - This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI-compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than OFFh.	RO

7.9.1.2 Port VC Capability Register 1 (Offset 04h)

The Port VC Capability Register 1 describes the configuration of the Virtual Channels associated with a PCI Express Port. Figure 7-173 details allocation of register fields in the Port VC Capability Register 1; Table 7-139 provides the respective bit definitions.

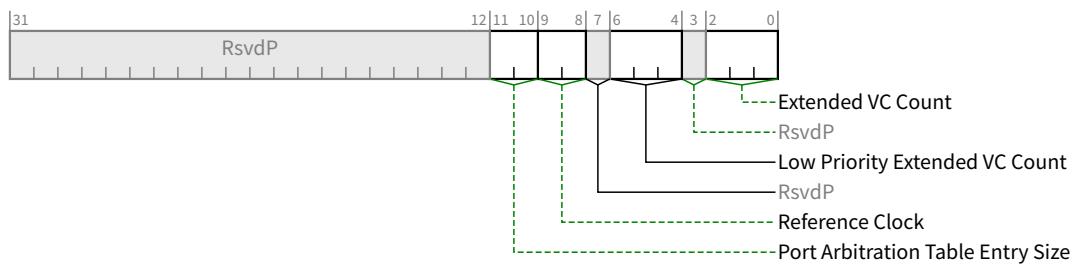


Figure 7-173 Port VC Capability Register 1

Table 7-139 Port VC Capability Register 1

Bit Location	Register Description	Attributes
2:0	<p>Extended VC Count - Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. This field is valid for all Functions.</p> <p>This value indicates the number of (extended) VC Resource Capability, Control, and Status registers that are present in Configuration Space in addition to the required VC Resource registers for the default VC.</p> <p>The minimum value of this field is 0 (for devices that only support the default VC and only have 1 set of VC Resource Registers for that VC). The maximum value is 7.</p>	RO
6:4	<p>Low Priority Extended VC Count - Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. This field is valid for all Functions.</p> <p>The minimum value of this field is 000b and the maximum value is <u>Extended VC Count</u>.</p>	RO
9:8	<p>Reference Clock - Indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. This field is valid for <u>RCRBs</u>, Switch Ports, and Root Ports that support peer-to-peer traffic. It is not valid for Root Ports that do not support peer-to-peer traffic, Endpoints, and Switches or Root Complexes not implementing WRR, and must be hardwired to 00b.</p> <p>Defined encodings are:</p> <ul style="list-style-type: none"> 00b 100 ns reference clock 01b - 11b Reserved 	RO
11:10	<p>Port Arbitration Table Entry Size - Indicates the size (in bits) of Port Arbitration table entry in the Function. This field is valid only for <u>RCRBs</u>, Switch Ports, and Root Ports that support peer-to-peer traffic. It is not valid and must be hardwired to 00b for Root Ports that do not support peer-to-peer traffic and Endpoints.</p> <p>Defined encodings are:</p> <ul style="list-style-type: none"> 00b The size of Port Arbitration table entry is 1 bit. 01b The size of Port Arbitration table entry is 2 bits. 10b The size of Port Arbitration table entry is 4 bits. 11b The size of Port Arbitration table entry is 8 bits. 	RO

7.9.1.3 Port VC Capability Register 2 (Offset 08h)

The Port VC Capability Register 2 provides further information about the configuration of the Virtual Channels associated with a PCI Express Port. Figure 7-174 details allocation of register fields in the Port VC Capability Register 2; Table 7-140 provides the respective bit definitions.

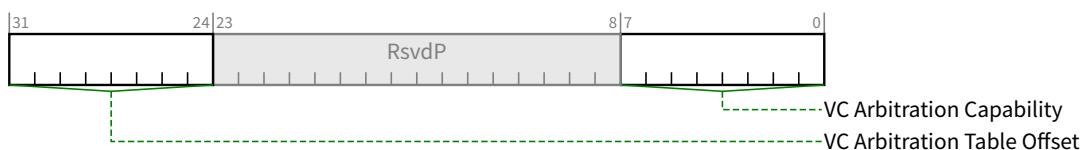


Figure 7-174 Port VC Capability Register 2

Table 7-140 Port VC Capability Register 2

Bit Location	Register Description	Attributes
7:0	<p>VC Arbitration Capability - Indicates the types of VC Arbitration supported by the Function for the LPVC group. This field is valid for all Functions that report a Low Priority Extended VC Count field greater than 0. For all other Functions, this field must be hardwired to 00h.</p> <p>Each Bit Location within this field corresponds to a <u>VC Arbitration Capability</u> defined below. When more than 1 bit in this field is Set, it indicates that the Port can be configured to provide different VC arbitration services.</p> <p>Defined bit positions are:</p> <ul style="list-style-type: none"> Bit 0 Hardware fixed arbitration scheme, e.g., Round Robin Bit 1 Weighted Round Robin (WRR) arbitration with 32 phases Bit 2 WRR arbitration with 64 phases Bit 3 WRR arbitration with 128 phases Bits 4-7 Reserved 	RO
31:24	<p>VC Arbitration Table Offset - Indicates the location of the VC Arbitration Table. This field is valid for all Functions.</p> <p>This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the <u>Virtual Channel Extended Capability</u> structure. A value of 0 indicates that the table is not present.</p>	RO

7.9.1.4 Port VC Control Register (Offset 0Ch)

Figure 7-175 details allocation of register fields in the Port VC Control Register; Table 7-141 provides the respective bit definitions.

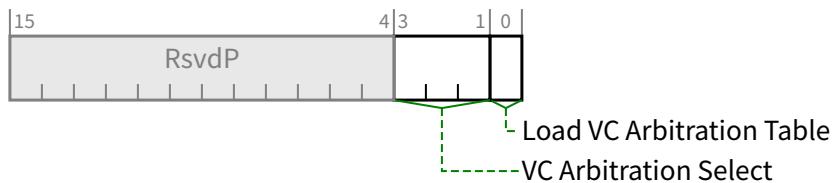


Figure 7-175 Port VC Control Register

Table 7-141 Port VC Control Register

Bit Location	Register Description	Attributes
0	<p>Load VC Arbitration Table - Used by software to update the VC Arbitration Table. This bit is valid for all Functions when the selected VC Arbitration uses the VC Arbitration Table.</p> <p>Software sets this bit to request hardware to apply new values programmed into VC Arbitration Table; clearing this bit has no effect. Software checks the <u>VC Arbitration Table Status</u> bit to confirm that new values stored in the VC Arbitration Table are latched by the VC arbitration logic.</p> <p>This bit always returns 0b when read.</p>	RW

Bit Location	Register Description	Attributes
3:1	<p>VC Arbitration Select - Used by software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the <u>VC Arbitration Capability</u> field in the <u>Port VC Capability Register 2</u>. This field is valid for all Functions.</p> <p>The permissible values of this field are numbers corresponding to one of the asserted bits in the <u>VC Arbitration Capability</u> field.</p> <p>This field cannot be modified when more than one VC in the LPVC group is enabled.</p>	RW

7.9.1.5 Port VC Status Register (Offset 0Eh)

The Port VC Status Register provides status of the configuration of Virtual Channels associated with a Port. Figure 7-176 details allocation of register fields in the Port VC Status Register; Table 7-142 provides the respective bit definitions.

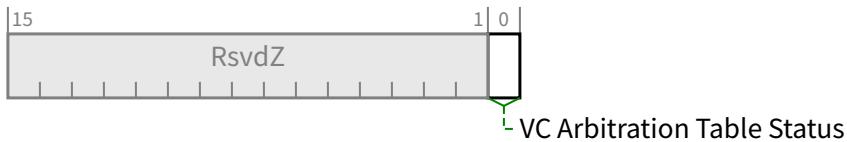


Figure 7-176 Port VC Status Register

Table 7-142 Port VC Status Register

Bit Location	Register Description	Attributes
0	<p>VC Arbitration Table Status - Indicates the coherency status of the VC Arbitration Table. This bit is valid for all Functions when the selected VC uses the VC Arbitration Table.</p> <p>This bit is Set by hardware when any entry of the VC Arbitration Table is written by software. This bit is Cleared by hardware when hardware finishes loading values stored in the VC Arbitration Table after software sets the Load VC Arbitration Table bit in the Port VC Control Register.</p> <p>Default value of this bit is 0b.</p>	RO

7.9.1.6 VC Resource Capability Register

The VC Resource Capability Register describes the capabilities and configuration of a particular Virtual Channel resource. Figure 7-177 details allocation of register fields in the VC Resource Capability Register; Table 7-143 provides the respective bit definitions.

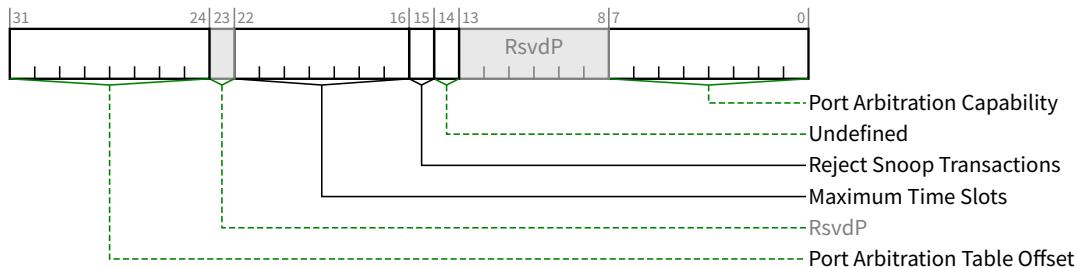


Figure 7-177 VC Resource Capability Register

Table 7-143 VC Resource Capability Register

Bit Location	Register Description	Attributes
7:0	<p>Port Arbitration Capability - Indicates types of Port Arbitration supported by the VC resource. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but not for Endpoints or Root Ports that do not support peer-to-peer traffic.</p> <p>Each Bit Location within this field corresponds to a Port Arbitration Capability defined below. When more than 1 bit in this field is Set, it indicates that the VC resource can be configured to provide different arbitration services.</p> <p>Software selects among these capabilities by writing to the <u>Port Arbitration Select</u> field (see Section 7.9.1.7).</p> <p>Defined bit positions are:</p> <ul style="list-style-type: none"> Bit 0 Non-configurable hardware-fixed arbitration scheme, e.g., Round Robin (RR) Bit 1 Weighted Round Robin (WRR) arbitration with 32 phases Bit 2 WRR arbitration with 64 phases Bit 3 WRR arbitration with 128 phases Bit 4 Time-based WRR with 128 phases Bit 5 WRR arbitration with 256 phases Bits 6-7 Reserved 	<u>RO</u>
14	Undefined - The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate Advanced Packet Switching. System software must ignore the value read from this bit.	<u>RO</u>
15	Reject Snoop Transactions - When Clear, transactions with or without the <u>No Snoop</u> bit Set within the TLP header are allowed on this VC. When Set, any transaction for which the <u>No Snoop</u> attribute is applicable but is not Set within the TLP header is permitted to be rejected as an Unsupported Request. Refer to Section 2.2.6.5 for information on where the <u>No Snoop</u> attribute is applicable. This bit is valid for Root Ports and RCRB; it is not valid for Endpoints or Switch Ports.	HwInit
22:16	Maximum Time Slots - Indicates the maximum number of time slots (minus one) that the VC resource is capable of supporting when it is configured for time-based WRR Port Arbitration. For example, a value 000 0000b in this field indicates the supported maximum number of time slots is 1 and a value of 111 1111b indicates the supported maximum number of time slots is 128. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. In addition, this field is valid only when the <u>Port Arbitration Capability</u> field indicates that the VC resource supports time-based WRR Port Arbitration.	HwInit

Bit Location	Register Description	Attributes
31:24	<p>Port Arbitration Table Offset - Indicates the location of the Port Arbitration Table associated with the VC resource. This field is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic.</p> <p>This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Extended Capability structure. A value of 00h indicates that the table is not present.</p>	RO

7.9.1.7 VC Resource Control Register

Figure 7-178 details allocation of register fields in the VC Resource Control Register; Table 7-144 provides the respective bit definitions.

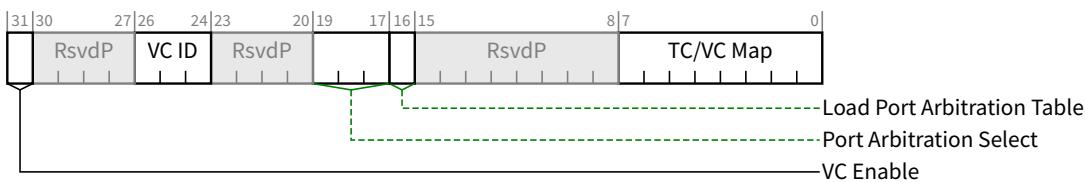


Figure 7-178 VC Resource Control Register

Table 7-144 VC Resource Control Register

Bit Location	Register Description	Attributes
7:0	<p>TC/VC Map - This field indicates the TCs that are mapped to the VC resource. This field is valid for all Functions.</p> <p>Bit locations within this field correspond to TC values. For example, when bit 7 is Set in this field, TC7 is mapped to this VC resource. When more than 1 bit in this field is Set, it indicates that multiple TCs are mapped to the VC resource.</p> <p>In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.</p> <p>Default value of this field is FFh for the first VC resource and is 00h for other VC resources.</p> <p>Note:</p> <p>Bit 0 of this field is read-only. It must be Set for the default VC0 and Clear for all other enabled VCs.</p>	RW (see the note for exceptions)
16	<p>Load Port Arbitration Table - When Set, this bit updates the Port Arbitration logic from the Port Arbitration Table for the VC resource. This bit is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. In addition, this bit is only valid when the Port Arbitration Table is used by the selected Port Arbitration scheme (that is indicated by a Set bit in the Port Arbitration Capability field selected by Port Arbitration Select).</p> <p>Software sets this bit to signal hardware to update Port Arbitration logic with new values stored in Port Arbitration Table; clearing this bit has no effect. Software uses the Port Arbitration Table Status bit to confirm whether the new values of Port Arbitration Table are completely latched by the arbitration logic.</p> <p>This bit always returns 0b when read.</p> <p>Default value of this bit is 0b.</p>	RW

Bit Location	Register Description	Attributes
19:17	<p>Port Arbitration Select - This field configures the VC resource to provide a particular Port Arbitration service. This field is valid for RCRBs, Root Ports that support peer-to-peer traffic, and Switch Ports, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic.</p> <p>The permissible value of this field is a number corresponding to one of the asserted bits in the <u>Port Arbitration Capability</u> field of the VC resource.</p>	<u>RW</u>
26:24	<p>VC ID - This field assigns a VC ID to the VC resource (see note for exceptions). This field is valid for all Functions.</p> <p>This field cannot be modified when the VC is already enabled.</p> <p>Note:</p> <p>For the first VC resource (default VC), this field is read-only and must be hardwired to 000b.</p>	<u>RW</u>
31	<p>VC Enable - This bit, when Set, enables a Virtual Channel (see note 1 for exceptions). The Virtual Channel is disabled when this bit is cleared. This bit is valid for all Functions.</p> <p>Software must use the <u>VC Negotiation Pending</u> bit to check whether the VC negotiation is complete.</p> <p>Default value of this bit is 1b for the first VC resource and is 0b for other VC resource(s).</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. This bit is hardwired to 1b for the default VC (VC0), i.e., writing to this bit has no effect for VC0. 2. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be Set in both components on a Link. 3. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both components on a Link. 4. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 5. Software must fully disable a Virtual Channel in both components on a Link before re-enabling the Virtual Channel. 	<u>RW</u>

7.9.1.8 VC Resource Status Register

Figure 7-179 details allocation of register fields in the VC Resource Status Register; Table 7-145 provides the respective bit definitions.

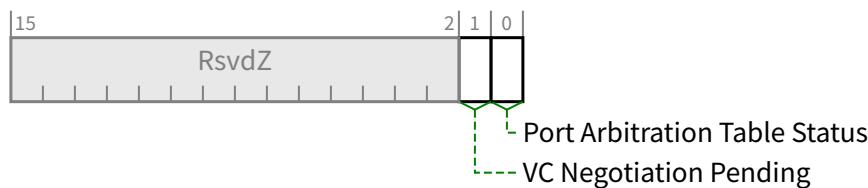


Figure 7-179 VC Resource Status Register

Table 7-145 VC Resource Status Register

Bit Location	Register Description	Attributes
0	<p>Port Arbitration Table Status - This bit indicates the coherency status of the <u>Port Arbitration Table</u> associated with the VC resource. This bit is valid for RCRBs, Root Ports that support peer-to-peer traffic, and Switch Ports, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. In addition, this bit is valid only when the <u>Port Arbitration Table</u> is used by the selected Port Arbitration for the VC resource.</p> <p>This bit is Set by hardware when any entry of the <u>Port Arbitration Table</u> is written to by software. This bit is Cleared by hardware when hardware finishes loading values stored in the <u>Port Arbitration Table</u> after software sets the Load Port Arbitration Table bit.</p> <p>Default value of this bit is 0b.</p>	<u>RO</u>
1	<p>VC Negotiation Pending -This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. This bit is valid for all Functions.</p> <p>The value of this bit is defined only when the Link is in the DL_Active state and the Virtual Channel is enabled (its <u>VC Enable</u> bit is Set).</p> <p>When this bit is Set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is Cleared by hardware after the VC negotiation is complete (on exit from the FC_INIT2 state). For VC0, this bit is permitted to be hardwired to 0b.</p> <p>Before using a Virtual Channel, software must check whether the <u>VC Negotiation Pending</u> bits for that Virtual Channel are Clear in both components on the Link.</p>	<u>RO</u>

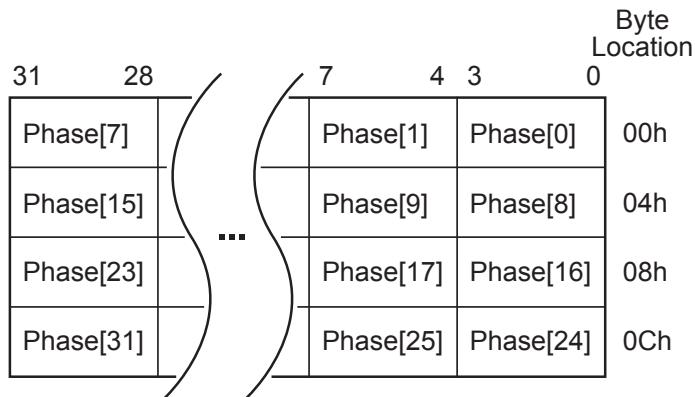
7.9.1.9 VC Arbitration Table

The VC Arbitration Table is a read-write register array that is used to store the arbitration table for VC Arbitration. This register array is valid for all Functions when the selected VC Arbitration uses a WRR table. Functions that do not support WRR VC arbitration are not required to implement a VC Arbitration Table. If it exists, the VC Arbitration Table is located by the VC Arbitration Table Offset field.

The VC Arbitration Table is a register array with fixed-size entries of 4 bits. Figure 7-180 depicts the table structure of an example VC Arbitration Table with 32 phases. Each 4-bit table entry corresponds to a phase within a WRR arbitration period. The definition of table entry is depicted in Table 7-146. The lower 3 bits (bits 0-2) contain the VC ID value, indicating that the corresponding phase within the WRR arbitration period is assigned to the Virtual Channel indicated by the VC ID (must be a valid VC ID that corresponds to an enabled VC).

The highest bit (bit 3) of the table entry is Reserved. The length of the table depends on the selected VC Arbitration as shown in Table 7-147.

When the VC Arbitration Table is used by the default VC Arbitration method, the default values of the table entries must be all zero to ensure forward progress for the default VC (with VC ID of 0).



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Figure 7-180 Example VC Arbitration Table with 32 Phases

Table 7-146 Definition of the 4-bit Entries in the VC Arbitration Table

Bit Location	Description	Attributes
2:0	VC ID	RW
3	RsvdP	RW

Table 7-147 Length of the VC Arbitration Table

VC Arbitration Select	VC Arbitration Table Length
001b	32 entries
010b	64 entries
011b	128 entries

7.9.1.10 Port Arbitration Table

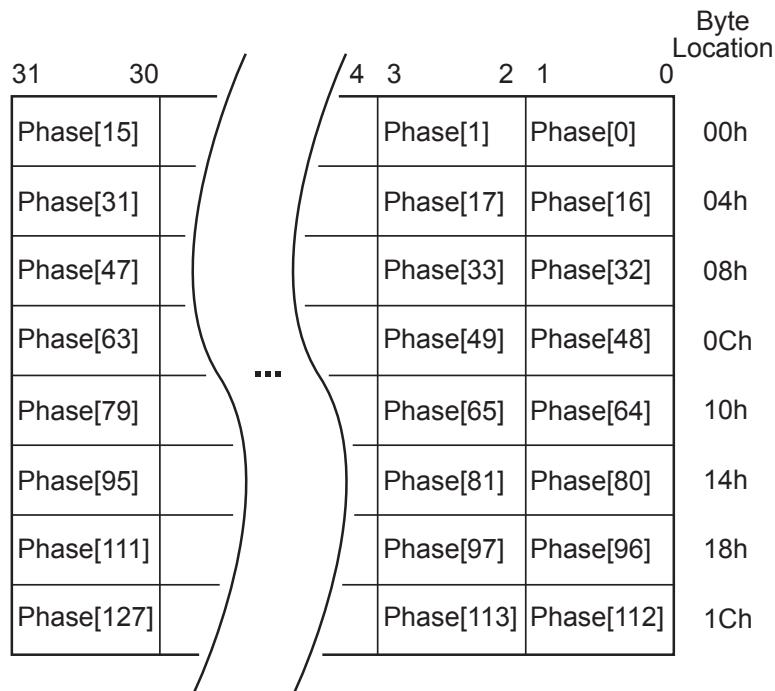
The Port Arbitration Table register is a read-write register array that is used to store the WRR or time-based WRR arbitration table for Port Arbitration for the VC resource. This register array is valid for all Switch Ports, Root Ports that support peer-to-peer traffic, and RCRBs, but is not valid for Endpoints or Root Ports that do not support peer-to-peer traffic. It is only present when one or more asserted bits in the Port Arbitration Capability field indicate that the component supports a Port Arbitration scheme that uses a programmable arbitration table. Furthermore, it is only valid when one of the above-mentioned bits in the Port Arbitration Capability field is selected by the Port Arbitration Select field.

The Port Arbitration Table represents one Port arbitration period. Figure 7-181 shows the structure of an example Port Arbitration Table with 128 phases and 2-bit table entries. Each table entry containing a Port Number corresponds to a phase within a Port arbitration period. For example, a table with 2-bit entries can be used by a Switch component with up to four Ports. A Port Number written to a table entry indicates that the phase within the Port Arbitration period is assigned to the selected PCI Express Port (the Port Number must be a valid one).

- When the WRR Port Arbitration is used for a VC of any Egress Port, at each arbitration phase, the Port Arbiter serves one transaction from the Ingress Port indicated by the Port Number of the current phase. When

finished, it immediately advances to the next phase. A phase is skipped, i.e., the Port Arbiter simply moves to the next phase immediately if the Ingress Port indicated by the phase does not contain any transaction for the VC (note that a phase cannot contain the Egress Port's Port Number).

- When the Time-based WRR Port Arbitration is used for a VC of any given Port, at each arbitration phase aligning to a virtual timeslot, the Port Arbiter serves one transaction from the Ingress Port indicated by the Port Number of the current phase. It advances to the next phase at the next virtual timeslot. A phase indicates an “idle” timeslot, i.e., the Port Arbiter does not serve any transaction during the phase, if:
 - the phase contains the Egress Port's Port Number, or
 - the Ingress Port indicated by the phase does not contain any transaction for the VC.
- The Port Arbitration Table Entry Size field in the Port VC Capability Register 1 determines the table entry size. The length of the table is determined by the Port Arbitration Select field as shown in Table 7-148.
- When the Port Arbitration Table is used by the default Port Arbitration for the default VC, the default values for the table entries must contain at least one entry for each of the other PCI Express Ports of the component to ensure forward progress for the default VC for each Port. The table may contain RR or RR-like fair Port Arbitration for the default VC.



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Figure 7-181 Example Port Arbitration Table with 128 Phases and 2-bit Table Entries

Table 7-148 Length of Port Arbitration Table

Port Arbitration Select	Port Arbitration Table Length
001b	32 entries
010b	64 entries
011b	128 entries