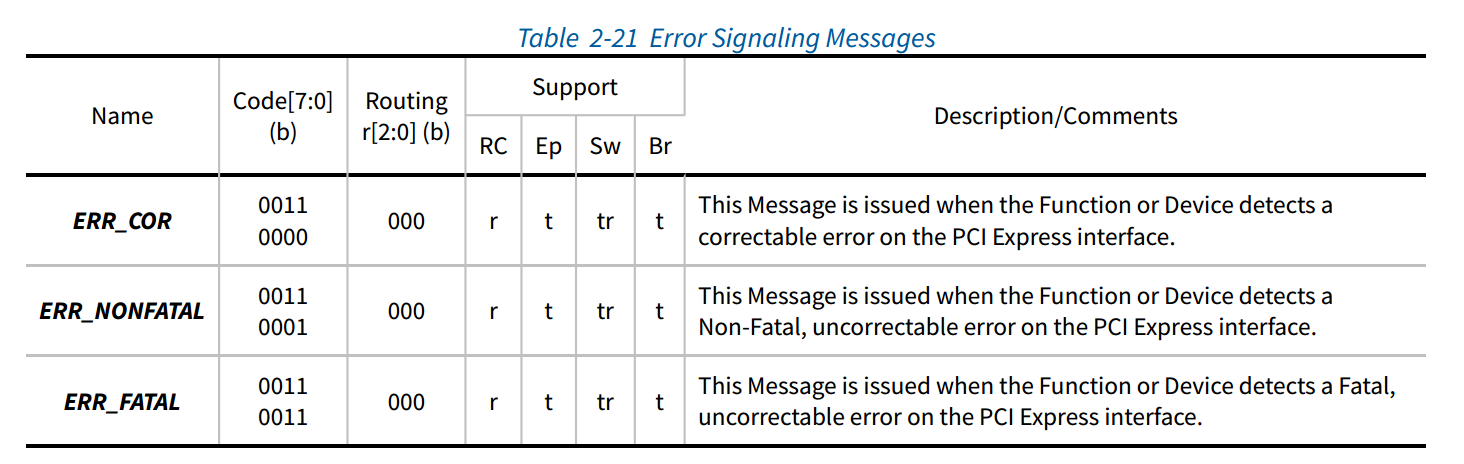
# DPC功能

Downstream Port Containment (DPC) is an optional normative feature of a Downstream Port. DPC halts PCI Express traffic below a Downstream Port after an unmasked uncorrectable error is detected at or below the Port, avoiding the potential spread of any data corruption, and supporting Containment Error Recovery (CER) if implemented by software. A Downstream Port indicates support for DPC by implementing a DPC Extended Capability structure, which contains all DPC control and status bits. See Section 7.9.15 .

下行端口遏制（DPC）是下行端口的可选规范功能。在下行端口或其下方检测到未屏蔽的不可纠正错误后，DPC会停止下行端口下方的PCI Express通信，避免任何数据损坏的潜在传播，并支持遏制错误恢复（CER）（如果由软件实现）。下行端口通过实现包含所有DPC控制和状态位的DPC扩展能力结构来指示对DPC的支持。参见第7.9.15节。

注：ERR\_COR message如下表所述。



DPC is disabled by default, and cannot be triggered unless enabled by software using the DPC Trigger Enable field. When the DPC Trigger Enable field is set to 01b, DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR\_FATAL Message. When the DPC Trigger Enable field is set to 10b, DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR\_NONFATAL or ERR\_FATAL Message. In addition to uncorrectable errors of the type managed by the PCI Express Extended Capability and Advanced Error Reporting (AER), RP PIO errors can be handled as uncorrectable errors. See Section 6.2.10.3 . There is also a mechanism described in Section 6.2.10.4 for software or firmware to trigger DPC.

默认情况下，DPC处于禁用状态，除非软件使用DPC触发器启用字段启用，否则无法触发。当DPC触发器启用字段设置为01b时，当下游端口检测到未屏蔽的不可纠正错误或当下游端口接收到ERR\_FATAL消息时，DPC被启用并被触发。当DPC触发器启用字段设置为10b时，当下游端口检测到未屏蔽的不可纠正错误或当下游端口接收到ERR\_NONFATAL或ERR\_FATAL消息时，DPC被启用并被触发。除了PCI Express扩展能力和高级错误报告（AER）管理的类型的不可纠正错误外，RP PIO错误也可以作为不可纠正的错误处理。参见第6.2.10.3节。第6.2.10.4节中还描述了软件或固件触发DPC的机制。

When DPC is triggered due to receipt of an uncorrectable error Message, the Requester ID from the Message is recorded in the DPC Error Source ID Register and that Message is discarded and not forwarded Upstream. When DPC is triggered by an unmasked uncorrectable error, that error will not be signaled with an uncorrectable error Message, even if otherwise enabled. However, when DPC is triggered, DPC can signal an interrupt or send an ERR\_COR Message if enabled. See Section 6.2.10.1 and Section 6.2.10.2 .

当由于接收到不可纠正的错误消息而触发DPC时，来自该消息的请求者ID被记录在DPC错误源ID寄存器中，并且该消息被丢弃并且不向上游转发。当DPC由未屏蔽的不可纠正错误触发时，即使以其他方式启用，也不会用不可纠正的错误消息来通知该错误。但是，当触发DPC时，如果启用，DPC可以发出中断信号或发送ERR\_COR消息。参见第6.2.10.1节和第6.2.10.2节。

When DPC is triggered, the Downstream Port immediately Sets the DPC Trigger Status bit and DPC Trigger Reason field to indicate the triggering condition (unmasked uncorrectable error, ERR\_NONFATAL, ERR\_FATAL, RP\_PIO error, or software triggered), and disables its Link by directing the LTSSM to the Disabled state. Once the LTSSM reaches the Disabled state,

it remains in that state until the DPC Trigger Status bit is Cleared. To ensure that the LTSSM has time to reach the Disabled state or at least to bring the Link down under a variety of error conditions, software must leave the Downstream Port in DPC until the Data Link Layer Link Active bit in the Link Status Register reads 0b; otherwise, the result is undefined. See Section 7.5.3.8 . See Section 2.9.3 for other important details on Transaction Layer behavior during DPC.

当DPC被触发时，下游端口立即设置DPC触发状态位和DPC触发原因字段以指示触发条件（未屏蔽的不可纠正错误、ERR\_NONFATAL、ERR\_FATAL、RP\_PIO错误或软件触发），并通过将LTSSM引导到Disabled状态来禁用其链路。一旦LTSSM达到禁用状态，它将保持该状态，直到DPC触发器状态位被清除。为了确保LTSSM有时间达到禁用状态或至少在各种错误条件下使链路停机，软件必须将下游端口留在DPC中，直到链路状态寄存器中的数据链路层链路活动位读取0b；否则，结果是未定义的。参见第7.5.3.8节。有关DPC期间事务层行为的其他重要细节，请参见第2.9.3节。

After DPC has been triggered in a Root Port that supports RP Extensions for DPC, the Root Port may require some time to quiesce and clean up its internal activities, such as those associated with DMA read Requests. When the DPC Trigger Status bit is Set and the DPC RP Busy bit is Set, software must leave the Root Port in DPC until the DPC RP Busy bit reads

0b.

在支持针对DPC的RP扩展的根端口中触发DPC之后，根端口可能需要一些时间来停止和清理其内部活动，例如与DMA读取请求相关联的活动。当DPC触发器状态位为Set，DPC RP Busy位为Set时，软件必须将根端口留在DPC中，直到DPC RP Busy位读取0b。

After software releases the Downstream Port from DPC, the Port’s LTSSM must transition to the Detect state, where the Link will attempt to retrain. Software can use Data Link Layer State Changed interrupts, DL\_Active ERR\_COR signaling, or both, to signal when the Link reaches the DL\_Active state again. See Section 6.7.3.3 and Section 6.2.10.5 .

软件从DPC释放下游端口后，端口的LTSSM必须转换到检测状态，链路将尝试重新训练。当链路再次达到DL\_Active状态时，软件可以使用数据链路层状态更改中断、DL\_ActiveERR\_COR信令或两者来发出信号。参见第6.7.3.3节和第6.2.10.5节。

## 6.2.10.1 DPC Interrupts

A DPC-capable Downstream Port must support the generation of DPC interrupts. DPC interrupts are enabled by the DPC Interrupt Enable bit in the DPC Control Register. DPC interrupts are indicated by the DPC Interrupt Status bit in the DPC Status Register.

具有DPC功能的下行端口必须支持生成DPC中断。DPC中断由DPC控制寄存器中的DPC中断启用位启用。DPC中断由DPC状态寄存器中的DPC中断状态位指示。

If the Port is enabled for level-triggered interrupt signaling using INTx messages, the virtual INTx wire must be asserted whenever and as long as the following conditions are satisfied:

如果使用INTx消息启用端口以进行电平触发中断信令，则只要满足以下条件，就必须断言虚拟INTx线：

• The value of the Interrupt Disable bit in the Command register is 0b.

• The value of the DPC Interrupt Enable bit is 1b.

• The value of the DPC Interrupt Status bit is 1b.

Note that all other interrupt sources within the same Function will assert the same virtual INTx wire when requesting service.

•命令寄存器中的中断禁用位的值为0b。

•DPC中断启用位的值为1b。

•DPC中断状态位的值为1b。

请注意，在请求服务时，同一Function内的所有其他中断源将断言相同的虚拟INTx线。

If the Port is enabled for edge-triggered interrupt signaling using MSI or MSI-X, an interrupt message must be sent every time the logical AND of the following conditions transitions from FALSE to TRUE:

如果端口使用MSI或MSI-X启用边缘触发中断信号，则每次下列条件的逻辑AND从FALSE转换为TRUE时，都必须发送中断消息：

• The associated vector is unmasked (not applicable if MSI does not support PVM).

• The value of the DPC Interrupt Enable bit is 1b.

• The value of the DPC Interrupt Status bit is 1b.

•相关矢量未屏蔽（如果MSI不支持PVM，则不适用）。

•DPC中断启用位的值为1b。

•DPC中断状态位的值为1b。

The Port may optionally send an interrupt message if interrupt generation has been disabled, and the logical AND of the above conditions is TRUE when interrupt generation is subsequently enabled.

The interrupt message will use the vector indicated by the DPC Interrupt Message Number field in the DPC Capability register. This vector may be the same or may be different from the vectors used by other interrupt sources within this Function.

如果中断生成已被禁用，则端口可以选择性地发送中断消息，并且当随后启用中断生成时，上述条件的逻辑and为TRUE。

中断消息将使用DPC能力寄存器中的DPC中断消息编号字段所指示的矢量。此矢量可能与此函数中其他中断源使用的矢量相同或不同。

## DPC ERR\_COR Signaling

A DPC-capable Downstream Port must support ERR\_COR signaling, independent of whether it supports Advanced Error Reporting (AER) or not. DPC ERR\_COR signaling is enabled by the DPC ERR\_COR Enable bit in the DPC Control Register. DPC triggering is indicated by the DPC Trigger Status bit in the DPC Status Register. DPC ERR\_COR signaling is managed independently of DPC interrupts, and it is permitted to use both mechanisms concurrently.

支持DPC的下行端口必须支持ERR\_COR信令，而与它是否支持高级错误报告（AER）无关。DPC ERR\_COR信令由DPC控制寄存器中的DPC ERR\_。DPC触发由DPC状态寄存器中的DPC触发器状态位指示。DPC ERR\_COR信令独立于DPC中断进行管理，并且允许同时使用这两种机制。

If the DPC ERR\_COR Enable bit is Set, and the Correctable Error Reporting Enable bit in the Device Control Register or the DPC SIG\_SFW Enable bit in the DPC Control Register is Set, the Port must send an ERR\_COR Message each time the DPC Trigger Status bit transitions from Clear to Set. DPC ERR\_COR signaling must not Set the Correctable Error Detected bit in the Device Status Register, since this event is not handled as an error. If the Downstream Port supports ERR\_COR Subclass capability, this DPC ERR\_COR signaling event must set the DPC SIG\_SFW Status bit in the DPC Status Register and also set the ERR\_COR Subclass field in the ERR\_COR Message to indicate ECS SIG\_SFW.

如果设置了DPC ERR\_COR启用位，并且设置了设备控制寄存器中的可纠正错误报告启用位或DPC控制寄存器中DPC SIG\_SFW启用位，则每当DPC触发器状态位从清除转换为设置时，端口必须发送ERR\_COR消息。DPC ERR\_COR信号不得在设备状态寄存器中设置Correctable Error Detected位，因为此事件不作为错误处理。如果下行端口支持ERR\_COR子类功能，则此DPC ERR\_COR信令事件必须在DPC状态寄存器中设置DPC SIG\_SFW状态位，并在ERR\_COR消息中设置ERR\_COR Subclass字段以指示ECS SIG\_SFW。

For a given DPC trigger event, if a Port is going to send both an ERR\_COR Message and an MSI/MSI-X transaction, then the Port must send the ERR\_COR Message prior to sending the MSI/MSI-X transaction. There is no corresponding requirement if the INTx mechanism is being used to signal DPC interrupts, since INTx Messages won’t necessarily remain ordered with respect to ERR\_COR Messages when passing through routing elements.

对于给定的DPC触发事件，如果端口将发送ERR\_COR消息和MSI/MSI-X事务，则该端口必须在发送MSI/MSIX事务之前发送ERR\_COR消息。如果INTx机制用于向DPC中断发送信号，则没有相应的要求，因为INTx消息在通过路由元件时不一定相对于ERR\_COR消息保持有序。

## Root Port Programmed I/O (RP PIO) Error Controls

The RP PIO error control registers enable fine-grained control over what happens when Non-Posted Requests that are tracked by the Root Port encounter certain uncorrectable or advisory errors. See Section 2.9.3 for a description of which Non-Posted Requests are tracked. A set of control and status bits exists for receiving Completion with Unsupported Request status (UR Cpl), receiving Completion with Completer Abort status (CA Cpl), and Completion Timeout (CTO) errors. Independent sets of these error bits exist for Configuration Requests, I/O Requests, and Memory Requests. This finer granularity enables more precise error handling for this subset of uncorrectable errors (UR Cpl, CA Cpl, and CTO). As a key example, UR Cpl errors with Memory Read Requests can be configured to trigger DPC for proper containment and error handling, while UR Cpl errors with Configuration Requests can be configured to return all 1’s (without trigging DPC) for normal probing and enumeration.

RP PIO错误控制寄存器能够对根端口跟踪的未发布请求遇到某些不可纠正或咨询错误时发生的情况进行细粒度控制。有关跟踪未投递请求的说明，请参见2.9.3节。存在一组控制和状态位，用于接收具有不支持的请求状态的完成（UR Cpl）、接收具有完成器中止状态的结束（CA Cpl）和完成超时（CTO）错误。对于配置请求、I/O请求和内存请求，存在这些错误位的独立集合。这种更精细的粒度能够对这一不可校正错误子集（UR Cpl、CA Cpl和CTO）进行更精确的错误处理。作为一个关键示例，内存读取请求的UR Cpl错误可以配置为触发DPC以进行正确的遏制和错误处理，而配置请求的UR Cpl错误可以设置为返回所有1（而不触发DPC）以进行正常探测和枚举。

A UR or CA error logged in AER is the result of the Root Port operating in the role of a Completer, and for a received Non-Posted Request, returning a Completion. In contrast, a UR Cpl or CA Cpl error logged as an RP PIO error is the result of the Root Port operating in the role of a Requester, and for an outstanding Non-Posted Request, receiving a Completion. CTO errors logged in both AER and RP PIO are the result of the Root Port operating in the role of a Requester, though the RP PIO error controls support per-space granularity. Depending upon the control register settings, CTO errors can be logged in AER registers, in RP PIO registers, or both. If software unmasks CTO errors in RP PIO, it is recommended that software mask CTO errors in AER in order to avoid unintended interactions.

AER中记录的UR或CA错误是根端口以完成者的身份运行的结果，对于收到的未发布请求，返回完成。相反，记录为RP PIO错误的UR Cpl或CA Cpl错误是根端口以请求者的身份运行的结果，对于未完成的未发布请求，接收完成。记录在AER和RP PIO中的CTO错误是根端口以请求者的身份运行的结果，尽管RP PIO错误控制了对每个空间粒度的支持。根据控制寄存器设置，CTO错误可以记录在AER寄存器、RP PIO寄存器或两者中。如果软件在RP PIO中屏蔽CTO错误，建议软件屏蔽AER中的CTO错误以避免意外交互。

The RP PIO Header Log Register, RP PIO ImpSpec Log Register, and RP PIO TLP Prefix Log Registers are referred to collectively as the RP PIO log registers. The RP PIO Header Log Register must be implemented; the RP PIO ImpSpec Log Register and RP PIO TLP Prefix Log Register are optional. The RP PIO Log Size field indicates how many DWORDs are allocated for the RP PIO log registers, and from this the allocated size for the RP PIO TLP Prefix Log Register can be calculated. See Section 7.9.15.2 . The RP PIO log registers always record information from a PIO Request, not any associated Completions.

RP PIO标头日志寄存器、RP PIO ImpSpec日志寄存器和RP PIO TLP前缀日志寄存器统称为RP PIO日志寄存器。必须实现RP PIO标头日志寄存器；RP PIO ImpSpec日志寄存器和RP PIO TLP前缀日志寄存器是可选的。RP PIO日志大小字段指示为RP PIO记录寄存器分配了多少DWORD，由此可以计算RP PIO TLP前缀记录寄存器的分配大小。参见第7.9.15.2节。RP PIO日志寄存器始终记录PIO请求中的信息，而不是任何相关的完成。

The RP PIO Status, Mask, and Severity registers behave similarly to the Uncorrectable Error Status, Mask, and Severity registers in AER. See Section 7.8.4.2 , Section 7.8.4.3 , and Section 7.8.4.4 >. When an RP PIO error is detected while it is unmasked, the associated bit in the RP PIO Status Register is Set, and the error is recorded in the RP PIO log registers (assuming that RP PIO error logging resources are available). When an RP PIO error is detected while it is masked, the associated bit is still Set in the RP PIO Status Register, but the error does not trigger DPC and the error is not recorded in the RP PIO log registers.

RP PIO状态、掩码和严重性寄存器的行为与AER中的不可更正错误状态、掩码及严重性寄存器类似。请参见第7.8.4.2节、第7.8.4.3节和第7.8.4.4>节。当RP PIO错误在未屏蔽时被检测到时，RP PIO状态寄存器中的相关位被设置，并且该错误被记录在RP PIO日志寄存器中（假设RP PIO故障日志资源可用）。当RP PIO错误被屏蔽时检测到时，相关的位仍在RP PIO状态寄存器中设置，但该错误不会触发DPC，并且该错误不会记录在RP PI奥日志寄存器中。

Each unmasked RP PIO error is handled either as uncorrectable or advisory, as determined by the value of the corresponding bit in the RP PIO Severity Register. If the associated Severity bit is Set, the error is handled as uncorrectable, triggering DPC (assuming that DPC is enabled) and signaling this event with a DPC interrupt and/or ERR\_COR (if enabled). If the associated Severity bit is Clear, the error is handled as advisory (without triggering DPC) and signaled with ERR\_COR (if enabled).根据RP PIO严重性寄存器中相应位的值，每个未屏蔽的RP PIO错误都被视为不可纠正或建议性错误处理。如果相关的Severity位为Set，则错误将被处理为不可纠正，触发DPC（假设DPC已启用），并用DPC中断和/或ERR\_COR（如果已启用）发信号通知此事件。如果相关的Severity位为Clear，则该错误将作为咨询处理（不触发DPC），并用ERR\_COR发出信号（如果启用）。

The RP PIO First Error Pointer, RP PIO Header Log, and RP PIO TLP Prefix Log behave similarly to the First Error Pointer, Header Log, and TLP Prefix Log in AER. The RP PIO First Error Pointer is defined to be valid when its value indicates a bit in the RP PIO Status Register that is Set. When the RP PIO First Error Pointer is valid, the RP PIO log registers contain the information associated with the indicated error. The RP PIO ImpSpec Log, if implemented, contains implementation-specific information, e.g., the source of the Request TLP.

RP PIO第一个错误指针、RP PIO标头日志和RP PIO TLP前缀日志的行为与AER中的第一个错误指示器、标头日志和TLP前缀记录类似。当RP PIO第一个错误指针的值指示RP PIO状态寄存器中的一个位被设置时，该指针被定义为有效。当RP PIO第一个错误指针有效时，RP PIO日志寄存器包含与指示错误相关的信息。RP PIO ImpSpec日志（如果实现）包含特定于实现的信息，例如请求TLP的源。

In contrast to AER, where the recording of CTO error information in the AER log registers is optional, RP PIO implementations must support recording RP PIO CTO error information in the RP PIO log registers.

与AER不同的是，在AER日志寄存器中记录CTO错误信息是可选的，RP PIO实现必须支持在RP PIO日志寄存器中录制RP PIO CTO错误消息。

If an error is detected with a received Completion TLP associated with an outstanding PIO Request, the set of RP PIO error control bits used to govern the error handling is determined in a similar manner. The DPC Completion Control bit determines whether UR or CA applies, and the Space (Configuration, I/O, or Memory) is that of the associated PIO Request. For example, if the DPC Completion Control bit is configured for CA, and a Root Port receives a poisoned Completion for a PIO Memory Read Request, the Mem CA Cpl bit (bit 17) is used in the RP PIO control and status registers for handling the error.

如果在接收到的与未完成PIO请求相关联的完成TLP中检测到错误，则以类似的方式确定用于管理错误处理的RP PIO错误控制位的集合。DPC完成控制位确定UR还是CA适用，并且空间（配置、I/O或内存）是相关联的PIO请求的空间。例如，如果为CA配置了DPC完成控制位，并且根端口接收到PIO内存读取请求的中毒完成，则在RP PIO控制和状态寄存器中使用Mem CA Cpl位（位17）来处理错误。

The RP PIO SysError Register provides a means to generate a System Error when an RP PIO error occurs. If an unmasked RP PIO error is detected while its associated bit in the RP PIO SysError Register is Set, a System Error is generated.

RP PIO系统错误寄存器提供了在发生RP PIO错误时生成系统错误的方法。如果在设置RP PIO系统错误寄存器中的相关位时检测到未屏蔽的RP PIO错误，则会生成系统错误。

The RP PIO Exception Register provides a means to generate a synchronous processor exception109 when an error occurs with certain tracked Non-Posted Requests that are generated by a processor instruction. See Section 2.9.3 . This exception must support all such tracked read Requests, and may optionally support Configuration write, I/O write, and AtomicOp Requests. If an error with an exception-supported Non-Posted Request is detected110 or a Completion for it is synthesized, and its associated bit in the RP PIO Exception Register is Set, the processor instruction that generated the Non-Posted Request must take a synchronous exception. This still applies even if the RP PIO or AER controls specify that the error be handled as masked or advisory.RP PIO异常寄存器提供了一种方法，用于在处理器指令生成的某些跟踪的未发布请求发生错误时生成同步处理器异常109。请参阅2.9.3节。此异常必须支持所有此类跟踪的读取请求，并且可以选择支持配置写入、I/O写入和AtomicOp请求。如果检测到异常支持的非Posted Request的错误110，或者对其进行了完成合成，并且RP PIO异常寄存器中的相关位为Set，则生成非Posted Request的处理器指令必须执行同步异常。即使RP PIO或AER控制规定将错误作为屏蔽或咨询处理，这仍然适用。

The details of a processor instruction taking a synchronous exception are processor-specific, but at a minimum, the mechanism must be able to interrupt the normal processor instruction flow either before completion of the instruction that generated the Non-Posted Request, or immediately following that instruction. The intent is that exception handling routines in system firmware, the operating system, or both, can examine the cause of the exception and take corrective action if necessary.

发生同步异常的处理器指令的细节是特定于处理器的，但至少，该机制必须能够在生成非Posted Request的指令完成之前或紧接在该指令之后中断正常的处理器指令流。其目的是，系统固件、操作系统或两者中的异常处理例程可以检查异常的原因，并在必要时采取纠正措施。

If an RP PIO error occurs with a processor-generated read or AtomicOp Request, and the RP PIO Exception Register value does not cause an exception, a value of all 1’s must be returned for the instruction that generated the Request.

如果处理器生成的读取或AtomicOp请求发生RP PIO错误，并且RP PIO异常寄存器值没有导致异常，则必须为生成请求的指令返回一个全部为1的值。

Root Port error handling for tracked Non-Posted Requests with errors other than receiving UR and CA Completions is governed by a combination of AER and RP PIO error controls. Examples are CTO 111 , Poisoned TLP Received, and Malformed TLP. For a given error managed by AER, the associated AER Mask and Severity bits determine if the error must be handled as an uncorrectable error, handled as an Advisory Non-Fatal Error, or handled as a masked error.

根端口错误处理由AER和RP PIO错误控制的组合控制，用于处理除接收UR和CA Completions以外有错误的跟踪未投递请求。例如CTO 111、接收的中毒TLP和格式错误的TLP。对于由AER管理的给定错误，相关的AER掩码和严重性位确定该错误是否必须作为不可纠正的错误处理、作为咨询非致命错误处理或作为掩码错误处理。

• If the AER-managed error is to be handled as an uncorrectable error (see Section 6.2.2.2 ), DPC is triggered. The RP PIO SysError and RP PIO Exception bits associated with the Request type and Completion Status apply.

• If the AER-managed error is to be handled as an Advisory Non-Fatal Error (see Section 6.2.3.2.4 ), DPC is not triggered. The RP PIO SysError and RP PIO Exception bits do apply.

• If the AER-managed error is to be handled as a masked error (see Section 6.2.3.2.2 ), DPC is not triggered. RP PIO SysError bit does not apply, but the RP PIO Exception bit does apply.

•如果AER管理的错误将作为不可纠正的错误处理（见第6.2.2.2节），则触发DPC。与请求类型和完成状态相关联的RP PIO SysError和RP PIO Exception位适用。

•如果AER管理的错误将作为咨询非致命错误处理（见第6.2.3.2.4节），则不会触发DPC。RP PIO系统错误和RP PIO异常位确实适用。

•如果将AER管理的错误作为屏蔽错误处理（见第6.2.3.2.2节），则不会触发DPC。RP PIO SysError位不适用，但RP PIO Exception位适用。

## Software Triggering of DPC

If the DPC Software Triggering Supported bit in the DPC Capability register is Set, then software can trigger DPC by writing a 1b to the DPC Software Trigger bit in the DPC Control Register, assuming that DPC is enabled and the Port isn’t currently in DPC. This mechanism is envisioned to be useful for software and/or firmware development and testing. It also supports usage models where software or firmware examines RP PIO Exceptions or RP PIO advisory errors, and decides to trigger DPC based upon the situation.

如果DPC能力寄存器中支持的DPC软件触发位为Set，则软件可以通过向DPC控制寄存器中的DPC软件触发位写入1b来触发DPC，假设DPC已启用并且端口当前不在DPC中。该机制被设想用于软件和/或固件开发和测试。它还支持软件或固件检查RP PIO异常或RP PIO咨询错误的使用模型，并根据情况决定触发DPC。

When this mechanism triggers DPC, the DPC Trigger Reason and DPC Trigger Reason Extension fields in the DPC Status Register will indicate this as the reason.

If a Port is already in DPC when a 1b is written to the DPC Software Trigger bit, the Port remains in DPC, and the DPC Trigger Reason and DPC Trigger Reason Extension fields are not modified.当该机制触发DPC时，DPC状态寄存器中的DPC触发原因和DPC触发理由扩展字段将指示这一原因。

当向DPC软件触发位写入1b时，如果端口已经在DPC中，则该端口保持在DPC内，并且不修改DPC触发原因和DPC触发理由扩展字段。

## DL\_Active ERR\_COR Signaling

Support for this feature is indicated by the DL\_Active ERR\_COR Signaling Supported bit in the DPC Capability register. The feature is enabled by the DL\_ACTIVE ERR\_COR Enable bit in the DPC Control Register. The DL\_ACTIVE state is indicated by the Data Link Layer Link Active bit in the Link Status Register. DL\_ACTIVE ERR\_COR signaling is managed independently of Data Link Layer State Changed interrupts, and it is permitted to use both mechanisms concurrently.

对该功能的支持由DPC能力寄存器中的DL\_Active ERR\_COR Signaling Supported位表示。该功能由DPC控制寄存器中的DL\_ACTIVE ERR\_COR Enable位启用。DL\_ACTIVE状态由链路状态寄存器中的数据链路层链路活动位指示。DL\_ACTIVE ERR\_COR信令独立于数据链路层状态更改中断进行管理，并且允许同时使用这两种机制。

If the DL\_ACTIVE ERR\_COR Enable bit is Set, and the Correctable Error Reporting Enable bit in the Device Control register or the DPC SIG\_SFW Enable bit in the DPC Control Register is Set, the Port must send an ERR\_COR Message each time the Link transitions into the DL\_ACTIVE state. DL\_ACTIVE ERR\_COR signaling must not Set the Correctable Error Detected bit in the Device Status register, since this event is not handled as an error. If the Downstream Port supports ERR\_COR Subclass capability, this DPC ERR\_COR signaling event must set the DPC SIG\_SFW Status bit in the DPC Status register and also set the ERR\_COR Subclass field in the ERR\_COR Message to indicate ECS SIG\_SFW. In contrast to Data Link Layer State Changed interrupts, DL\_Active ERR\_COR signaling only indicates the Link enters the DL\_Active state, not when the Link exits the DL\_Active state.

如果DL\_ACTIVE ERR\_COR使能位设置，并且设备控制寄存器中的可纠正错误报告使能位或DPC控制寄存器中DPC SIG\_SFW使能位被设置，则每当链路转换到DL\_ACTIVE状态时，端口必须发送一条ERR\_COR消息。DL\_ACTIVE ERR\_COR信号不得设置设备状态寄存器中的Correctable Error Detected位，因为此事件不会作为错误处理。如果下行端口支持ERR\_COR子类功能，则此DPC ERR\_COR信令事件必须在DPC状态寄存器中设置DPC SIG\_SFW状态位，并在ERR\_COR消息中设置ERR\_COR Subclass字段以指示ECS SIG\_SFW。与数据链路层状态更改中断相反，DL\_Active ERR\_COR信令仅指示链路进入DL\_Actives状态，而不是当链路退出DL\_Activity状态时。

For a given DL\_ACTIVE event, if a Port is going to send both an ERR\_COR Message and an MSI/MSI-X transaction, then the Port must send the ERR\_COR Message prior to sending the MSI/MSI-X transaction. There is no corresponding requirement if the INTx mechanism is being used to signal DL\_ACTIVE interrupts, since INTx Messages won’t necessarily remain ordered with respect to ERR\_COR Messages when passing through routing elements.

对于给定的DL\_ACTIVE事件，如果端口将发送ERR\_COR消息和MSI/MSI-X事务，则该端口必须在发送MSI/MSIX事务之前发送ERR\_COR消息。如果INTx机制用于发出DL\_ACTIVE中断的信号，则没有相应的要求，因为INTx消息在通过路由元件时不一定相对于ERR\_COR消息保持有序。