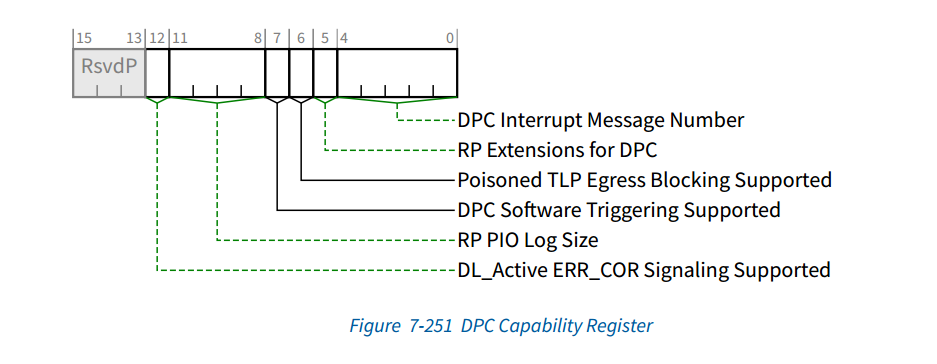
# DPC功能

DPC则是一种用于处理PCIe链路中错误情况的机制。当PCIe链路上的一个设备发送错误信号时，DPC机制允许系统采取相应的措施来隔离故障设备，以限制错误的传播范围（当本端口接收到本机或下游的uncorrect error时，依据相关配置会触发DPC事件，然后阻塞下游端口到本端口的报文、阻塞本端口接收的转发报文、使能本端口ltssm状态机直接跳转到disable状态，并根据配置上报ERR\_COR message或中断），确保其他设备继续正常工作。DPC机制依赖于AER提供的错误信息来进行错误处理。

所以，AER用于检测和报告PCIe设备的错误，而DPC用于处理错误情况并限制错误的传播范围，两者共同为PCIe系统提供了强大的错误处理和容错功能。

虽然AER和DPC在某种程度上可以协同工作，但它们是独立的机制，并不是逻辑上的包含关系。AER提供了错误的检测和报告，而DPC则是根据这些错误信息来采取相应的隔离措施，以维护系统的稳定性和可靠性。

## DPC Capability Register



### DPC Interrupt Message Number（已实现，RO）

This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with the DPC Capability structure.

For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the Message Control Register for MSI.

该字段指示哪个MSI/MSI-X矢量用于与DPC能力结构相关联地生成的中断消息。

对于MSI，此字段中的值表示基本消息数据和生成的中断消息之间的偏移量。硬件需要更新此字段，以便在软件写入MSI的消息控制寄存器中的多消息启用字段时，如果分配给功能的MSI消息数发生更改，则该字段是正确的。

For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry must be one of the first 32 entries even if the Function implements more than 32 entries. For a given MSI-X implementation, the entry must remain constant.

If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field must indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field must indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined.

对于MSI-X，该字段中的值指示哪个MSI-X表条目用于生成中断消息。即使函数实现了超过32个条目，该条目也必须是前32个条目中的一个。对于给定的MSI-X实现，条目必须保持不变。

如果同时实现MSI和MSI-X，则允许它们使用不同的矢量，尽管软件一次只能启用一种机制。如果启用了MSI-X，则此字段中的值必须指示MSI-X的矢量。如果MSI已启用或两者都未启用，则此字段中的值必须指示MSI的矢量。如果软件同时启用MSI和MSI-X，则此字段中的值未定义。

225已实现，具体在配置空间intreg模块中提取k\_pexconf[`KPEXCONF\_DPC\_MSINUM+:5]作为msi的数据的低五位

### RP Extensions for DPC（已实现，RO）

If Set, this bit indicates that a Root Port supports a defined set of DPC Extensions that are specific to Root Ports. Switch Downstream Ports must not Set this bit.

225已实现，具体在配置空间errmgt模块中的k\_rpio实现，由于是RP功能，实际功能有但未启用。

### Poisoned TLP Egress Blocking Supported（已实现，RO）

Poisoned TLP Egress Blocking Supported - If Set, this bit indicates that the Root Port or Switch

Downstream Port supports the ability to block the transmission of a poisoned TLP from its Egress Port.

Root Ports that support RP Extensions for DPC must Set this bit

如果设置，此位表示根端口或交换机下游端口支持阻止从其出口端口传输中毒TLP的能力。

支持DPC RP扩展的根端口必须设置此位。

225已实现，具体在hsio\_decoder\_up/dn中的dpc\_eg\_blck实现，注：上游端口dpc\_eg\_blck为0；

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **分类** | **子类** | **情况** | **Device** | **数据输出** | **备注** |
| FMT\_TYPE\_MWR64  FMT\_TYPE\_MRD64  FMT\_TYPE\_ATO64 | 广播 | dpc\_eg\_blck | DISCARD | —— | 广播，丢弃 |
| eg\_blck | (|(fmt\_type\_64\_good  & dpc\_eg\_blck)  & tl\_rx\_poisoned)|| |(fmt\_type\_64\_good  & dpc\_actived) | DN\_UR\_CA | cpl\_dpc | 对MRD64，丢弃并回复CPL |
| DISCARD | —— | 其他类型，丢弃 |
| FMT\_TYPE\_MWR32  FMT\_TYPE\_MRD32  FMT\_TYPE\_ATO32 | 广播 | dpc\_eg\_blck | DISCARD | —— | 丢弃 |
| eg\_blck | (|(fmt\_type\_32\_good  & dpc\_eg\_blck)  & tl\_rx\_poisoned)|| |(fmt\_type\_32\_good  & dpc\_actived) | DN\_UR\_CA | cpl\_dpc | 对MRD32，丢弃并回复CPL |
| DISCARD | —— | 其他类型，丢弃 |
| ~tl\_rx\_unexp\_cpl | (|{fmt\_type\_cpl\_good  & dpc\_eg\_blck)  & tl\_rx\_poisoned)|| |(fmt\_type\_cpl\_good  & dpc\_actived) | DISCARD | —— | 丢弃 |
| acs\_u\_en  & fmt\_type\_cpl\_good | UPSTREAM | tl\_rx\_data | 转发至RC |
| acs\_c\_en  & ~tl\_rx\_relaxed\_o | UPSTREAM | tl\_rx\_data | 转发至RC |
| 其他情况 | fmt\_type\_cpl\_good | tl\_rx\_data | 转发 |
| FMT\_TYPE\_IORD  FMT\_TYPE\_IOWR | fmt\_type\_io\_good  & dpc\_eg\_blck  & tl\_rx\_poisoned | dpc\_activated | DN\_UR\_CA | cpl\_dpc | 丢弃并回复CPL |
| ~dpc\_activated | DISCARD | —— | 丢弃 |
| fmt\_type\_io\_good | fmt\_type\_io\_good | tl\_rx\_data | 转发 |
| FMT\_TYPE\_MESD\_RRC  FMT\_TYPE\_MES\_RRC  FMT\_TYPE\_MESD\_GRRC  FMT\_TYPE\_MES\_GRRC | —— | —— | UPSTREAM | tl\_rx\_data | 转发 |
| FMT\_TYPE\_MESD\_ID  FMT\_TYPE\_MES\_ID | |fmt\_type\_mes\_  id\_good | (|(fmt\_type\_mes\_id\_good& dpc\_eg\_blck)  & tl\_rx\_poisoned)|| |(fmt\_type\_mes\_id\_good  & dpc\_actived) | DISCARD | —— | 丢弃 |
| FMT\_TYPE\_MES\_ILTR | —— | —— | DISCARD | —— | 丢弃 |
| FMT\_TYPE\_MESD\_ILTR | —— | —— | DISCARD | —— | 丢弃 |
| 其他类型 | —— | —— | UPSTREAM | tl\_rx\_data | 转发 |

### DPC Software Triggering Supported（已实现，RO）

DPC Software Triggering Supported - If Set, this bit indicates that a Root Port or Switch Downstream Port supports the ability for software to trigger DPC. Root Ports that support RP Extensions for DPC must Set this bit.如果设置，此位表示根端口或交换机下游端口支持软件触发DPC的能力。支持DPC RP扩展的根端口必须设置此位。

225已实现，具体在配置空间errmgt模块中的k\_pexconf[`KPEXCONF\_DPC\_SOFT\_TRIG\_SUP]，当配置为0时，DPC Software Trigger强制为0。

### RP PIO Log Size -（已实现，RO）

This field indicates how many DWORDs are allocated for the RP PIO log registers,

comprised by the RP PIO Header Log, the RP PIO ImpSpec Log, and RP PIO TLP Prefix Log. If the Root Port supports RP Extensions for DPC, the value of this field must be 4 or greater; otherwise, the value of this field must be 0. See Section 7.9.15.11 , Section 7.9.15.12 , and Section 7.9.15.13 .

225已实现，具体在配置空间errmgt模块中的rpio\_log\_size实现，由于是RP功能，实际功能有但未启用

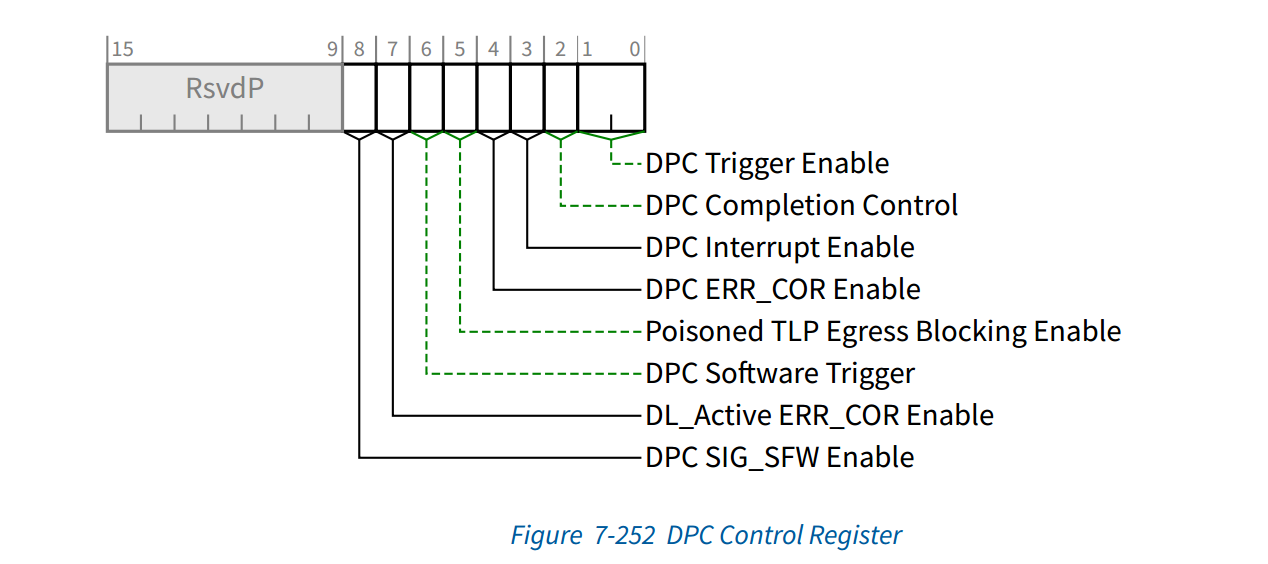
### DL\_Active ERR\_COR Signaling Supported（1bit，RO）

DL\_Active ERR\_COR Signaling Supported - If Set, this bit indicates that the Root Port or Switch Downstream Port supports the ability to signal with ERR\_COR when the Link transitions to the DL\_Active state. Root Ports that support RP Extensions for DPC must Set this bit.

如果设置，此位表示根端口或交换机下游端口支持在链路转换到DL\_Active状态时用ERR\_COR发出信号的能力。支持DPC RP扩展的根端口必须设置此位。

225已实现，具体在配置空间errmgt模块；当配置值k\_pexconf[`KPECONF\_DPC\_DL\_ACT\_ERR\_COR] （对应该DL\_Active ERR\_COR Signaling Supported比特位）为0时，DPC Control Register 中的DL\_Active ERR\_COR Enable位(dpc\_dl\_active\_err\_cor\_en)为0。

## DPC Control Register



### DPC Trigger Enable（已实现,RW）

This field enables DPC and controls the conditions that cause DPC to be triggered. Defined encodings are:

00，DPC is disabled

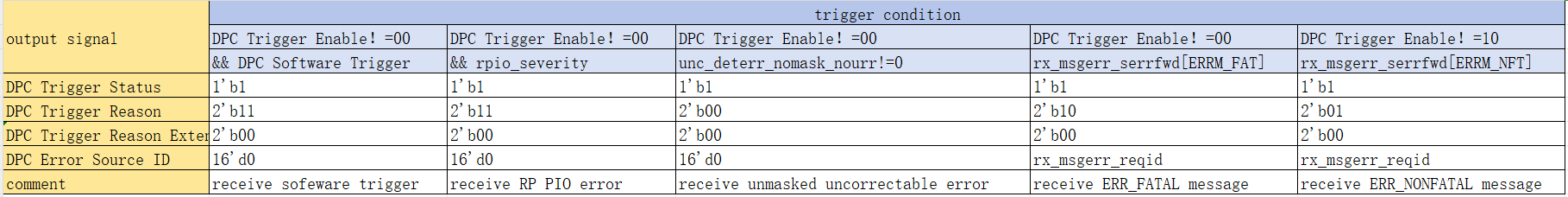
01，DPC is enabled and is triggered when the Downstream Port detects an unmasked uncorrectable error or when the Downstream Port receives an ERR\_FATAL Message

10，DPC is enabled and is triggered when the Downstream Port detects an unmasked

uncorrectable error or when the Downstream Port receives an ERR\_NONFATAL or

ERR\_FATAL Message

11，Reserved225已实现，具体在配置空间errmgt模块中；通过dpc\_trig\_en与触发条件同时判断产生dpc\_trig\_status，即触发DPC事件。



注： rx\_msgerr\_reqid为接收message中的requester id;

### DPC Completion Control（已实现,RW）

DPC Completion Control - This bit controls the Completion Status for Completions formed during DPC. See Section 2.9.3 .

Defined encodings are:

0 ，Completer Abort (CA) Completion Status

1 ，Unsupported Request (UR) Completion Status

Default value of this bit is 0b.

225已实现，具体在decoder模块中；根据|(fmt\_type\_64\_good&dpc\_eg\_blck)&tl\_rx\_poisoned或|(fmt\_type\_64\_good&dpc\_activated)条件,产生相应的cpl\_dpc，其中cpl字段Cpl. Status根据dpc\_cpl\_crtl进行选择CA/UR

### DPC Interrupt Enable（已实现,RW）

When Set, this bit enables the generation of an interrupt to indicate that DPC has been triggered. See Section 6.2.10.1 .

Default value of this bit is 0b.

225已实现，具体在配置空间errmgt模块中；当DPC Interrupt Enable （dpc\_int\_en）为1时，若 dpc\_trig\_status为1，则dpc\_int\_status置1。

### DPC ERR\_COR Enable（已实现,RW）

When Set, this bit enables the sending of an ERR\_COR Message to indicate that

DPC has been triggered. See Section 6.2.10.2 .

Default value of this bit is 0b.

225已实现，具体在配置空间errmgt模块中；当DPC ERR\_COR Enable （dpc\_err\_cor\_en）为1时，若dpc\_trig\_status上升沿或RP PIO uncorrectable error下，发送 ERR\_COR message；

### Poisoned TLP Egress Blocking Enable（已实现, RW/RO）

This bit must be RW if the Poisoned TLP Egress Blocking

Supported bit is Set; otherwise, it is permitted to be hardwired to 0b. Software must not Set this bit unless the Poisoned TLP Egress Blocking Supported bit is Set.

When Set, this bit enables the associated Egress Port to block the transmission of poisoned TLPs. See Section 2.7.2.2 .

Default value of this bit is 0b.

225已实现，具体在decoder模块中；若Poisoned TLP Egress Blocking Supported为0，则强制为0；否则根据输入报文EP字段（tl\_rx\_poisoned）是否为1，且Poisoned TLP Egress Blocking Enable（dpc\_eg\_blck）同时为1，则对报文进行阻塞，并响应CA/UR；

### DPC Software Trigger（已实现,RW/RO）

This bit must be RW if the DPC Software Triggering Supported bit is Set;

otherwise, it is permitted to be hardwired to 0b.

If DPC is enabled and the DPC Trigger Status bit is Clear, when software writes 1b to this bit, DPC is triggered. Otherwise, software writing a 1b to this bit has no effect.

It is permitted to write 1b to this bit while simultaneously writing updated values to other fields in this register, notably the DPC Trigger Enable field. For this case, the DPC Software Trigger semantics are based on the updated value of the DPC Trigger Enable field.

This bit always returns 0b when read.

225已实现，具体在配置空间errmgt模块中dpc\_soft\_trig实现，用于触发dpc\_trig\_status。在decoder模块中作为dpc\_activated，当dpc\_activated || （dpc\_eg\_blck & tl\_rx\_posioned）为1时，对输入报文进行阻塞。若DPC Software Triggering Supported为0，则强制为0，否则使用配置值。

### DL\_Active ERR\_COR Enable（已实现,RW/RO）

This bit must be RW if the DL\_Active ERR\_COR Signaling Supported bit is Set; otherwise, it is permitted to be hardwired to 0b. Software must not Set this bit unless the DL\_Active ERR\_COR Signaling Supported bit is Set.

When Set, this bit enables the associated Downstream Port to signal with ERR\_COR when the Link transitions to the DL\_Active state. See Section 6.2.10.5 .

Default value of this bit is 0b.

225已实现，具体在配置空间errmgt模块中，若DL\_Active ERR\_COR Signaling Supported配置为0，则强制为0，否则使用配置值。DL\_Active ERR\_COR Enable（dpc\_dl\_active\_err\_cor\_en）为1、dl\_active\_r=0、shb\_dl\_active=1（on rising edge of shb\_dl\_active,shb\_dl\_active is dlcmsm\_act，indicate dlcms状态机进入DLCM\_DL\_ACTIVE状态即fcinit\_done）时，dpc\_send\_err\_cor为1，则send ERR\_COR message。

### DPC SIG\_SFW Enable（未实现,RW/RO）

This bit must be implemented if the ERR\_COR Subclass Capable bit in the Device Capabilities Register is Set; otherwise, it is permitted to be hardwired to 0b. If the ERR\_COR Subclass Capable bit is Clear and software Sets this bit, the behavior is undefined.

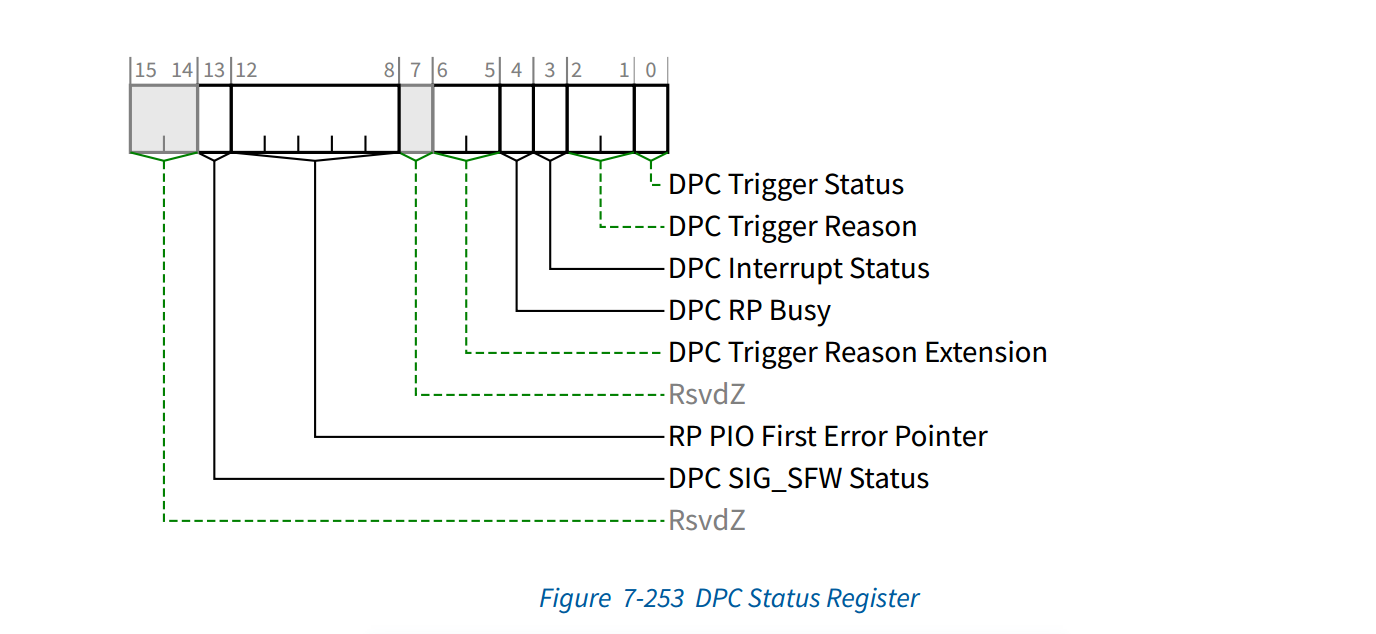
When Set, this bit enables sending an ERR\_COR Message to indicate a DPC event that’s been enabled for ERR\_COR signaling. See Section 6.2.10.2 and Section 6.2.10.5 . This is an additional and alternative way to enable overall DPC ERR\_COR signaling beyond the Correctable Error Reporting Enable bit in the Device Control Register. This bit does not affect a Function’s ability to send ERR\_COR Messages other than the ECS SIG\_SFW subclass.

Default value of this bit is 0b.

If the DL\_ACTIVE ERR\_COR Enable bit is Set, and the Correctable Error Reporting Enable bit in the Device Control register or the DPC SIG\_SFW Enable bit in the DPC Control Register is Set, the Port must send an ERR\_COR Message each time the Link transitions into the DL\_ACTIVE state. DL\_ACTIVE ERR\_COR signaling must not Set the Correctable Error Detected bit in the Device Status register, since this event is not handled as an error. If the Downstream Port supports ERR\_COR Subclass capability, this DPC ERR\_COR signaling event must set the DPC SIG\_SFW Status bit in the DPC Status register and also set the ERR\_COR Subclass field in the ERR\_COR Message to indicate ECS SIG\_SFW. In contrast to Data Link Layer State Changed interrupts, DL\_Active ERR\_COR signaling only indicates the Link enters the DL\_Active state, not when the Link exits the DL\_Active state.

未实现，具体在配置空间errmgt模块中，目前使用的是Correctable Error Reporting Enable bit in the Device Control Register(tl\_pex\_enable[`PEXEN\_REP\_CORERR\_EN])

## DPC Status Register



### DPC Trigger Status（已实现,RW1CS）

When Set, this bit indicates that DPC has been triggered, and by definition the Port is “in DPC”. DPC is event triggered.

While this bit is Set, hardware must direct the LTSSM to the Disabled State. This bit must be cleared before the LTSSM can be released from the Disabled State, after which the Port is no longer in DPC, and the LTSSM must transition to the Detect State. See Section 6.2.10 for requirements on how long software must leave the Downstream Port in DPC. Once these requirements are met, software is permitted to clear this bit regardless of the state of other status bits associated with the triggering event.

After clearing this bit, software must honor timing requirements defined in Section 6.6.1 with

respect to the first Configuration Read following a Conventional Reset.

Default value of this bit is 0b.

225已实现，具体在配置空间errmgt模块中dpc\_trig\_status，有效时即DPC事件触发；若配置报文写寄存器1，则对寄存器清零，详见上述1.2.1章节DPC Trigger Status。模块输出dpc\_trig\_status到ltssm作为状态机直接跳转到disable state信号。模块输出dpc\_trig\_status到decoder模块作为dpc\_activated信号进行报文阻塞。

### DPC Trigger Reason（已实现,ROS）

This field indicates why DPC has been triggered. Defined encodings are:

00, DPC was triggered due to an unmasked uncorrectable error

01, DPC was triggered due to receiving an ERR\_NONFATAL

10, DPC was triggered due to receiving an ERR\_FATAL

11, DPC was triggered due to a reason that is indicated by the DPC Trigger Reason Extension field.

This field is valid only when the DPC Trigger Status bit is Set; otherwise the value of this field is undefined.225已实现，具体在配置空间errmgt模块中dpc\_trig\_reason，详见上述1.2.1章节DPC Trigger Reason。

### DPC Interrupt Status（已实现, RW1CS）

This bit is Set if DPC is triggered while the DPC Interrupt Enable bit is Set.

This may cause the generation of an interrupt. See Section 6.2.10.1 .

Default value of this bit is 0b

225已实现，具体在配置空间errmgt模块中，若配置报文写寄存器1，则优先对寄存器清零，否则使用本地逻辑寄存器值。当dpc\_int\_en和dpc\_trig\_status均为1时，DPC Interrupt Status（dpc\_int\_status）置1，并将dpc\_int\_status输出给intreg模块生成中断。

### DPC RP Busy（未实现, RO/RsvdZ）

When the DPC Trigger Status bit is Set and this bit is Set, the Root Port is busy with internal activity that must complete before software is permitted to Clear the DPC Trigger Status bit.

If software Clears the DPC Trigger Status bit while this bit is Set, the behavior is undefined.

This field is valid only when the DPC Trigger Status bit is Set; otherwise the value of this field is undefined.

This bit is applicable only for Root Ports that support RP Extensions for DPC, and is Reserved for Switch Downstream Ports.

Default value of this bit is undefined.

未实现，具体在配置空间errmgt模块中，tl\_report\_state[`PFSTATE\_DPC\_RP\_BUSY]外部输入为0。

### DPC Trigger Reason Extension（已实现, ROS）

This field serves as an extension to the DPC Trigger Reason field.

When that field is valid and has a value of 11b, this field indicates why DPC has been triggered.

Defined encodings are:

00, DPC was triggered due to an RP PIO error

01, DPC was triggered due to the DPC Software Trigger bit

10, Reserved

11, Reserved

This field is valid only when the DPC Trigger Status bit is Set and the value of the DPC Trigger Reason field is 11b; otherwise the value of this field is undefined.

225已实现，具体在配置空间errmgt模块中dpc\_trig\_reason\_ext，详见上述1.2.1章节DPC Trigger Reason Extension。

### RP PIO First Error Pointer（未实现 ROS/RsvdZ）

The value of this field identifies a bit position in the RP PIO Status Register, and this field is considered valid when that bit is Set. When this field is valid, and software writes a 1b to the indicated RP PIO Status bit (thus clearing it), this field must revert to its default value.

This field is applicable only for Root Ports that support RP Extensions for DPC, and otherwise is Reserved.

If this field is not Reserved, its default value is 11111b, indicating a permanently Reserved RP PIO Status bit, thus guaranteeing that this field is not considered valid.

### DPC SIG\_SFW Status（未实现, RW1CS/RsvdZ）

If the Function supports ERR\_COR Subclass capability, this bit must be implemented; otherwise, it must be hardwired to 0b. If implemented, this bit is Set when a SIG\_SFW ERR\_COR Message is sent to signal a DPC event. See Section 6.2.10.2 and Section 6.2.10.5 .

Default value of this bit is 0b225未实现，固定为0；

## DPC Error Source ID Register

### DPC Error Source ID（已实现, ROS）

When the DPC Trigger Reason field indicates that DPC was triggered due to the reception of an ERR\_NONFATAL or ERR\_FATAL, this register contains the Requester ID of the received Message. Otherwise, the value of this register is undefined.

225已实现，具体在配置空间errmgt模块中dpc\_err\_source\_id，详见上述1.2.1章节DPC Error Source ID。