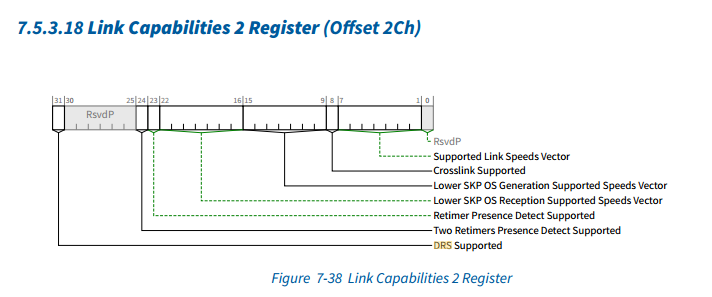
# PCI Express Capability

## Link Capabilities 2 Register (Offset 2Ch)



### DRS Supported（未实现）

When Set, indicates support for the optional Device Readiness Status (DRS) capability.

Must be Set in Downstream Ports that support DRS.

Must be Set in Downstream Ports that support FRS.

For Upstream Ports that support DRS, it is strongly recommended that this bit be Set in Function 0.

For all other Functions associated with an Upstream Port, this bit must be Clear.

Must be Clear in Functions that are not associated with a Port. RsvdP in all other Functions.

该字段设置时，表示支持可选的设备就绪状态（DRS）功能。

必须在支持DRS的下游端口中设置。

必须在支持FRS的下游端口中设置。

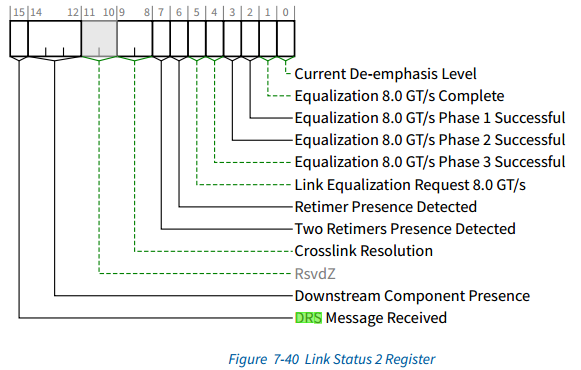
对于支持DRS的上行端口，强烈建议在功能0中设置此位。

对于与上游端口相关的所有其他功能，此位必须为Clear（清除）。

在与端口无关的Function中必须清除。所有其他Function中的RsvdP。

225未实现，该DRS Supported字段表示是否支持设备就绪状态DRS能力， 在pcie5\_pexreg模块中该字段是直接赋值为0，并没有进行配置实现。另外225相关设计模块没有看到有关DRS的设计实现内容，只有在decoder\_up模块中看到声明了与DRS消息报文的message code有关的参数，但是该参数并没有在decoder模块中所使用到。

## Link Status 2 Register (Offset 32h)



### DRS Message Received（未实现）

This bit must be Set whenever the Port receives a DRS Message.

This bit must be Cleared in DL\_Down.

This bit must be implemented in any Downstream Port where the DRS Supported bit is Set in the Link Capabilities 2 Register

This bit is RsvdZ for all other Functions. Default value of this bit is 0b.

每当端口接收到DRS消息时，必须设置此位。

当处于DL\_Down状态时，此位必须清除。

该比特必须在Link Capabilities 2 Register中设置DRS Supported位的任何下行端口中实现。

对于所有其他Function，此位为RsvdZ。此位的默认值为0b

225未实现，该DRS Message Received字段表示当前下行端口是否接收到DRS message报文，在pcie5\_pexreg模块中该寄存器的DRS Message Received字段是直接赋值为0的，并没有进行配置使用。

### Downstream Component Presence（未实现）

This field indicates the presence and DRS status for the Downstream Component, if any, connected to the Link; defined values are:

000b：Link Down - Presence Not Determined

001b：Link Down - Component Not Present indicates the Downstream Port (DP) has determined that a Downstream Component is not present

010b：Link Down - Component Present indicates the DP has determined that a Downstream Component is present, but the Data Link Layer is not active

011b：Reserved

100b：Link Up - Component Present indicates the DP has determined that a Downstream Component is present, but no DRS Message has been received since the Data Link Layer became active.

101b：Link Up - Component Present and DRS Received indicates the DP has received a DRS Message since the Data Link Layer became active

110b：Reserved

111b：Reserved

Downstream Component Presence state must be determined by the logical “OR” of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism implemented for the Link. If no out-of-band presence detect mechanism is implemented, then Downstream Component Presence state must be determined solely by the Physical Layer in-band presence detect mechanism

If the In-Band PD Disable bit in the Slot Control Register is Set, the Physical Layer in-band presence detect mechanism must always indicate that no component is present.

Component Presence, Link Up, and DRS Received states indicated by this field must reflect their maskable states, which are controlled by the SFI PD State Mask, SFI DLL State Mask, or SFI DRS Mask bits in the SFI Control Register. See Section 7.9.23.3 .

This field must be implemented in any Downstream Port where the DRS Supported bit is Set in the Link Capabilities 2 Register

This field is RsvdZ for all other Functions. Default value of this field is 000b.

该字段指示连接到链路下游组件（如果有的话）的存在状态和DRS状态；定义的值为：

000b：Link Down -未确定是否存在

001b：Link Down - Component Not Present表示下游端口（DP）已确定下游组件不存在

010b：Link Down-Component Present表示DP已确定存在下游组件，但数据链路层未激活

011b：预留位

100b：Link Up-Component Present表示DP已确定存在下游组件，但自数据链路层变为活动状态以来，尚未接收到DRS消息

101b：Link Up-Component Present and DRS Received（存在组件并接收到DRS）表示自数据链路层激活以来DP已接收到DRS消息

110b：预留位

111b：预留位

下游组件存在状态必须由物理层带内存在检测机制的逻辑“或”以及为链路实现的任何带外存在检测机制（如果存在）来确定。如果没有实现带外存在检测机制，则下游组件存在状态必须仅由物理层带内存在检测机制确定

如果设置了插槽控制寄存器中的带内PD禁用位，则物理层带内存在检测机制必须始终指示不存在任何组件。

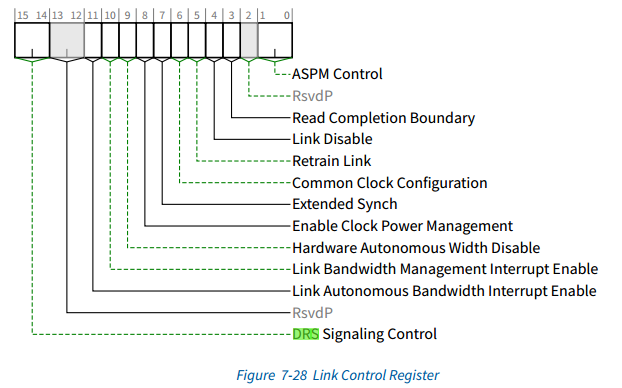
此字段指示的组件存在、链路连接和DRS接收状态必须反映其可屏蔽状态，这些状态由SFI控制寄存器中的SFI PD状态掩码、SFI DLL状态掩码或SFI DRS掩码位控制。参见第7.9.23.3节。

该字段必须在链路能力2寄存器中设置DRS支持位的任何下行端口中实现。

对于所有其他Function，此字段为RsvdZ。此字段的默认值为000b。

225未实现，该Downstream Component Presence字段用来指示下游组件是否存在以及当前DRS是否收到的状态，在pcie5\_pexreg模块中该寄存器的DRS Message Received字段是直接赋值为0的，并没有进行配置使用。

## Link Control Register (Offset 10h)



### DRS Signaling Control（未实现）

Indicates the mechanism used to report reception of a DRS message. Must be implemented for Downstream Ports with the DRS Supported bit Set in the Link Capabilities 2 Register.

Encodings are:

00b: DRS not Reported: If DRS Supported is Set, receiving a DRS Message will set DRS Message Received in the Link Status 2 Register but will otherwise have no effect

01b： DRS Interrupt Enabled: If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, and either MSI or MSI-X is enabled, an MSI or MSI-X interrupt is generated using the vector in Interrupt Message Number (Section 7.5.3.2 )

10b： DRS to FRS Signaling Enabled: If the DRS Message Received bit in the Link Status 2 Register transitions from 0 to 1, the Port must send an FRS Message Upstream with the FRS Reason field set to DRS Message Received.

Behavior is undefined if this field is set to 10b and the FRS Supported bit in the Device Capabilities 2 Register is Clear. Behavior is undefined if this field is set to 11b.

Downstream Ports with the DRS Supported bit Clear in the Link Capabilities 2 Register must hardwire this field to 00b. This field is Reserved for Upstream Ports. Default value of this field is 00b.

该DRS Signaling Control字段指示用于报告接收到DRS消息的机制，必须在Link Capabilities 2 Register中设置DRS Supported位的下游端口上实现。

编码如下：

00b：未报告DRS：如果设置了“DRS Supported”，则接收到DRS消息将在Link Status 2 Register中设置“DRS Message Received”，否则将无效。

01b：DRS中断使能：如果Link Status 2 Register中的DRS Message Received位从0转换为1，并且启用了MSI或MSI-X，则使用中断消息编号中的矢量生成MSI或MSIX中断（第7.5.3.2节）。

10b：DRS到FRS信令已启用：如果Link Status 2 Register中的DRS Message Received位从0转换为1，则端口必须向上游发送FRS消息，其中FRS Reason字段设置为DRS Message Received。

如果此字段设置为10b，并且Device Capabilities 2 Register中的FRS Supported位为清除，则行为未定义。如果此字段设置为11b，则行为未定义。

如果下游端口的Link Capabilities 2 Register中DRS Supported位被清除，必须将此字段硬接线到00b。此字段对于上游端口是预留位。此字段的默认值为00b。

225未实现，该DRS Signaling Control字段指示用于报告接收到DRS消息的机制，必须在Link Capabilities 2 Register中设置了DRS Supported位的下游端口上实现。但是在pcie5\_pexreg模块中该寄存器中的DRS Signaling Control字段是直接赋值为0的，并没有被配置使用。